## **TSPi Quality Plan - Form SUMQ** Name **ECOS** Date 14/04/2014 Team EAIT Instructor Luis Daniel Bena Cycle 1 **Assembly SYSTEM SYSTEM Percent Defect Free** Actual In Compile 100,0% In Unit Test 100,0% In Build and Integration Test 100,0% 100,0% In System Test 100,0% In Acceptance Test In Product Life 100,0% Defects/Page Plan Actual **REQ** Inspection 0,00 0,00 **HLD** Inspection 0,00 0,00 **Defects/KLOC** Plan **Actual DLD Review** 21,72 14,25 **DLD** Inspection 6,52 0,00 Code Review 28,20 0,00 6,04 0,00 Compile **Code Inspection** 4,23 0,00 **Unit Test** 2,76 0,00 **Build and Integration Test** 0,25 0,00 System Test 0,05 0,00 80,93 17,09 **Total Development** 0,00 Acceptance Test 0,01 Product Life 0,00 0,00 Total 80,94 17,09 **Defect Ratios** Plan Actual **DLD Review/Unit Test** 7,86 0,00 0,00 Code Review/Compile 4,67 **Development Time Ratios** Actual Plan **REQ Inspection/Requirements** 0,50 0,00 0,00 HLD Inspection/High-Level Design 0,40 Detailed Design/Code 2,00 0,71 DLD Review/Detailed Design 0,50 0,60 Code Review/Code 0,00 0,00 Inspection/Review Rates Plan Actual **REQ Inspection** 0,00 0,00 **HLD Inspection** 0,00 0,00 **DLD Review** 53,33 117,00 32,00 87,75 **DLD** Inspection Code Review 0,00 0,00 40,00 117,00 **Code Inspection** A/FR 4,00 0,00

## **TSPi Quality Plan - Form SUMQ** Name **ECOS** Date 14/04/2014 Team EAIT Instructor Luis Daniel Bena Cycle 1 **Assembly SYSTEM Phase Yields** Plan Actual **Planning** 0% 0% Requirements 0% 0% System Test Plan 0% 0% 70% 0% **REQ** Inspection 0% 0% High-Level Design Integration Test Plan 0% 0% **HLD** Inspection 70% 0% **Detailed Design** 0% 0% 83% **DLD Review** 70% **Test Development** 0% 0% 0% **DLD Inspection** 70% Code 0% 100% Code Review 70% 0% Compile 50% 0% Code Inspection 70% 0% 0% **Unit Test** 90% **Build and Integration Test** 80% 0% System Test 80% 0% 0% Acceptance Test 65% Plan **Process Yields** Actual 85% 100% % Before Compile 98% 100% % Before Unit Test 100% % Before Build and Integration Test 100% % Before System Test 100% 100% % Before Acceptance Test 100% 100% **Defect Injection Rates** (Defects Injected Per Hour) Plan **Actual Planning** 0,00 Requirements 0,25 0,00 System Test Plan 0,00 0 **REQ** Inspection 0 0,00 0,00 High-Level Design 0,25 Integration Test Plan 0,00 0 **HLD** Inspection 0 0,00 **Detailed Design** 0,75 1,20 0,00 **DLD Review** 0 0 0,00 **Test Development** 0 0,00 **DLD Inspection** Code 2 0,00 Code Review 0 0,00 0,3 0,00 Compile Code Inspection 0 0,00 0,067 0,00 **Unit Test** 0,00 **Build and Integration Test** 0 System Test 0 0,00

## **TSPi Quality Plan - Form SUMQ** Name **ECOS** Date 14/04/2014 Team EAIT Instructor Luis Daniel Bena Cycle 1 **Assembly** SYSTEM **Defect Removal Rates** Plan Actual **Planning** 0,00 0,00 Requirements 0,00 0,00 System Test Plan 0,00 0,00 **REQ** Inspection 0,35 0,00 0,00 High-Level Design 0,00 Integration Test Plan 0,00 0,00 **HLD** Inspection 0,54 0,00 **Detailed Design** 0,00 0,00 **DLD** Review 1,16 1,67 0,00 Test Development 0,00 0,21 0,00 **DLD** Inspection 0,14 Code 0,00 Code Review 0,00 0,00 Compile 0,00 0,00 0,00 Code Inspection 0,17 **Unit Test** 0,00 0,15 **Build and Integration Test** 0,08 0,00 System Test 0,00 0,00

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