CS/EE 120A Lab Report

Name: James Luo Email:jluo011@ucr.edu Partner's Name:Albert Dang

Section:026 login:jluo011

Lab number and title: Lab 5 Adders

Note: every individual must submit a unique lab report form.

Summarize (in your own words) the subject of this lab:

The purpose of this lab is to design a simple 4 bit full adder.

Describe the new concepts covered in this lab:

We needed to understand how data paths work along with carry over bit gates. This made us have to understand how there can be delays in the system

Describe how this lab built upon previous ones:

This lab builds on the previous one because of how we had to deal with system states. This required us to know how data is stored and how to access them when we need them.

Describe the most difficult part of this lab for you:

The hardest part of the lab was figuring out that we needed to worry about a system delay in the circuit board. This is because of how we normally do not have to worry about that issue when writing code.

Describe problems you faced and how you solved them:

The way we solved the system delay issue was that we put a slight wait so that the machine can keep up with the computation that was needed to proceed.

Do you verify that the code included with this report is your's and your partner's original work (yes/no)?

Yes

Submit your source code, testbench, and simulation output.