```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    18:09:52 01/28/2019
7   // Design Name:
8   // Module Name:    bcd_to_7led_bh
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module bcd_to_7led_bh(
22     input wire sw0 , // Switches
23     input wire sw1 ,
24     input wire sw2 ,
25     input wire sw3 ,
26     output reg a , // LED segments
27     output reg b ,
28     output reg c ,
29     output reg d ,
30     output reg e ,
31     output reg f ,
32     output reg g ,
33     output reg an0, // LED display control
34     output reg an1,
35     output reg an2,
36     output reg an3
37      );
38
39      // Internal wire
40     wire [3:0] bundle ;
41     assign bundle = {sw3,sw2,sw1,sw0} ;
42
43     always @(*) begin
44
45     // Setting the ANs signals
46     an0 = 1'b1;
47     an1 = 1'b1;
48     an2 = 1'b1;
49     an3 = 1'b0; // Display in the module AN3
50
51     // Setting the segments signals
52     a = 1'b1;
53     b = 1'b1;
54     c = 1'b1;
55     d = 1'b1;
56     e = 1'b1;
57     f = 1'b1;
```

```
 58      g = 1'b1;
 59
 60      case ( bundle )
 61         4'b0000 : begin // 0
 62            a = 1'b0;
 63            b = 1'b0;
 64            c = 1'b0;
 65            d = 1'b0;
 66            e = 1'b0;
 67            f = 1'b0;
 68            g = 1'b1;
 69         end
 70
 71         4'b0001 : begin // 0
 72            a = 1'b1;
 73            b = 1'b0;
 74            c = 1'b0;
 75            d = 1'b1;
 76            e = 1'b1;
 77            f = 1'b1;
 78            g = 1'b1;
 79         end
 80
 81         4'b0010 : begin // 0
 82            a = 1'b0;
 83            b = 1'b0;
 84            c = 1'b1;
 85            d = 1'b0;
 86            e = 1'b0;
 87            f = 1'b1;
 88            g = 1'b0;
 89         end
 90
 91         4'b0011 : begin // 0
 92            a = 1'b0;
 93            b = 1'b0;
 94            c = 1'b0;
 95            d = 1'b0;
 96            e = 1'b1;
 97            f = 1'b1;
 98            g = 1'b0;
 99         end
100
101         4'b0100 : begin // 0
102            a = 1'b1;
103            b = 1'b0;
104            c = 1'b0;
105            d = 1'b1;
106            e = 1'b1;
107            f = 1'b0;
108            g = 1'b0;
109         end
110
111         4'b0101 : begin // 0
112            a = 1'b0;
113            b = 1'b1;
114            c = 1'b0;
```

```
115             d = 1'b0;
116             e = 1'b1;
117             f = 1'b0;
118             g = 1'b0;
119          end
120
121          4'b0110 : begin // 0
122             a = 1'b0;
123             b = 1'b1;
124             c = 1'b0;
125             d = 1'b0;
126             e = 1'b0;
127             f = 1'b0;
128             g = 1'b0;
129          end
130
131          4'b0111 : begin // 0
132             a = 1'b0;
133             b = 1'b0;
134             c = 1'b0;
135             d = 1'b1;
136             e = 1'b1;
137             f = 1'b1;
138             g = 1'b1;
139          end
140
141          4'b1000 : begin // 0
142             a = 1'b0;
143             b = 1'b0;
144             c = 1'b0;
145             d = 1'b0;
146             e = 1'b0;
147             f = 1'b0;
148             g = 1'b0;
149          end
150
151          4'b1001 : begin // 0
152             a = 1'b0;
153             b = 1'b0;
154             c = 1'b0;
155             d = 1'b0;
156             e = 1'b1;
157             f = 1'b0;
158             g = 1'b0;
159          end
160
161          default : begin // 0
162             a = 1'b1;
163             b = 1'b1;
164             c = 1'b1;
165             d = 1'b1;
166             e = 1'b1;
167             f = 1'b1;
168             g = 1'b1;
169          end
170
171       endcase
```

```
172     end
173
174     endmodule
175
```