CS/EE 120A Lab Report

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Lab number and title: Lab 3Programming Combinatorial Logic
Note: every individual must submit a unique lab report form.

Summarize (in your own words) the subject of this lab:
The goal of this lab is to program logic circuits onto the FPGA boards. This ranged from a simple logic gate to a number system using logic circuits and code.

Describe the new concepts covered in this lab:

We learned how to design a 7 segment logic system that involved 4 inputs. We also learned how to program the FPGA boards and how to attach our code to the system.

Describe how this lab built upon previous ones:
We had to use our knowledge of decoders to determine what value we should print out in the 7 segment logic system.

Describe the most difficult part of this lab for you:

The most difficult part of the lab was getting the system to connect to the board. It was hard because the setup was quite easy to mess up.

Describe problems you faced and how you solved them:
We had issues with the Map portion of the system. The was we handled it was that we compare the variable names to the board and made sure that we were on the correct config. IE The default config was not Jtag

Do you verify that the code included with this report is your's and your partner's original work (yes/no)?

Yes

Submit your source code, testbench, and simulation output.

and_gate.ucf

```
# Pin assignment for LEDs
NET "d" LOC = "m5" ; # Bank = 2, Signal name = LD0

# Pin assignment for SWs
NET "i1" LOC = "l3"; # Bank = 3, Signal name = SW1
NET "i2" LOC = "p11"; # Bank = 2, Signal name = SW0
```

sprinkler_circuit.ucf

```
# Pin assignment for LEDs
NET "d0" LOC = "m5";
NET "d1" LOC = "m11";
NET "d2" LOC = "p7";
NET "d3" LOC = "p6";
NET "d4" LOC = "n5";
NET "d5" LOC = "n4";
NET "d6" LOC = "p4";
NET "d7" LOC = "g1";

# Pin assignment for SWs
NET "enable" LOC = "n3";
NET "a" LOC = "k3";
NET "b" LOC = "l3";
NET "c" LOC = "p11";
```

bcd_to_7led_bh.ucf

```
# Enables
NET "enable0" LOC = "g3";
NET "enable1" LOC = "f3";
NET "enable2" LOC = "e2";
NET "enable3" LOC = "n3";

# Inputs
NET "sw0" LOC = "p11";
NET "sw1" LOC = "l3";
NET "sw2" LOC = "k3";
NET "sw3" LOC = "b4";
# Outputs
NET "a" LOC = "l14";
```

```
NET "b" LOC = "h12";
NET "c" LOC = "n14";
NET "d" LOC = "n11";
NET "e" LOC = "p12";
NET "f" LOC = "l13";
NET "g" LOC = "m12";
// ANx
NET "an0" LOC = "k14";
NET "an1" LOC = "m13";
NET "an2" LOC = "j12";
NET "an3" LOC = "f12";
```

bcd_to_7led_bh.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    18:09:52 01/28/2019
// Design Name:
// Module Name:    bcd_to_7led_bh
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module bcd_to_7led_bh(
        input wire sw0 , // Switches
        input wire sw1 ,
        input wire sw2 ,
        input wire sw3 ,
        output reg a , // LED segments
        output reg b ,
        output reg c ,
        output reg d ,
        output reg e ,
        output reg f ,
        output reg g ,
        output reg an0, // LED display control
        output reg an1,
        output reg an2,
        output reg an3
    );

         // Internal wire
        wire [3:0] bundle ;
        assign bundle = {sw3,sw2,sw1,sw0} ;

        always @(*) begin

        // Setting the ANs signals
```

```
an0 = 1'b1;
an1 = 1'b1;
an2 = 1'b1;
an3 = 1'b0; // Display in the module AN3

// Setting the segments signals
a = 1'b1;
b = 1'b1;
c = 1'b1;
d = 1'b1;
e = 1'b1;
f = 1'b1;
g = 1'b1;

case ( bundle )
        4'b0000 : begin // 0
                a = 1'b0;
                b = 1'b0;
                c = 1'b0;
                d = 1'b0;
                e = 1'b0;
                f = 1'b0;
                g = 1'b1;
        end

        4'b0001 : begin // 0
                a = 1'b1;
                b = 1'b0;
                c = 1'b0;
                d = 1'b1;
                e = 1'b1;
                f = 1'b1;
                g = 1'b1;
        end

        4'b0010 : begin // 0
                a = 1'b0;
                b = 1'b0;
                c = 1'b1;
                d = 1'b0;
                e = 1'b0;
                f = 1'b1;
                g = 1'b0;
        end

        4'b0011 : begin // 0
                a = 1'b0;
```

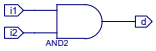
```
        b = 1'b0;
        c = 1'b0;
        d = 1'b0;
        e = 1'b1;
        f = 1'b1;
        g = 1'b0;
end

4'b0100 : begin // 0
        a = 1'b1;
        b = 1'b0;
        c = 1'b0;
        d = 1'b1;
        e = 1'b1;
        f = 1'b0;
        g = 1'b0;
end

4'b0101 : begin // 0
        a = 1'b0;
        b = 1'b1;
        c = 1'b0;
        d = 1'b0;
        e = 1'b1;
        f = 1'b0;
        g = 1'b0;
end

4'b0110 : begin // 0
        a = 1'b0;
        b = 1'b1;
        c = 1'b0;
        d = 1'b0;
        e = 1'b0;
        f = 1'b0;
        g = 1'b0;
end

4'b0111 : begin // 0
        a = 1'b0;
        b = 1'b0;
        c = 1'b0;
        d = 1'b1;
        e = 1'b1;
        f = 1'b1;
        g = 1'b1;
end
```

```
                4'b1000 : begin // 0
                        a = 1'b0;
                        b = 1'b0;
                        c = 1'b0;
                        d = 1'b0;
                        e = 1'b0;
                        f = 1'b0;
                        g = 1'b0;
                end

                4'b1001 : begin // 0
                        a = 1'b0;
                        b = 1'b0;
                        c = 1'b0;
                        d = 1'b0;
                        e = 1'b1;
                        f = 1'b0;
                        g = 1'b0;
                end

                default : begin // 0
                        a = 1'b1;
                        b = 1'b1;
                        c = 1'b1;
                        d = 1'b1;
                        e = 1'b1;
                        f = 1'b1;
                        g = 1'b1;
                end

        endcase
end

endmodule
```

```
1   # Pin assignment for LEDs
2   NET "d" LOC = "m5" ; # Bank = 2, Signal name = LD0
3
4   # Pin assignment for SWs
5   NET "i1" LOC = "l3"; # Bank = 3, Signal name = SW1
6   NET "i2" LOC = "p11"; # Bank = 2, Signal name = SW0
7
```



```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    18:09:52 01/28/2019
7   // Design Name:
8   // Module Name:    bcd_to_7led_bh
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module bcd_to_7led_bh(
22     input wire sw0 , // Switches
23     input wire sw1 ,
24     input wire sw2 ,
25     input wire sw3 ,
26     output reg a , // LED segments
27     output reg b ,
28     output reg c ,
29     output reg d ,
30     output reg e ,
31     output reg f ,
32     output reg g ,
33     output reg an0, // LED display control
34     output reg an1,
35     output reg an2,
36     output reg an3
37      );
38
39      // Internal wire
40     wire [3:0] bundle ;
41     assign bundle = {sw3,sw2,sw1,sw0} ;
42
43     always @(*) begin
44
45     // Setting the ANs signals
46     an0 = 1'b1;
47     an1 = 1'b1;
48     an2 = 1'b1;
49     an3 = 1'b0; // Display in the module AN3
50
51     // Setting the segments signals
52     a = 1'b1;
53     b = 1'b1;
54     c = 1'b1;
55     d = 1'b1;
56     e = 1'b1;
57     f = 1'b1;
```




```
1   # Enables
2   NET "enable0" LOC = "g3";
3   NET "enable1" LOC = "f3";
4   NET "enable2" LOC = "e2";
5   NET "enable3" LOC = "n3";
6
7   # Inputs
8   NET "sw0" LOC = "p11";
9   NET "sw1" LOC = "l3";
10  NET "sw2" LOC = "k3";
11  NET "sw3" LOC = "b4";
12  # Outputs
13  NET "a" LOC = "l14";
14  NET "b" LOC = "h12";
15  NET "c" LOC = "n14";
16  NET "d" LOC = "n11";
17  NET "e" LOC = "p12";
18  NET "f" LOC = "l13";
19  NET "g" LOC = "m12";
20  // ANx
21  NET "an0" LOC = "k14";
22  NET "an1" LOC = "m13";
23  NET "an2" LOC = "j12";
24  NET "an3" LOC = "f12";
25
```

sprinkler_circuit.ucf **Mon Feb 04 09:19:09 2019**

```
1   # Pin assignment for LEDs
2   NET "d0" LOC = "m5";
3   NET "d1" LOC = "m11";
4   NET "d2" LOC = "p7";
5   NET "d3" LOC = "p6";
6   NET "d4" LOC = "n5";
7   NET "d5" LOC = "n4";
8   NET "d6" LOC = "p4";
9   NET "d7" LOC = "g1";
10
11  # Pin assignment for SWs
12  NET "enable" LOC = "n3";
13  NET "a" LOC = "k3";
14  NET "b" LOC = "l3";
15  NET "c" LOC = "p11";
16
```