Name (LAST, first): _____ Username: _____

CSEE 120A – Digital Design **Fall - 2018**

Final Exam -- Version 1

Time: 2 hours 50 minutes (plus 10 min setup)
Questions: 60 multiple choice (MC) questions

Do not turn the page until instructed.
No "breaks". If you leave the exam room, you may not return.
You may use the pages as scratch. Do NOT detach any pages.

Please:
1. Remove caps or hats, Lower hoods
2. Turn off electronics, place UNDER DESK
3. Do not start until we give the word

You may have on your desks ONLY:
1. This exam & your "bubble sheet"
2. Pen/pencil & eraser
3. Your student ID

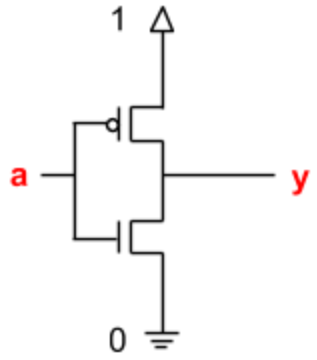
DO THE FOLLOWING NOW:
1. Fill out your details at the top of the bubble sheet
    - Write the test version on the top right corner of the bubble sheet.
    - name, username/netID, SID
    .
2. Write your name and username also in this exam booklet:
   - *(now)* at the top of this page
   - *(when instructed to start)* at the top of all the coding question pages

Answer all MC questions using the bubble sheet provided. C**hoose the single best choice per question.**

Show your student ID or a photo ID when you hand in your exam.

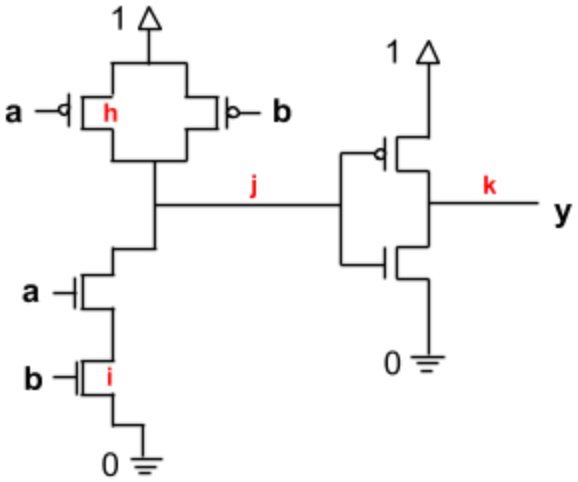
Multiple choice section (60 x 1 point)

1. Given the CMos circuit below, what is y when a is 0?



   a. 0
   b. 1
   c. Does not conduct

2. If a = 1 and b = 0, what would be the value of k?

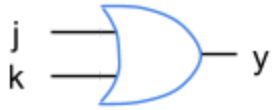


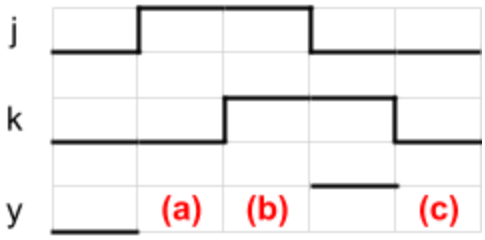
   a. 0
   b. 1
   c. Does not conduct

3. Indicate which one logic gate is best suited to implement the functionality of a system used to trigger a sensor light if a tire pressure is low. Assume there are 4 tires and one low sensor light.
   a. And
   b. Or
   c. Not
   d. No single gate

4. Directly translate `(a AND b) OR c` to an expression using digital-designer shorthand notation.
    a. (a+b)c
    b. ab'c
    c. (ab)' + c
    d. ab + c

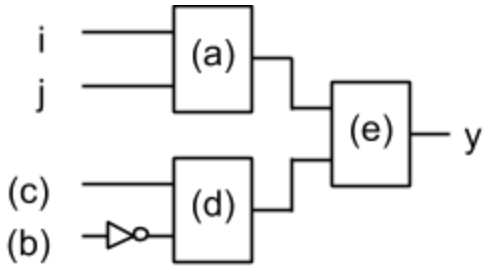
5. Complete the timing diagram. Assume answers are listed as abc





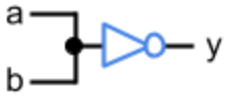
    a. 010
    b. 100
    c. 110
    d. 001

6. Use the figure below to determine the missing gates for the equation y = ij + mn'. Assume the answers are in the order a b c d e.



    a. And m n and or
    b. And n m and or
    c. Or m n or and
    d. Or n m or and

7. The wiring in the figure below is the proper way to connect the gate.



    a. True
    b. false

8. The wiring in the figure below is the proper way to connect the gate.

   a. True
   b. false

9. Simplify the expression (e + 1)(e'f + fe' + d').
   a. e' + d'
   b. ef + ed'
   c. e'f + d'
   d. e(e'f+d')

10. Transform Y = a + c(b + ab') to sum of product form. Simplify if possible.
   a. Y = a + bc + ab'c
   b. Y = a'(b' +c') (a' + b + c)
   c. Y = bc + ab'c
   d. Y = a + bc

11. Consider the following truth table. How would it be populated correctly? Assume the answers are in form jklmn.

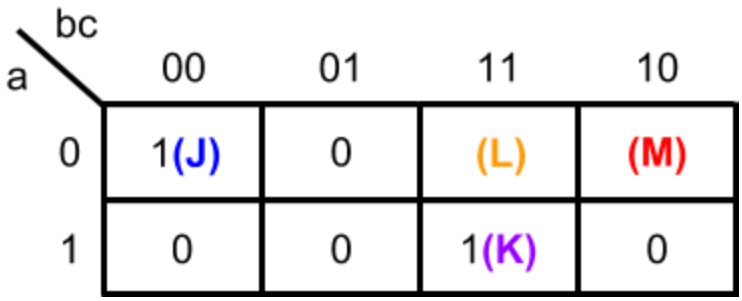
a	b	f(a, b)
0	0	M
K	J	
1	0	N
1	L	

   a. 10111
   b. 01111
   c. 10100
   d. 01100

12. A designer uses the capture and convert process for the combinational problem described below. A particular medical device delivers radiation to a patient to treat cancer. The device has two radiation strength levels, low (s = 0) and high (s = 1). The device has two radiation durations: short (d = 0) and long (d = 1). The device normally is used to deliver high strength for short duration, or low strength for long duration. A hardware safety component can be enabled (e = 1) that detects high strength for long duration and automatically turns off the device after a minute, but on rare occasion a radiation therapist may disable that component. To prevent accidents, a designer wishes to sound an alarm if the device is ever configured to high strength for long duration with the safety off. How many rows does the truth table have?
    a. 2
    b. 4
    c. 8
    d. 16
    e. 32

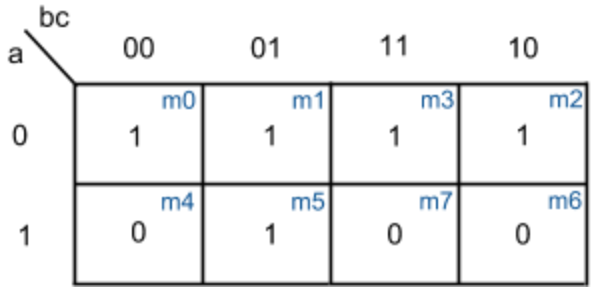
13. The equation for the system described in problem 12 has how many AND and OR gates total?
    a. 1
    b. 2
    c. 3
    d. 4
    e. 5

14. Using the KMap below, cells (L) and (K) differ in what variable: a, b, or c?



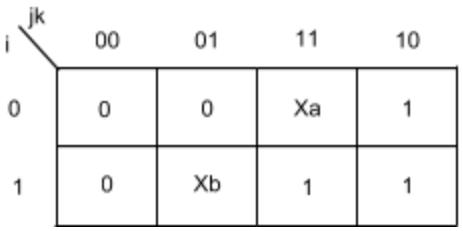
    a. A
    b. B
    c. C
    d. Does not differ

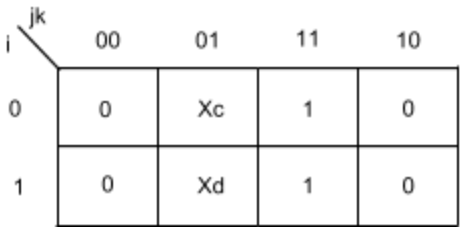
15. Using the KMap below, which groups should be circled



a. m0m1, m3m2, m5
b. m0m1, m3m2, m1m5
c. m0m2, m1m3, m5
d. m0m1m3m2, m5
e. m0m1m3m2, m1m5

16. What should the don't cares in the KMap below be set to in order to minimize the minterms? Assume the answers given are written XaXbXcXd





a. 1011
b. 1111
c. 1000
d. 0100
e. 1100

17. Given a 4x1 mux with inputs i3 i2 i1 i0 and output y. If i3 i2 i1 i0 are 0 1 1 0. If s1s0 = 10, then y = _____ .
a. 0
b. 1
c. Z
d. Unable to tell based on information given

18. How many select lines does a 16x1 mux require?
a. 1
b. 2
c. 4
d. 16
e. none

19. What should i1i0 be configured to so a decoder outputs are y0 = 0, y1 = 0, y2 = 0, and y3 = 1.
    a. 00
    b. 01
    c. 10
    d. 11
    e. Not possible

20. How many AND gates does a 2x4 decoder require?
    a. 8
    b. 4
    c. 2
    d. 1
    e. 0

21. Using a SR Latch, indicate q's present value for the input sequence. "s: 0..1" means s was 0 and is presently 1.

    s: 0..0..1..0..1

    r: 1..0..0..0..0

    a. 0
    b. 1
    c. Undefined
    d. Not enough information

22. What happens in a SR Latch when S=1 and R=1 at the same time?
    a. Setting s and r to 1's simultaneously initially sets q to 1.
    b. q oscillates while s and r are both 1's.
    c. If s and r are both 1's, and then both change to 0's, q may oscillate.
    d. q is maintained until both s and r return to 0 and then q is 0.
    e. q is maintained until both s and r return to 0 and then q is 1.

23. Using a SR Latch, indicate q's present value for the input sequence. "s: 0..1" means s was 0 and is presently 1.
    d: 0..0..1..1..0
    e: 1..0..0..1..0
    a. 0
    b. 1
    c. Undefined
    d. Not enough information

24. A change of the clock signal from 0 to 1 is called a rising _____ .
    a. edge
    b. cliff
    c. event
    d. Period

25. If a clock's period is 1 microsecond, the clock's frequency is _____.
    a. 1 KHz
    b. 1 MHz
    c. 1 GHz
    d. 1 THz

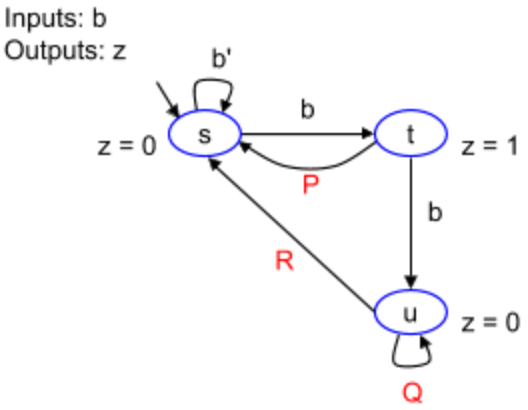
26. Given a single D flip-flop with data input d, clock input clk, and output q. d is 0, clk is 0, q is 0. d changes to 1, then clk changes to 1. Moments later, what is q?
    a. 0
    b. 1
    c. Undefined
    d. Not enough information

27. Given a single D flip-flop implemented with a master-servant arrangement. d is 0, clk is 0, q is 1. What is in the first latch?
    a. 0
    b. 1
    c. Undefined
    d. Not enough information

28. Given a single D flip-flop implemented with a master-servant arrangement. d is 0, clk is 0, q is 1. What is in the second latch?
    a. 0
    b. 1
    c. Undefined
    d. Not enough information

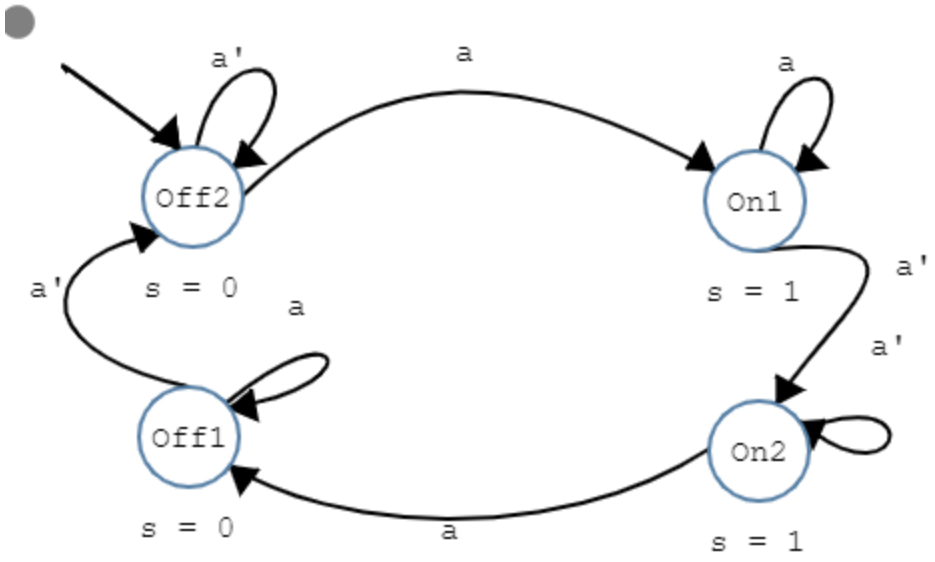
29. Given a 3-bit register with data inputs d2, d1, d0, clock input clk, and outputs q2, q1, q0. d2d1d0 is 101, and q2q1q0 is 000. clk rises. What does q2q1q0 become?
    a. 000
    b. 101
    c. 111
    d. 010

30. For each unique 0-to-1 transition of b, the below FSM sets z to 1 for exactly one clock cycle. Determine the missing transition conditions. Assume the answers are written in PRQ



a. bb'b
b. b'bb'
c. b'b' b
d. b' null null
e. b null null

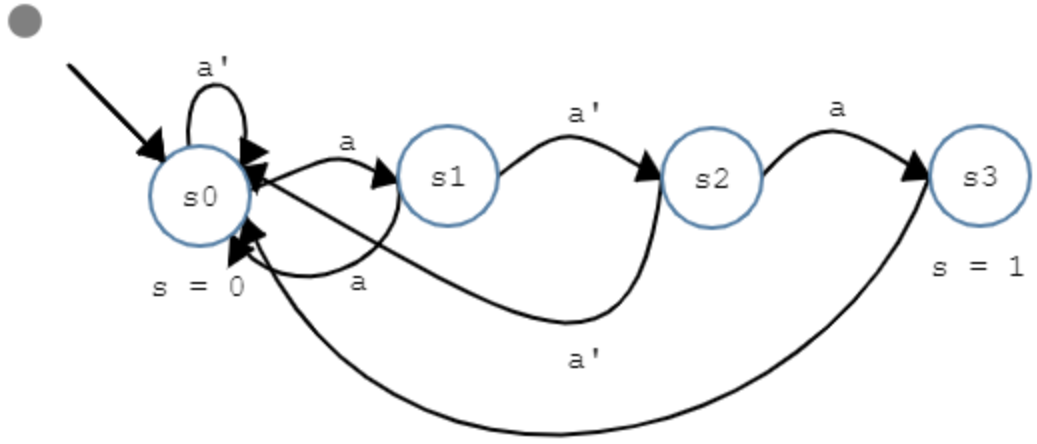
31. Using the state machine below, suppose the FSM just started execution and so is in state Off2, with s = 0. Then input a rises from 0 to 1. Does the output s toggle?



a. Yes
b. No

32. Using the state machine in problem 31, while in On2, if input a rises to 1, the output s will toggle from 0 to 1.
a. True
b. False

33. Using the state machine below, can the sequence 101 on input occur at any rate to cause output s to pulse?



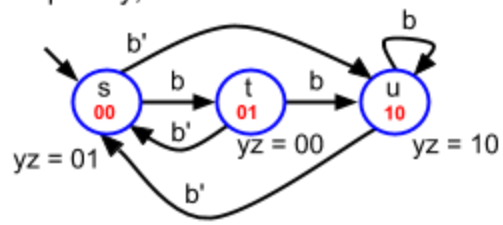
a. Yes
b. No

34. Using the state machine from problem 33, does the sequence 101101 cause two pulses on s?

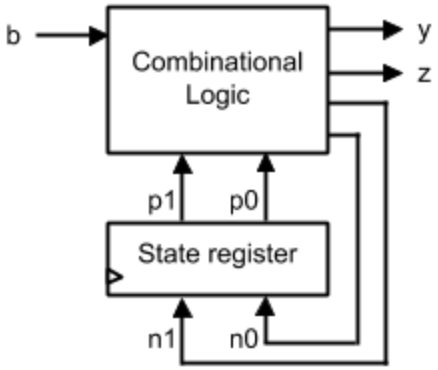
a. Yes
b. No

35. Complete the truth table for the given FSM. Assume the answers are CDEFG.

Inputs: b
Outputs: y, z



*State encodings are in red

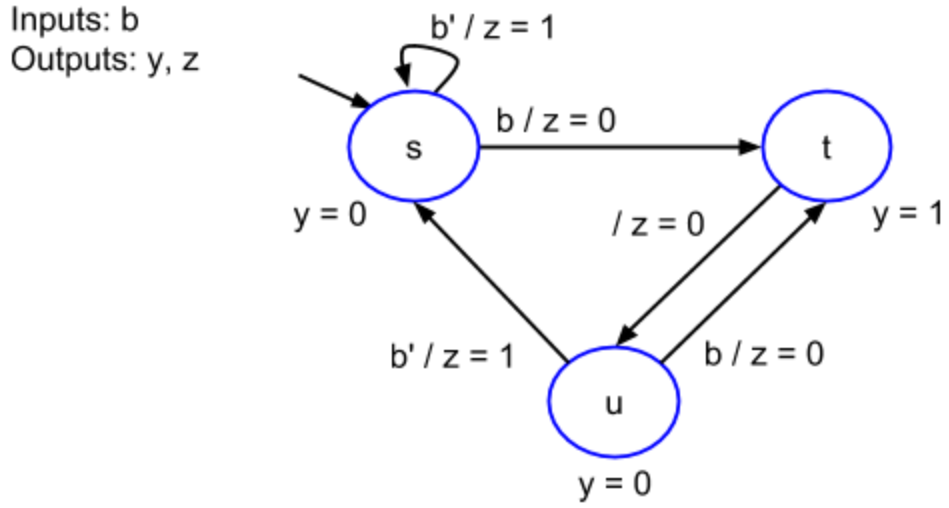


	p1	p0	b	n1	n0	y	z
s	0	0	0	1	0	0	1
	0	0	1	0	(F)	0	1
t	0	1	0	0	0	(C)	(D)
	0	1	1	1	0	0	(E)
u	1	0	0	(G)	0	1	0
	1	0	1	1	0	1	0
unused	1	1	0	0	0	0	0
	1	1	1	0	0	0	0

a. 01010
b. 01000
c. 00011
d. 00010
e. 00000

36. Convert the truth table from 35 to a circuit that can be used in the combinational logic part of the controller.
a. Z = p1'p0'b' + p1'p0'b
b. Z = p1'p0'b' + p1'p0'b + p1'p0b'
c. Z = p1'p0'b' + p1'p0'b + p1'p0b' + p1'p0b
d. Z = p1p0'b' + p1p0'b + p1p0b' + p1p0b

37. Consider the Mealy state machine below. When is the transition " / z = 0" from t to u taken?



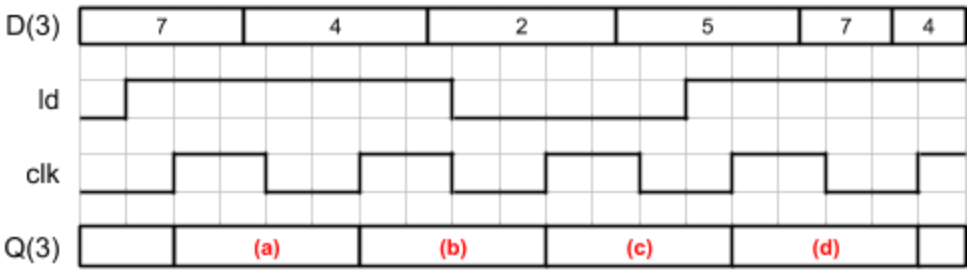
a. Rising edge of clk.
b. Falling edge of clk.
c. Only when b is 0 and rising edge of clk.
d. Only when b is 1 and rising edge of clk.

38. If the inputs to a 4-bit carry ripple adder ars B3B2B1B0 = 1111 and A3A2A1A0 = 0001 and Cin = 0, what is the output?
a. Cout = 0 S3S2S1S0 = 0000
b. Cout = 1 S3S2S1S0 = 0000
c. Cout = 1 S3S2S1S0 = 1111
d. Cout = 0 S3S2S1S0 = 1111

39. How many full adders are needed to create a 7-bit carry-ripple adder?
a. 7
b. 14
c. 21
d. 0

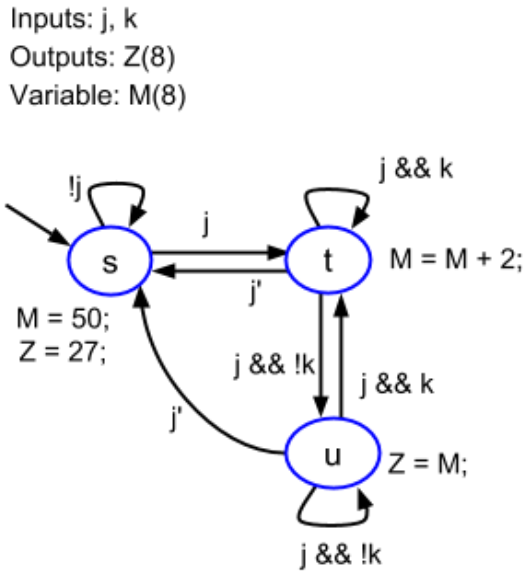
40. What is -3 in eight-bit two's-complement representation?
a. 1101
b. 00001101
c. 11111101
d. 00001100
e. 11111100

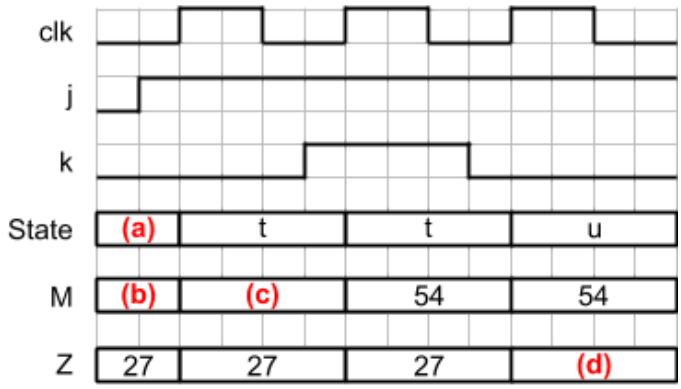
41. For a subtractor built from an adder, the adder is configured to subtract by setting the adder's cin bit to ___.
    a. Cannot use an adder to make a subtractor
    b. Cin does not need to be set to use an adder to make a subtractor.
    c. 0
    d. 1
42. Configure the adder/subtractor to perform the following operation: 7 - 2
    a. a3a2a1a0 = 0111 b3b2b1b0 = 0010 sub = 0
    b. a3a2a1a0 = 0111 b3b2b1b0 = 0010 sub = 1
    c. a3a2a1a0 = 0010 b3b2b1b0 = 0111 sub = 1
    d. a3a2a1a0 = 0010 b3b2b1b0 = 0111 sub = 0
43. Indicate which comparator output will be 1 if A=0100 and B = 1000
    a. gt
    b. eq
    c. lt
    d. All outputs will be 0
44. Consider a 4-bit carry-ripple comparator . If inputs are a3a2a1a0 = 0100 (4) and b3b2b1b0 = 0010 (2), indicate which output will be 1 for digit 1. (a1 and b1)
    a. Gt
    b. Eq
    c. Lt
    d. All outputs will be 0
45. For the given values of D, ld, and clk, indicate the value of Q. Assume the answers are in the form abcd.



    a. 4 2 5 7
    b. 4 2 2 7
    c. 7 4 2 5
    d. 7 4 4 5
46. Assume rst = 0, ld = 1, d2d1d0 are 110, and q2q1q0 are 111. When a rising clock occurs, what do q2q1q0 become?
    a. 111
    b. 110
    c. 000
    d. undefined

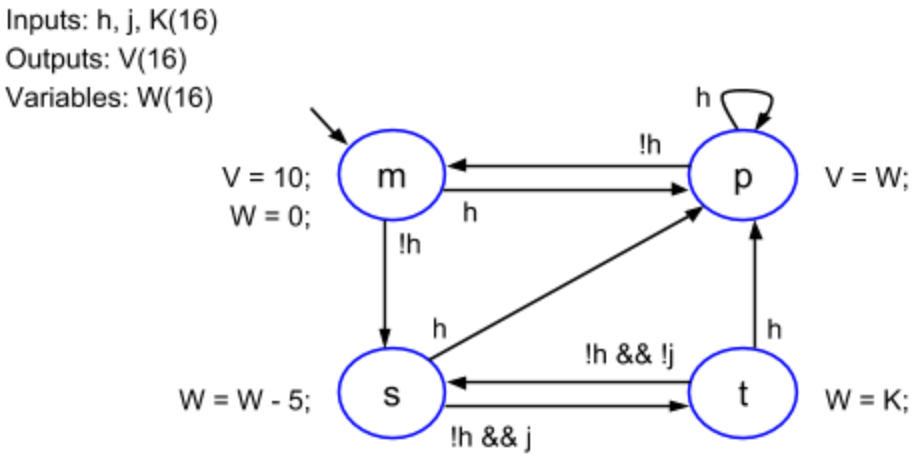
47. Using the HLSM below, complete the timing diagram. Assume answers are in order abcd.





a. S 50 50 27
b. S 0 52 27
c. S 50 52 27
d. S 50 50 54
e. S 50 52 54

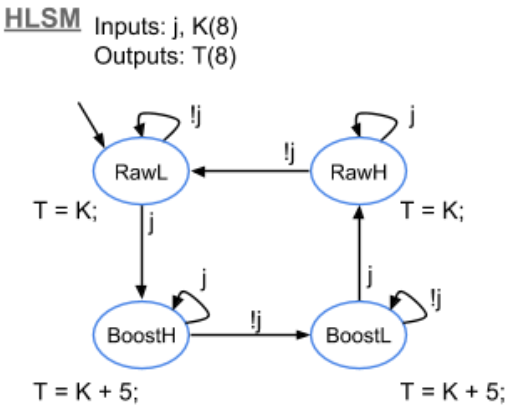
48. Given the following HLSM. How many registers does the datapath need?

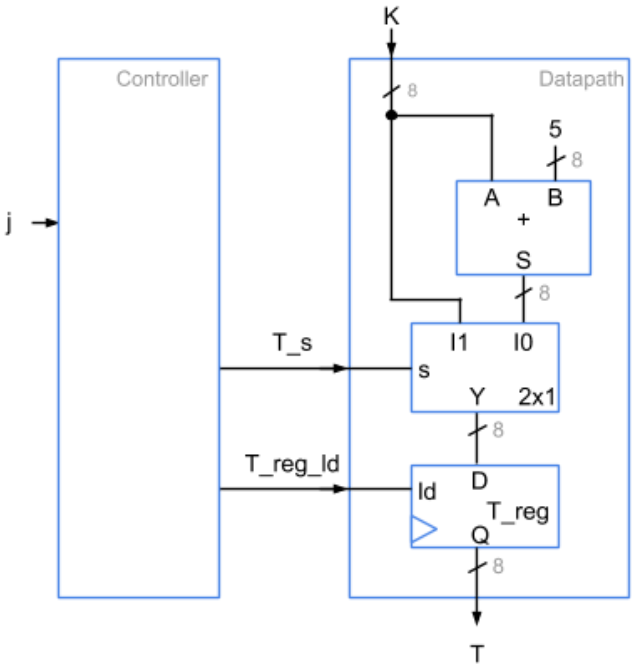


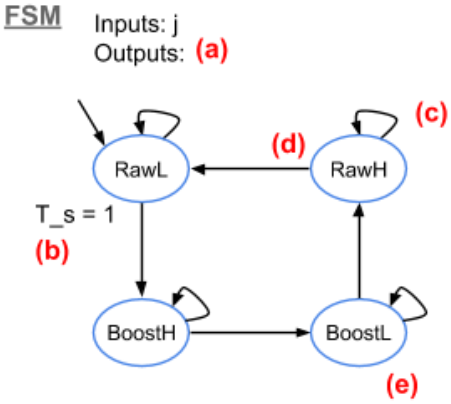
a. 0
b. 1
c. 2
d. 3

49. Using the HLSM from problem 50, what components besides registers are needed?
    a. Comparator, 2 x 1 mux, 2 x 1 mux, subtractor
    b. Comparator, 2 x 1 mux, subtractor
    c. 2 x 1 mux, 2 x 1 mux, subtractor
    d. 2 x 1 mux, subtractor

50. Complete the HLSM to FSM conversion. What should replace (a)?







a. T
b. T_s
c. T_reg_ld
d. T_s, T_reg_ld
e. T, T_s, T_reg_ld

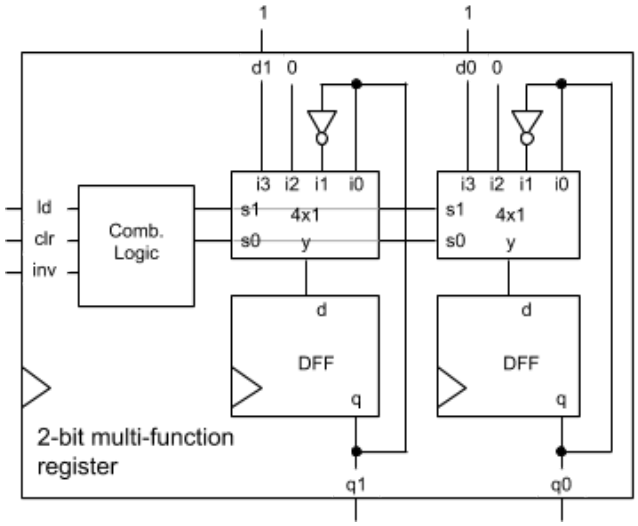
51. Complete the HLSM to FSM conversion in problem 50. What should replace (c)?

a. j
b. !j
c. 0
d. 1
e.

52. Complete the HLSM to FSM conversion in problem 50. What should replace (e)?

a. T_reg_ld = 1
b. T_s = 0
c. T_s = 1
d. T_s = 0 T_reg_ld = 1
e. T_s = 1 T_reg_ld = 1

53. Given a three-state buffer with control input a, data input b, and data output y. If a = 0 and b = 0, then y = ?
    a. 0
    b. 1
    c. 'Z'
    d. Not enough information
54. Given a 32x8 register file, how many bits is W_addr?
    a. 0
    b. 5
    c. 3
    d. 2
55. Complete the truth table for the multi-functional register below. Assume answers are in the form FGH.



ld	clr	inv	s1	s0	Register function
0	0	0	0	0	Maintain
0	0	1	(F)		Invert bits
0	1	0	(G)		Clear
0	1	1	0	0	(Maintain)
1	0	0	(H)		Load
1	0	1	0	0	(Maintain)
1	1	0	0	0	(Maintain)
1	1	1	0	0	(Maintain)

    a. 00 10 11
    b. 01 10 11
    c. 01 11 00
    d. 01 10 00
56. Assume an 8-bit ALU. Determine the mux configuration needed to implement the ALU operation S = E AND F
    a. A = E AND F, B = 1, cin = 1
    b. A = E AND F, B = 0, cin = 1
    c. A = E AND F, B = 0, cin = 0
    d. A = 0, B = E AND F, cin = 0
57. For a fixed size, which can store more bits?
    a. SRAM
    b. DRAM
    c. They hold the same.

58. A 64x4 memory has how many *bits*?
    a. 64
    b. 128
    c. 256
    d. 4096
59. Programming a floating-gate transistor in a ROM is done via a large _____.
    a. Positive voltage
    b. Negative voltage
    c. UV light
    d. hammer
60. A chip maker currently sells a 128 MB chip for $10. A customer wants 10,000 256 MB chips for $50 per chip. The NRE cost for designing a 256 MB chip will be $10 million. Should the chip maker design a new 256 MB chip for the customer?
    a. Yes
    b. No
    c. Only if the maker can get more customers.
    d. Only if the customer will commit to a multi year contract.