FAET630004: AI-Core and RISC Architecture **(Due: 4/2/20)**

Homework Assignment #1

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Problem 1: Implement a simple RISC Core

(2+5+8=15 points)

On class, we define an extremely simple RISC ISA and its hardware organization, which are both shown below. For this homework assignment, we need to design/implement/simulate this core.

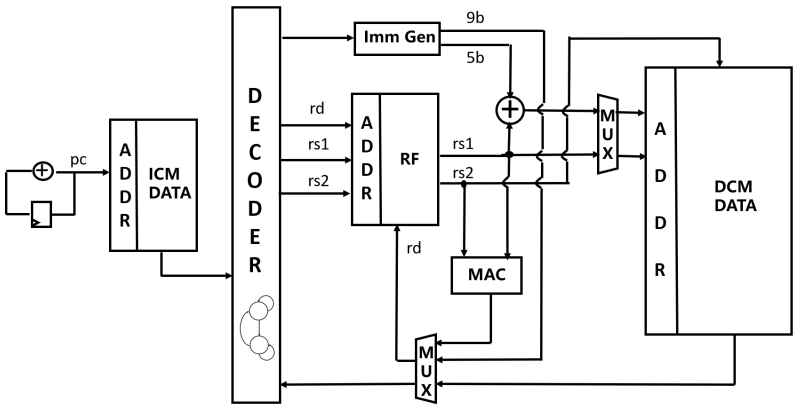
极简指令集（RISC）Load/Store 架构			
opcode	目标 Reg	源寄存器/立即数	说明
Load	rd	rs+imm(5b)	//在 rst imm 地址→rd
Store	/	rs(地址)/rs(DATA)	//rs(DAI)→Mem index =rs(地址)
MOV	rd	imm(9b)	//赋值→rd
MAC	rd rd	rs1,rs2,funct=0 rs1,/,funct=1	//乘加 //初始赋值清除

(a) Which HDL you want to use ?

I want to use Verilog HDL.

(b) For Verilog-players, please write an top-level structural verilog file to decribe the system.
For C-players, please complete a header filer and .cc file , compatible to Vivado HLS, to describe the system.
(Hint: Please submit your script as well)

Please see the attachment.



(c) For Verilog-players, please write a testbench verilog file to simulate the system. It should complete a 4-MAC

(neuron) computing.
For C-players, please complete a _test.cc file , compatible to Vivado HLS, to simulate the system. It should complete a 4-MAC (neuron) computing.
(Hint: Please submit your script and simulated waveform, highlight the final results and compare it with the theoretical value.)

- Theoretical calculation

- Simulation results and waveform(simulation environment:VCS)