计算机与智能处理器体系结构

Al-Core and RISC Architecture



课程主页 扫一扫

第二十四节:期末汇报要求(2021年度)

Lecture 24: Final Project

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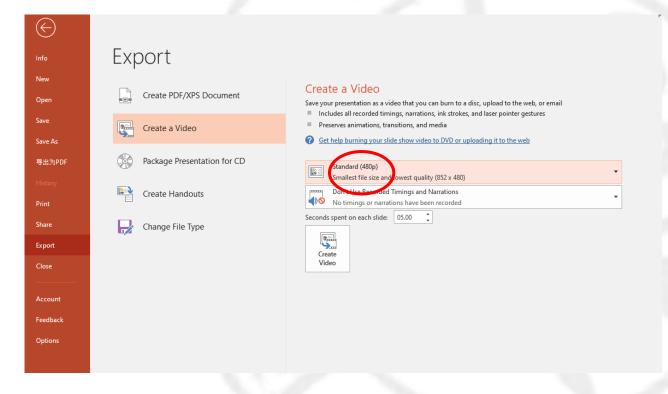
Final Project

- You have two options. Choose one to complete
- Homework 4 is merged with the project.
- Option 1: [Easier] Paper Reading and Record a 15-minitue video (For example: Video I upload for the class.)
- Option 2: [Harder] Design a specific ISA and AI-core to speedup your processor's computing for the neural network from HW3. Pick up 5 correct inference result and perform the entire inference on your design (using Verilog).

Option 1: Presentation



- Read paper, prepare a slides, and record your narrations using PowerPoint Record slide show functions. The video should be about 15 minutes.
- Export your recordings with the lowest video resolution (480p)
- To minimize the file, do not use any animation in your slides.



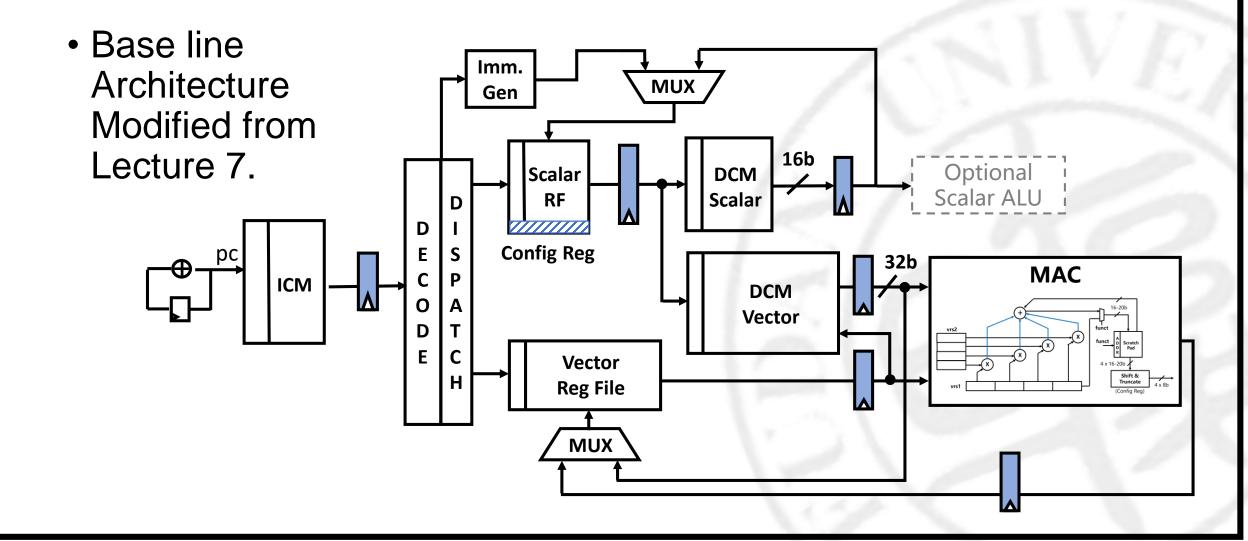
Option 2 (i) DLP Design

Assuming you are an engineer in charge of a deep learning processor (DLP) in a startup. Please use the architecture in the next slides as the base line, and design a specific ISA/AI-core to speedup your processor's computing for the neural network from HW3. Pick up 5 correct inference result and perform the entire inference on your design.

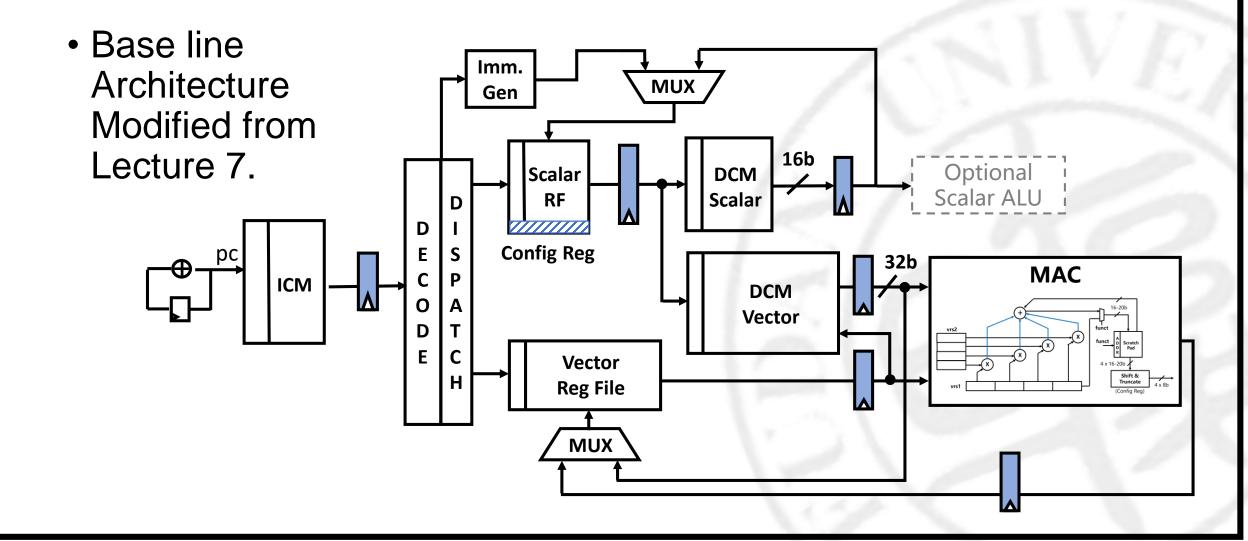
Additional architecture advance will be regarded as bonus.

Each team should only have 1 member.

Option 2 (ii) DLP Design



Option 2 (ii) DLP Design



Option 2 (iii) DLP Design

- Prepare a ppt to describe your design (including your simulation Results),
 and also answer question below:
- (a) What's your design throughput in terms of TMAC/s
- (b) What's your ideal utilization, and what's your real utilization in terms of MAC-Operation per second? Discuss the gap.
- (c) Compared with the ideal python computing result, is your implementation still correct? What's the score difference between your result and the python result?

Deadline

- Don't forget name and ID.
- The deadline is July 9th, 2021, 12am. (午夜12点)
- Submit the video/slides to faet_english@126.com