

R6331

16,777,216–Color, 1080RGB x 1920 -Dot Graphics Liquid Crystal Controller Driver for TFT Panel

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Description

The R63311 is liquid crystal controller driver LSI for TFT panel sized 1080RGB x 1920-dot at maximum. For high-speed data transfer, the R63311 supports MIPI DSI (2 lanes/3 lanes/4 lanes) as system interface to microcomputer. The R63311 also supports MIPI DBI Type C (Option 1 and 3), and I²C.

The R63311 incorporates step-up and voltage follower circuits to generate drive voltage required for TFT liquid crystal panel and a dynamic backlight control function to control backlight brightness depending on image data, reducing power consumption at the backlight with the slightest influence on image quality.

Other features include a power management function, making the R63311 best suitable for mid-sized portable devices with color graphics display such as digital mobile phones, PDAs, Smartphone, and photo frames.

*MIPI: Mobile Industry Processor Interface, *DSI: Display Serial Interface, *DBI: Display Bus Interface.

Features

- Single chip driver for 16, 777, 216-color TFT 1080RGB x 1920-dot graphics (with power supply circuits and supporting LTPS panel)
- Resolution: 1080RGB x 1920 , 1024RGB x(1600, 1280),960RGB x1280, 900RGB x1600,
800RGB x 1280, 768RGB x (1366, 1280,1024), 720RGB x 1280
- Command set (Compliant with MIPI DCS Version 1.01.00) *DCS: Display Command Set
- System interface
 - MIPI DSI : 2 data lanes / 3 data lanes / 4 data lanes and 1 clock lane
MIPI DSI: Version 1.01.00r11 21-Feb-2008 (Video Mode supported)
MIPI D-PHY: Version 1.00.00 14-May-2009
 - MIPI DBI Type C Option 1/Option 3 (MIPI DBI Version 2.00)
 - I²C (Inter-Integrated Circuit)
- Multi Interface function
- Abundant color display and drawing functions
 - 16,777,216-color display
 - RGB separate gamma correction function
 - Color Enhancement with skin tone correction function
 - Auto Contrast Optimization function
 - Outline sharpening function to improving quality of image
- Low-power consumption architecture (allowing direct input of interface I/O power supply)
 - Deep standby mode
 - Input power supply voltage:
 - Interface and logic power supply: IOVCC
 - Analog power supply: VCI,VSP,VSN
 - MIPI D-PHY power supply: DPHYVCC
- Advanced n-line inversion function for reducing power consumption of dot inversion panel without smear.
- Dynamic backlight control function
- Synchronization function for touch panel controller

- General Purpose Output function (GPO)
- Internal liquid crystal drive power supply circuit
 - Source driver and VCOM: VSP-AGND
VSN-AGND
 - DC power supply for VCOM drive: VCOMDC
 - Interface to the panel: VGH-AGND
AGND-VGL
- Interface to the panel: SOUT1-32
- Liquid crystal panel drive circuits: 1080 source signal lines (3mux)
- One-chip solution for COG module
- Internal NVM: Data can be rewritten up to 10 times.
- Dummy pins used to fix pin to IOVCC, or GND (see note 2)

Notes: 1. Japanese Patent No. 3,826,159

Korean Patent No. 747,636

United States Patent No. 7,176,870

2. Japanese Patent No. 3,980,066

United States Patent No. 6,323,930

Korean Patent No. 401,270

Taiwan Patent No. 175,413

Japanese Patent No. 4,226,627

United States Patent No. 6,924,868

Power Supply Specification

Table 1 R63311 Power Supply Specification

No.	Item	R63311
1	TFT data lines drive circuit	1080 outputs
2	Liquid crystal drive output	S1-S1080
		VCOMDC -2.00V ~ 2.00 V
3	Panel interface	SOUTn GVDD - GVSS
4	Input voltages	IOVCC (interface voltage) 1.65V ~ 3.30V (See note)
		VCI (power supply voltage for LCD drive) 2.50V ~ 3.30V
		DPHYVCC (MIPI DSI-PHYpower supply) 1.65V ~ 3.30V (See note)
5	System interface (MIPI DBI Type C, I ² C)	CSX, DCX, DIN, DOUT, IM[2:0], RESX IOVCC - GND (See note)
7	Differential small-amplitude interface (MIPI DSI)	CLKP/N, DATA0P/N, DATA1P/N DATA2P/N, DATA3P/N DPHYVCC - DPHYGND
8	LED I/F	LEDPWM IOVCC - GND (See note)
9	TN liquid crystal drive	PBCTLA1, PBCTLA2, PBCTLB1, PBCTLB2, High level: 3.0V ~ 5.6V Low level: GND
10	TPC synchronization signal	VSOUT, HSOUT IOVCC - GND (See note)
11	LCD drive supply voltages	VSP 4.5V ~ 6.0V (max.)
		VSN -4.5V ~ -6.0V (min.)
		VCL ~ -3.0V(min.)
		VGH 5.0V ~ 13.0V
		VGL -12.0V ~ -5.0V
		VGH-VGL Max. 30V

Note: Connect these power supplies to other power supplies on the FPC when they are set at the same electrical potential as other power supplies. For voltage, see DC Characteristics in Electrical Characteristics.

Block Diagram

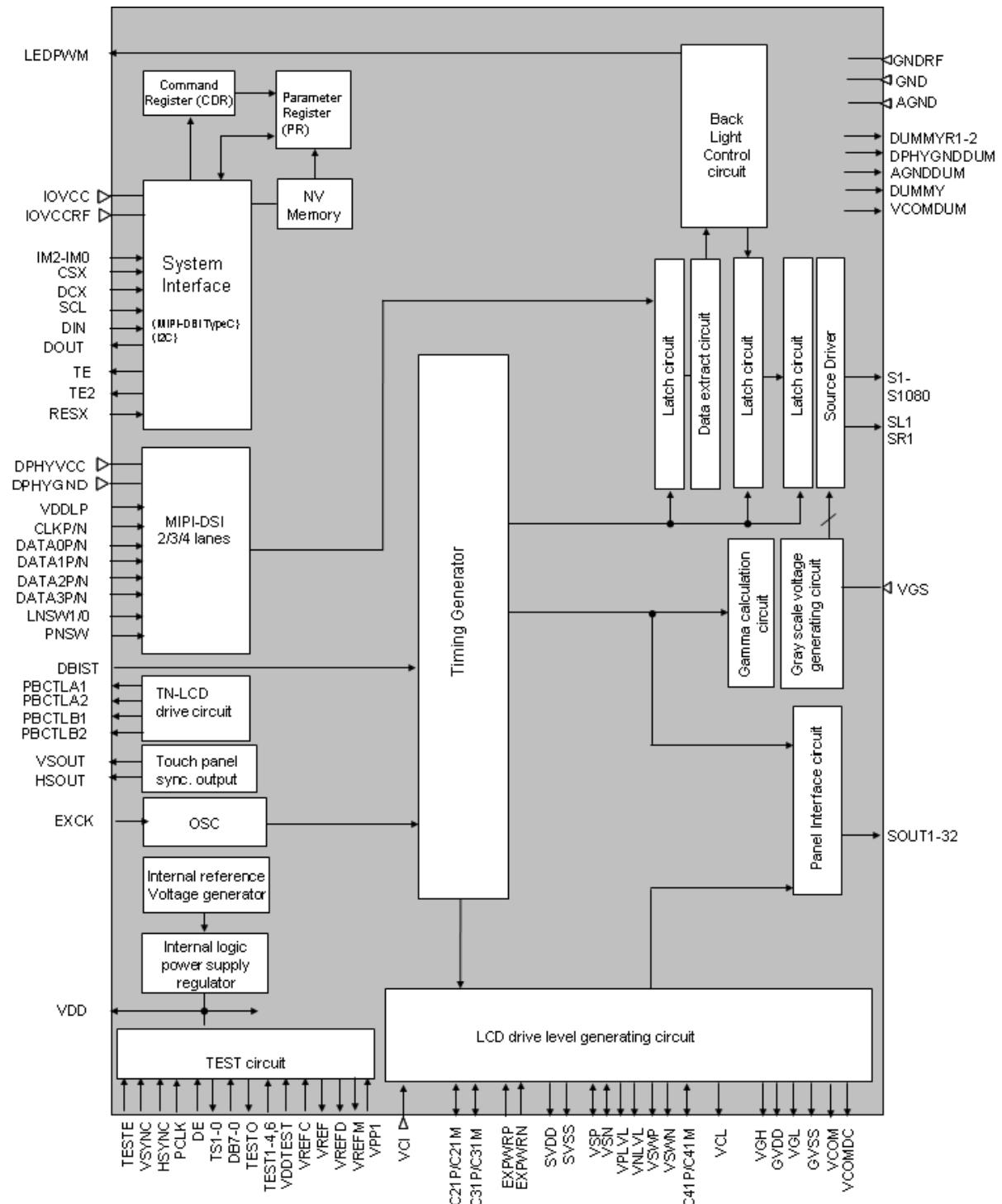


Figure 1

Block Function

(1) System Interface

The RSP LCD driver supports MIPI DSI Video Mode, MIPI DBI Type C (Option 1 and Option 3) and I²C.

The RSP LCD driver supports multi interface. A primary interface is set by the IM pins. A secondary interface is set by the SIMEN and SIM registers. For the setting, see “Multi Interface.”

Table 2

IM2	IM1	IM0	Interface	Used pin	Number of available colors
0	0	0	I ² C(Notes 1 and 2)	DIN	-
0	0	1	Setting disabled	-	-
0	1	0	MIPI DBI Type C 9bits (Option 1) (Note 1)	DIN, DOUT	-
0	1	1	MIPI DBI Type C 8bits (Option 3) (Note 1)	DIN, DOUT	-
1	0	0	Setting disabled	-	-
1	0	1	Setting disabled	-	-
1	1	0	MIPI DSI	DATA0P/N, DATA1P/N, DATA2P/N, DATA3P/N	65,536/262,144/16,777,216
1	1	1	Setting disabled	-	-

Notes: 1. For details, see “System Interface Configuration (I²C)”.

2. The DM register chooses interface to be used as display interface from MIPI DBI Type C.

(a) MIPI DSI

The RSP LCD driver supports MIPI DSI. The number of data lanes can be chosen by setting register.

Table 3 Function

SEL_DL[1:0]	Number of lanes	Enabled pins	Disabled pin
'h0	Setting disabled	—	All (CLKP/N, DATA0P/N, DATA1P/N, DATA2P/N, DATA3P/N)
'h1	2	CLKP/N, DATA0P/N, DATA1P/N	DATA2P/N, DATA3P/N
'h2	3	CLKP/N, DATA0P/N, DATA1P/N, DATA2P/N	DATA3P/N
'h3	4	All (DATA0P/N, DATA1P/N, DATA2P/N, DATA3P/N)	—

(b) MIPI DBI Type C (Option 1 and Option 3)

The RSP LCD driver supports 9-bit (Option 1) and 8-bit (Option 3) serial interface that uses signals CSX, DCX, SCL, DIN, and DOUT.

(2)Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the gamma correction registers. RGB separate gamma correction setting enables maximum 16,777,216-color display.

(3)LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates voltage levels to drive the liquid crystal panel.

(4)Timing Generator

The timing generator is used to generate timing signals for operating internal circuits.

(5)Oscillator (OSC)

The RSP LCD driver incorporates an oscillator.

(6)LCD Driver Circuit

The LCD driver circuit has the 1080-channels source driver (S1-S1080). When 1080RGB pixels of data are input, the display pattern data is latched. The voltage is output from the source driver according to the latched data.

(7)Panel Interface Circuit

The panel interface circuit generates and outputs the interface signals (SOUTn) to the TFT panel.

(8)Internal Logic Power Supply Regulator

The internal logic power supply regulator generates power supply for the internal logic circuit.

(9)Backlight Control Circuit

The backlight control circuit adjusts backlight brightness according to the histogram of image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

(10)NVM

The RSP LCD driver supports NVM that stores manufacturer command setting values.

(11)TN-LCD drive Circuit

The RSP LCD driver can output signals for TN liquid crystal panel different from the display liquid crystal panel. There are two output pins for the control signals. These pins can change the output of alternating signals and two drive systems can be supported.

(12) Synchronization signal Output for touch panel controller

The RSP LCD driver can output the synchronization signals to capture touch sensing signal for touch panel controller. To use these signals, touch panel controller can capture touch sensing signal while avoiding display changing noise.

Pin Function

Table 4 External Power Supply Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VCI	I	Power supply Stabilizing capacitor	Power supply to analog circuit. VCI < 0.3V (When power is turned off.)	Power supply Stabilizing capacitor
IOVCC	I	Power supply Stabilizing capacitor	Power supply to interface pins. IOVCC < 0.3V (When power is turned off.)	Power supply Stabilizing capacitor
IOVCCRF	I	Power supply	Connect to IOVCC on the FPC to prevent noise in case of COG.	Power supply
DPHYVCC	I	Power supply Stabilizing capacitor	Power supply to MIPI DSI D-PHY Connect to IOVCC on the FPC when DPHYVCC is set at the same electrical potential as IOVCC.	Power supply Stabilizing capacitor
GND	I	Power supply	GND for internal logic and interface pins. GND=0V.	Power supply
GNDRF	I	Power supply	Connect to GND on the FPC to prevent noise in case of COG.	Power supply
AGND	I	Power supply	Analog GND (logic regulator and LCD power supply circuit). AGND = 0V. Connect to GND on the FPC to prevent noise in case of COG.	Power supply
DPHYGND	I	Power supply	GND for MIPI DSI D-PHY Connect to GND on the FPC to prevent noise in case of COG.	Power supply

Table 5 System Interface Pins (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
IM2-0	I	IOVCC or GND	Interface select signal. Select interface from MIPI DSI and MIPI DBI Type C (Option 1 and Option 3) and I ² C.	IOVCC or GND
RESX	I	Host Processor or external RC circuit	Reset pin. The RSP LCD driver is initialized when RESX is Low. Make sure to execute power-on reset when turning power supply on.	Host Processor or external RC circuit
TE	O	Host processor	Tearing effect output signal. Leave it open when not in use.	Open

Table 6 MIPI Type C/ I²C Pins (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
CSX	I	Host Processor	Chip select signal. Low: Select (Accessible) High: Not Select (Inaccessible) Make sure to connect to the host processor and control following AC characteristics.	IOVCC
DCX	I	Host Processor	Command/data select signal. Low: Select command High: Select data	IOVCC
SCL	I	Host Processor	A synchronous clock signal in MIPI DBI Type C and I ² C operation.	IOVCC
DIN	I/O	Host Processor	A serial data input pin in MIPI Type C operation to input data on the rising edge of the SCL signal. A serial input/output and ACK output pin in I ² C operation.	IOVCC or GND
DOUT	O	Host Processor	A serial data output pin in MIPI DBI Type C operation.	Open

Table 7 MIPI DSI Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
CLKP	I	Host Processor	MIPI DSI Clock (+).	DPHYGND
CLKN	I	Host Processor	MIPI DSI Clock (-).	DPHYGND
DATA0P	I/O	Host Processor	MIPI DSI (+).	DPHYGND
DATA0N	I/O	Host Processor	MIPI DSI (-).	DPHYGND
DATA1P	I	Host Processor	MIPI DSI (+).	DPHYGND
DATA1N	I	Host Processor	MIPI DSI (-).	DPHYGND
DATA2P	I	Host Processor	MIPI DSI (+).	DPHYGND
DATA2N	I	Host Processor	MIPI DSI (-).	DPHYGND
DATA3P	I	Host Processor	MIPI DSI (+).	DPHYGND
DATA3N	I	Host Processor	MIPI DSI (-).	DPHYGND
DPHYGNDD MY1 - 4	I/O	Open or GND	When MIPI DSI is used, DPHYGNDDMY must be put on the FPC and fixed to GND. When DSI is not used, DPHYGNDDMY can be used to fix GND potential across the CLKP/N pin and DataxP/N pin.	Open

Table 8 LED Driver Control Pins (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
LEDPWM	O	LED driver	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High). When light is turned on, LEDPWM is High. When light is turned off, LEDPWM is Low.	Open

Table 9 VSP External Application Control Pin (Amplitude: VSP – AGND)

Signal	I/O	Connect to	Function	Connection when signal is unused
EXPWRP	I	VSP or AGND	A pin to determine whether voltage is externally applied to VSP. High: Voltage is externally applied to them. Low: Voltage is not externally applied to them. (The RSP LCD driver operates by internal power supply)	AGND

Table 10 VSN External Application Control Pin (Amplitude: VSP – AGND)

Signal	I/O	Connect to	Function	Connection when signal is unused
EXPWRN	I	VSP or AGND	A pin to determine whether voltage is externally applied to VSN. High: Voltage is externally applied to them. Low: Voltage is not externally applied to them. (The RSP LCD driver operates by internal power supply)	AGND

Table 11 Power Supply Circuit Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VDD	O	Stabilizing capacitor	A pin to output voltage from internal logic power supply regulator. Connect to stabilizing capacitor.	Stabilizing capacitor
VDDLP	O	Stabilizing capacitor	internal LDO output (1.2V typical). Used as power supply for the MIPI low power receiver.	Stabilizing capacitor
VSP	O	Stabilizing capacitor	A pin to output positive step-up voltage for the source driver and the gamma circuit.	Stabilizing capacitor
SVDD	O	Stabilizing capacitor	Internal LDO output. Used as the analog power supply instead of VSP.	Stabilizing capacitor
VSWP	O	N-channel MOSFET	A pin to output on/off control signal of external N-channel MOSFET when VSP is generated by a switching regulator method (VCI-GND amplitude). For details, see "Power Supply Generating Circuit". When using external VSP supply, VSWP is fixed to GND.	Open
VSN	O	Stabilizing capacitor	A pin to output negative step-up voltage for the source driver and the gamma circuit.	Stabilizing capacitor
SVSS	O	Stabilizing capacitor	Internal LDO output. Used as the analog power supply instead of VSN.	Stabilizing capacitor
VSWN	O	P-channel MOSFET	A pin to output on/off control signal of external P-channel MOSFET when VSN is generated by a switching regulator method (VCI-GND amplitude). For details, see "Power Supply Generating Circuit". When using external VSN supply, VSWN is fixed to VSP.	Open
VGH	O	Stabilizing capacitor	Output voltage from step-up circuit 2.	Stabilizing capacitor
GVDD	O	Liquid crystal panel, Stabilizing capacitor	Internal regulator output for liquid crystal driving power supply. A pin to output positive voltage for the liquid crystal panel.	Stabilizing capacitor
VGL	O	Stabilizing capacitor	Output voltage from step-up circuit 2.	Stabilizing capacitor
GVSS	O	Liquid crystal panel, Stabilizing capacitor	Internal regulator output for liquid crystal driving power supply. A pin to output negative voltage for the liquid crystal panel.	Stabilizing capacitor

C21P/M, C31P/M,	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit. For details, see "Power Supply Generating Circuit."	Stabilizing capacitor
C41P/M	I/O	Step-up capacitor	Capacitor connection pins for step-up VCL generator.	Stabilizing capacitor
VCL	O	Stabilizing capacitor	Internal analog power supply for VCOMDC generator. Connect to stabilizing capacitor.	Stabilizing capacitor

Table 12 Liquid Crystal Drive Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VCOMDC	O	Stabilizing capacitor	VCOMDC level, which is set by internal electronic volume (VDC).	Open
VCOM	O	Liquid crystal panel	VCOM level, which is supplied to the liquid crystal panel.	Open
VGS	I	Power supply	Reference level of the grayscale voltage generating circuit (GND level). Connect to GND on the FPC prevent noise in case of COG.	Power supply
VPLVL	O	Open	Positive reference voltage for the liquid crystal panel. Put on the FPC to monitor voltage.	Open
VNLVL	O	Open	Negative reference voltage for the liquid crystal panel. Put on the FPC to monitor voltage.	Open
S1-S1080	O	Liquid crystal panel	Liquid crystal application voltages.	Open
SL1	O	Liquid crystal panel	When using ZigZag inversion mode, it connects with Liquid crystal panel	Open
SR1	O	Liquid crystal panel	When using ZigZag inversion mode, it connects with Liquid crystal panel	Open

Table 13 Liquid Crystal Panel Power Supply Interface Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
SOUT1-32	O	Liquid crystal panel	Panel control signals	Open

Table 14 TN Liquid Crystal Drive Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
PBCTLA1	O	Liquid crystal panel	GPO to drive TN liquid crystal panel different from the display panel.	Open
PBCTLA2	O	Liquid crystal panel	GPO to drive TN liquid crystal panel different from the display panel.	Open
PBCTLB1	O	Liquid crystal panel	GPO to drive TN liquid crystal panel different from the display panel.	Open
PBCTLB2	O	Liquid crystal panel	GPO to drive TN liquid crystal panel different from the display panel.	Open

Table 15 TPC synchronization pin

Signal	I/O	Connect to	Function	Connection when signal is unused
VSOUT	O	Host Processor	Signal to synchronize LCD driver and touch panel controller. (Vertical scan)	Open
HSOUT	O	Host Processor	Signal to synchronize LCD driver and touch panel controller. (Horizontal scan)	Open

Table 16 Clock External Application Control pin (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
EXCK	I	Host Processor	External clock input pin. The internal clock and the external supply clock can be switched by register control.	GND

Table17 DSI Pin Arrangemanet Control pin (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function						Connection when signal is unused																																																
LNSW1/0 PNSW	I	IOVCC or GND	LNSW1/0 control swapping MIPI Lane <table border="1"> <tr> <td>LNSW1/0</td><td colspan="5">Pin arrangement(bump to top)</td> </tr> <tr> <td>Low/Low</td><td>DATA3</td><td>DATA2</td><td>CLK</td><td>DATA1</td><td>DATA0</td></tr> <tr> <td>Low/High</td><td>DATA3</td><td>DATA0</td><td>CLK</td><td>DATA1</td><td>DATA2</td></tr> <tr> <td>High/Low</td><td>DATA0</td><td>DATA1</td><td>CLK</td><td>DATA2</td><td>DATA3</td></tr> <tr> <td>High/High</td><td>DATA2</td><td>DATA1</td><td>CLK</td><td>DATA0</td><td>DATA3</td></tr> </table> PNSW control Polarity of MIPI Pin <table border="1"> <tr> <td>PNSW</td><td colspan="5">Pin arrangement(bump to top)</td> </tr> <tr> <td>Low</td><td>DATAxN</td><td>DATAxP</td><td>CLKxN</td><td>CLKxP</td><td></td></tr> <tr> <td>High</td><td>DATAxP</td><td>DATAxN</td><td>CLKxP</td><td>CLKxN</td><td></td></tr> </table>						LNSW1/0	Pin arrangement(bump to top)					Low/Low	DATA3	DATA2	CLK	DATA1	DATA0	Low/High	DATA3	DATA0	CLK	DATA1	DATA2	High/Low	DATA0	DATA1	CLK	DATA2	DATA3	High/High	DATA2	DATA1	CLK	DATA0	DATA3	PNSW	Pin arrangement(bump to top)					Low	DATAxN	DATAxP	CLKxN	CLKxP		High	DATAxP	DATAxN	CLKxP	CLKxN		GND
LNSW1/0	Pin arrangement(bump to top)																																																								
Low/Low	DATA3	DATA2	CLK	DATA1	DATA0																																																				
Low/High	DATA3	DATA0	CLK	DATA1	DATA2																																																				
High/Low	DATA0	DATA1	CLK	DATA2	DATA3																																																				
High/High	DATA2	DATA1	CLK	DATA0	DATA3																																																				
PNSW	Pin arrangement(bump to top)																																																								
Low	DATAxN	DATAxP	CLKxN	CLKxP																																																					
High	DATAxP	DATAxN	CLKxP	CLKxN																																																					

PNSW	LNSW		CLKP(Pin)	CLKN(Pin)	DATA0P(Pin)	DATA0N(Pin)	DATA1P(Pin)	DATA1N(Pin)	DATA2P(Pin)	DATA2N(Pin)	DATA3P(Pin)	DATA3N(Pin)	
	[1]	[0]											
0	0	0	CLKN	CLKP	DATA1N	DATA1P	DATA2N	DATA2P	DATA3N	DATA3P	DATA0N	DATA0P	
0	0	1	CLKN	CLKP	DATA1N	DATA1P	DATA0N	DATA0P	DATA3N	DATA3P	DATA2N	DATA2P	
0	1	0	CLKN	CLKP	DATA2N	DATA2P	DATA1N	DATA1P	DATA0N	DATA0P	DATA3N	DATA3P	
0	1	1	CLKN	CLKP	DATA0N	DATA0P	DATA1N	DATA1P	DATA2N	DATA2P	DATA3N	DATA3P	
1	0	0	CLKP	CLKN	DATA1P	DATA1N	DATA2P	DATA2N	DATA3P	DATA3N	DATA0P	DATA0N	
1	0	1	CLKP	CLKN	DATA1P	DATA1N	DATA0P	DATA0N	DATA3P	DATA3N	DATA2P	DATA2N	
1	1	0	CLKP	CLKN	DATA2P	DATA2N	DATA1P	DATA1N	DATA0P	DATA0N	DATA3P	DATA3N	
1	1	1	CLKP	CLKN	DATA0P	DATA0N	DATA1P	DATA1N	DATA2P	DATA2N	DATA3P	DATA3N	

Table 18 The test free-running mode Control pin (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused						
DBIST	I	IOVCC or GND	<p>Enables the Test Image Generation function</p> <table border="1"> <tr> <td>DBIST</td><td>Test Image Generator</td></tr> <tr> <td>Low</td><td>Off</td></tr> <tr> <td>High</td><td>On</td></tr> </table>	DBIST	Test Image Generator	Low	Off	High	On	GND
DBIST	Test Image Generator									
Low	Off									
High	On									

Table 19 Other Pins (Test and Dummy)

Signal	I/ O	Connect to	Function	Connection when signal is unused
DUMMYR1-2	O	Open	Dummy pins to measure contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the LSI.	Open
TESTE	I	GND	Test pins. Connect to GND	GND
TEST1-4,6	I	Open or GND	Test pins. Fix to GND or leave open.	Open or GND
VDDTEST	I	GND	Test pins. Fix to GND or leave open.	Open or GND
VREFC	I	GND	Test pins. Fix to GND or leave open.	Open or GND
VREF	O	Open	Test pin. Leave open.	Open
VREFD	O	Open	Test pin. Leave open.	Open
VREFM	O	Open	Test pin. Leave open.	Open
TE2	O	Open	Test pin. Leave open.	Open
VSYNC HSYNC PCLK DE	I	Open or GND	Test pins. Fix to GND or leave open.	Open or GND
DB7-1	I	Open or GND	Test pins. Fix to GND or leave open.	Open or GND
TS1-0	O	Open	Test pin. Leave open.	Open
TESTO	O	Open	Test pin. Leave open.	Open
VPP1	I	Open or AGND	Test pin. Fix to AGND or leave open. To leave open, do not pull out ITO wiring.	Open or AGND
DPHYGNDDUM AGNDDUM	O	Open or Fixed pin	Pins to fix electrical potential. Do not use them for other purposes. The electrical potential can be fixed by connecting unused interface pins and test pins to these dummy pins on the glass. Leave them open when they are not used.	Open
DUMMY	O	Open	Dummy pins. Leave open.	Open
VCOMDUM	O	Open	Dummy pins. Leave open.	Open

Power Supply Generating Circuit

The following figure shows the configuration of liquid crystal drive voltage generating circuit of the R63311.

Power Supply Circuit Connection Example 1 (VSP and VSN: Generated by Switching Regulator Method)

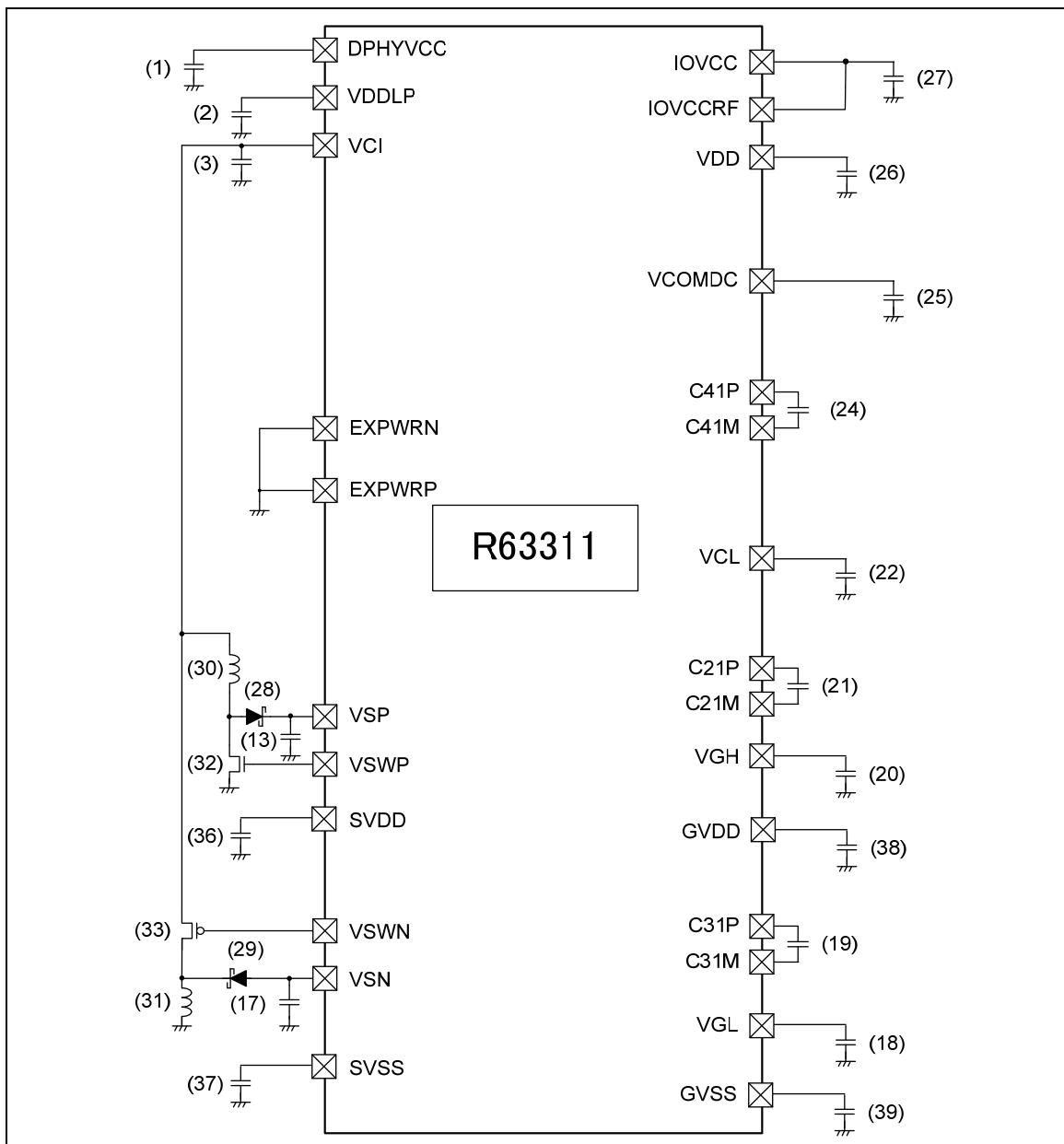


Figure 2

Power Supply Circuit Connection Example 2 (VSP and VSN: External supply Method)

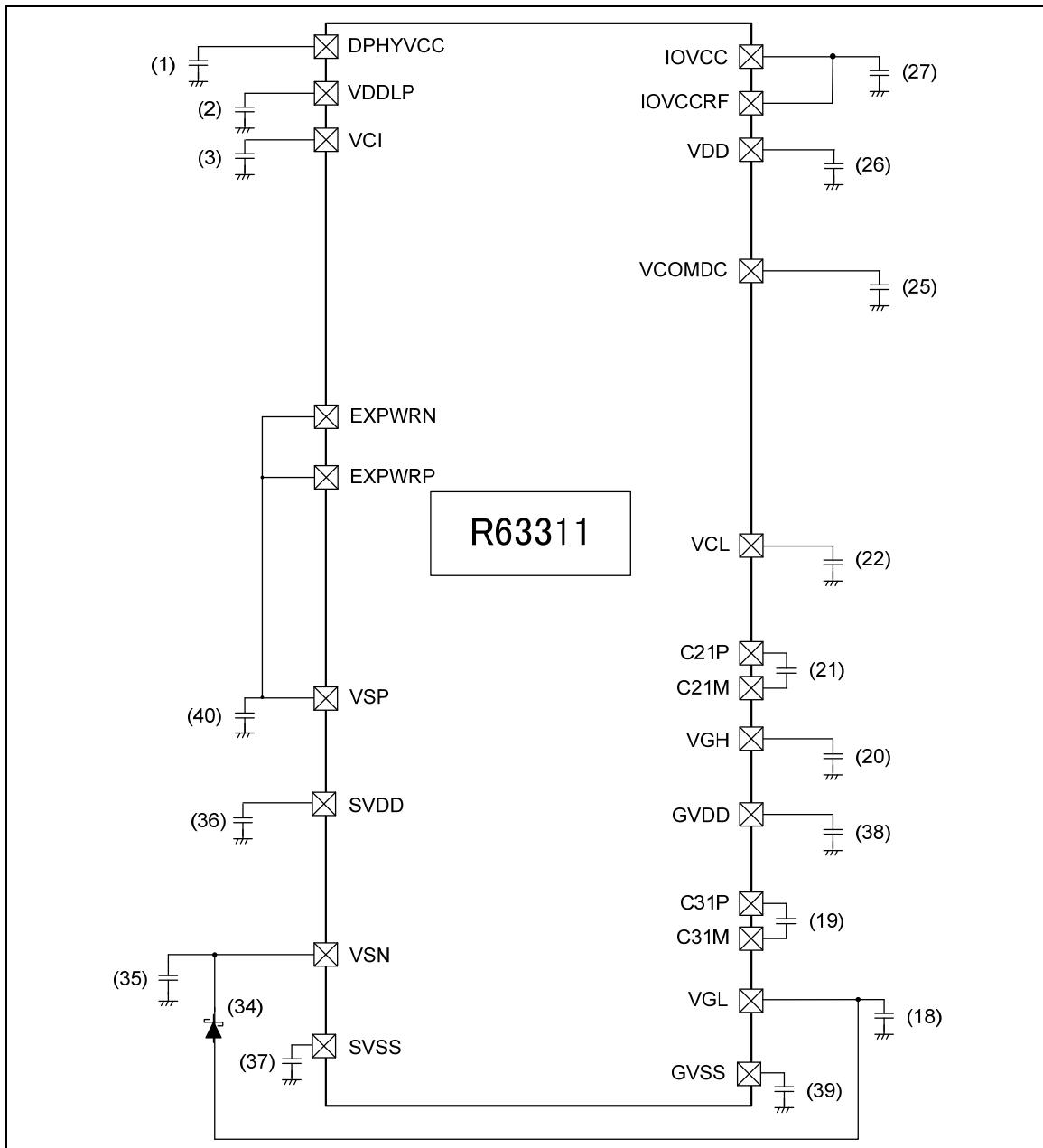


Figure 3

Power Supply Circuit Connection Example 3 (VSP: External supply Method, VSN: Generated by Switching Regulator Method)

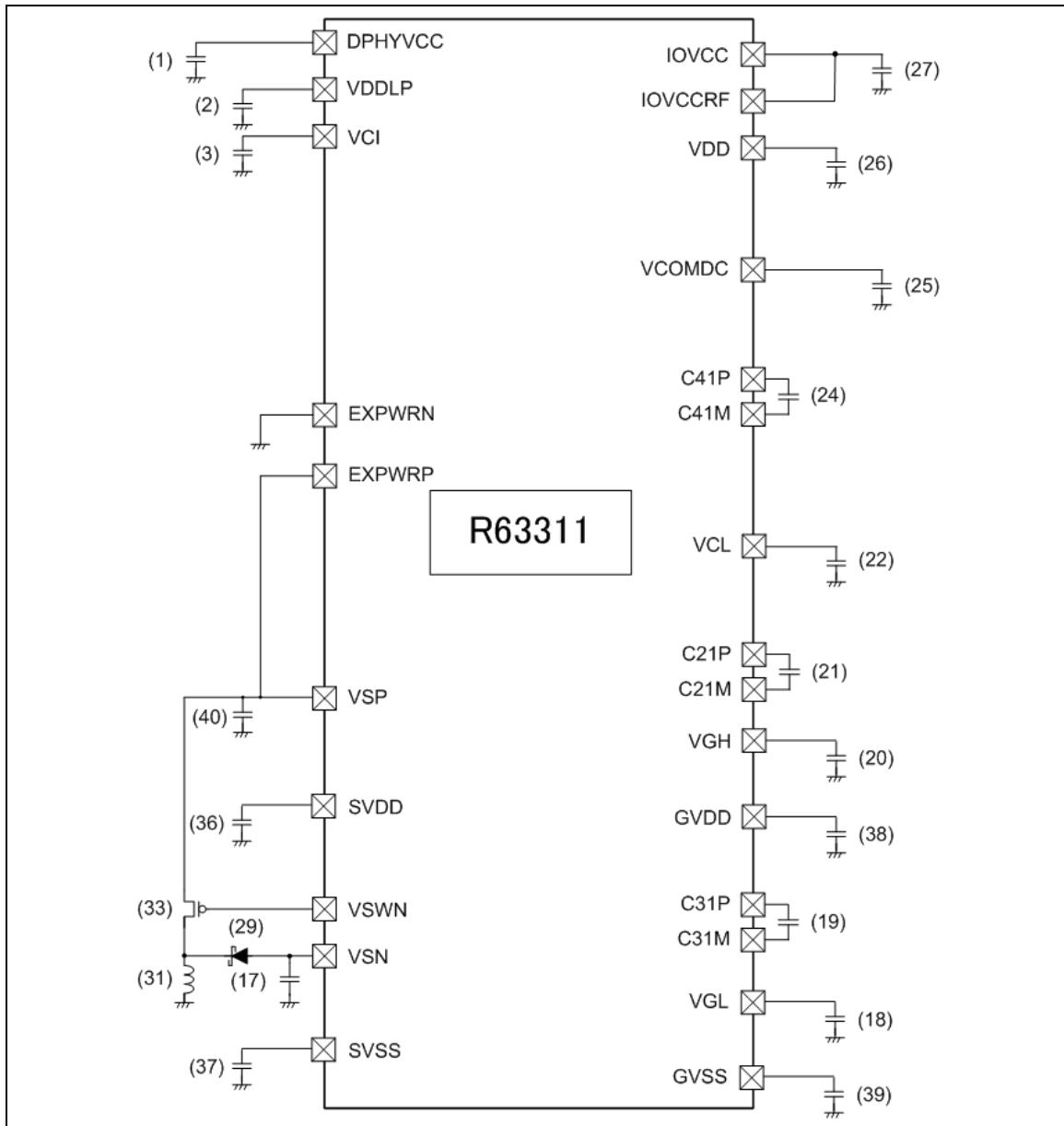


Figure 4

Specifications of External Elements Connected to the Power Supply Circuit

The following table shows specifications of external elements connected to the R63311's power supply circuit. The numbers of the connection pins correspond to the numbers shown in "Power Supply Generating Circuit."

Table 20 Capacitor Specifications

Capacitor	Recommended voltage	Pins to connect
1μF (B characteristics)	3V	(2) VDDLP
	6V	(22) VCL, (24) C41P/M,
2.2μF (B characteristics)	3V	(26) VDD,
2.2μF (B characteristics)	6V	(1) DPHYVCC, (3) VCI, (25) VCOMDC, (27) IOVCC,
2.2μF (B characteristics)	10V	(35) VSN (External Supply Method), (40) VSP (External Supply Method)
4.7μF (B characteristics)	10V	(13) VSP, (17) VSN (Switching Regulator Method), (36)SVDD, (37)SVSS
1.0μF (B characteristics)	25V	(18) VGL, (21) C21P/M, (19) C31P/M, (20) VGH, (38)GVDD, (39)GVSS

Table 21 Schottky Diode Specifications

Specifications	Pins to connect
VF<0.38V/200 mA, VR=10V/10uA at 25°C (Recommended diode: HRC0201A) or VF < 0.38V/300 mA, VR=10V/10 uA at 25°C (when load current on panel is large)	(28) VSP – NMOS, (29) VSN – PMOS
VF < 0.4V/20mA@25°C, VR ≥ 25V (Recommended diode: HSC226)	(34) VSN – VGL (External VSP/VSN mode)

Table 22 Inductor Specifications

Specifications	Pins to connect
2.2~10 μH, Rdc ≤ 1Ω, Imax ≥ 300mA	(30) VCI – NMOS, (31) GND – PMOS

Table 23 Transistor Specifications

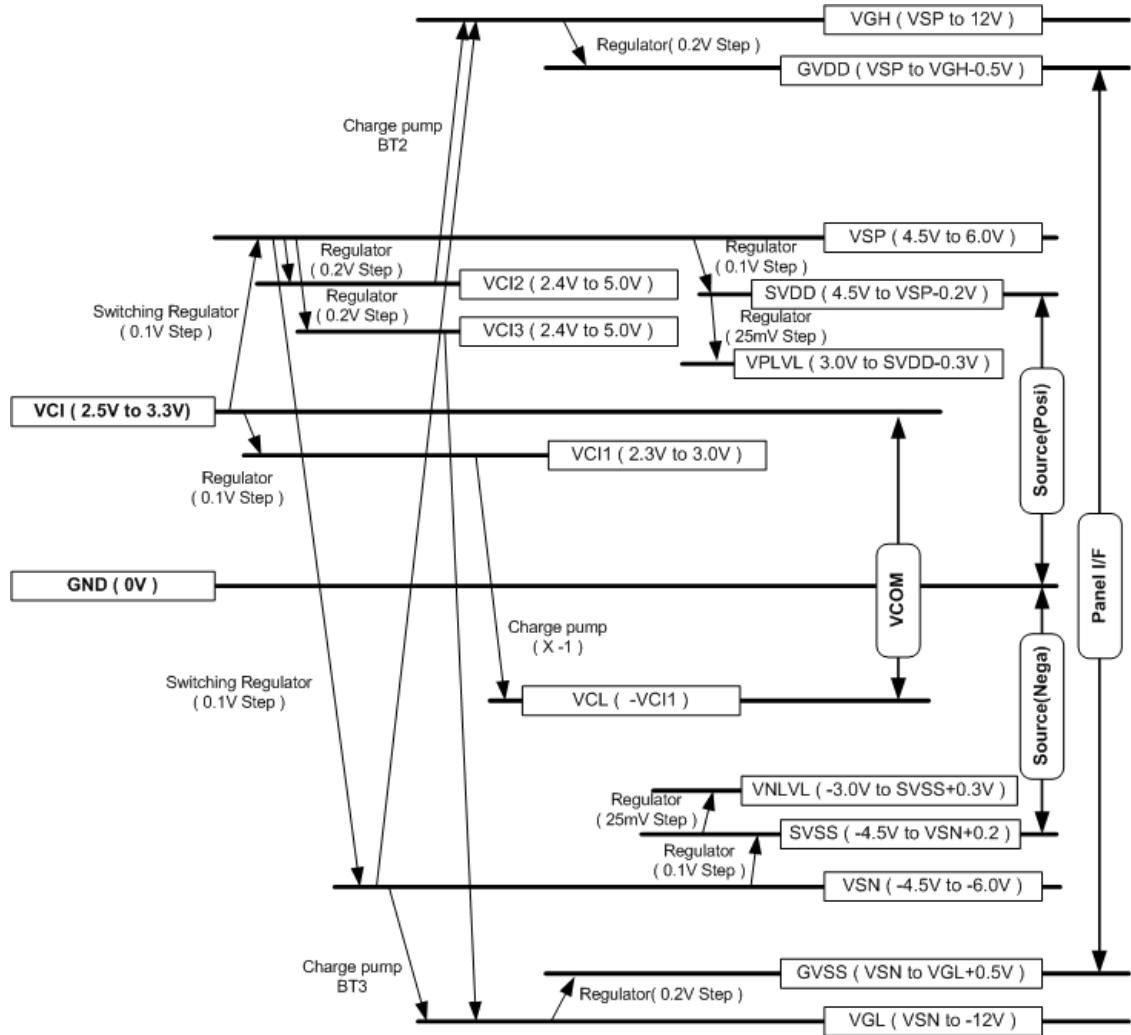
Specifications	Pins to connect
PMOS Ron < 1Ω, VDS > 16V, VGS > 6V Toff < 50ns, Qg < 3nC ID > 200mA (Duty Cycle = 0.5)	(33) VCI – Schottky Diode(VSP is generated by switching regulator) (33)VSP- Schottky Diode(VSP is external supply)
NMOS Ron < 1Ω, VDS > 10V, VGS > 6V Toff < 50ns, Qg < 3nC ID > 200mA (Duty Cycle = 0.5)	(32) GND – Schottky Diode

Note: Connecting a bypass capacitor between VCI, DPHYVCC, and IOVCC.

Voltage Setting Pattern Diagram

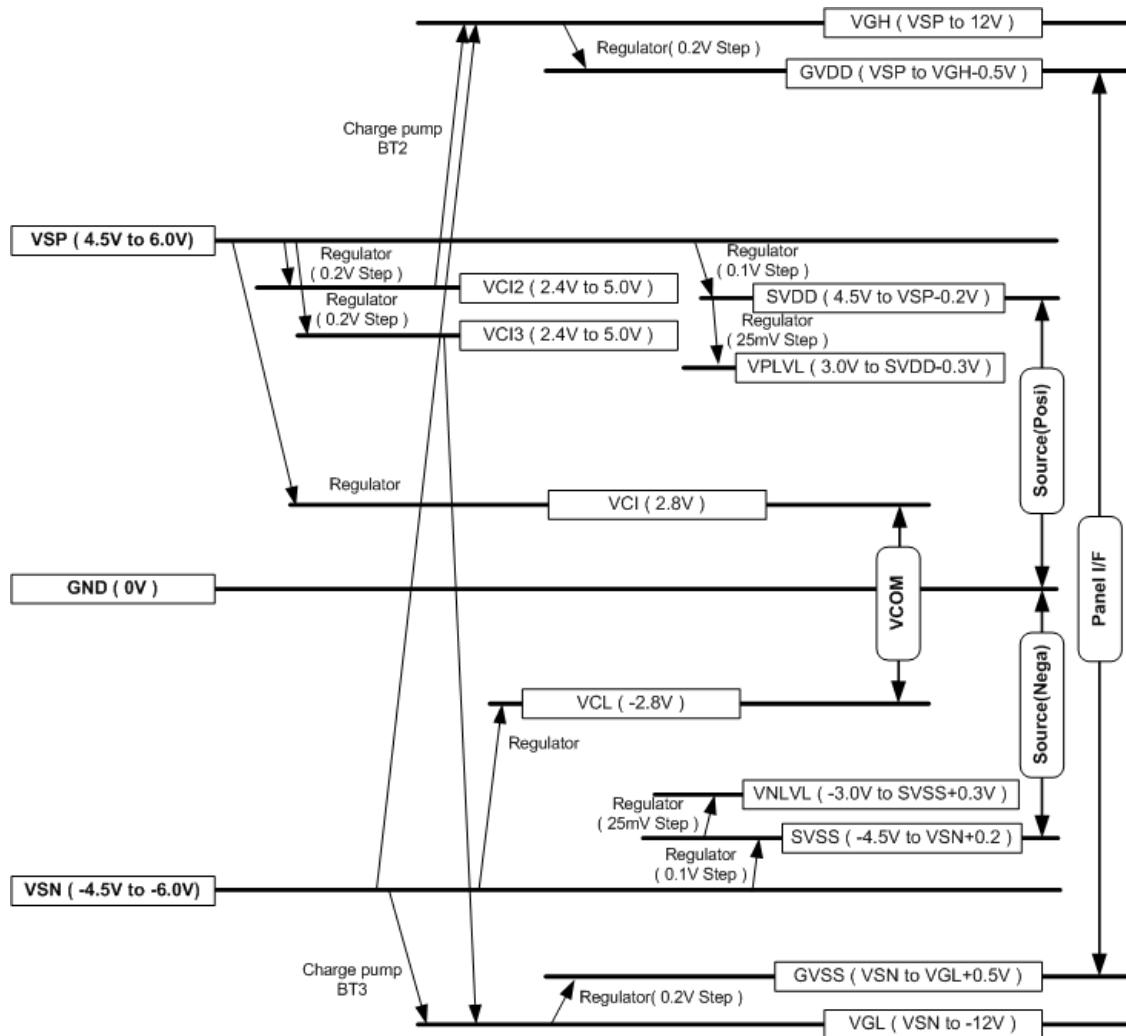
Voltage Setting Pattern Diagram (Generated by Switching Regulator)

The following are the diagrams of voltage generation using internal mode with Switching Regulator in the R63311 and the relationship between TFT display application voltages.



Voltage Setting Pattern Diagram (External Supply)

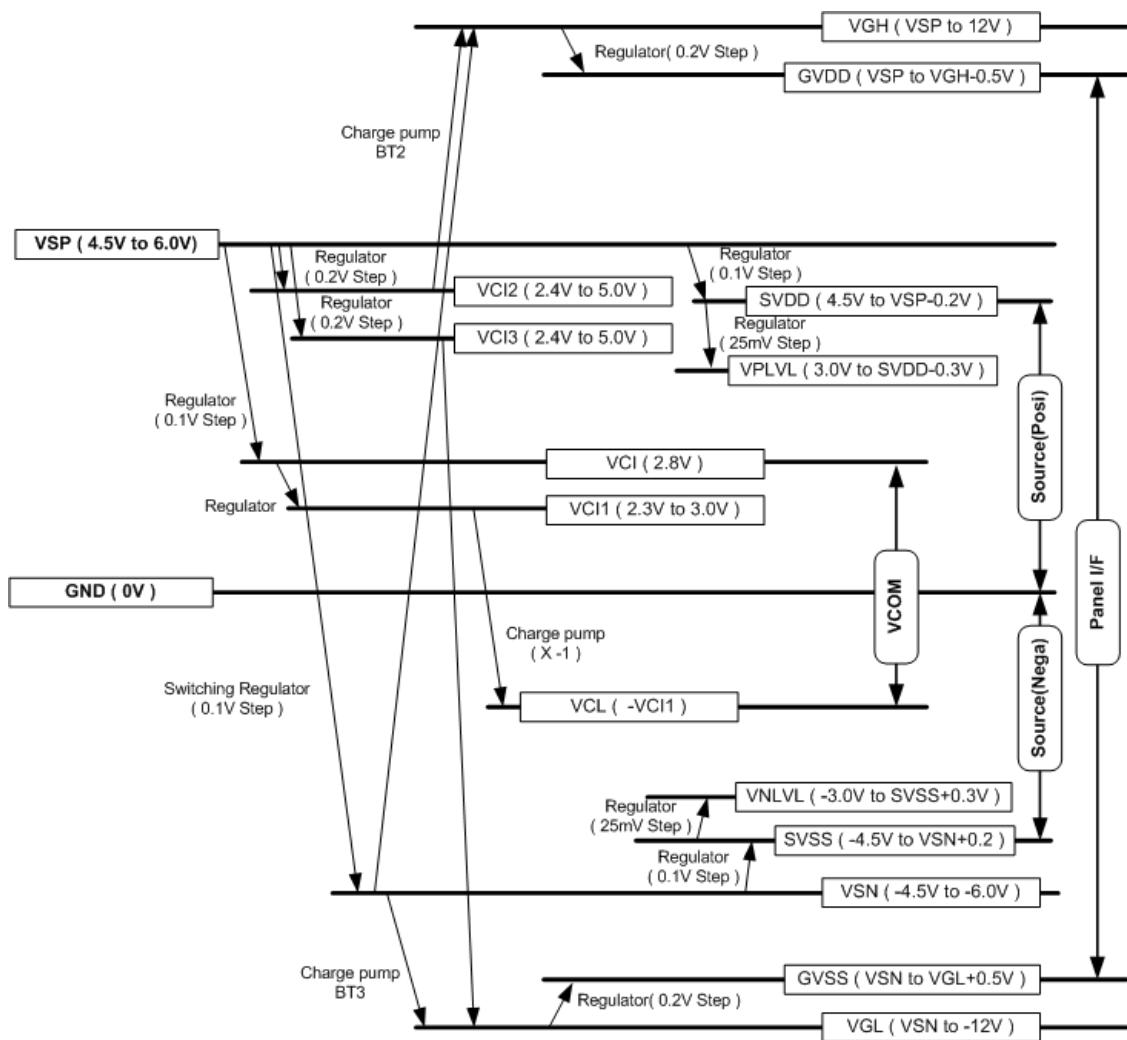
The following are the diagrams of voltage generation using External VSP/VSN supply in the R63311 and the relationship between TFT display application voltages.



Voltage Setting Pattern Diagram

(VSP: External Supply, VSN: Generated by Swithing Regulator)

The following are the diagrams of voltage generation using External VSP Supply and VSN generated by Swiching Regulator in the R63311.and the relationship between TFT display application voltages.



Notes: 1. Make sure that the following relationships are satisfied:

$$(VSP-SVDD) \geq 0.2V$$

$$(SVDD-VPLVL) \geq 0.3V$$

$$(VSN-SVSS) \geq -0.2V$$

$$(SVSS-VNLVL) \geq -0.3V$$

2. The above voltage ranges are recommended.

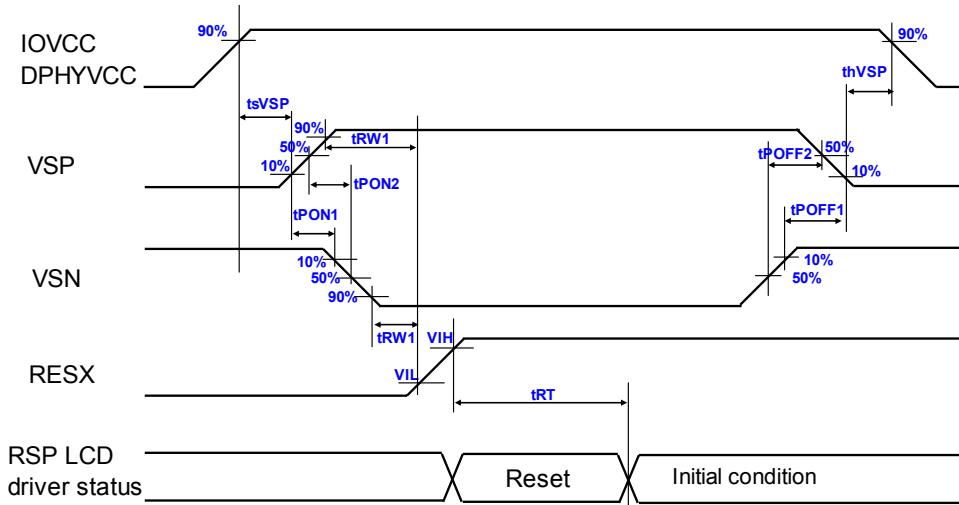
3.VCI1,VCI2,VCI3 is internal voltage.

External VSP/VSN Supply mode

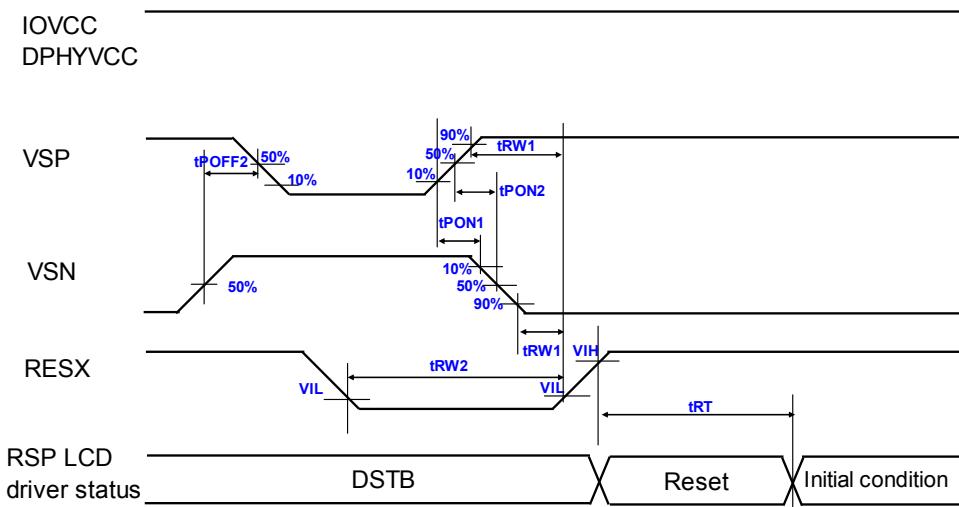
R63311 can be operated by supplying VSP and VSN power supply directly. This operation mode is effective by EXPWRP pin = VSP and EXPWRN pin = VSN.

Refer to "Power Supply Generating Circuit" for detail.

a) Power On Sequence



b) Deep standby mode Sequence



Item	Symbol	Unit	Test Condition	Min	Max
VSP-VSN delay time(10% to 10%)	tPON1	us	Power On	0	—
VSP-VSN delay time(50% to 50%)	tPON2	us	Power On	0	—
System power on to VSP ON time	tsVSP	ms	Power On	1	—
Reset low-level width1	tRW1	ms	Power On	1	—
Reset low-level width2	tRW2	ms	Power Off	1	—
Reset time(Sleep IN)	tRT	ms	Power On	3	—
VSN-VSP delay time(10% to 10%)	tPOFF1	us	Power Off	0	—
VSN-VSP delay time(50% to 50%)	tPOFF2	us	Power Off	0	—
VSP OFF to system power off time	thVSP	us	Power Off	0	—

Figure 5 Power supply on sequence

Notes: 1. Make sure that the following relationships are power supply sequence.

Reset

The RSP LCD driver is initialized by reset input. During the reset period, the RSP LCD driver is set to its internal initial setting and no command is accepted from the processor. The source driver unit and the power supply circuit unit are also reset to the respective initial states when reset signal is input to the RSP LCD driver.

(1) Command Default Values

The initial states of commands are shown in the “register map” table. See “register map” The command setting is initialized to the default value when a hardware reset is executed.

(2) Initial States of Input/Output Pins and Output Pins

A table below shows initial states of input/output pins and output pins after reset.

Table 24 Initial States of Input/Output Pins and Output Pins after Reset

Pin name	Pin state	Pin name	Pin state
VSP	VCI(case by VCI external input)	VSOUT	GND
VSN	GND(case by VCI external input)	HSOUT	GND
VPLVL	Hi-Z	DIN	note1
VNLVL	Hi-Z	DOUT	GND
VCL	GND	LEDPWM	GND
VGH	VCI(case by VCI external input) VSP(case by VSP external input)	DATA0P/N	Hi-Z
VGL	GND(case by VCI external input) VSN(case by VSN external input)	DATA1P/N	Hi-Z
VSWP	GND	DATA2P/N	Hi-Z
VSWN	VCI	DATA3P/N	Hi-Z
GVDD	GND	C21P	Hi-Z
GVSS	GND	C21M	Hi-Z
SVDD	VCI	C31P	Hi-Z
SVSS	GND	C31M	Hi-Z
VGS	GND	C41P	VCI
VCOMDC	GND	C41M	Hi-Z
VCOM	GND		
SOUTn	GND		
S1-1080	GND		
PBCTLA1	GND		
PBCTLA2	GND		
PBCTLB1	GND		
PBCTLB2	GND		

note1) Please keep the input of High or Low.

Absolute Maximum Rating

Table 25

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	IOVCC – GND	V	-0.3 ~ +4.6	1,2
Power supply voltage (2)	VCI – AGND	V	-0.3 ~ +6.5	1,2
Power supply voltage (3)	DPHYVCC – DPHYGND	V	-0.3 ~ +4.6	1,2
Power supply voltage (4)	VCI – VCL	V	-0.3 ~ +6.5	1,2
Power supply voltage (5)	VSP – AGND	V	-0.3 ~ +6.5	1,3
Power supply voltage (6)	AGND – VSN	V	-0.3 ~ +6.5	1,3
Power supply voltage (7)	AGND – VGL	V	-0.3 ~ +16.0	1,4
Power supply voltage (8)	VGH – AGND	V	-0.3 ~ +19.0	1
Power supply voltage (9)	VGH – VGL	V	-0.3 ~ +32.0	1
Input voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1,6
Input voltage (DSI)	Vt(DSI)	V	-0.3 ~ 1.8	1,7
Operating temperature	Topr	°C	-40 ~ +85	1,5
Storage temperature	Tstg	°C	-55 ~ +110	1

- Notes:
1. If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.
 2. Make sure (High) IOVCC \geq GND (Low), (High) VCI \geq AGND (Low), (High) DPHYVCC \geq DPHYGND (Low), (High) VCI \geq VCL (Low).
 3. Make sure (High) VSP \geq AGND (Low), (High) VSP \geq VCI (Low), (Low) VSN \leq AGND (High).
 4. Make sure (High) AGND \geq VGL (Low).
 5. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.
 6. IOVCC amplitude input pin.
 7. DSI input pin. (CLKP/N, DATA0P/N, DATA1P/N, DATA2P/N, DATA3P/N)

Electrical Characteristics

(1) Power Supply Voltage Range

Table 26 (Ta = -40°C ~ +85°C)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Power supply voltage	IOVCC	V	—	1.65	1.80	3.30	1
	VCI	V	—	2.50	2.80	3.30	1
	DPHYVCC	V	—	1.65	1.80	3.30	1

Table 27 (Ta = -40°C ~ +85°C)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Power supply voltage External VSP supply mode	IOVCC	V	—	1.65	1.80	3.30	1
	DPHYVCC	V	—	1.65	1.80	3.30	1
	VSP	V	—	4.50	5.60	6.00	1

Notes: 1. The DC/AC electrical characteristics of bare die and wafer are guaranteed at +85°C.

Table 28 (Ta = -40°C ~ +85°C)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Power supply voltage External VSP/VSN supply mode	IOVCC	V	—	1.65	1.80	3.30	1
	DPHYVCC	V	—	1.65	1.80	3.30	1
	VSP	V	—	4.50	5.60	6.00	1
	VSN	V	—	-6.00	-5.60	-4.50	1

Notes: 1. The DC/AC electrical characteristics of bare die and wafer are guaranteed at +85°C.

(2) DC Characteristics

Table 29

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note	
Input high-level voltage 1	V _{IH1}	V	IOVCC=1.65V ~ 3.300V	0.70 x IOVCC	—	IOVCC	1, 2	
Input low-level voltage 1	V _{IL1}	V	IOVCC=1.65V ~ 3.300V	0	—	0.30 x IOVCC	1, 2	
Output high-level voltage 1 (LEDPWM)	V _{OH1}	V	IOVCC=1.65V ~ 3.300V, IOUT = -0.1mA	0.80 x IOVCC	—	—	1	
Output low-level voltage 1 (LEDPWM)	V _{OL1}	V	IOVCC=1.65V~3.300V, IOUT=0.1mA	—	—	0.20 x IOVCC	1	
Input high-level current	I _{IH}	µA	Vin=IOVCC	—	—	10	4	
Input low-level current	I _{IL}	µA	Vin=0V	-10	—	—	4	
Current consumption (IOVCC-GND)	Normal Mode + Sleep out	I _{OPN}	mA	1920-line drive, IOVCC= 1.8 V, VCI= 2.8 V, fFLM= 60Hz, Ta= 25°C, DSIData:24'h000000,C[1:0]=2'h0, DSI4Lanes, fDSICLK=500MHz,1080RGB(HRE 1[1:0]=2'h0, DM[2:0]= 3'h1	—	—	17.0	5
	Deep Standby Mode	I _{DST}	µA	IOVCC=1.80V, VCI=2.80V, Ta=25°C	—	0.1	3.0	5
Current consumption (VCI-GND)	Normal Mode + Sleep out	I _{CIN3}	mA	1920-Linedrive,IOVCC=1.8V, VCI= 2.8 V, fFLM=60Hz, Ta= 25°C, RGB Data:24'h000000, no load on the panel, 1080RGB(HRE1[1:0]=2'h0), REV=0, LINEINVA= 4'hF, VC1= 3'h5,VC2=4'h8,VC3=4'h3,BT2=1'h 0, BT3=1'h0, VLM1 = 4'h0, VLM1M = 1'h0, VLM2= 6'hB, VLM3= 6'hB, DC2= 3'h1,DC3= 3'h1, DC4= 3'h1,DC1SPHA= 6'h10, DC1SPHB= 6'h10, DC1SPHC= 6'h10, DC1SPHD= 6'h10, DC1SMHA =6'h10, DC1SMHB= 6'h10, DC1SMHB 6'h10, DC1SMHD= 6'h10, SVD= 4'h0, SVS=4'h0, APAP= 3'h3, APAN= 3'h3, APSGP1 = 3'h4, APSGP2 = 3'h4, APSGN1 = 3'h4, APSGN2 = 3'h4, Gamma Register setting = Default Value	—	—	22.0	5
	Deep Standby Mode	I _{DST3}	µA	IOVCC=1.80V, VCI=2.80V, Ta=25°C	—	1.0	10.0	5

Table 29(Continued)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
VSP and VSN: External supply mode Current consumption (VSP-GND)	I _{CIN4}	mA	1920-Line drive, VSP= 4.5 V, VSN= -4.5 V, IOVCC1= 1.8 V, IOVCC2=1.8 V, fFLM=60Hz, Ta= 25°C, RGB Data:24'h000000, no load on the panel, 1080RGB(HRE1[1:0]=2'h0), REV=0, LINEINVA= 4'hF, VC1= 3'h5, VC2= 4'h8, VC3= 4'h3, BT2=1'h0, BT3=1'h0, VLM1= 4'h0, VLM1M= 4'h0, VLM2= 6'hB, VLM3= 6'hB, DC2= 3'h1, DC3= 3'h1, DC4= 3'h1, DC1SPHA= 6'h10, DC1SPHB= 6'h10, DC1SPHC= 6'h10, DC1SPHD= 6'h10, DC1SMHA =6'h10, DC1SMHB= 6'h10, DC1SMHB 6'h10, DC1SMHD= 6'h10, SVD= 4'h0, SVS=4'h0, APAP= 3'h3, APAN= 3'h3, APSGP1 = 3'h4, APSGP2 = 3'h4, APSGN1 = 3'h4, APSGN2 = 3'h4, Gamma Register setting = Default Value	—	—	11.0	5
			IOVCC= 1.8 V, VSP= 6.0 V, VSN= -6.0 V, Ta= 25°C	—	1.0	25.0	5
VSP and VSN: External supply mode Current consumption (GND-VSN)	I _{CIN5}	mA	1920-Line drive, VSP= 4.5 V, VSN= -4.5 V, IOVCC1= 1.8 V, IOVCC2=1.8 V, fFLM=60Hz, Ta= 25°C, RGB Data:24'h000000, no load on the panel, 1080RGB(HRE1[1:0]=2'h0), REV=0, LINEINVA= 4'hF, VC1= 3'h5, VC2= 4'h8, VC3= 4'h3, BT2=1'h0, BT3=1'h0, VLM1= 4'h0, VLM1M= 4'h0, VLM2= 6'hB, VLM3= 6'hB, DC2= 3'h1, DC3= 3'h1, DC4= 3'h1, DC1SPHA= 6'h10, DC1SPHB= 6'h10, DC1SPHC= 6'h10, DC1SPHD= 6'h10, DC1SMHA =6'h10, DC1SMHB= 6'h10, DC1SMHB 6'h10, DC1SMHD= 6'h10, SVD= 4'h0, SVS=4'h0, APAP= 3'h3, APAN= 3'h3, APSGP1 = 3'h4, APSGP2 = 3'h4, APSGN1 = 3'h4, APSGN2 = 3'h4, Gamma Register setting = Default Value	—11.0	—	—	5
			IOVCC= 1.8 V, VSP= 6.0 V, VSN= -6.0 V, Ta= 25°C	-25.0	-1.0	-	5

Table 30

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Output voltage dispersion	ΔV_{o1}	mV	$V_0 \sim V_{63}, V_{192} \sim V_{255}$	—	—	35	6
	ΔV_{o2}	mV	$V_{64} \sim V_{191}$	—	—	15	6
Average output variance	ΔV	mV	—	-35	—	+35	7

(3) DC Characteristics (MIPI DSI)**Table 31**

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSI current consumption (DPHYVCC-DPHYGND)	HS mode I_{HS}	mA	IOVCC=1.800V, DPHYVCC=1.800V, VCI=2.800V, DSI 4 lanes, fDSICLK=500MHz, DSI Data:24'h000000 Ta=25°C	-	-	5.2	-
	LP mode I_{LP}	μA	IOVCC=1.800V, DPHYVCC=1.800V, VCI=2.800V, Clock lane=LP11, Data lane=LP11, Ta=25°C	-	-	430	-

Note on Electrical Characteristics

- Notes:
1. The DC/AC electrical characteristics of bare die and wafer are guaranteed at +85°C.
 2. The following figures illustrate the configurations of input, I/O, and output pins.

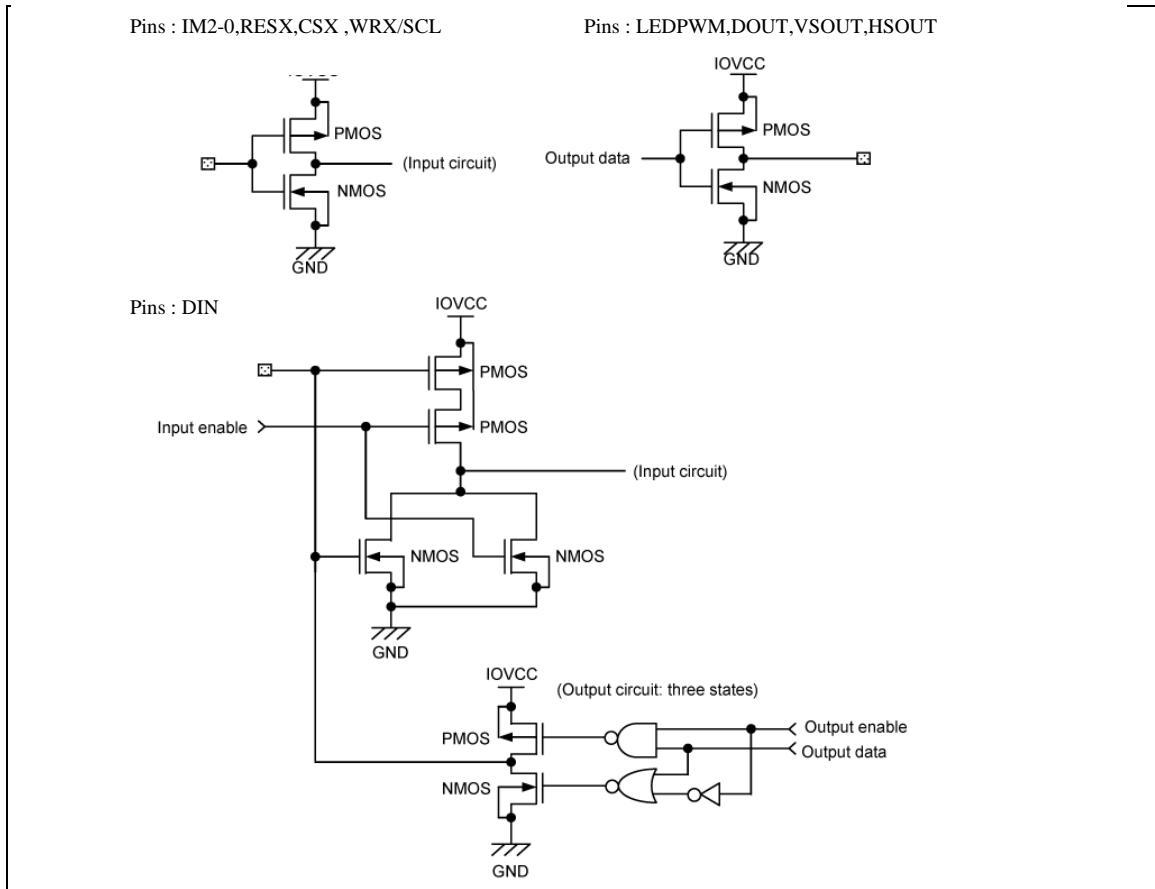


Figure 6

3. The TESTE pin must be grounded (GND).
4. This excludes the current in the output-drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CSX pin is "High" or "Low" while not accessing via interface pins.
6. The output voltage deviation is the difference in the voltages between output pins that are placed side by side in the same display mode. The output voltage deviation is reference value.
7. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display data.

(4) Step-up Circuit Characteristics**Table 32**

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Step-up output voltage Charge Pump	VSP	V	VCI=2.8 V, Ta=25°C, VLM1=4'h0, Iload1= -10 [mA]	4.3	4.5	-
	VSN	V	VCI=2.8 V, Ta=25°C, VLM1=4'h0, Iload1= +10 [mA]	-	-4.45	-4.25
	VGH	V	VCI=2.8 V, Ta=25°C, VC2=4'h8, VC3=4'h3 , BT2=1'h0, VLM1M= 4'h0, Iload= -1 [mA]	7.6	7.85	-
	VGL	V	VCI=2.8 V, Ta=25°C, VC2= 4'h8, VC3=4'h3, BT3=1'h0, VLM1M= 4'h0, Iload= +1 [mA]	-	-7.35	-7.1
	VCL1	V	VCI=2.8 V, Ta=25°C, VLM1=4'h0 , VC1= 3'h5, Iload1= +10 [mA]	-	-2.30	-2.10
Step-up output voltage LDO output	SVDD	V	SP=6.0 V, VSN= -6.0 V,Ta=25°C, SVD=4'h0, Iload1= -10 [mA]	4.3	4.5	-
	SVSS	V	VSP=6.0 V, VSN= -6.0 V, Ta=25°C, SVS=4'h0, Iload1= +10 [mA]	-	-4.45	-4.30
	GVDD	V	VSP=6.0 V, VSN= -6.0 V, Ta=25°C, VLM2=6'h0F, Iload= -1 [mA]	6.60	6.95	-
	GVSS	V	VSP=6.0 V, VSN= -6.0 V, Ta=25°C, VLM3=6'h0F, Iload= +1 [mA]	-	-6.95	-6.60
	VCL2	V	VSP=6.0 V, VSN= -6.0 V, Ta=25°C, Iload1= +10 [mA]	-	-2.78	-2.63

(5) Clock Characteristics**Table 33**

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Oscillation clock	fosc	MHz	VCI = 2.8V, IOVCC = 1.8V	26.6	28.0	29.4

(6) Reset Timing Characteristics

Table 34

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	—
Reset low-level width2	tRW2	us	Operation	1000	—
Reset time (Sleep IN)	tRT1	ms	—	—	3
Reset time (Sleep OUT)	tRT2	ms	—	—	3
Noise reject width	tRESNR	us	—	—	1

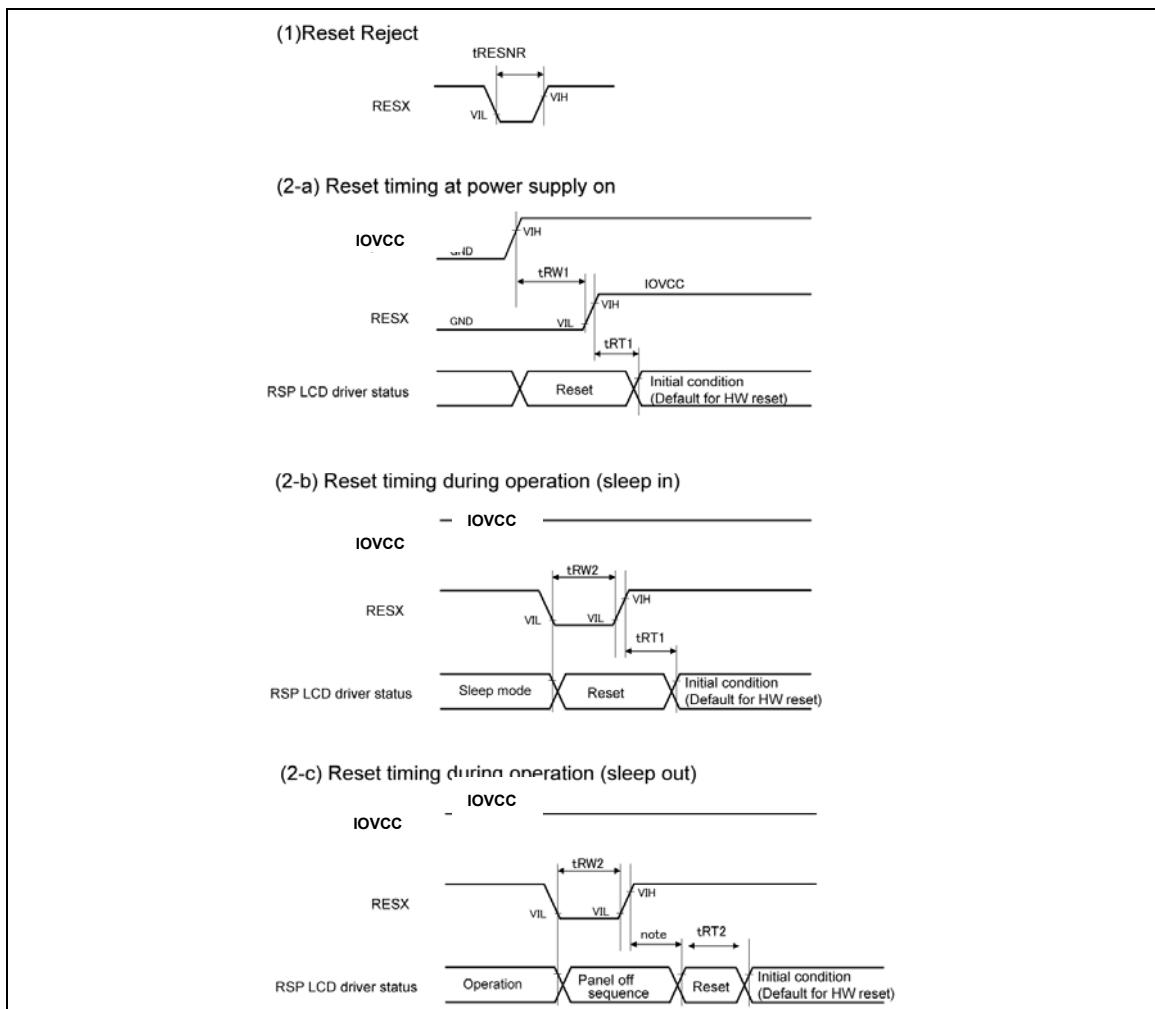


Figure 7 Reset Timing Characteristics

Note: Refer to the appendix for details of "Panel off sequence".

(7) Liquid Crystal Driver Output Characteristics

Table 35

Item	Symbol	Unit	Test condition	Min.	Typ.	Max	Note
Source driver output delay time	tdds	us	IOVCC=1.8V, VCI=2.8V, Ta=25°C, reached voltage: defined grayscale voltage $\pm 35mV$ VPL=7'h3B,VNL=7'h3B Load resistor R = 5k Ω Load capacitance C = 35pF	—	—	1.7	1

Note1: LCD driver output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one-line cycle needs to be specified checking image quality on the panel to be used.

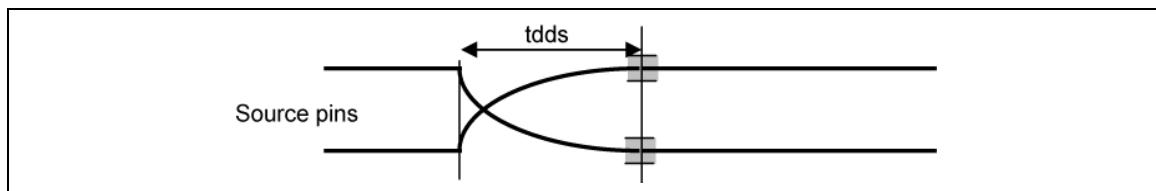


Figure 8 Liquid Crystal Driver Output Timing

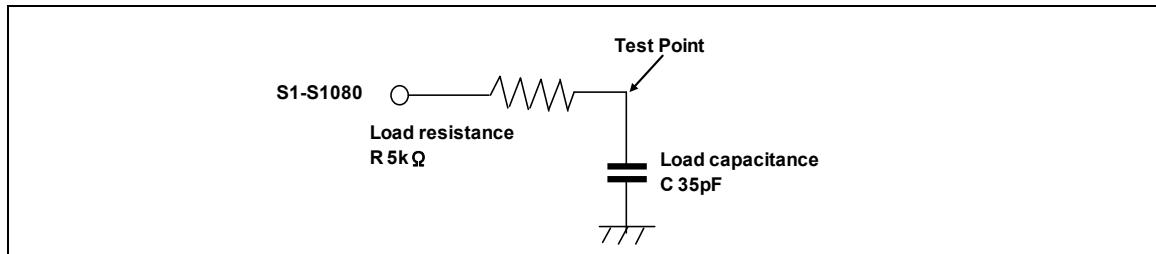


Figure 9 Load Circuit for Testing LCD Driver Output Characteristics

(9) MIPI DBI Type C Timing Characteristics

Table 36

Item	Symbol	Unit	Test condition	Min.	Max.
Chip select setup time	CSX	tcss	ns	-	40
Chip select hold time		tcsh	ns	-	40
Chip select "High" pulse width		tchw	ns	-	100
Address setup time	DCX	tas	ns	-	10
Address hold time (Write/Read)		tah	ns	-	10
Write cycle time	SCL (Write)	twc	ns	-	100
SCL "High" period (Write)		twrh	ns	-	40
SCL "Low" period (Write)		twrl	ns	-	40
Read cycle time	SCL (Read)	trc	ns	-	300
SCL "High" period (Read)		trdh	ns	-	120
SCL "Low" time (Read)		trdl	ns	-	120
Data setup time	DIN	tds	ns	-	30
Data hold time		tdh	ns		30
Access time	DOUT	tacc	ns	CL Max.30pF Min.8pF	-
Output disable time		tod	ns		10
Rise/ Fall time	-	tr/tf	ns	-	15

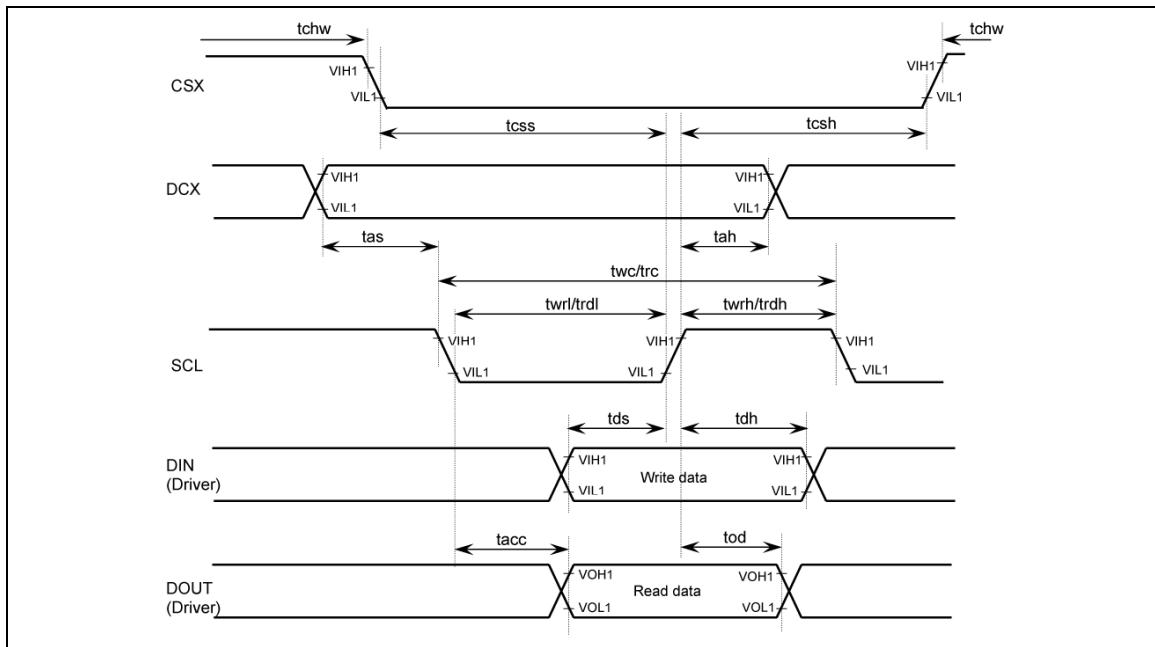


Figure 10 MIPI DBI Type C Timing

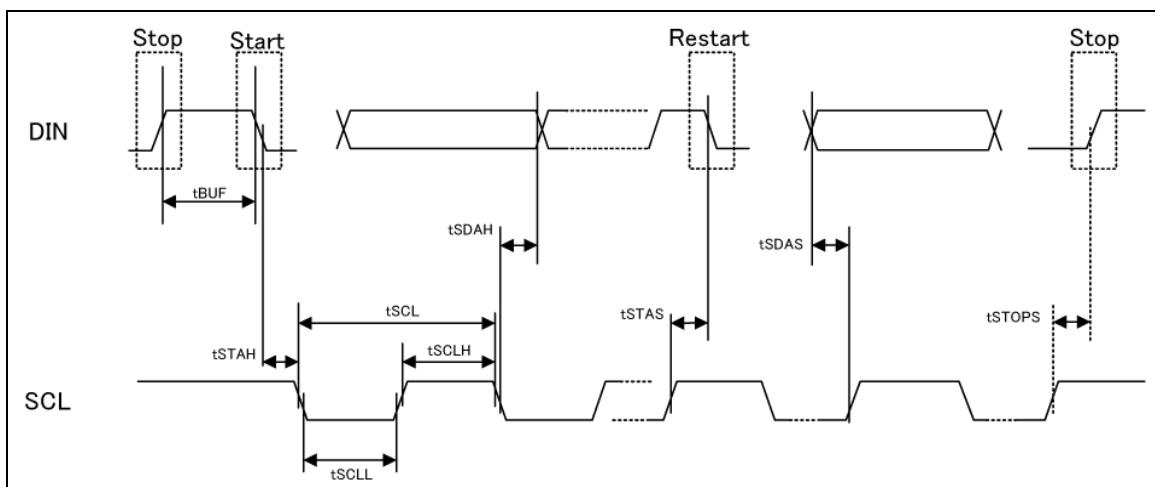
(11) I²C Serial Interface Timing Characteristics

Table 37

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Serial clock cycle time	t_{SCL}	ns	-	650	-	-
Serial clock "High" period	t_{SCLH}	ns	-	160	-	-
Serial clock "Low" period	t_{SCLL}	ns	-	320	-	-
Bus free time	t_{BUF}	ns	-	320	-	-
Start condition Hold time	t_{STAH}	ns	-	150	-	-
Restart condition setup time	t_{STAS}	ns	-	150	-	-
Stop condition setup time	t_{STOPS}	ns	-	150	-	-
Data setup time	t_{SDAS}	ns	-	70	-	-
Data hold time	t_{SDAH}	ns	-	0	-	-

Notes: 1. The line connected to the DIN pin requires an external pull-up resistor in I²C bus interface operation.

2. The output data delay time is based on the load condition compliant with I²C.

Figure 11 I²C Timing

(12) MIPI DSI Characteristics

Table 38

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	70	3
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-70	-	-	3
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 3.30V v	880	-	1350	
	I/O leakage current	ILEAK	µA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2

2. Excluding COG resistance (contact resistance and ITO wiring resistance). The values are tentative.
3. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

MIPI DSI HS-RX Clock and Data-Clock Specifications**Table 39**

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V DSI 2 lanes, 3 lanes,4lane	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	5,6

Notes:

- 4. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
- 5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
- 6. tSETUP/tHOLD Time are measured without HS-TX Jitter.

MIPI DSI LP-RX/TX Clock and Data-Clock Specifications**Table 40**

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE} + T_{HS-ZERO}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	$4*T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}		OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	$5*T_{LPTX}$			
Length of any Low-Power state period	T_{LPX}	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	50	-	-	
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	UI	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	$105\text{ ns} + n*12*\text{UI}$	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	OVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	1/fosc	-	

- Notes:
1. If $a > b$ then $\max(a, b) = a$, otherwise $\max(a, b) = b$
 2. Where $n = 1$ for Forward-direction HS mode.
 3. The R63311 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63311 can work without the remained process if tCLK-POST is more than 256 UI.
 4. The R63311 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, "fosc" is the frequency of oscillator clock, typical 28 MHz.

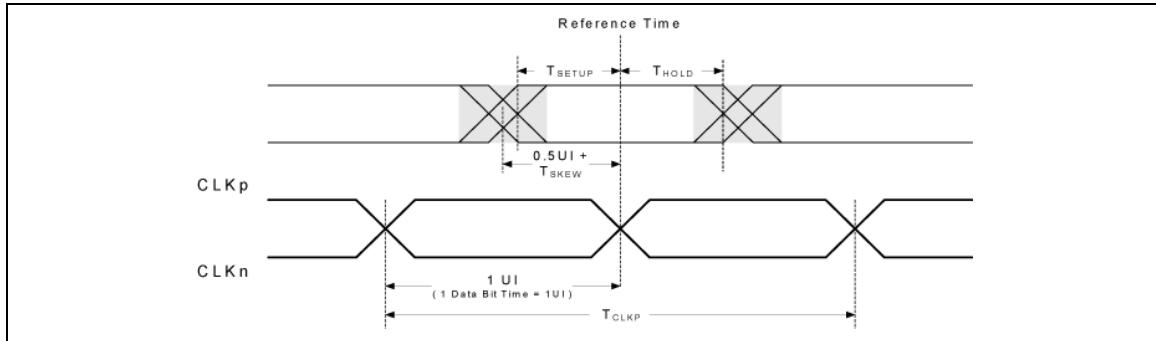


Figure 12 Data to Clock Timing Definitions

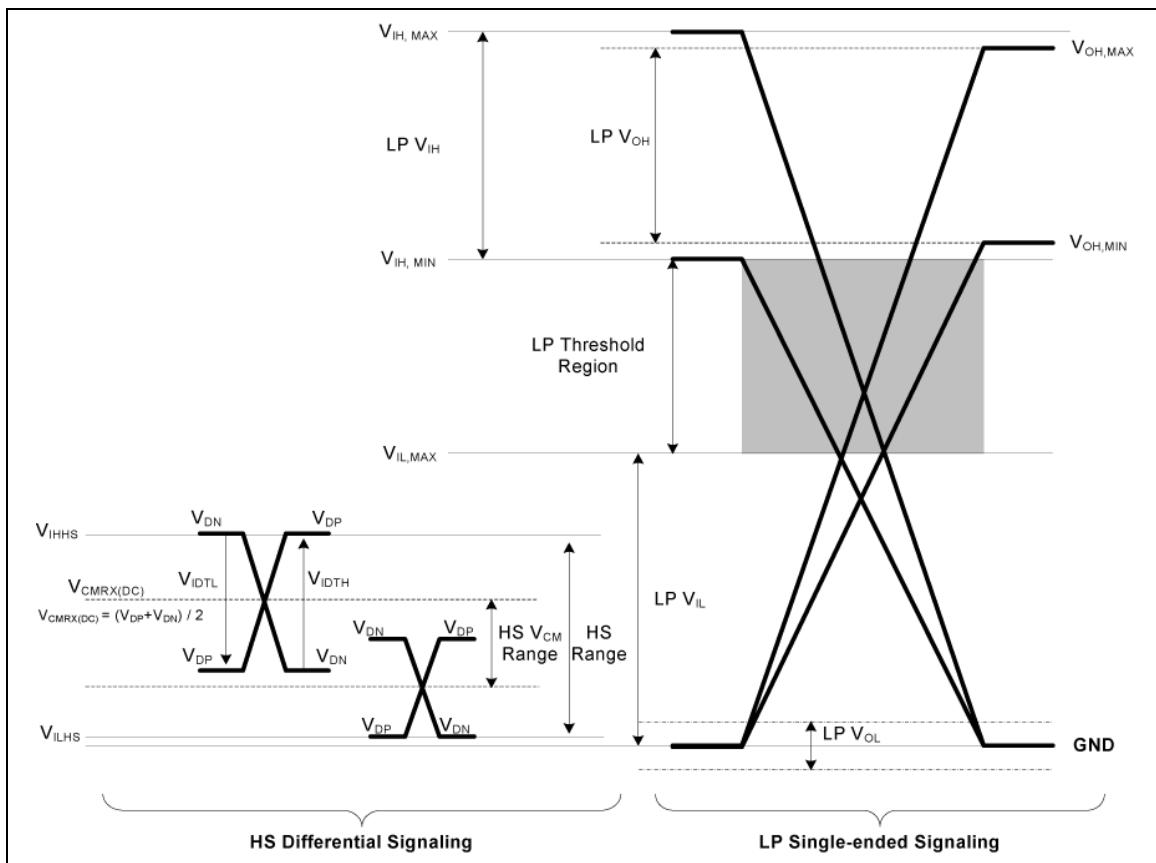


Figure 13 DSI LP Mode

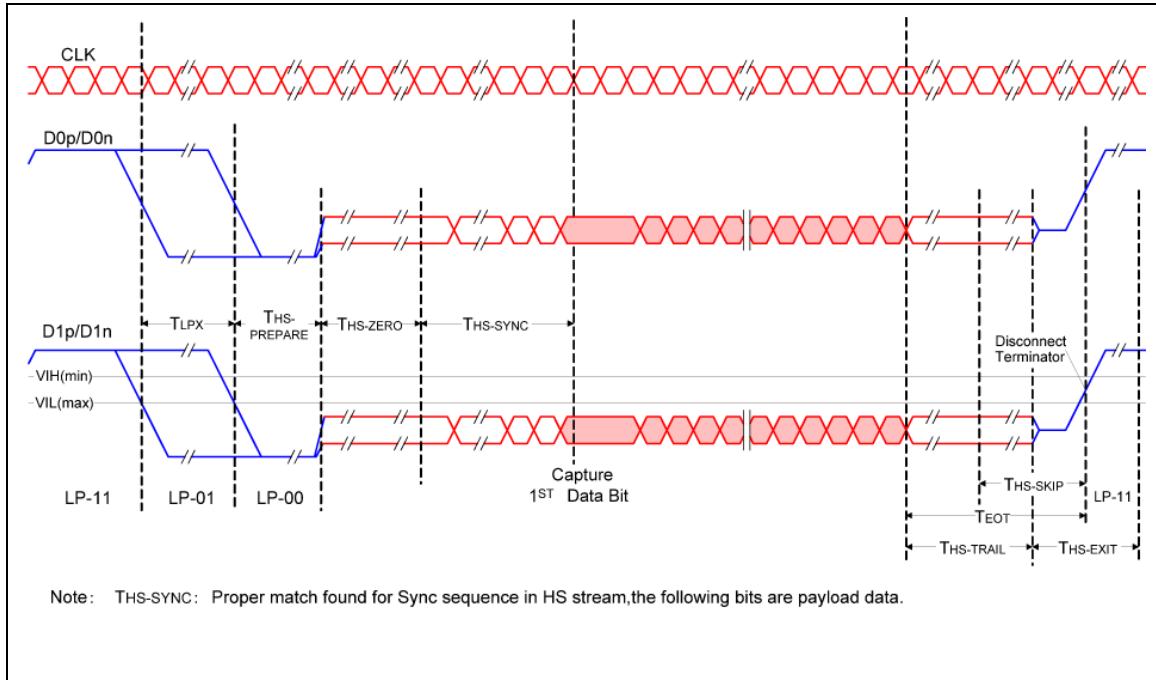


Figure 14 HS Data Transmission in Bursts

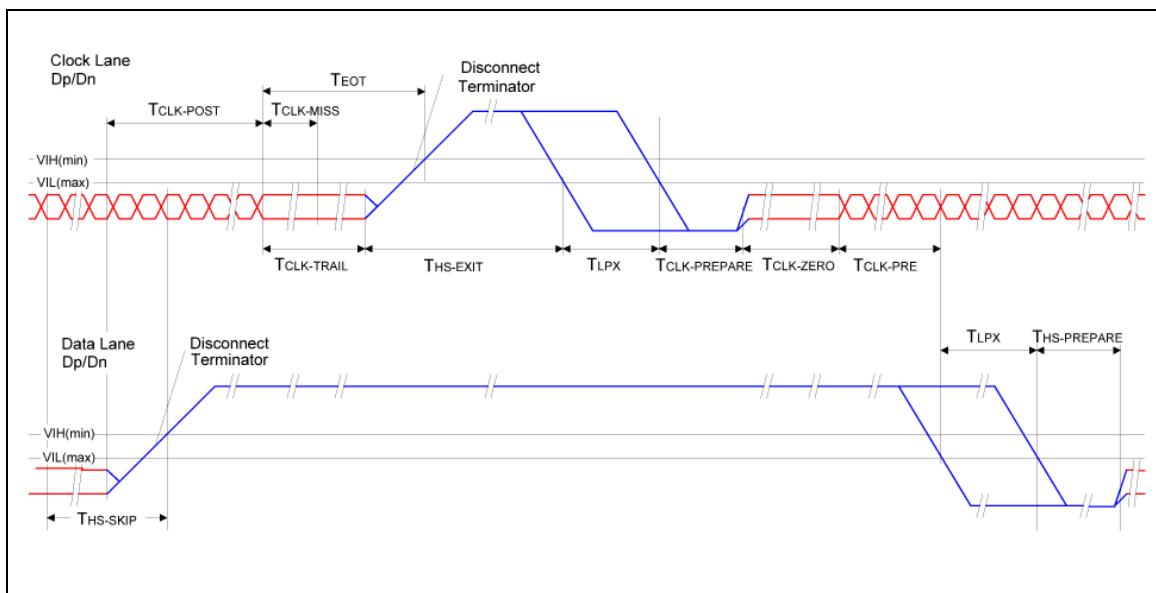


Figure 15 Switching the Clock Lane between Clock Transmission and LP Mode

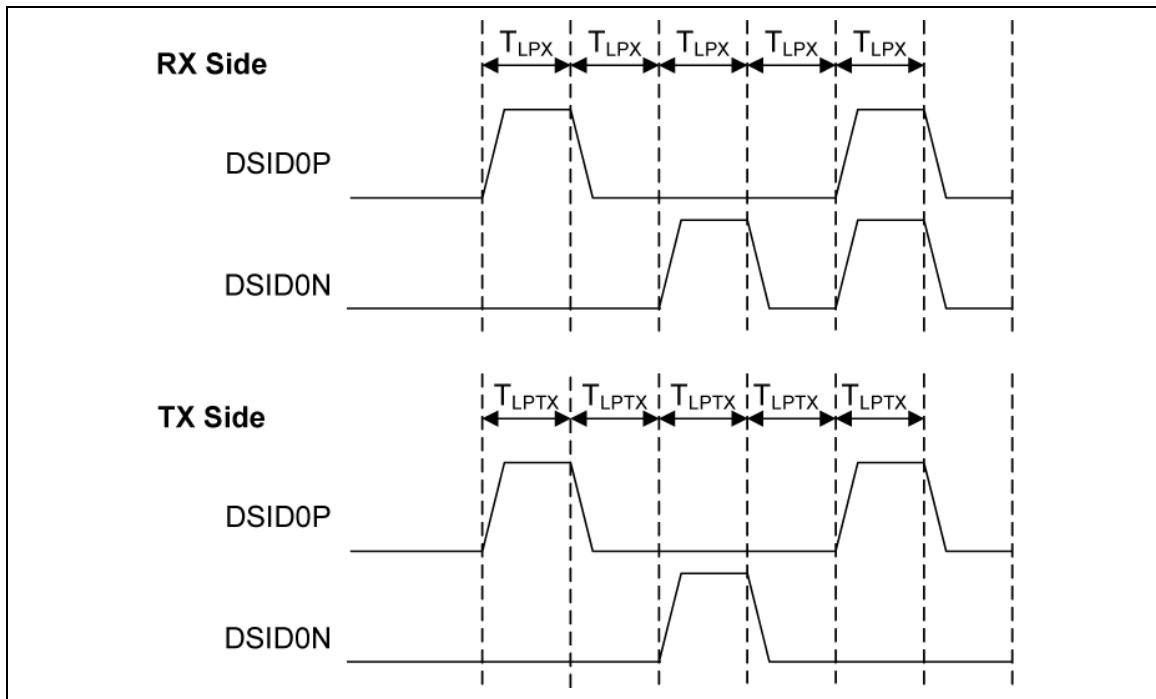


Figure 16 DSI LP Mode

Command List

Table 41 User Command

Operational Code (Hex)	Command	Command (C) /Read (R) /Write(W)	Number Of Parameter	MIPI DCS Type 3 Requirement	RSP LCD driver Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
04h	Read_DDB_start	R	16	No	Yes	
05h	read_Number_of_the_Errorson_DSI	R	1	No	Yes	
06h	get_red_channel	R	1	Yes	Yes	
07h	get_green_channel	R	1	Yes	Yes	
08h	get_blue_channel	R	1	Yes	Yes	
0Ah	get_power_mode	R	1	Yes	Yes (Bit 4/2 only)	
0Bh	get_address_mode	R	1	Yes	Yes (Bit 7/6/3 only)	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes (Bit 5/2/1/0 only)	
0Eh	get_signal_mode	R	1	Yes	Yes (Bit 7/6/0 only)	
0Fh	get_diagnostic_result	R	1	Yes (Bit 6 only)	Yes (Bit 6 only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	No	No	
13h	enter_normal_mode	C	0	No	No	
20h	exit_invert_mode	C	0	Yes	No	
21h	enter_invert_mode	C	0	Yes	No	
26h	set_gamma_curve	W	1	Yes	Yes	
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	No	No	
2Bh	set_page_address	W	4	No	No	
2Ch	write_memory_start	W	Variable	No	No	
2Dh	write_LUT	W	Variable	No	No	
2Eh	Read_memory_start	R	Variable	No	No	

Table 42 User Command (continued)

Operational Code (Hex)	Command	Command (C) /Read (R) /Write(W)	Number Of Parameter	MIPI DCS Type 3 Requirement	RSP LCD driver Implementation	Note
30h	set_partial_area	W	4	No	No	
33h	set_scroll_area	W	6	No	No	
34h	set_tear_off	C	0	No	Yes	
35h	set_tear_on	W/R	1	No	Yes	
36h	set_address_mode	W/R	1	Yes	Yes (Bit 7/6/3 only)	
37h	set_scroll_start	W	2	No	No	
38h	exit_idle_mode	C	0	No	No	
39h	enter_idle_mode	C	0	No	No	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory_continue	W	Variable	No	No	
3Eh	read_memory_continue	R	Variable	No	No	
44h	set_tear_scanline	W	2	No	Yes	
45h	get_scanline	R	2	No	No	
51h	write_display_brightness	W	2	No	Yes	
52h	read_display_brightness_value	R	2	No	Yes	
53h	wite_CTRL_display	W	1	No	Yes (Bit 5/3/2 only)	
54h	read_control_value_display	R	1	No	Yes (Bit 5/3/2 only)	
55h	write_content_adaptive_brightness_control	W	1	No	Yes	
56h	read_content_adaptive_brightness_control	R	1	No	Yes	
5Eh	write_CABC_minimum_brightness	W	2	No	Yes	
5Fh	read_CABC_minimum_brightness	R	2	No	Yes	
68h	read_automatic_brightness_control_self-diagnostic_result	R	1	No	Yes (Bit 6 only)	
A1h	read_DDB_start	R	16	Yes	Yes	
A8h	read_DDB_continue	R	Variable	Yes	Yes	
DAh	Read ID1	R	1	No	Yes	
DBh	Read ID2	R	1	No	Yes	
DCh	Read ID3	R	1	No	Yes	
F5h	Read Mode In for DBI Only	C	0	No	Yes	
F6h	Read Mode Out for DBI Only	C	0	No	Yes	

Table 43 Manufacturer Command

Operational Code (Hex)	Function	Command® /Read® /Write(W)	Number Of Parameter	Category
B0h	Manufacturer Command Access Protect	W/R	1	
B1h	Low Power Mode Control	W/R	1	
B3h	Interface Setting	W/R	6	
B4h	Interface ID Setting	W/R	2	
B5h	Read Checksum and ECC Error Count	R	3	
B6h	DSI Control	W/R	2	
B7h	Checksum and ECC Error Count Reset	W/R	1	
B8h	Backlight Control (1) (Common)	W/R	25	
B9h	Backlight Control (2) (Movie/Still)	W/R	7	
BAh	Backlight Control (4) (GUI)	W/R	7	
BBh	External Clock Setting	W	2	
BFh	Device code Read	R	5	
C0h	Test Register	W/R	2	
C1h	Display Setting 1	W/R	34	
C2h	Display Setting 2	W/R	7	
C3h	TP Sync Control	W/R	3	
C4h	Source Timing Setting	W/R	22	
C6h	LTPS Timing Setting	W/R	40	
C7h	Gamma Setting (A Set)	W/R	24	
C8h	Gamma Setting (B Set)	W/R	24	
C9h	Gamma Setting (C Set)	W/R	24	
CAh	Color enhancement	W/R	32	
CBh	Panal PIN Control	W/R	9	
CCh	Panel Interface Control	W/R	1	
CDh	Backlight Control (5)	W/R	3	
CEh	Backlight Control (6)	W/R	7	
CFh	GPO Control	W/R	5	
D0h	Power Setting (Charge Pump Setting)	W/R	14	
D1h	Power Setting (Switching Regulator Setting)	W/R	29	
D2h	Power Setting for Common	W/R	3	
D3h	Power Setting for Internal Power	W/R	26	

Table 44 Manufacturer Command (continued)

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number Of Parameter	Category
D5h	VCOM Setting	W/R	7	
D6h	Sequencer Test Control	W/R	1	
D7h	Sequencer Timing Control for Power On	W/R	20	
D8h	Sequencer Timing Control for Power Off	W/R	6	
D9h	Sequencer Control	W/R	2	
DDh	Outline Sharpening Control	W/R	2	
DEh	Test Image generator	W/R	6	
E0h	NVM Access Control	W/R	6	
E1h	set_DDB write Control	W/R	10	
E2h	Read ID code	W/R	6	
E3h	NVM Load Control	W/R	1	
E4h	Test Register	W/R	7	
E5h	Test Register	W/R	4	
E6h	Test Register	W/R	1	
E7h	Test Register	W/R	1	
E8h	Test Register	W/R	11	
E9h	Test Register	W/R	1	
EC _h	Panel synchronous output (1)	W/R	2	
ED _h	Panel synchronous output (2)	W/R	3	
EE _h	Panel synchronous output (3)	W/R	2	
EF _h	Panel synchronous output (4)	W/R	12	
F3h	Test Register	W/R	4	
FAh	Test Register	W/R	1	
FBh	Test Register	W/R	1	
FD _h	Test Register	W/R	6	
FE _h	Test Register	W/R	9	
FF _h	Test Register	W/R	0	

Command Accessibility

In the default status, only User Commands and Manufacturer Command Access Protect (MCAP) register can be accessed. Other commands are recognized as “nop”.

Manufacturer Commands except the MCAP register are accessible by releasing Access Protect. See Command the description of the MCAP register for details.

Table 45 User Command

Operational Code (Hex) Command		Command Accessibility	
		Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes
01h	soft_reset	Yes	Yes
04h	read_DDB_start	Yes	Yes
05h	read_Number_of_the_Errors_on_DSI	Yes	Yes
06h	get_red_channel	Yes	Yes
07h	get_green_channel	Yes	Yes
08h	get_blue_channel	Yes	Yes
0Ah	get_power_mode	Yes	Yes
0Bh	get_address_mode	Yes	Yes
0Ch	get_pixel_format	Yes	Yes
0Dh	get_display_mode	Yes	Yes
0Eh	get_signal_mode	Yes	Yes
0Fh	get_diagnostic_result	Yes	Yes
10h	enter_sleep_mode	Yes	Yes
11h	exit_sleep_mode	Yes	Yes
26h	Set_gamma_curve	Yes	Yes
28h	set_display_off	Yes	Yes
29h	set_display_on	Yes	Yes
34h	set_tear_off	Yes	Yes
35h	Set_teer_on	Yes	Yes
36h	set_address_mode	Yes	Yes
3Ah	set_pixel_format	Yes	Yes
44h	Set_tear_scanline	Yes	Yes

Table 46 User Command (continued)

Operational Code (Hex) Command		Command Accessibility	
		Sleep Mode Off	Sleep Mode On
51h	write_display_brightness	Yes	Yes
52h	read_display_brightness_value	Yes	Yes
53h	write_control_display	Yes	Yes
54h	read_control_value_display	Yes	Yes
55h	write_content_adaptive_brightness_control	Yes	Yes
56h	read_content_adaptive_brightness_control	Yes	Yes
5Eh	write_CABC_minimum_brightness	Yes	Yes
5Fh	read_CABC_minimum_brightness	Yes	Yes
68h	read_automatic_brightness_control_self-diagnostic_result	Yes	Yes
A1h	read_DDB_start	Yes	Yes
A8h	read_DDB_continue	Yes	Yes
DAh	Read ID1	Yes	Yes
DBh	Read ID2	Yes	Yes
DCh	Read ID3	Yes	Yes
F5h	Read Mode In for DBI Only	Yes	Yes
F6h	Read Mode Out for DBI Only	Yes	Yes

Table 47 Manufacturer Command

Operational Code (Hex) Command		Command Accessibility	
		Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes
B1h	Low Power Mode Control	No	Yes
B3h	Interface Setting	Yes	Yes
B4h	Interface ID Setting	Yes	Yes
B5h	Read Checksum and ECC Error Count	Yes	Yes
B6h	DSI Control	Yes	Yes
B7h	Checksum and ECC Error Count Reset	Yes	Yes
B8h	Backlight Control (1) (Common)	Yes	Yes
B9h	Backlight Control (2) (Movie/Still)	Yes	Yes
BAh	Backlight Control (4) (GUI)	Yes	Yes
BFh	Device code Read	Yes	Yes
C0h	Test Register	Yes	Yes
C1h	Display Setting 1	Yes	Yes
C2h	Display Setting 2	Yes	Yes
C3h	Panel Interface Mode	Yes	Yes
C4h	Source Timing Setting	Yes	Yes
C6h	LTPS Timing Setting	Yes	Yes
C7h	Gamma Setting (A Set)	Yes	Yes
C8h	Gamma Setting (B Set)	Yes	Yes
C9h	Gamma Setting (C Set)	Yes	Yes
CAh	Color enhancement	Yes	Yes
CBh	Panel PIN Control	Yes	Yes
CCh	Panel Interface Control	Yes	Yes
CDh	Backlight Control (5)	Yes	Yes
CEh	Backlight Control (6)	Yes	Yes
CFh	GPO Control	Yes	Yes

Table 48 Manufacturer Command (continued)

Operational Code (Hex) Command		Command Accessibility	
		Sleep Mode Off	Sleep Mode On
D0h	Power Setting (Charge Pump Setting)	Yes	Yes
D1h	Power Setting (Switching Regulator Setting)	Yes	Yes
D2h	Power Setting for Common	Yes	Yes
D3h	Power Setting for common	Yes	Yes
D4h	VPLVL/VNLVL Setting	Yes	Yes
D5h	VCOM Setting	Yes	Yes
D6h	Sequencer Test Control	Yes	Yes
D7h	Sequencer Timing Control for Power On	Yes	Yes
D8h	Sequencer Timing Control for Power Off	Yes	Yes
D9h	Sequencer Control	Yes	Yes
DDh	Outline Sharpening Cintrol	Yes	Yes
DEh	Test Image Generator	Yes	Yes
E0h	NVM Access Control	Yes	No
E1h	set_DDB write Control	Yes	Yes
E2h	Read ID code	Yes	Yes
E3h	NVM Load Control	Yes	Yes
E4h	Test Register	No	No
E5h	Test Register	No	No
E6h	Test Register	No	No
E7h	Test Register	No	No
E8h	Read Chip Information	No	No
E9h	Read Chip Information Enable	No	No
ECh	Panel synchronous output (1)	Yes	Yes
EDh	Panel synchronous output (2)	Yes	Yes
EEh	Panel synchronous output (3)	Yes	Yes
EFh	Panel synchronous output (4)	Yes	Yes
F3h	Test Register	No	No
F5h	Read Mode In for DBI only	Yes	Yes
F6h	Read Mode Out for DBI only	Yes	Yes
FAh	Test Register	No	No
FBh	Test Register	No	No
FCh	Test Register	No	No
FDh	Test Register	No	No
FEh	Test Register	No	No
FFh	Test Register	No	No

Default Modes and Values

Table 49 User Command

Operational Code(Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
04h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	Extend DDB ID1 (Note2)	Extend DDB ID1 (Note2)	Extend DDB ID1 (Note2)
		6th	Extend DDB ID2 (Note2)	Extend DDB ID2 (Note2)	Extend DDB ID2 (Note2)
		7th	Extend DDB ID3 (Note2)	Extend DDB ID3 (Note2)	Extend DDB ID3 (Note2)
		8th - 15th	XXh	XXh	XXh
		16th	FFh	FFh	FFh
05h	read_Number_of_the_Error_on_DSI	1st	00h	00h	00h
06h	get_red_channel	1st	00h	00h	00h
07h	get_green_channel	1st	00h	00h	00h
08h	get_blue_channel	1st	00h	00h	00h
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	70h	70h	70h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic_result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
26h	set_gamma_curve	1st	01h	01h	01h
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off

Table 50 User Command (continued)

Operational Code(Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
34h	set_tear_off	None	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
3Ah	set_pixel_format	1st	70h	70h	70h
44h	set_tear_scanline	1st/2nd STS[10:0]	000h	000h	000h
51h	write_display_brightness	1st/2nd DBV[11:0]	00h	00h	00h
52h	read_display_brightness_value	1st/2nd DBV[11:0]	00h	00h	00h
53h	wite_CTRL_display	1st	00h	00h	00h
54h	read_control_value_display	1st	00h	00h	00h
55h	write_content_adaptive_brightness_control	1st	00h	00h	00h
56h	read_content_adaptive_brightness_control	1st	00h	00h	00h

Table 51 User Command (continued)

Operational Code(Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
5Eh	write_CABC_minimum_brightness	1st/2nd CMB[11:0]	00h	00h	00h
5Fh	read_CABC_minimum_brightness	1st/2nd CMB[11:0]	00h	00h	00h
68h	read_automatic_brightness_control_self-diagnostic_result	1st	00h	00h	00h
A1h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	Extend DDB ID1 (Note2)	Extend DDB ID1 (Note2)	Extend DDB ID1 (Note2)
		6th	Extend DDB ID2 (Note2)	Extend DDB ID2 (Note2)	Extend DDB ID2 (Note2)
		7th	Extend DDB ID3 (Note2)	Extend DDB ID3 (Note2)	Extend DDB ID3 (Note2)
		8th - 15th	XXh	XXh	XXh
		16th	FFh	FFh	FFh
A8h	read_DDB_continue	Variable	See read_DDB_start.	See read_DDB_start.	See read_DDB_start.
DAh	Read ID1	1st	00h	00h	00h
DBh	Read ID2	1st	00h	00h	00h
DCh	Read ID3	1st	00h	00h	00h

Notes: 1. No change from the value before soft_reset command.

2. Data are loaded from internal NVM. If user writes VCM register values, Supplier ID, and Supplier Elective Data to the NVM, the values are set to default.

User Command

nop : 00h

00h		nop											
		DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command		0	1	↑	0	0	0	0	0	0	0	0	00h
Parameter	None												
Description	This command is an empty command. It has no effect on the display module. X = Don't care												
Restriction	-												
Flow chart	-												

soft_reset: 01h

soft_reset												Hex
01h	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	0	0	0	0	1	01h
Parameter	None											
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See "Default Modes and Values") X = Don't care											
Restriction	If a soft_reset is sent when the display module is not in Sleep Mode, the host processor needs waittime before sending an exit_sleep_mode command. (please refer to the Appendix for waitime.) Soft_reset shall not be sent during exit_sleep_mode sequence. No new command setting is allowed until the RSP LCD driver enters the Sleep Mode. See "State Transition Diagram" for the sequence to enter Sleep Mode. If a soft_reset is sent when the display module is in Sleep Mode, data in NVM are read. No new command setting is inhibited when data are read (3 ms).											
Flow chart	<pre> graph TD A[soft_reset] --> B{Blank Display Device} B --> C{Reset to SW Defaults} C --> D[Sleep Mode On] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

Read_Display_Idetification_Infomation(RDDIDIF): 04h

RDDIDIF												
04h	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	0	0	1	0	0	04h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	xxh
1 st parameter	1	↑	1	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2 nd parameter	1	↑	1	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3 rd parameter	1	↑	1	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4 th parameter	1	↑	1	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5 th parameter	1	↑	1	ID3 [7]	ID3 [6]	ID3 [5]	ID3 [4]	ID3 [3]	ID3 [2]	ID3 [1]	ID3 [0]	XXh
6 th parameter	1	↑	1	ID4 [7]	ID4 [6]	ID4 [5]	ID4 [4]	ID4 [3]	ID4 [2]	ID4 [1]	ID4 [0]	XXh
7 th parameter	1	↑	1	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
8 th - 15 th parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
16 th parameter	1	↑	1	1	1	1	1	1	1	1	1	FFh
Description	ID1[15:0] ID2[15:0] ID3[7:0] ID4[7:0] IFID[6:0] The command returns information from the display module as follows: 1 st parameter: MS byte of Supplier ID (ID1[15:8]) 2 nd parameter: LS byte of Supplier ID (ID1[7:0]) 3 rd parameter: Supplier Elective Data (ID2[15:8]) 4 th parameter: Supplier Elective Data (ID2[7:0]) 5 th parameter: Extend DDB ID1 (ID3[7:0]) 6 th parameter: Extend DDB ID2 (ID4[7:0]) 7 th parameter: Extend DDB ID3 (IFID[6:0]) 16 th parameter: Exit code (FFh) Supplier ID and Supplier Elective Data stored in internal NVM are read. X = Don't care											
Restriction	-											

04h	read_DDB_start	
Flow chart	<pre> graph TD Start[read_DDB_start] --> Dummy[Dummy Read] subgraph Host [Host] direction TB P1[/1st parameter ID1[15:8] (MS byte of Supplier ID)] P2[/2nd parameter ID1[7:0] (LS byte of Supplier ID)] P3[/3rd parameter ID2[15:8] (MS byte of Supplier Elective Data)] P4[/4th parameter ID2[7:0] (LS byte of Supplier Elective Data)] P5[/5th parameter ID3[7:0] (Extend DDB ID1)] P6[/6th parameter ID4[[7:0] (Extend DDB ID2)] P7[/7th parameter IFID[6:0] (Extend DDB ID3)] P8[/8th - 15th parameter xxh] P16[/16th parameter FFh (Exit code)] end subgraph RSP_LCD_driver [RSP LCD driver] direction TB DR[Dummy Read] P1 P2 P3 P4 P5 P6 P7 P8 P16 end Start --> DR DR --> P1 P1 --> P2 P2 --> P3 P3 --> P4 P4 --> P5 P5 --> P6 P6 --> P7 P7 --> P8 P8 --> P16 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 	<p>04h</p> <p>read_DDB_start</p> <p>Flow chart</p> <p>Host</p> <p>RSP LCD driver</p> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <p>Note : When this command is read via DSI, dummy read operation is not performed.</p>

read_Number_of_the_Errors_on_DSI: 05h

05h	read_Number_of_the_Errors_on_DSI											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	0	0	1	0	1	05h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	P7	P6	P5	P4	P3	P2	P1	P0	XXh
Description	This command returns an error count when DSI is used. P[6:0] indicate an error count. When a count overflows, P[7] is set to 1. When P[7:0] is 0, D0 (0Eh of get_signal_mode) is set to 0. When this command is read via DSI, P[7:0] is cleared. When this command is read via interface except DSI, P[7:0] is not cleared. X = Don't care											
Restriction	-											
Flow chart	<p>Note : When this command is read via DSI, dummy read operation is not performed.</p>											

get_red_channel: 06h

06h												get_red_channel																																																																																		
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																																		
Command	0	1	↑	0	0	0	0	0	1	1	0	06h																																																																																		
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh																																																																																		
1 st parameter	1	↑	1	R7	R6	R5	R4	R3	R2	R1	R0	XXh																																																																																		
Description	<p>The display module returns the red component value of the first pixel in the active frame.</p> <p>This command is only valid for Type 2 and Type 3 display modules.</p> <p>R7 is the MSB and R0 is the LSB.</p> <p>Only the relevant bits are used according to the pixel format; unused bits are set to '0'</p> <ul style="list-style-type: none"> • 12 bit format: R3 is MSB and R0 is LSB. R[7:4] are set to '0'. • 16 bit format: R5 is MSB, R1 is LSB and R7, R6 and R0 are set to '0'. • 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. • 24 bit format: R7 is MSB and R0 is LSB. All bits are used. <table border="1" style="margin-left: 20px;"> <tr> <td>12bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>0</td><td>0</td><td>0</td><td>0</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td> </tr> <tr> <td>16bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>0</td><td>0</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>0</td> </tr> <tr> <td>18bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>0</td><td>0</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td> </tr> <tr> <td>24bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>R7</td><td>R6</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td> </tr> </table>	12bit format	D7	D6	D5	D4	D3	D2	D1	D0		0	0	0	0	R3	R2	R1	R0	16bit format	D7	D6	D5	D4	D3	D2	D1	D0		0	0	R4	R3	R2	R1	R0	0	18bit format	D7	D6	D5	D4	D3	D2	D1	D0		0	0	R5	R4	R3	R2	R1	R0	24bit format	D7	D6	D5	D4	D3	D2	D1	D0		R7	R6	R5	R4	R3	R2	R1	R0																					
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24bit format	D7	D6	D5	D4	D3	D2	D1	D0																																																																																						
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Restriction	-																																																																																													
Flow chart	<pre> graph TD HP[Host Processor] -- "get_red_channel" --> DM[Display Module] DM -- "Parameter 1" --> P1[Parameter 1] </pre>																																																																																													

get_green_channel: 07h

07h												get_green_channel																																																																																		
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																																		
Command	0	1	↑	0	0	0	0	0	1	1	1	07h																																																																																		
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh																																																																																		
1 st parameter	1	↑	1	G7	G6	G5	G4	G3	G2	G1	G0	XXh																																																																																		
Description	<p>The display module returns the red component value of the first pixel in the active frame.</p> <p>This command is only valid for Type 2 and Type 3 display modules.</p> <p>G7 is the MSB and G0 is the LSB.</p> <p>Only the relevant bits are used according to the pixel format; unused bits are set to '0'</p> <ul style="list-style-type: none"> • 12 bit format: G3 is MSB and G0 is LSB. G[7:4] are set to '0'. • 16 bit format: G5 is MSB, G1 is LSB. G7 and G6 are set to '0'. • 18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. • 24 bit format: G7 is MSB and G0 is LSB. All bits are used. <table border="1" style="margin-left: 20px;"> <tr> <td>12bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>0</td><td>0</td><td>0</td><td>0</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td> </tr> <tr> <td>16bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>0</td><td>0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td> </tr> <tr> <td>18bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>0</td><td>0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td> </tr> <tr> <td>24bit format</td> <td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td> </tr> <tr> <td></td> <td>G7</td><td>G6</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td> </tr> </table>	12bit format	D7	D6	D5	D4	D3	D2	D1	D0		0	0	0	0	G3	G2	G1	G0	16bit format	D7	D6	D5	D4	D3	D2	D1	D0		0	0	G5	G4	G3	G2	G1	G0	18bit format	D7	D6	D5	D4	D3	D2	D1	D0		0	0	G5	G4	G3	G2	G1	G0	24bit format	D7	D6	D5	D4	D3	D2	D1	D0		G7	G6	G5	G4	G3	G2	G1	G0																					
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Restriction	-																																																																																													
Flow chart	<pre> graph TD HP[Host Processor] -- "get_green_channel" --> DM[Display Module] DM -- "Parameter 1" --> P1[Parameter 1] </pre>																																																																																													

get_blue_channel: 08h

08h												get_blue_channel																										
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																										
Command	0	1	↑	0	0	0	0	1	0	0	0	08h																										
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh																										
1 st parameter	1	↑	1	B7	B6	B5	B4	B3	B2	B1	B0	XXh																										
Description	<p>The display module returns the red component value of the first pixel in the active frame.</p> <p>This command is only valid for Type 2 and Type 3 display modules.</p> <p>B7 is the MSB and B0 is the LSB.</p> <p>Only the relevant bits are used according to the pixel format; unused bits are set to '0'</p> <ul style="list-style-type: none"> • 12 bit format: B3 is MSB and B0 is LSB. B[7:4] are set to '0'. • 16 bit format: B5 is MSB, B1 is LSB and B7, B6 and B0 are set to '0'. • 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. • 24 bit format: B7 is MSB and B0 is LSB. All bits are used. <table border="1" style="margin-left: 20px;"> <tr> <td>12bit format</td> <td>D7 D6 D5 D4 D3 D2 D1 D0</td> </tr> <tr> <td></td> <td>0 0 0 0 B3 B2 B1 B0</td> </tr> <tr> <td>16bit format</td> <td>D7 D6 D5 D4 D3 D2 D1 D0</td> </tr> <tr> <td></td> <td>0 0 B4 B3 B2 B1 B0 0</td> </tr> <tr> <td>18bit format</td> <td>D7 D6 D5 D4 D3 D2 D1 D0</td> </tr> <tr> <td></td> <td>0 0 B5 B4 B3 B2 B1 B0</td> </tr> <tr> <td>24bit format</td> <td>D7 D6 D5 D4 D3 D2 D1 D0</td> </tr> <tr> <td></td> <td>B7 B6 B5 B4 B3 B2 B1 B0</td> </tr> </table>																						12bit format	D7 D6 D5 D4 D3 D2 D1 D0		0 0 0 0 B3 B2 B1 B0	16bit format	D7 D6 D5 D4 D3 D2 D1 D0		0 0 B4 B3 B2 B1 B0 0	18bit format	D7 D6 D5 D4 D3 D2 D1 D0		0 0 B5 B4 B3 B2 B1 B0	24bit format	D7 D6 D5 D4 D3 D2 D1 D0		B7 B6 B5 B4 B3 B2 B1 B0
12bit format	D7 D6 D5 D4 D3 D2 D1 D0																																					
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	0 0 B5 B4 B3 B2 B1 B0																																					
24bit format	D7 D6 D5 D4 D3 D2 D1 D0																																					
	B7 B6 B5 B4 B3 B2 B1 B0																																					
Restriction	-																																					
Flow chart	<pre> graph TD HP[Host Processor] -- "get_blue_channel" --> DM[Display Module] DM -- "Parameter 1" --> P1[Parameter 1] </pre>																																					

get_power_mode: 0Ah

0Ah	get_power_mode											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	0	1	0	1	0	0Ah
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	0	0	0	SLPOUT	1	DSPON	0	0	XXh
Description	The display module returns the current power mode as listed below.											
Bit	Description				Comment			Command list symbol				
D7	Reserved				Set to '0'.			-				
D6	Reserved				Set to '0'			-				
D5	Reserved				Set to '0'			-				
D4	Sleep Mode On/Off							SLPOUT				
D3	Reserved							1				
D2	Display On/Off							DSPON				
D1	Reserved				Set to '0'.			-				
D0	Reserved				Set to '0'.			-				
<ul style="list-style-type: none"> Bit D[7:5] – Reserved This bit is not applicable. Set to '0'. (Not supported) <p>SLPOUT</p> <ul style="list-style-type: none"> Bit D4 – Sleep Mode On/Off '0' = Sleep Mode On '1' = Sleep Mode Off Bit D3 – Reserved This bit is not applicable. Set to '0'. (Not supported) 												

0Ah	get_power_mode
Description	<p>DSPON</p> <ul style="list-style-type: none"> Bit D2 – Display On/Off ‘0’ = Display is Off. ‘1’ = Display is On. Bit D1 – Reserved This bit is not applicable. Set to ‘0’. (Not supported) Bit D0 – Reserved This bit is not applicable. Set to ‘0’. (Not supported) X = Don’t care
Restriction	-
Flow chart	<pre> graph TD Host[Host] -- "get_power_mode" --> RSP[RSP LCD driver] RSP -- "Dummy Read" --> Action[Send 1st parameter] </pre> <p>Note : When this command is read via DSI, dummy read operation is not performed.</p> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

get_address_mode: 0Bh

0Bh	get_address_mode																																															
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																				
Command	0	1	↑	0	0	0	0	1	0	1	1	0Bh																																				
Dummy parameter	0	1	↑	X	X	X	X	X	X	X	X	XXh																																				
1 st parameter	1	↑	1	B7	B6	0	0	B3	0	0	0	XXh																																				
Description	<p>The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h).</p> <p>For B3 and B0, please refer to the Appendix for each mode.</p> <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Page Address Order</td><td></td><td>B7</td></tr> <tr> <td>D6</td><td>Column Address Order</td><td></td><td>B6</td></tr> <tr> <td>D5</td><td>Page/column Order</td><td>Set to '0'</td><td></td></tr> <tr> <td>D4</td><td>Line Address Order</td><td>Set to '0'</td><td>-</td></tr> <tr> <td>D3</td><td>RGB/BGR Order</td><td></td><td>B3</td></tr> <tr> <td>D2</td><td>Display Data Latch Order</td><td>Set to '0'.</td><td></td></tr> <tr> <td>D1</td><td>Reserved</td><td>Set to '0'.</td><td></td></tr> <tr> <td>D0</td><td>Switching between common outputs and frame memory</td><td>Set to '0'</td><td>-</td></tr> </tbody> </table> <ul style="list-style-type: none"> Bit D7 - Page Address Order '0' = Top to Bottom (When set_address_mode D7='0') '1' = Bottom to Top (When set_address_mode D7='1') Bit D6 – Column Address Order '0' = Left to Right (When set_address_mode D6='0') '1' = Right to Left (When set_address_mode D6='1') Bit D5 – Page/column Order This bit is not applicable. Set to '0'. (Not supported) Bit D4 – Line Address Order This bit is not applicable. Set to '0'. (Not supported) <p>Note: B3 and B0 depend on each Panel Interface Mode. See the appendix of each mode.</p>												Bit	Description	Comment	Command list symbol	D7	Page Address Order		B7	D6	Column Address Order		B6	D5	Page/column Order	Set to '0'		D4	Line Address Order	Set to '0'	-	D3	RGB/BGR Order		B3	D2	Display Data Latch Order	Set to '0'.		D1	Reserved	Set to '0'.		D0	Switching between common outputs and frame memory	Set to '0'	-
Bit	Description	Comment	Command list symbol																																													
D7	Page Address Order		B7																																													
D6	Column Address Order		B6																																													
D5	Page/column Order	Set to '0'																																														
D4	Line Address Order	Set to '0'	-																																													
D3	RGB/BGR Order		B3																																													
D2	Display Data Latch Order	Set to '0'.																																														
D1	Reserved	Set to '0'.																																														
D0	Switching between common outputs and frame memory	Set to '0'	-																																													

0Bh	get_address_mode
Description	<ul style="list-style-type: none"> Bit D3 – RGB/BGR Order For bit D3, see “set_address_mode (36h)” and the appendix data sheet. Bit D2 – Display DataLatch Data Order This bit is not applicable. Set to ‘0’. (Not supported) Bit D1 – Reserved This bit is not applicable. Set to ‘0’. (Not supported) Bit D0 – Switching between common outputs and frame memory This bit is not applicable. Set to ‘0’. (Not supported) <p>X = Don't care</p>
Restriction	-
Flow Chart	<pre> graph TD Host[Host] -- "get_address_mode" --> RSP[RSP LCD driver] RSP -- "Dummy Read" --> RSP RSP -- "Send 1st parameter" --> RSP </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <p>Note : When this command is read via DSI, dummy read operation is not</p>

Note: For display mode transition, see “State Transition Diagram.”

get_pixel_format: 0Ch

0Ch	get_pixel_format																																															
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																				
Command	0	1	↑	0	0	0	0	1	1	0	0	0Ch																																				
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh																																				
1 st parameter	1	↑	1	0	D6	D5	D4	0	0	0	0	XXh																																				
Description	This command indicates the current status of the display as described in the table below. This command setting depends on set_pixel_format (3Ah).																																															
	<table border="1"> <thead> <tr> <th>Bit</th> <th colspan="3">Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td colspan="3" rowspan="4">DPI Pixel Format (RGB Interface Color Format)</td><td>Set to '0'.</td></tr> <tr> <td>D6</td> <td>D6</td></tr> <tr> <td>D5</td> <td>D5</td></tr> <tr> <td>D4</td> <td>D4</td></tr> <tr> <td>D3</td> <td colspan="3" rowspan="4">DBI Pixel Format (Control Interface Color Format)</td><td>Set to '0'.</td></tr> <tr> <td>D2</td> <td>Set to '0'.</td></tr> <tr> <td>D1</td> <td>Set to '0'.</td></tr> <tr> <td>D0</td> <td>Set to '0'.</td></tr> </tbody> </table>												Bit	Description			Comment	D7	DPI Pixel Format (RGB Interface Color Format)			Set to '0'.	D6	D6	D5	D5	D4	D4	D3	DBI Pixel Format (Control Interface Color Format)			Set to '0'.	D2	Set to '0'.	D1	Set to '0'.	D0	Set to '0'.									
Bit	Description			Comment																																												
D7	DPI Pixel Format (RGB Interface Color Format)			Set to '0'.																																												
D6				D6																																												
D5				D5																																												
D4				D4																																												
D3	DBI Pixel Format (Control Interface Color Format)			Set to '0'.																																												
D2				Set to '0'.																																												
D1				Set to '0'.																																												
D0				Set to '0'.																																												
	<ul style="list-style-type: none"> Bits D[6:4] – DPI Pixel Format (DSI Video Mode Control Interface Color Format Selection) Bits D7 and D[3:0] <p>This bit is not applicable. Set to '0'.</p>																																															
	Note: See "set_pixel_format (3Ah)."																																															
	<table border="1"> <thead> <tr> <th>Control Interface Color Format</th> <th>D6</th> <th>D5</th> <th>D4</th> </tr> </thead> <tbody> <tr> <td>Setting inhibited</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Setting inhibited</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Setting inhibited</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Setting inhibited</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Setting inhibited</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>Setting inhibited</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 bits/pixel (262,144 colors)</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 bits/pixel (16,777,216 colors)</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>												Control Interface Color Format	D6	D5	D4	Setting inhibited	0	0	0	Setting inhibited	0	0	1	Setting inhibited	0	1	0	Setting inhibited	0	1	1	Setting inhibited	1	0	0	Setting inhibited	1	0	1	18 bits/pixel (262,144 colors)	1	1	0	24 bits/pixel (16,777,216 colors)	1	1	1
Control Interface Color Format	D6	D5	D4																																													
Setting inhibited	0	0	0																																													
Setting inhibited	0	0	1																																													
Setting inhibited	0	1	0																																													
Setting inhibited	0	1	1																																													
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18 bits/pixel (262,144 colors)	1	1	0																																													
24 bits/pixel (16,777,216 colors)	1	1	1																																													
	X = Don't care																																															

0Ch	get_pixel_format
Flow chart	<p>Host</p> <p>RSP LCD driver</p> <p>Note : When this command is read via DSI, dummy read operation is not performed.</p> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer

get_display_mode: 0Dh

get_display_mode																																																									
0Dh	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																													
Command	0	1	↑	0	0	0	0	1	1	0	1	0Dh																																													
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh																																													
1 st parameter	1	↑	1	0	0	0	0	0	D2	D1	D0	XXh																																													
Description	The display module returns the current status of the display as described in the table below.																																																								
	Bit	Description						Comment	Command list symbol																																																
	D7	Vertical Scrolling Status						Set to '0'.																																																	
	D6	Reserved						Set to '0'.																																																	
	D5	Reserved						Set to '0'.																																																	
	D4	Reserved						Set to '0'.																																																	
	D3	Reserved						Set to '0'.																																																	
	D2	Gamma Curve Selection							D2																																																
	D1	Gamma Curve Selection							D1																																																
	D0	Gamma Curve Selection							D0																																																
	<ul style="list-style-type: none"> Bit D7 – Vertical Scrolling Status This bit is not applicable. Set to '0'. Bit D6 – Reserved This bit is not applicable. Set to '0'. Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. Bit D[4:3] – Reserved This bit is not applicable. Set to '0'. Bit D[2:0] – Gamma Curve Selection 																																																								
	<table border="1"> <thead> <tr> <th>Gamma Curve Selection</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set(26h) Parameter</th> </tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve 2</td> <td>0</td> <td>0</td> <td>1</td> <td>GC1</td> </tr> <tr> <td>Gamma Curve 3</td> <td>0</td> <td>1</td> <td>0</td> <td>GC2</td> </tr> <tr> <td>Gamma Curve 4</td> <td>0</td> <td>1</td> <td>1</td> <td>GC3</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </tbody> </table>												Gamma Curve Selection	D2	D1	D0	Gamma Set(26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	GC1	Gamma Curve 3	0	1	0	GC2	Gamma Curve 4	0	1	1	GC3	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
Gamma Curve Selection	D2	D1	D0	Gamma Set(26h) Parameter																																																					
Gamma Curve 1	0	0	0	GC0																																																					
Gamma Curve 2	0	0	1	GC1																																																					
Gamma Curve 3	0	1	0	GC2																																																					
Gamma Curve 4	0	1	1	GC3																																																					
Not Defined	1	0	0	Not Defined																																																					
Not Defined	1	0	1	Not Defined																																																					
Not Defined	1	1	0	Not Defined																																																					
Not Defined	1	1	1	Not Defined																																																					
	X = Don't care																																																								
Restriction	-																																																								

0Dh	get_display_mode
Flow chart	<p>Host</p> <p>RSP LCD driver</p> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer <pre>graph TD; A[get_display_mode] --> B{Dummy Read}; B --> C[Send 1st parameter]</pre> <p>Note : When this command is read via DSI, dummy read operation is not performed.</p>

get_signal_mode: 0Eh

get_signal_mode												
0Eh	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	0	1	1	1	0	0Eh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	xxh
1 st parameter	1	↑	1	TEO N	TELO M	0	0	0	0	0	RDD SM_D0	xxh
Description	The display module returns the current status of the display as described in the table below.											
	Bit	Description						Comment		Command list symbol		
	D7	Tearing Effect Line On/Off								TEON		
	D6	Tearing Effect Line Output Mode								TELOM		
	D5	Reserved						Set to '0'.		-		
	D4	Reserved						Set to '0'.		-		
	D3	Reserved						Set to '0'.		-		
	D2	Reserved						Set to '0'.		-		
	D1	Reserved						Set to '0'.		-		
	D0	Errors on DSI								RDDSM_D0		
Restriction	-											

- Bit D[7:1] – Reserved

This bit is not applicable. Set to '0'. (Not supported)

- Bit D0 – Errors on DSI (See “read_Number_of_the_Errors_on_DSI: 05h”)

'0' = No error
'1' = Error

X = Don't care

0Eh	get_signal_mode
Flow chart	<p>Host</p> <p>RSP LCD driver</p> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer <p>Note : When this command is read via DSI, dummy read operation is not performd.</p>

get_diagnostic_result: 0Fh

get_diagnostic_result																						
0Fh	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex										
Command	0	1	↑	0	0	0	0	1	1	1	1	0F										
Dummy parameter	0	↑	1	X	X	X	X	X	X	X	X	XXh										
1 st parameter	0	↑	1	0	FUN CD	0	0	0	0	0	0	XXh										
Description	Bit	Description						Comment		Command list symbol												
	D7	Register Loading Detection						Set to '0'.		-												
	D6	Functionality Detection								FUNCD												
	D5	Chip Attachment Detection						Set to '0'.		-												
	D4	Display Glass Break Detection						Set to '0'.		-												
	D3	Reserved						Set to '0'.		-												
	D2	Reserved						Set to '0'.		-												
	D1	Reserved						Set to '0'.		-												
	D0	Reserved						Set to '0'.		-												
X = Don't care	The display module returns the self-diagnostic results following the exit_sleep_mode (11h) as shown in the table above.																					
	<ul style="list-style-type: none"> Bit D7 – Register Loading Detection This bit is not applicable. Set to "0". <p>FUNCD</p> <ul style="list-style-type: none"> Bit D6 – Functionality Detection Note: For D6, see "Self-Diagnostic Function." Bit D5 – Chip Attachment Detection This bit is not applicable. Set to "0". Bit D4 – Display Glass Break Detection This bit is not applicable. Set to "0". Bit D[3:0] – Reserved Reserved. Set to 0. 																					
Restriction	-																					

0Fh	get_diagnostic_result
Flow chart	<p>Host RSP LCD driver</p> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer <p>Note : When this command is read via DSI, dummy read operation is not performd.</p>

enter_sleep_mode: 10h

enter_sleep_mode												
10h	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	0	0	0	0	10h
Parameter	None											
Description	<p>This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop.</p> <p>See "State Transition Diagram" for each stage of transition.</p> <p>X = Don't care</p>											
Restriction	<p>This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted.</p> <p>Sending a new command is prohibited while the RSP LCD driver performs either display off sequence or power off sequence.</p>											
Flow chart	<pre> graph TD AnyMode([Any Mode]) --> EnterSleepMode[enter_sleep_mode] EnterSleepMode --> BlankDisplayDevice{Blank Display Device} BlankDisplayDevice --> PowerOffDisplayDevice{Power Off Display Device} EnterSleepMode --> StopPowerSupply{Stop Power Supply} StopPowerSupply --> StopInternalOscillator{Stop Internal Oscillator} StopInternalOscillator --> SleepMode([Sleep Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

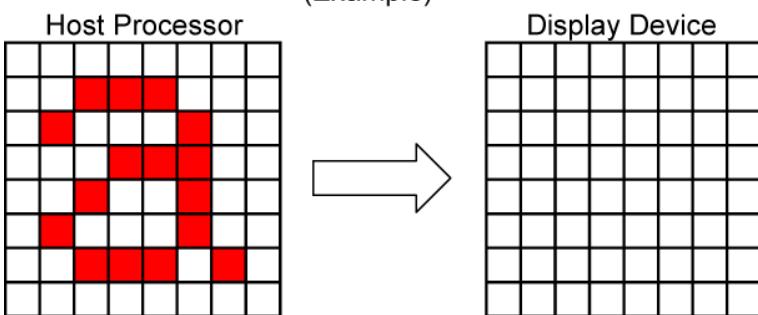
exit_sleep_mode: 11h

exit_sleep_mode												
11h	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	0	0	0	1	11h
Parameter	None											
Description	<p>This command causes the display module to exit Sleep mode. The DC/DC converter, internal oscillator, and panel scanning start.</p> <p>See "State Transition Diagram" for each stage of transition.</p> <p>X = Don't care</p>											
Restriction	<p>This command shall not cause any visual effect on display device when the display module is not in Sleep mode.</p> <p>No new command setting is allowed during power on sequence. Operation may continue due to power on sequence setting. The host processor needs waittime.(please refer to the Appendix for waittime.) Do not send any command either in this case.</p> <p>The host processor needs waittime after sending an enter_sleep_mode command before sending an exit_sleep_mode command. (please refer to the Appendix for waittime.)</p> <p>The display runs the self-diagnostic function after this command is received.</p>											
Flow chart	<pre> graph TD A([Sleep Mode]) --> B[exit_sleep_mode] B --> C{Start Internal Oscillator} C --> D{Start Power Supply} D --> E{Power On Display Device} E --> F{Blank Display Device} F --> G{Display Memory contents} G --> H([Sleep Mode Off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

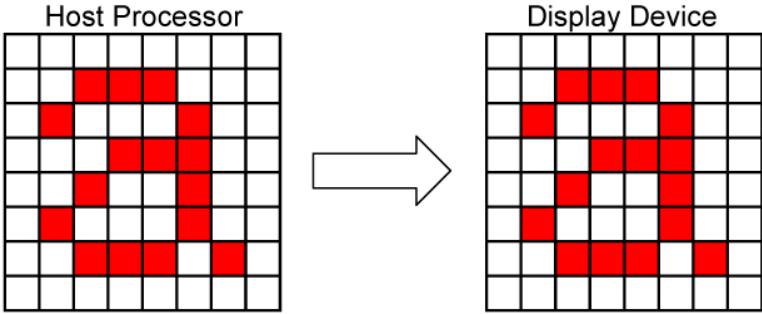
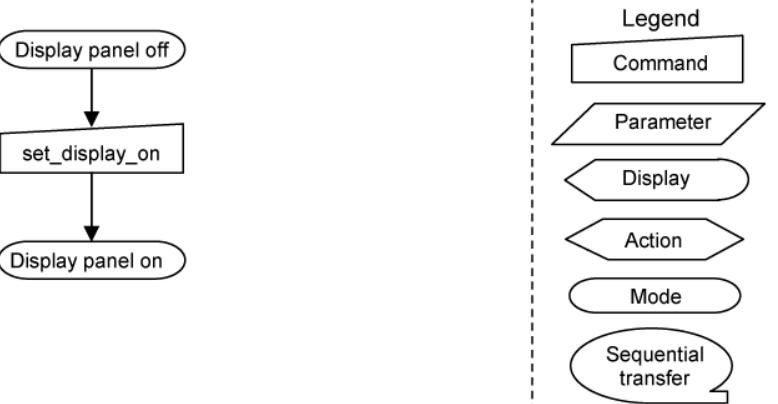
set_gamma_curve: 26h

set_gamma_curve																														
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																		
Command	0	1	↑	0	0	1	0	0	1	1	0	26h																		
Parameter	1	1	↑	0	0	0	GC [4]	GC [3]	GC [2]	GC [1]	GC [0]	XXh																		
Description	This command selects a gamma curve set beforehand. A gamma curve is selected from four curves according to image data.																													
	<table border="1"> <thead> <tr> <th>GC[7:0]</th> <th>parameter</th> <th>Selection</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>GC[0]</td> <td>Gamma Curve 1</td> </tr> <tr> <td>2</td> <td>GC[1]</td> <td>Gamma Curve 2</td> </tr> <tr> <td>4</td> <td>GC[2]</td> <td>Gamma Curve 3</td> </tr> <tr> <td>8</td> <td>GC[3]</td> <td>Gamma Curve 4</td> </tr> <tr> <td>-</td> <td>GC[7:4]</td> <td>Reserved (Set to "0")</td> </tr> </tbody> </table> <p>X=Don't care</p>												GC[7:0]	parameter	Selection	1	GC[0]	Gamma Curve 1	2	GC[1]	Gamma Curve 2	4	GC[2]	Gamma Curve 3	8	GC[3]	Gamma Curve 4	-	GC[7:4]	Reserved (Set to "0")
GC[7:0]	parameter	Selection																												
1	GC[0]	Gamma Curve 1																												
2	GC[1]	Gamma Curve 2																												
4	GC[2]	Gamma Curve 3																												
8	GC[3]	Gamma Curve 4																												
-	GC[7:4]	Reserved (Set to "0")																												
Restriction	Setting parameters except the above ones is disabled. A selected gamma curve is not changed until a correct value is set.																													
Flow chart	<pre> graph TD Start[set_gamma_curve] --> Param1[/1st parameter GC[7:0]/] Param1 --> Load{New gamma curve loaded} Load --- Merge(()) style Param1 fill:#ffffcc style Load fill:#ffffcc style Merge fill:#ffffcc style Start fill:#ffffcc style Legend fill:#ffffcc style Legend border:1px solid black style Legend padding:5px subgraph Legend direction TB C[Command] --- P[Parameter] D[Display] --- A[Action] M[Mode] --- ST[Sequential transfer] end </pre>																													

set_display_off: 28h

set_display_off												
28h	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	1	0	1	0	0	0	28h
Parameter	None											
Description	This command causes the display module to stop displaying image data on the display device. (Example)  X = Don't care											
Restriction	This command has no effect when the display panel is already off.											
Flow chart	 <pre> graph TD A([Display panel on]) --> B[set_display_off] B --> C([Display panel off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

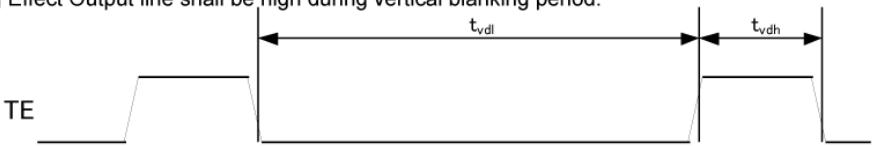
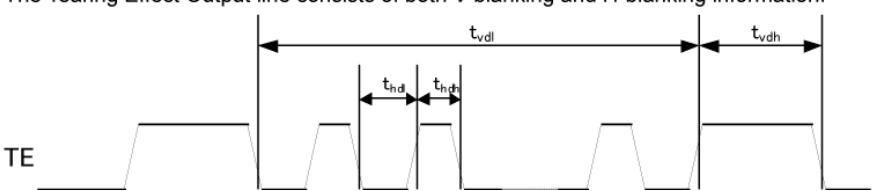
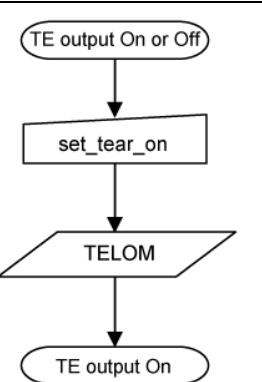
set_display_on: 29h

29h	set_display_on											Hex
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	1	0	1	0	0	1	29h
Parameter	None											
Description	This command causes the display module to start displaying the image data on the display device.											
	(Example)											
	 <p style="text-align: center;">Host Processor</p> <p style="text-align: center;">Display Device</p> <p style="text-align: center;">X = Don't care</p>											
Restriction	This command has no effect when the display panel is already on.											
Flow chart	 <pre> graph TD A([Display panel off]) --> B[set_display_on] B --> C([Display panel on]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

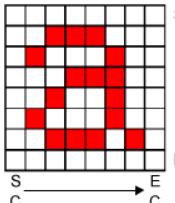
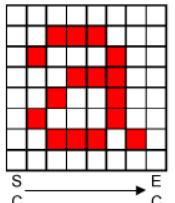
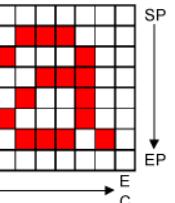
set_tear_off: 34h

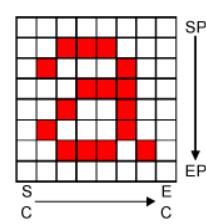
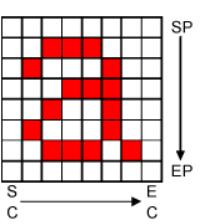
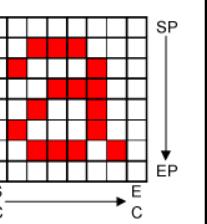
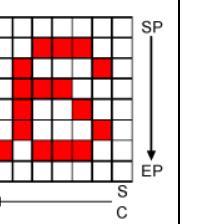
34h												Hex
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	1	1	0	1	0	0	34h
Parameter	None											
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care											
Restriction	This command has no effect when Tearing Effect output is already off.											
Flow chart	<pre> graph TD A([TE output On or Off]) --> B[/set_tear_off/] B --> C([TE output off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

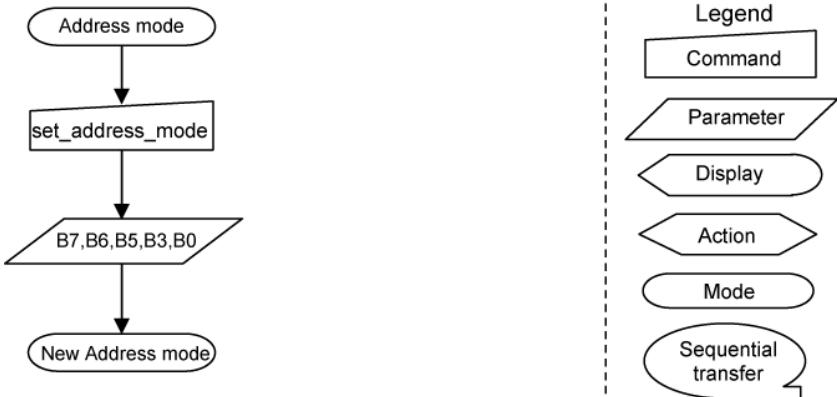
set_tear_on: 35h

35h												
set_tear_on												
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	1	1	0	1	0	1	35h
1 st parameter	1	1	↑	X	X	X	X	X	X	X	TELO M	XXh
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal line. Changing B4 (Line Refresh Order of set_address_mode (36h)) does not change this output. The Tearing Effect Line On has one parameter, TELO, which describes the Tearing Effect Output Line mode. See "TE Pin Output Signal" for detail.</p> <p>TELO = 0: The Tearing Effect Output line consists of V-Blinking information only. The Tearing Effect Output line shall be high during vertical blanking period.</p>  <p>TELO = 1: The Tearing Effect Output line consists of both V-blanking and H-blanking information.</p>  <p>Vertical blanking period: BP + FP</p> <p>Note 1: The Tearing Effect Output line shall be low when the display module is in Sleep mode.</p> <p>Note 2: Set TELO to 0 when DSI TE-reporting function is used.</p> <p>X = Don't care</p>											
Restriction	This command has no effect when Tearing Effect output is already ON. Changes in parameter TELO is enabled from the next frame period.											
Flow Chart	 <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>											

set_address_mode: 36h

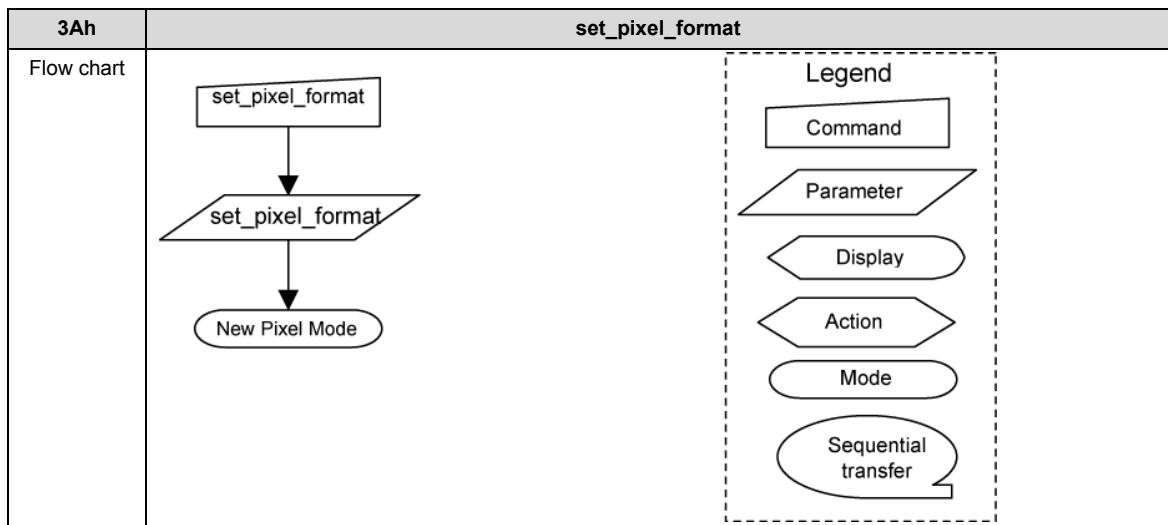
36h		set_address_mode											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex	
Command	0	1	↑	0	0	1	1	0	1	1	0	36h	
1 st parameter	1	1	↑	B7	B6	0	0	B3	0	0	0	XXh	
Description													
Bit	Description				Comment			Symbol					
D7	Page Address Order							B7					
D6	Column Address Order							B6					
D5	Page/Column Addressing Order				Set to "0"			-					
D4	Display Device Line Refresh Order				Set to "0"			-					
D3	RGB/BGR Order							B3					
D2	Display Data Latch Data Order				Set to "0"			-					
D1	Flip Horizontal				Set to "0"			-					
D0	Flip Vertical				Set to "0"			-					
<ul style="list-style-type: none"> Bit D7 – Page Address Order '0' = Top to Bottom. '1' = Bottom to Top. 													
		B7=0				B7=1							
		Host Processor B6=0 B5=0 B3=X		Display Device 		Host Processor 		Display Device 					
See the appendix when Video mode is used on DSI, and DPI.													

36h	set_address_mode			
Description	<ul style="list-style-type: none"> Bit D6 – Column Address Order '0' = Left to Right. '1' = Right to Left. 			
	B6=0	Host Processor	Display Device	B6=1
B7=0 B5=0 B3=X				
	<ul style="list-style-type: none"> Bit D5 – Page/Column Addressing Order This bit is not applicable. Set to '0'. (Not supported) Bit D4 – Display Device Line Refresh Order This bit is not applicable. Set to '0'. (Not supported) Bit D3 – RGB/BGR Order '0' = RGB When set_address_mode D3 ='0' '1' = BGR When set_address_mode D3 ='1' Bit D2 – Display Data Latch Order This bit is not applicable. Set to '0'. (Not supported) Bit D1 – Flip Horizontal This bit is not applicable. Set to '0'. (Not supported) Bit D0 – Flip Vertical This bit is not applicable. Set to '0'. (Not supported) 			
	X = Don't care			

36h	set_address_mode
Restriction	-
Flow chart	 <pre>graph TD; A([Address mode]) --> B[set_address_mode]; B --> C{B7,B6,B5,B3,B0}; C --> D([New Address mode]);</pre> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer

set_pixel_format: 3Ah

set_pixel_format																																																
3Ah	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																				
Command	0	1	↑	0	0	1	1	1	0	1	0	3Ah																																				
1 st parameter	1	1	↑	0	D6	D5	D4	0	0	0	0	XXh																																				
Description	This command is used to define the format of RGB picture data, which are to be transferred via the interface. The formats are shown in the following table. <ul style="list-style-type: none"> Bit D[6:4] –Pixel Format (Video Mode Control Interface Color Format Selection) Bits D7 and D[3:0] This bit is not applicable. Set to '0'. (Not supported)																																															
	<table border="1"> <thead> <tr> <th>Control Interface Color Format</th><th>D6</th><th>D5</th><th>D4</th></tr> </thead> <tbody> <tr> <td>Setting inhibited</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>Setting inhibited</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>Setting inhibited</td><td>0</td><td>1</td><td>0</td></tr> <tr> <td>Setting inhibited</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>Setting inhibited</td><td>1</td><td>0</td><td>0</td></tr> <tr> <td>Setting inhibited</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>18 bits/pixel (262,144 colors)</td><td>1</td><td>1</td><td>0</td></tr> <tr> <td>24 bits/pixel (16,777,216 colors)</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> See "Data Format" for each interface data format. Note : When the setting disabled bits are set, undesirable image will be displayed on the panel. X = Don't care												Control Interface Color Format	D6	D5	D4	Setting inhibited	0	0	0	Setting inhibited	0	0	1	Setting inhibited	0	1	0	Setting inhibited	0	1	1	Setting inhibited	1	0	0	Setting inhibited	1	0	1	18 bits/pixel (262,144 colors)	1	1	0	24 bits/pixel (16,777,216 colors)	1	1	1
Control Interface Color Format	D6	D5	D4																																													
Setting inhibited	0	0	0																																													
Setting inhibited	0	0	1																																													
Setting inhibited	0	1	0																																													
Setting inhibited	0	1	1																																													
Setting inhibited	1	0	0																																													
Setting inhibited	1	0	1																																													
18 bits/pixel (262,144 colors)	1	1	0																																													
24 bits/pixel (16,777,216 colors)	1	1	1																																													
Restriction																																																



set_tear_scanline:44h

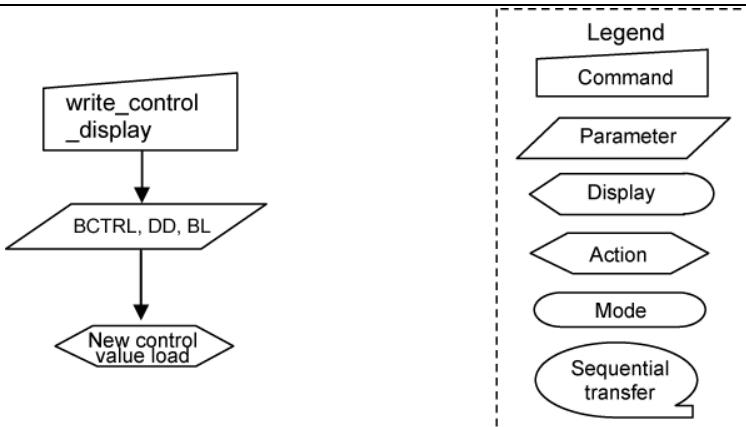
44h												
	set_tear_scanline											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	1	0	0	0	1	0	0	44h
1 st parameter	1	1	↑	0	0	0	0	0	STS [10]	STS [9]	STS [8]	0Xh
2 nd parameter	1	1	↑	STS[7] 1	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by STS [n:0].</p> <p>TE line is unaffected by change in B4 bit of set_address_mode command.</p> <p>See figure in "TE Pin Output Signal".</p> <p>X = Don't care.</p>											
Restriction	<p>The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame.</p> <p>Setting is disabled when TELOM=1 of set_tear_on (35h).</p> <p>Make sure that STS [n:0] ≤ NL (number of line) + 1.</p> <p>For the number of bits (n) supported in STS[n:0], See "Term Definition."</p>											
Flow chart	<pre> graph TD A([TE Output On or Off]) --> B[set_tear_scanline] B --> C[/Send 1st parameter STS[15:8]/] C --> D[/Send 2nd parameter STS[7:0]/] D --> E([TE Output On the Nth line]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

write_display_brightness: 51h

read_display_brightness_value: 52h

52h	read_display_brightness_value											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	1	0	1	0	0	1	0	52h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	0	0	0	0	DBV [11]	DBV [10]	DBV [9]	DBV [8]	XXh
2 nd parameter	1	↑	1	DBV [7]	DBV [6]	DBV [5]	DBV [4]	DBV [3]	DBV [2]	DBV [1]	DBV [0]	XXh
Description	This command returns the current brightness value. DBV This register returns the brightness data of the LED that is the source of the current LEDPWM signal, whether the CABC function is on or off. X = Don't care											
Restriction	In Sleep Mode On, this register setting value is disabled.											
Flow chart	<p>Note : When this command is read via DSI, dummy read operation is not performed.</p>											

write_control_display: 53h

53h												write_control_display											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex											
Command	0	1	↑	0	1	0	1	0	0	1	1	53h											
1 st parameter	1	1	↑	X	X	BCTRL L	X	DD	BL	X	X	XXh											
Description	This command is used to control the CABC function. Set each register only in Sleep Mode On. Do not change the setting during operation.																						
	BCTRL The register is used to enable LEDPWM pin output. Set to 0 in a system configuration without the LEDPWM pin. Set to 1 in a system configuration with the LEDPWM pin.																						
	DD This register is used to enable / disable PWM's dimming function. The register is used to control change in brightness (change in PWM signal) when DBV register is rewritten or LEDPWM pin is turned on. This bit is applied to DBV register setting and not to brightness change by the CABC function.																						
	<table border="1"> <thead> <tr> <th>DD</th> <th>Dimming function</th> <th>Brightness change</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> <td>Changes immediately.</td> </tr> <tr> <td>1</td> <td>On</td> <td>Changes about PWM_DIV setting.</td> </tr> </tbody> </table>													DD	Dimming function	Brightness change	0	Off	Changes immediately.	1	On	Changes about PWM_DIV setting.	
DD	Dimming function	Brightness change																					
0	Off	Changes immediately.																					
1	On	Changes about PWM_DIV setting.																					
	BL This register controls on/off of the LEDPWM signal output. Note that LEDPWM is off in sleep mode regardless of BL value.																						
	<table border="1"> <thead> <tr> <th>BL</th> <th>LEDPWM signal output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>On</td> </tr> </tbody> </table>													BL	LEDPWM signal output	0	Off	1	On				
BL	LEDPWM signal output																						
0	Off																						
1	On																						
	X = Don't care																						
Restriction																							
Flow chart	 <p>The flowchart illustrates the sequence of operations:</p> <ul style="list-style-type: none"> The process begins with a rectangular box labeled "write_control_display". An arrow points down to a trapezoidal box labeled "BCTRL, DD, BL". From the trapezoidal box, an arrow points down to a diamond-shaped box labeled "New control value load". <p>A legend on the right side of the flowchart defines the symbols used:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a trapezoid. Action: Represented by a parallelogram. Mode: Represented by an oval. Display: Represented by a diamond. Sequential transfer: Represented by a double-headed arrow. 																						

read_control_value_display: 54h

read_control_value_display																													
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																	
Command	0	1	↑	0	1	0	1	0	1	0	0	54h																	
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh																	
1 st parameter	1	↑	1	X	X	BCTR L	X	DD	BL	X	X	XXh																	
Description	<p>This command indicates the current status of the CABC function set by write_control_display (53h) as follows.</p> <p>BCTRL</p> <p>This register controls on/off of the LEDPWM signal output. Note that LEDPWM is off in sleep mode regardless of BL value.</p> <p>DD</p> <p>This register is used to enable / disable LEDPWM's dimming function.</p> <table border="1"> <thead> <tr> <th>DD</th> <th>Dimming function</th> <th>Brightness change</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> <td>Changes immediately.</td> </tr> <tr> <td>1</td> <td>On</td> <td>Changes about PWM_DIV setting.</td> </tr> </tbody> </table> <p>BL</p> <p>The register is used to enable LEDPWM pin output.</p> <table border="1"> <thead> <tr> <th>BL</th> <th>LED PWM signal output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> <td>System configuration without the LEDPWM pin.</td> </tr> <tr> <td>1</td> <td>On</td> <td>System configuration with the LEDPWM pin.</td> </tr> </tbody> </table> <p>X = Don't care</p>												DD	Dimming function	Brightness change	0	Off	Changes immediately.	1	On	Changes about PWM_DIV setting.	BL	LED PWM signal output	0	Off	System configuration without the LEDPWM pin.	1	On	System configuration with the LEDPWM pin.
DD	Dimming function	Brightness change																											
0	Off	Changes immediately.																											
1	On	Changes about PWM_DIV setting.																											
BL	LED PWM signal output																												
0	Off	System configuration without the LEDPWM pin.																											
1	On	System configuration with the LEDPWM pin.																											
Restriction																													
Flow chart	<p>Note : When this command is read via DSI, dummy read operation is not performed.</p>																												

write_content_adaptive_brightness_control: 55h

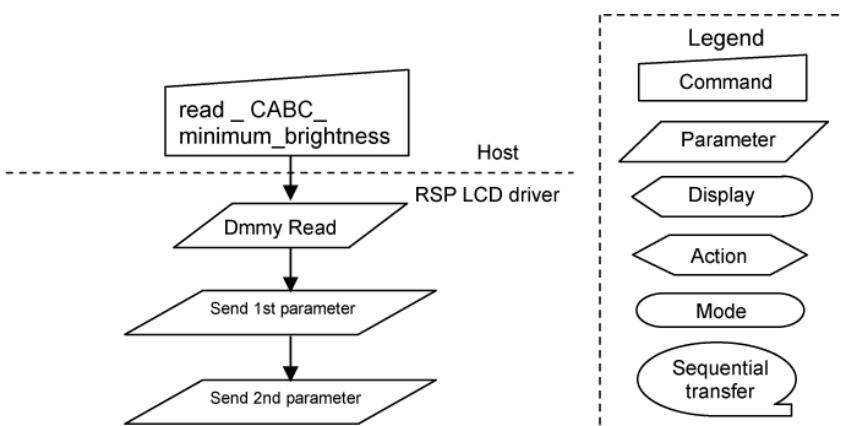
read_content_adaptive_brightness_control: 56h

56h	read_content_adaptive_brightness_control																										
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex															
Command	0	1	↑	0	1	0	1	0	1	1	0	56h															
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh															
1 st parameter	1	↑	1	X	X	X	X	X	X	C[1]	C[0]	XXh															
Description	The CABC function adjusts backlight brightness dynamically and processes image. This command indicates the current mode set by write_content_adaptive_brightness_control (55h) as follows.																										
	<table border="1"> <thead> <tr> <th>C[1]</th> <th>C[0]</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User interface image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still image</td> </tr> <tr> <td>1</td> <td>1</td> <td>Video image</td> </tr> </tbody> </table>												C[1]	C[0]	Function	0	0	Off	0	1	User interface image	1	0	Still image	1	1	Video image
C[1]	C[0]	Function																									
0	0	Off																									
0	1	User interface image																									
1	0	Still image																									
1	1	Video image																									
	X = Don't care																										
Restriction	-																										
Flow chart	<p>Note : When this command is read via DSI, dummy read operation is not performd.</p>																										

write_CABC_minimum_brightness: 5Eh

5Eh																												
	write_CABC_minimum_brightness																											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																
Command	0	1	↑	0	1	0	1	1	1	1	0	5Eh																
1 st parameter	1	1	↑	X	X	X	X	CMB [11]	CMB[10]	CMB [9]	CMB [8]	XXh																
2 nd parameter	1	1	↑	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	XXh																
Description	<p>This command is used to adjust the brightness of the CABC function.</p> <p>CMB</p> <p>When the CABC function is used, minimum brightness data is set by setting CMB register. This register setting value is enabled when the CABC function is on.</p> <table border="1"> <thead> <tr> <th>CMB[11:0]</th> <th>Amount of light</th> </tr> </thead> <tbody> <tr> <td>12'h000</td> <td>None (0%)</td> </tr> <tr> <td>12'h001</td> <td>1/4095</td> </tr> <tr> <td>12'h002</td> <td>2/4095</td> </tr> <tr> <td>12'h003</td> <td>3/4095</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>12'hFFE</td> <td>4094/4095</td> </tr> <tr> <td>12'hFFF</td> <td>4095/4095 (100%)</td> </tr> </tbody> </table> <p>X = Don't care</p>												CMB[11:0]	Amount of light	12'h000	None (0%)	12'h001	1/4095	12'h002	2/4095	12'h003	3/4095	:	:	12'hFFE	4094/4095	12'hFFF	4095/4095 (100%)
CMB[11:0]	Amount of light																											
12'h000	None (0%)																											
12'h001	1/4095																											
12'h002	2/4095																											
12'h003	3/4095																											
:	:																											
12'hFFE	4094/4095																											
12'hFFF	4095/4095 (100%)																											
Restriction																												
Flow chart	<pre> graph TD A[write_CABC_minimum_brightness] --> B{CMB[11:0]} B --> C{New display luminance value load} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																											

read_CABC_minimum_brightness: 5Fh

read_CABC_minimum_brightness												
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	1	0	1	1	1	1	1	5Fh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	X	X	X	X	CMB [11]	CMB [10]	CMB [9]	CMB [8]	XXh
2 nd parameter	1	↑	1	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	XXh
Description	This command returns the current minimum brightness value of the CABC function. CMB This register returns the minimum brightness data of the CABC function. X = Don't care											
Restriction	-											
Flow chart	 <p>Note : When this command is read via DSI, dummy read operation is not performed.</p>											

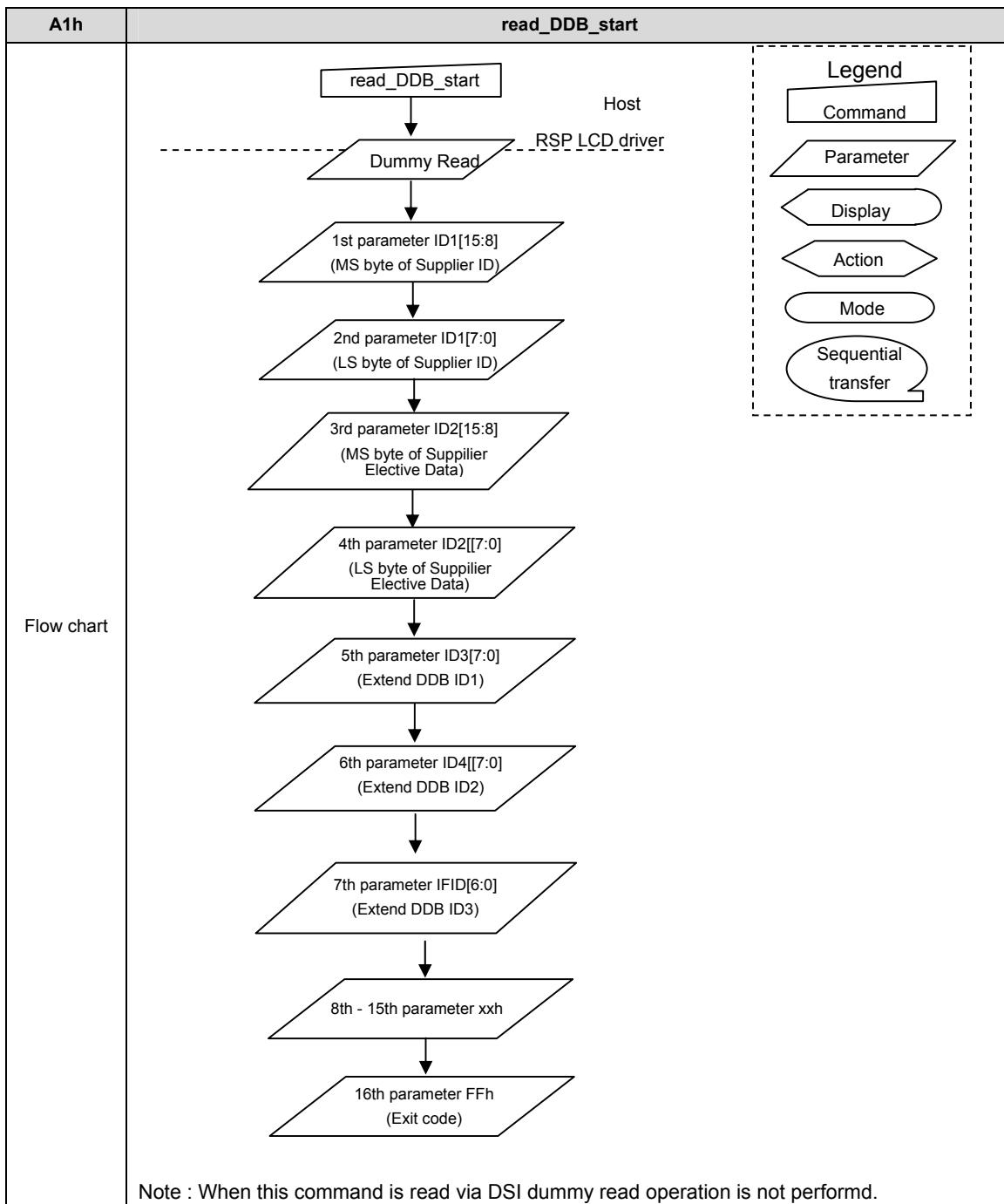
read_automatic_brightness_control_self-diagnostic: 68h

68h		read_automatic_brightness_control_self_diagnostic																																																																														
		DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																			
Command		0	1	↑	0	1	1	0	1	0	0	0	68h																																																																			
Dummy parameter		1	↑	1	X	X	X	X	X	X	X	X	XXh																																																																			
1 st parameter		1	↑	1	0	FUN CD	0	0	0	0	0	0	XXh																																																																			
Description	<table border="1"> <thead> <tr> <th>Bit</th><th colspan="5">Description</th><th>Comment</th><th>Command list symbol</th></tr> </thead> <tbody> <tr> <td>D7</td><td colspan="5">Register Loading Detection</td><td>Set to '0'.</td><td>-</td></tr> <tr> <td>D6</td><td colspan="5">Functionality Detection</td><td></td><td>FUNC</td></tr> <tr> <td>D5</td><td colspan="5">Chip Attachment Detection</td><td>Set to '0'.</td><td>-</td></tr> <tr> <td>D4</td><td colspan="5">Display Glass Break Detection</td><td>Set to '0'.</td><td>-</td></tr> <tr> <td>D3</td><td colspan="5">Reserved</td><td>Set to '0'.</td><td>-</td></tr> <tr> <td>D2</td><td colspan="5">Reserved</td><td>Set to '0'.</td><td>-</td></tr> <tr> <td>D1</td><td colspan="5">Reserved</td><td>Set to '0'.</td><td>-</td></tr> <tr> <td>D0</td><td colspan="5">Reserved</td><td>Set to '0'.</td><td>-</td></tr> </tbody> </table>								Bit	Description					Comment	Command list symbol	D7	Register Loading Detection					Set to '0'.	-	D6	Functionality Detection						FUNC	D5	Chip Attachment Detection					Set to '0'.	-	D4	Display Glass Break Detection					Set to '0'.	-	D3	Reserved					Set to '0'.	-	D2	Reserved					Set to '0'.	-	D1	Reserved					Set to '0'.	-	D0	Reserved					Set to '0'.	-
Bit	Description					Comment	Command list symbol																																																																									
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D2	Reserved					Set to '0'.	-																																																																									
D1	Reserved					Set to '0'.	-																																																																									
D0	Reserved					Set to '0'.	-																																																																									
<p>The display module returns the self-diagnostic results following the exit_sleep_mode (11h) as shown in the table above.</p> <ul style="list-style-type: none"> Bit D7 – Register Loading Detection This bit is not applicable. Set to "0". <p>FUNC</p> <ul style="list-style-type: none"> Bit D6 – Functionality Detection Note: For D6, see "Self-Diagnostic Function." Bit D5 – Chip Attachment Detection This bit is not applicable. Set to "0". Bit D4 –Display Glass Break Detection This bit is not applicable. Set to "0". Bit D[3:0] – Reserved Reserved. Set to 0. <p>X = Don't care</p>																																																																																
Restriction																																																																																

68h	get_diagnostic_result
Flow chart	<p>Host RSP LCD driver</p> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer <p>Note : When this command is read via DSI, dummy read operation is not performed.</p>

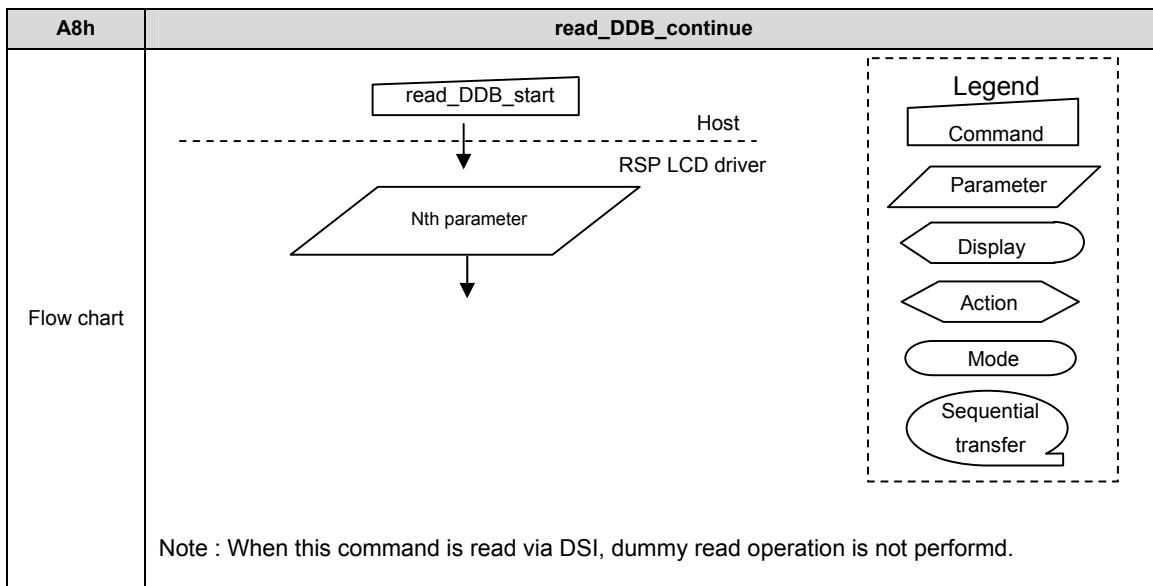
read_DDB_start: A1h

A1h	read_DDB_start											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	1	0	1	0	0	0	0	1	A1h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	xxh
1 st parameter	1	↑	1	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2 nd parameter	1	↑	1	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3 rd parameter	1	↑	1	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4 th parameter	1	↑	1	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5 th parameter	1	↑	1	ID3 [7]	ID3 [6]	ID3 [5]	ID3 [4]	ID3 [3]	ID3 [2]	ID3 [1]	ID3 [0]	XXh
6 th parameter	1	↑	1	ID4 [7]	ID4 [6]	ID4 [5]	ID4 [4]	ID4 [3]	ID4 [2]	ID4 [1]	ID4 [0]	XXh
7 th parameter	1	↑	1	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
8 th - 15 th parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
16 th parameter	1	↑	1	1	1	1	1	1	1	1	1	FFh
Description	ID1[15:0] ID2[15:0] ID3[7:0] ID4[7:0] IFID[6:0] The command returns information from the display module as follows: 1 st parameter: MS byte of Supplier ID (ID1[15:8]) 2 nd parameter: LS byte of Supplier ID (ID1[7:0]) 3 rd parameter: Supplier Elective Data (ID2[15:8]) 4 th parameter: Supplier Elective Data (ID2[7:0]) 7 th parameter: Extend DDB ID3 (IFID[6:0]) 16 th parameter: Exit code (FFh) Supplier ID and Supplier Elective Data stored in internal NVM are read. X = Don't care											
Restriction	-											



read_DDB_continue: A8h

A8h		read_DDB_continue											
		DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	1	0	1	0	1	0	0	0	0	A8h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	xxh
1 st parameter	1	↑	↑	DDB0 [7]	DDB0 [6]	DDB0 [5]	DDB0 [4]	DDB0 [3]	DDB0 [2]	DDB0 [1]	DDB0 [0]	XXh	
:	1	↑	↑	DDBx [7]	DDBx [6]	DDBx [5]	DDBx [4]	DDBx [3]	DDBx [2]	DDBx [1]	DDBx [0]	XXh	
N th parameter	1	↑	1	1	1	1	1	1	1	1	1	FFh	
Description	This command continues read operation from the position where the operation is halted by read_DDB_continue or read_DDB_start. For the position that information is returned, see read_DDB_start (A1h). X=Don't care												
Restriction	To fix the position that information is returned, execute read_DDB_start command and parameter read operation at least once before read_DDB_continue command is executed. If they are not executed, the value returned by read_DDB_continue command is invalid. [When MIPI DSI is selected] To fix the position that information is returned, execute read_DDB_start command at least once and parameter read operation at least once before read_DDB_continue command is executed. Otherwise, data read with a read_DDB_continue command is undefined. Note: When this command is read via DSI , dummy read operation is not performed.												



READ_ID1: DAh

DAh	READ_ID1											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	1	1	0	1	1	0	1	0	DAh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	RD ID1 [7]	RD ID1 [6]	RD ID1 [5]	RD ID1 [4]	RD ID1 [3]	RD ID1 [2]	RD ID1 [1]	RD ID1 [0]	XXh
Description	RDID1[7:0]											
	The command returns information from the display module as follows: 1 st parameter: RDID1 [7:0] RDID1 Data stored in internal NVM are read. X = Don't care											
Restriction	-											

READ_ID2: DBh

DBh	READ_ID2											
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	1	1	0	1	1	0	1	1	DBh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	RD ID2 [7]	RD ID2 [6]	RD ID2 [5]	RD ID2 [4]	RD ID2 [3]	RD ID2 [2]	RD ID2 [1]	RD ID2 [0]	XXh
Description	RDID2[7:0]											
	The command returns information from the display module as follows: 1 st parameter: RDID2 [7:0] RDID2 Data stored in internal NVM are read. X = Don't care											
Restriction	-											

READ_ID3: DCh

DCh		READ_ID3										
	DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	1	1	0	1	1	1	0	0	DCh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	XXh
1 st parameter	1	↑	1	RD ID3 [7]	RD ID3 [6]	RD ID3 [5]	RD ID3 [4]	RD ID3 [3]	RD ID3 [2]	RD ID3 [1]	RD ID3 [0]	XXh
Description	RDID3[7:0] The command returns information from the display module as follows: 1 st parameter: RDID3 [7:0] RDID3 Data stored in internal NVM are read. X = Don't care											
Restriction	-											

Read Mode In for DBI Only: F5h

F5h		Read Mode In for DBI Only											
		DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command		0	1	↑	1	1	1	1	0	1	0	1	F5h
Description	<p>When MIPI DBI Type C is selected, the RSP LCD driver enters Manufacturer Command read mode after accepting this command.</p> <p>When Manufacturer command is input after this command, a parameter is output in synchronization with a falling edge of SCL.</p> <p>To exit the read mode, input the F6h command after read operation.</p> <p>In read sequence, CSX should not be raised between sending read command and read parameter, and between read parameters before all parameters are read. If a pause is invoked between read command and read parameter, write sequence is executed and data is overwritten.</p> <p>X = Don't care</p>												
Restriction	Available only when MIPI DBI Type C is selected.												

Read Mode Out for DBI Only: F6h

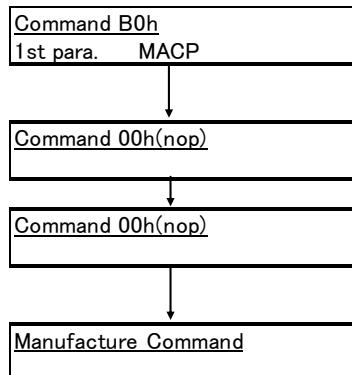
F6h		Read Mode Out for DBI only											
		DCX	RDX	WRX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command		0	1	↑	1	1	1	1	0	1	1	0	F6h
Description	Input this command to exit the read mode entered by the F5h command.												
Restriction	X = Don't care												
Restriction	Available only when MIPI DBI Type C is selected.												

Manufacturer Command

Notes of Manufacture Command

- Command B0h

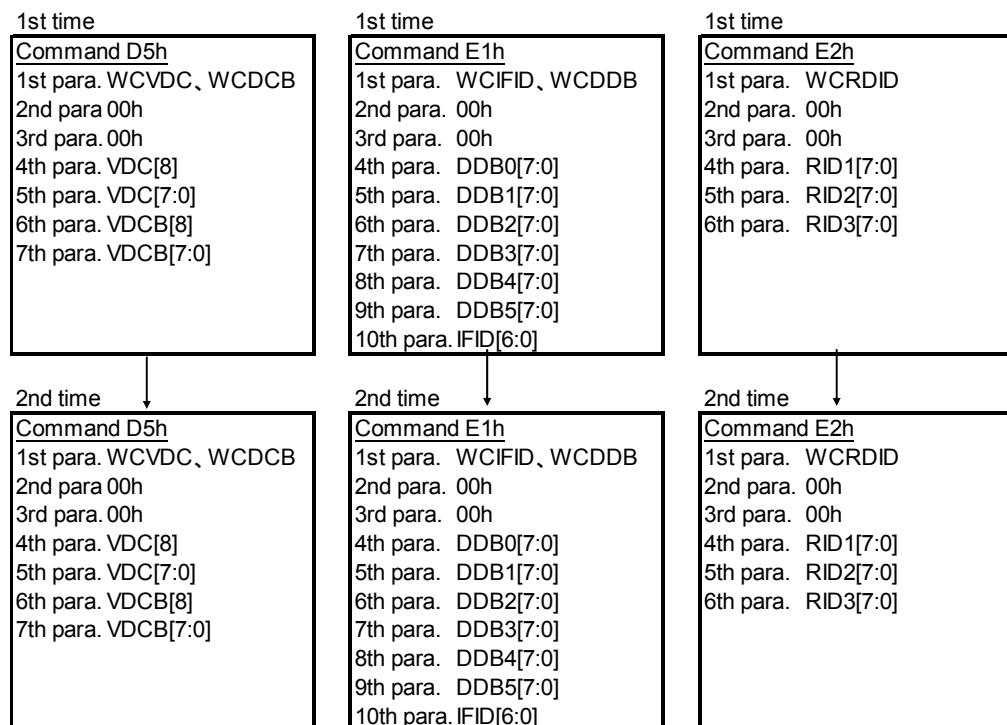
When command B0h is set in MIPI DSI HS mode, command 00h (nop) should be input twice after command B0h is set. Then, set a Manufacturer Command. Inputting command 00h (nop) is unnecessary when MIPI DSI (LP mode), MIPI DBI Type C, or I2C interface is used.



Setting Sequence of Command B0h in MIPI DSI HS Mode

- Commands D5h, E1h and E2h

When commands D5h, E1h and E2h are set in MIPI DSI HS mode, the same value should be set in the commands twice in a row. Inputting command 00h (nop) is unnecessary when MIPI DSI (LP mode), MIPI DBI Type C or I2C interface is used.



Setting Sequence of Commands D5h, D1h and E2h in MIPI DSI HS Mode

- Command E1h

When MIPI DSI is used, the WCDDDB register is used to control access to the DDB0 to DDB5 and IFID registers. When MIPI DBI Type C or I2C interface is used, the WCDDDB register is used to control access to the DDB0 to DDB5 registers and the WCIFID register is used to control access to the IFID register.

I/F	WCDDDB	WCIFID	DDB[5:0]	IFID
MIPI DSI	0	*	Access disable	Access disable
	1		Access enable	Access enable
MIPI DBI Type C I2C	0	0	Access disable	Access disable
	0	1	Access disable	Access enable
	1	0	Access enable	Access disable
	1	1	Access enable	Access enable

• *Manufacture Command Access Protect : B0h*

	Please refer to Application Note
	Please refer to Appendix

B0h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	0	0	B0
1st parameter	1	↑	↑	0	0	0	0	0	MCAP[2]	MCAP[1]	MCAP[0]	xx
init	-	-	-	0	0	0	0	0	0	1	1	03

MCAP

Description

This register controls access protect of MCS (Manufacturer command Set).

Function Table

Command		MCAP					
		0	1	2	3 (default)	4	other
MCAP	B0h	Yes	Setting inhibited	Yes	Yes	Yes	Setting Not defined
Additional User Command	B1h	Yes		Yes	No	Yes	
Manufacturer	B3h-BEh C0h-D8h E1h-E3h	Yes		No	No	Yes	
NVM access	E0h	Fixed		Fixed	Fixed	Yes	

Yes: Access Possible (Protect Off)

No: Access impossible (Protect On)

Fixed: Fixed to initial value

Restriction

The all MCS read data in Access Protect On ("No", "Fixed" in above function table) is "0".
(Excluding Device Code Read (ALMIDx)).

- Low Power Mode Function : B1h**

B1h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	0	1	B1
1st parameter	1	↑	↑	0	0	0	0	0	0	0	DSTB	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

DSTB

Description

This register controls Deep Standby mode.

Function Table

DSTB	Deep Standby mode
0	off
1	on

Restriction

- In enter_sleep_mode only, DSTB can set to 1.

- *Interface Setting 1 : B3h*

B3h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	1	1	B3
1st parameter	1	↑	↑	DM[3]	DM[2]	DM[1]	DM[0]	0	1	0	0	xx
init	-	-	-	0	0	0	0	0	1	0	0	04
2nd parameter	1	↑	↑	0	0	0	0	I2CNCOFF	IFIDEN	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	EPFV[2]	EPFV[1]	EPFV[0]	0	0	0	0	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	0	0	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00

DM

Description

This register controls display mode.

Function Table

Assignment of Display Mode and Based signals

DM	Display Mode	Display clock	Display Sync	Data latch clock	cABC PWM
'h0	built-in TCON	OSC	OSC	OSC	OSC
'h1	DSI-Video-Burst	OSC	DSI	DSI (*1)	OSC
'h2	Setting inhibited	-	-	-	-
'h3	Setting inhibited	-	-	-	-
'h4	Setting inhibited	-	-	-	-
'h5	Setting inhibited	-	-	-	-
'h6	Setting inhibited	-	-	-	-
'h7	Setting inhibited	-	-	-	-
'h8	Setting inhibited	-	-	-	-
'h9	Setting inhibited	-	-	-	-
'hA	Setting inhibited	-	-	-	-
'hB	Setting inhibited	-	-	-	-
'hC	Setting inhibited	-	-	-	-
'hD	Setting inhibited	-	-	-	-
'hE	Setting inhibited	-	-	-	-
'hF	Setting inhibited	-	-	-	-

(*1): Data latch clock is changed to the clock based on OSC during blank period.

Restriction

Please do not change this register setting in displaying.

Please set DM's value in Sleep_in.

Please input display clock of each interface before sending exit_sleep_mode command.

IFIDEN**Description**

This register controls Slave Address (IFID) using I²C I/F.

After setting this register value to "1", please transfer data with Slave Address=IFID.

Function Table

IFIDEN	IFID	I2C Slave Address
0	*	don't care
1	IFID	IFID

Restriction

IFID default value (no ID data writing to NVM) is all"0". (It does not corresponded General Call Address.)

During NVM writing operation:

Please write the Slave Address into IFID register before writing IFIDEN=1.

When sending IFIDEN=1, please send the first byte with Slave Addres = IFID.

I2CNCOFF**Description**

This register controls I2C Interface operating frequency.

Function Table

Item	Symbol	Unit	Min.	
			I2CNCOFF=1	I2CNCOFF=0
Serial clock cycle time	tSCL	ns	650	1000
Serial clock "High" period	tSCLH	ns	160	300
Serial clock "Low" period	tSCLL	ns	320	600
Bus free time	tBUF	ns	320	600
Start condition Hold time	tSTAH	ns	150	600
Restart condition setup time	tSTAS	ns	150	600
Stop condition setup time	tSTOP	ns	150	600
Data setup time	tSDAS	ns	70	300
Data hold time	tSDAH	ns	0	0

Restriction -

EPFV**Description**

This register controls data format of 16bpp(R,G,B)→24bpp(r,g,b) expansion and 18bpp(R,G,B)→24bpp(r,g,b) expansion in video mode.

Function Table

< 24bpp Gray Scale (video mode) >

EPFV	set_pixel_format= 18bpp 18bpp(R,G,B)→24bpp(r,g,b) expansion	set_pixel_format=24bpp
'h0	Set "0" to lower bit r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 } Exception : R[5:0], G[5:0],B[5:0]=6'h3F → r[7:0],g[7:0],b[7:0]=8'hFF	r[7:0]={ R[7:0] } g[7:0]={ G[7:0] } b[7:0]={ B[7:0] }
'h1	Set "1" to lower bit r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 } Exception : R[5:0], G[5:0],B[5:0]=6'h00 → r[7:0],g[7:0],b[7:0]=8'h00	
'h2	Set upper bit data to lower bit r[7:0]={ R[5:0], R[5:4] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[5:0], B[5:4] }	
'h3-7	Setting inhibit	Setting inhibit

Restriction -

• *Interface Setting 2 : B4h*

B4h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	1	0	0	B4
1st parameter	1	↑	↑	0	0	0	0	SELDL[1]	SELDL[0]	DSIVC[1]	DSIVC[0]	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C
2nd parameter	1	↑	↑	0	0	0	SIMEN	SIM[3]	SIM[2]	SIM[1]	SIM[0]	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00

DSIVC

Description

This register controls DSI virtual channel setting.

The corresponding packet to DSIVC[1:0] are acceptable.

Function Table

DSIVC	Configuration
'h0	VC=00
'h1	VC=01
'h2	VC=10
'h3	VC=11

Restriction

Initial value (without writing to NVM) is "0".

If changing DSIVC value, please use excluding DSI I/F and write the setting to NVM.

SELDL

Description

This register controls the number of data lane using DSI.

Please tie unused data lane pin (DATAxP/N) to GND.

In DSI, please set this register in Escape mode.

The setting for the number of DSI Data Lane

In case of using command (SELDL) for changing the number of DSI Data lane, please set after negating RESET by using following flow.

When NVM is not written any data, SELDL are setted to 3(4lane) as initial setting.

If you want to use as 2 Data lane, please set SELDL=1 and write the setting to NVM using following flow.

After writing setting to NVM, you do not repeat the setting flow.

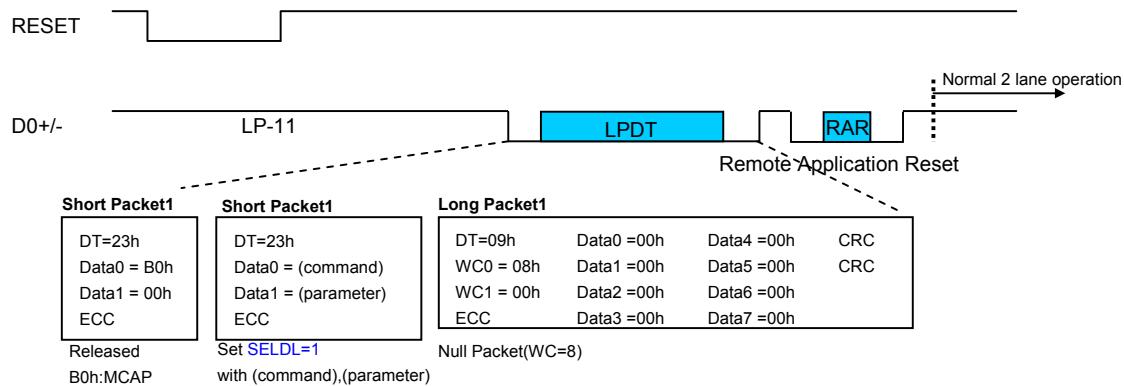


Figure 17 The flow of switching the number of DSI Data lane

Function Table

SELDL	DSI data lane
'h0	Setting inhibited
'h1	2 lane
'h2	3 lane
'h3	4 lane

Restriction -**SIM****Description**

This register controls Secondary Interface Mode.

Function Table

SIM	Secondary interface
'h0	I ² C
'h1	setting inhibit
'h2	DBI.C option1
'h3	DBI.C option3
'h4	Reserved
'h5	setting inhibit
'h6	setting inhibit
'h7	setting inhibit
'h8	setting inhibit

Restriction

There are restrictions of the interface combination. Refer to SIMEN for combination of functions.

SIMEN**Description**

This register controls Secondary Interface Mode (SIM).

Primary Interface is selected using IM pin.

Secondary Interface is selected SIM register.

Function Table

SIMEN	Interface mode		Notes
	Primary interface mode (IM pin)	Secondary interface mode (SIM register)	
0	Enable	Disable	Stand alone I/F
1	Enable	Enable	Multi I/F

Table 52 Multi interface combination

Primary I/F (IM pin)	DBI. C	option 1	(stand alone I/F)				Secondary I/F (SIM)	
			option1	option3	DBI.C	I ² C		
	option 3	•	-	-	-	-		
		•	-	-	-	-		
	I ² C	•	-	-	-	-		
	DSI	2lane	•	•	•	•		
		3lane	•	•	•	•		
		4lane	•	•	•	•		

note) The data lane of each interface is defined as below.
DSI -> SELDL command

Restriction

The Primary interface is used for writing NV memory (including SIM, SIMEN) and evaluating the first. It's necessary to select the Primary interface above the table.

• ***Read Checksum and ECC Error Count : B5h***

B5h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	1	0	1	B5
1st parameter	1	↑	1	DSICCSOUT[7]	DSICCSOUT[6]	DSICCSOUT[5]	DSICCSOUT[4]	DSICCSOUT[3]	DSICCSOUT[2]	DSICCSOUT[1]	DSICCSOUT[0]	xx
init	-	-	-	1	1	1	1	1	1	1	1	00
2nd parameter	1	↑	1	DSIECP[7]	DSIECP[6]	DSIECP[5]	DSIECP[4]	DSIECP[3]	DSIECP[2]	DSIECP[1]	DSIECP[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	1	DSIECE[7]	DSIECE[6]	DSIECE[5]	DSIECE[4]	DSIECE[3]	DSIECE[2]	DSIECE[1]	DSIECE[0]	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00

DSICCSOUT

Description

The value of Checksum Error count is read out.

Checksum Error count is count up when Checksum Error occurs at receiving DSI Long Packet
This register is cleared to 0 after read out and soft reset. (only operating DSI I/F)

Function Table -

Restriction

The clear operation at DSICCSOUT read out is executed only selected DSI I/F.

Other I/F can read this register's value (DSICCSOUT value is kept in case of using other I/F).

DSIECP

Description

The value of single ECC Error count is read out. Single bit ECC Error count is count up when 1bit ECC Error occurs at receiving, DSI Packet Header.

This register is clear to 0 after read out and soft reset. (only operating DSI I/F)

Function Table

Restriction

The clear operation at DSIECP read out is executed only selected DSI I/F.

Other I/F can read this register's value (DSIECP value is kept in case of using other I/F.)

DSIECE

Description

The value of Multi bits ECC Error count is read out. Multi bits ECC Error count is count up when 2bit or more ECC Error occurs at receiving, DSI Packet Header.

This register is clear to 0 after read out and soft reset. (only operating DSI I/F)

Function Table -

Restriction

The clear operation at DSIECE read out is executed only selected DSI I/F.

Other I/F can read this register's value.(DSIECE value is kept in case of using other I/F.)

• **DSI Control : B6h**

B6h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	1	1	0	B6
1st parameter	1	↑	↑	0	0	1	1	1	0	DSITXDIV[1]	DSITXDIV[0]	xx
init	-	-	-	0	0	1	1	1	0	1	0	3A
2nd parameter	1	↑	↑	1	DSI_THSSET [2]	DSI_THSSET [1]	DSI_THSSET [0]	0	0	1	1	xx
init	-	-	-	1	1	0	0	0	0	1	1	C3

DSITXDIV

Description

This register controls the DSICLK dividing ratio for LP mode data transmission.

In case of stopping DSICLK, internal OSC (28MHz) is selected for data transmission clock instead of DSICLK.

Function Table

DSITXDIV	DSICLK dividing ratio
'b00	fDSICLK/8
'b01	fDSICLK/16
'b10	fDSICLK/24 (default)
'b11	fDSICLK/32

Table 53 Configuration of DSITXDIV

Status of Clock Lane	Host to DriverIC		DriverIC to Host		
	Bit Rate [Mbps]	fDSICLK [MHz]	Setting of DSITXDIV (example)	fTXCLK (=1/T _{LPTX}) [MHz]	Bit rate [Mbps]
Active	1000	500	'b10	20.83	10.42
	950	475		19.79	9.90
	900	450		18.75	9.38
	850	425		17.71	8.85
	800	400		16.67	8.33
	750	375		15.63	7.81
	700	350		14.58	7.29
	650	325		13.54	6.77
	600	300		18.75	9.38
	550	275		17.19	8.59
	500	250		15.63	7.81
	450	225		14.06	7.03
	400	200		12.50	6.25
	350	175		10.94	5.47
	300	150	'b00	18.75	9.38
	250	125		15.63	8.13
	200	100		12.50	6.25
Inactive (Stop)	-	-	-	14.0 (fOSCCLK/2)	7.0

Restriction

-

DSI_THSSET**Description**

This register controls MIPI-DSI DPHY operating frequency.

Please set the suitable value for tHS-PREPARE and tHS-PREPARE+tHS-ZERO.

Function Table

DSI_THSSET	DSI DPHY operating frequency	
	Min	Max
'h0	100Mbps	180Mbps
'h1	180Mbps	280Mbps
'h2	280Mbps	420Mbps
'h3	420Mbps	590Mbps
'h4	590Mbps	740Mbps
'h5	740Mbps	1000Mbps
'h6	Reserved	Reserved
'h7	Reserved	Reserved

Restriction -

- **DSI Error Count Reset : B6h**

	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	1	1	1	B7
1st parameter	1	↑	↑	0	0	0	0	0	0	0	ERR_CNT_RST	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

ERR_CNT_RST

Description

This register resets a DSI error count.

Function Table

ERR_CNT_RST	DSI Error count
0	Not clear
1	0 clear

Restriction

After resetting an error count by ERR_CNT_RST=1, it returns to ERR_CNT_RST=0.

Test : B8h

B8h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	1	0	0	0	B8
1st parameter	1	1	↑	0	0	0	1	1	0	0	0	00..FF
init	-	-	-	0	0	0	1	1	0	0	0	18
2nd parameter	1	1	↑	1	0	0	0	0	0	0	0	00..FF
init	-	-	-	1	0	0	0	0	0	0	0	80
3rd parameter	1	1	↑	0	0	0	1	1	0	0	0	00..FF
init	-	-	-	0	0	0	1	1	0	0	0	18
4th parameter	1	1	↑	0	0	0	1	1	0	0	0	00..FF
init	-	-	-	0	0	0	1	1	0	0	0	18
5th parameter	1	1	↑	1	1	0	0	1	1	1	1	00..FF
init	-	-	-	1	1	0	0	1	1	1	1	CF
6th parameter	1	1	↑	0	0	0	1	1	1	1	1	00..FF
init	-	-	-	0	0	0	1	1	1	1	1	1F
7th parameter	1	1	↑	0	0	0	0	0	0	0	0	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	1	↑	0	0	0	0	1	1	0	0	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C
9th parameter	1	1	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
10th parameter	1	1	↑	0	1	0	1	1	1	0	0	xx
init	-	-	-	0	1	0	1	1	1	0	0	5C
11th parameter	1	1	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
12th parameter	1	1	↑	1	0	1	0	1	1	0	0	xx
init	-	-	-	1	0	1	0	1	1	0	0	AC
13th parameter	1	1	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
14th parameter	1	1	↑	0	0	0	0	1	1	0	0	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C
15th parameter	1	1	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
16th parameter	1	1	↑	1	1	0	1	1	0	1	0	xx
init	-	-	-	1	1	0	1	1	0	1	0	DA
17th parameter	1	1	↑	0	1	1	0	1	1	0	1	xx
init	-	-	-	0	1	1	0	1	1	0	1	6D
18th parameter	1	1	↑	1	1	1	1	1	1	1	1	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
19th parameter	1	1	↑	1	1	1	1	1	1	1	1	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
20th parameter	1	1	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10

21st parameter	1	↑	↑	0	1	1	0	0	1	1	1	xx
init	-	-	-	0	1	1	0	0	1	1	1	67
22nd parameter	1	↑	↑	1	0	0	0	1	0	0	1	xx
init	-	-	-	1	0	0	0	1	0	0	1	89
23rd parameter	1	↑	↑	1	0	1	0	1	1	1	1	xx
init	-	-	-	1	0	1	0	1	1	1	1	AF
24th parameter	1	↑	↑	1	1	0	1	0	1	1	0	xx
init	-	-	-	1	1	0	1	0	1	1	0	D6
25th parameter	1	↑	↑	1	1	1	1	1	1	1	1	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF

Backlight Control 2 (Movie/Still) : B9h

Please refer to Application Note	
	Please refer to Appendix

B9h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	1	0	0	1	B9
1st parameter	1	↑	↑	0	0	SSD_THRE3[5]	SSD_THRE3[4]	SSD_THRE3[3]	SSD_THRE3[2]	SSD_THRE3[1]	SSD_THRE3[0]	xx
init	-	-	-	0	0	0	0	1	1	1	1	0F
2nd parameter	1	↑	↑	0	0	SD_THRE3[5]	SD_THRE3[4]	SD_THRE3[3]	SD_THRE3[2]	SD_THRE3[1]	SD_THRE3[0]	00..FF
init	-	-	-	0	0	0	1	1	1	1	1	18
3rd parameter	1	↑	↑	IPK_INTP03[7]	IPK_INTP03[6]	IPK_INTP03[5]	IPK_INTP03[4]	IPK_INTP03[3]	IPK_INTP03[2]	IPK_INTP03[1]	IPK_INTP03[0]	00..FF
init	-	-	-	0	0	0	0	0	1	0	0	04
4th parameter	1	↑	↑	IPK_TRANS3[7]	IPK_TRANS3[6]	IPK_TRANS3[5]	IPK_TRANS3[4]	IPK_TRANS3[3]	IPK_TRANS3[2]	IPK_TRANS3[1]	IPK_TRANS3[0]	00..FF
init	-	-	-	0	1	0	0	0	0	0	0	40
5th parameter	1	↑	↑	1	0	0	1	1	1	1	1	00..FF
init	-	-	-	1	0	0	1	1	1	1	1	9F
6th parameter	1	↑	↑	0	0	0	1	1	1	1	1	00..FF
init	-	-	-	0	0	0	1	1	1	1	1	1F
7th parameter	1	↑	↑	LLMT3[7]	LLMT3[6]	LLMT3[5]	LLMT3[4]	LLMT3[3]	LLMT3[2]	LLMT3[1]	LLMT3[0]	00..FF
init	-	-	-	1	0	0	0	0	0	0	0	80

Note) Please refer to Application Note for CABC Function.

Backlight Control 4 (GUI) : BAh

	Please refer to Application Note
	Please refer to Appendix

BAh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	1	0	1	0	BA
1st parameter	1	↑	↑	0	0	SSD_THRE1[5]	SSD_THRE1[4]	SSD_THRE1[3]	SSD_THRE1[2]	SSD_THRE1[1]	SSD_THRE1[0]	xx
init	-	-	-	0	0	0	0	1	1	1	1	0F
2nd parameter	1	↑	↑	0	0	SD_THRE1[5]	SD_THRE1[4]	SD_THRE1[3]	SD_THRE1[2]	SD_THRE1[1]	SD_THRE1[0]	00..FF
init	-	-	-	0	0	0	1	1	1	1	1	18
3rd parameter	1	↑	↑	IPK_INTP01[7]	IPK_INTP01[6]	IPK_INTP01[5]	IPK_INTP01[4]	IPK_INTP01[3]	IPK_INTP01[2]	IPK_INTP01[1]	IPK_INTP01[0]	00..FF
init	-	-	-	0	0	0	0	0	1	0	0	04
4th parameter	1	↑	↑	IPK_TRANS1[7]	IPK_TRANS1[6]	IPK_TRANS1[5]	IPK_TRANS1[4]	IPK_TRANS1[3]	IPK_TRANS1[2]	IPK_TRANS1[1]	IPK_TRANS1[0]	00..FF
init	-	-	-	0	1	0	0	0	0	0	0	40
5th parameter	1	↑	↑	1	0	0	1	1	1	1	1	00..FF
init	-	-	-	1	0	0	1	1	1	1	1	9F
6th parameter	1	↑	↑	0	0	0	1	1	1	1	1	00..FF
init	-	-	-	0	0	0	1	1	1	1	1	1F
7th parameter	1	↑	↑	LLMT1[7]	LLMT1[6]	LLMT1[5]	LLMT1[4]	LLMT1[3]	LLMT1[2]	LLMT1[1]	LLMT1[0]	00..FF
init	-	-	-	1	1	0	1	0	1	1	1	D7

Note) Please refer to Application Note for CABC Function.

Test : BBh

BBh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	1	0	1	1	BB
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10

• *Device Code Read Function : BFh*

BFh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	1	1	1	1	BF
1st parameter	1	↑	1	ALMID0[7]	ALMID0[6]	ALMID0[5]	ALMID0[4]	ALMID0[3]	ALMID0[2]	ALMID0[1]	ALMID0[0]	00..FF
init	-	-	-	0	0	0	0	0	0	0	1	01
2nd parameter	1	↑	1	ALMID1[7]	ALMID1[6]	ALMID1[5]	ALMID1[4]	ALMID1[3]	ALMID1[2]	ALMID1[1]	ALMID1[0]	00..FF
init	-	-	-	0	0	1	0	0	0	1	0	22
3rd parameter	1	↑	1	ALMID2[7]	ALMID2[6]	ALMID2[5]	ALMID2[4]	ALMID2[3]	ALMID2[2]	ALMID2[1]	ALMID2[0]	00..FF
init	-	-	-	0	0	1	1	0	0	1	1	33
4th parameter	1	↑	1	ALMID3[7]	ALMID3[6]	ALMID3[5]	ALMID3[4]	ALMID3[3]	ALMID3[2]	ALMID3[1]	ALMID3[0]	00..FF
init	-	-	-	0	0	0	1	0	0	0	1	11
5th parameter	1	↑	1	ALMID4[7]	ALMID4[6]	ALMID4[5]	ALMID4[4]	ALMID4[3]	ALMID4[2]	ALMID4[1]	ALMID4[0]	00..FF
init	-	-	-	0	0	0	0	0	0	0	0	00

ALMID0

Description

Upper 8bit of Supplier ID can read by accessing this register.

Function Table

	D7	D6	D5	D4	D3	D2	D1	D0	HEX
parameter	ALMID0 [7]	ALMID0 [6]	ALMID0 [5]	ALMID0 [4]	ALMID0 [3]	ALMID0 [2]	ALMID0 [1]	ALMID0 [0]	
Register init	0	0	0	0	0	0	0	1	01h

Restriction

ALMID0 can be reading at all MCAP protect level.

ALMID1

Description

Lower 8bit of Supplier ID can read by accessing this register.

Function Table

	D7	D6	D5	D4	D3	D2	D1	D0	HEX
parameter	ALMID1 [7]	ALMID1 [6]	ALMID1 [5]	ALMID1 [4]	ALMID1 [3]	ALMID1 [2]	ALMID1 [1]	ALMID1 [0]	
Register init	0	0	1	0	0	0	1	0	22h

Restriction

ALMID1 can be reading at all MCAP protect level.

ALMID2**Description**

Upper 8bit of IC part number can read by accessing this register.

Function Table

	D7	D6	D5	D4	D3	D2	D1	D0	HEX
parameter	ALMID2 [7]	ALMID2 [6]	ALMID2 [5]	ALMID2 [4]	ALMID2 [3]	ALMID2 [2]	ALMID2 [1]	ALMID2 [0]	
Register init	0	0	1	1	0	0	1	1	33h

Restriction

ALMID2 can be reading at all MCAP protect level.

ALMID3**Description**

Lower 8bit of IC part number can read by accessing this register.

Function Table

	D7	D6	D5	D4	D3	D2	D1	D0	HEX
parameter	ALMID3 [7]	ALMID3 [6]	ALMID3 [5]	ALMID3 [4]	ALMID3 [3]	ALMID3 [2]	ALMID3 [1]	ALMID3 [0]	
Register init	0	0	0	1	0	0	0	1	11h

Restriction

ALMID3 can be reading at all MCAP protect level.

ALMID4**Description**

Chip version code for user can read by accessing this register.

Function Table

	D7	D6	D5	D4	D3	D2	D1	D0	HEX
parameter	ALMID4 [7]	ALMID4 [6]	ALMID4 [5]	ALMID4 [4]	ALMID4 [3]	ALMID4 [2]	ALMID4 [1]	ALMID4 [0]	
Register init	0	0	0	0	0	0	0	0	00h

Restriction

ALMID4 can be reading at all MCAP protect level.

- Slew Rate Control : C0h**

C0h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	0	C0
1st parameter	1	↑	↑	0	0	0	0	SOUTTF1[1]	SOUTTF1[0]	SOUTTR1[1]	SOUTTR1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	SOUTTF2[1]	SOUTTF2[0]	SOUTTR2[1]	SOUTTR2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

SOUTTR1/2, SOUTTF1/2

Description

These registers set s Driving ability(Tr/Tf)

SOUTTR1: sets a Driving ability(Tr) SOUT14,15,16

SOUTTR2: sets a Driving ability(Tf) SOUT17,18,19

SOUTTF1: sets a Driving ability(Tf) SOUT14,15,16

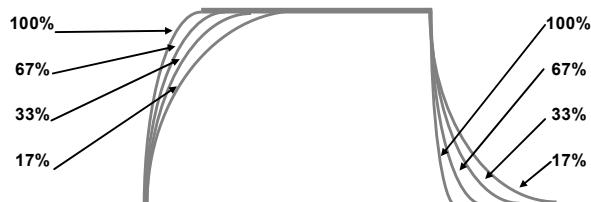
SOUTTF2: sets a Driving ability(Tf) SOUT17,18,19

Function Table

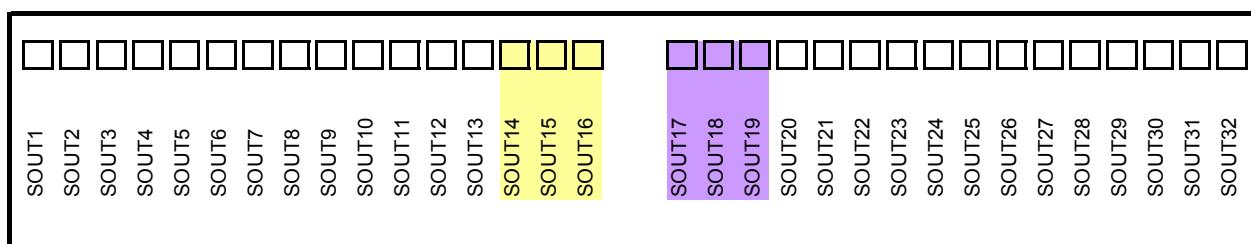
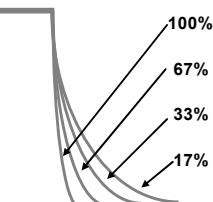
SOUTTR1/2	Driving ability(Tr)
'h00	100%
'h01	67%
'h02	33%
'h03	17%

SOUTTF1/2	Driving ability(Tf)
'h0	100%
'h1	67%
'h2	33%
'h3	17%

SOUTTR1/2



SOUTTF1/2



[Yellow] SOUT14,15,16

SOUTTF1,SOUTTR1

[Purple] SOUT17,18,19

SOUTTF2,SOUTTR2

Restriction

-

• *Display Setting 1 : C1h*

	Please refer to Application Note
	Please refer to Appendix

C1h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	1	C1
1st parameter	1	↑	↑	BLS	BLREV	0	REV	BGR1	SS1	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	1	1	0	GMMD	HRE1[2]	HRE1[1]	HRE1[0]	xx
init	-	-	-	0	1	1	0	0	0	0	0	60
3rd parameter	1	↑	↑	0	1	0	0	0	0	0	0	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
4th parameter	1	↑	↑	GSWAP[7]	GSWAP[6]	GSWAP[5]	GSWAP[4]	GSWAP[3]	GSWAP[2]	GSWAP[1]	GSWAP[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	GSWAP[15]	GSWAP[14]	GSWAP[13]	GSWAP[12]	GSWAP[11]	GSWAP[10]	GSWAP[9]	GSWAP[8]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	GSWAP[23]	GSWAP[22]	GSWAP[21]	GSWAP[20]	GSWAP[19]	GSWAP[18]	GSWAP[17]	GSWAP[16]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	GSWAP[31]	GSWAP[30]	GSWAP[29]	GSWAP[28]	GSWAP[27]	GSWAP[26]	GSWAP[25]	GSWAP[24]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	GSWAP[39]	GSWAP[38]	GSWAP[37]	GSWAP[36]	GSWAP[35]	GSWAP[34]	GSWAP[33]	GSWAP[32]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	GSWAP[47]	GSWAP[46]	GSWAP[45]	GSWAP[44]	GSWAP[43]	GSWAP[42]	GSWAP[41]	GSWAP[40]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	GSWAP[55]	GSWAP[54]	GSWAP[53]	GSWAP[52]	GSWAP[51]	GSWAP[50]	GSWAP[49]	GSWAP[48]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
11th parameter	1	↑	↑	GSWAP[63]	GSWAP[62]	GSWAP[61]	GSWAP[60]	GSWAP[59]	GSWAP[58]	GSWAP[57]	GSWAP[56]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
12th parameter	1	↑	↑	GSWAP[71]	GSWAP[70]	GSWAP[69]	GSWAP[68]	GSWAP[67]	GSWAP[66]	GSWAP[65]	GSWAP[64]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
13th parameter	1	↑	↑	GSWAP[79]	GSWAP[78]	GSWAP[77]	GSWAP[76]	GSWAP[75]	GSWAP[74]	GSWAP[73]	GSWAP[72]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
14th parameter	1	↑	↑	GSWAP[87]	GSWAP[86]	GSWAP[85]	GSWAP[84]	GSWAP[83]	GSWAP[82]	GSWAP[81]	GSWAP[80]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
15th parameter	1	↑	↑	GSWAP[95]	GSWAP[94]	GSWAP[93]	GSWAP[92]	GSWAP[91]	GSWAP[90]	GSWAP[89]	GSWAP[88]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
16th parameter	1	↑	↑	GSWAP[103]	GSWAP[102]	GSWAP[101]	GSWAP[100]	GSWAP[99]	GSWAP[98]	GSWAP[97]	GSWAP[96]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
17th parameter	1	↑	↑	GSWAP[111]	GSWAP[110]	GSWAP[109]	GSWAP[108]	GSWAP[107]	GSWAP[106]	GSWAP[105]	GSWAP[104]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
18th parameter	1	↑	↑	GSWAP[119]	GSWAP[118]	GSWAP[117]	GSWAP[116]	GSWAP[115]	GSWAP[114]	GSWAP[113]	GSWAP[112]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
19th parameter	1	↑	↑	GSWAP[127]	GSWAP[126]	GSWAP[125]	GSWAP[124]	GSWAP[123]	GSWAP[122]	GSWAP[121]	GSWAP[120]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
20th parameter	1	↑	↑	GSWAP[135]	GSWAP[134]	GSWAP[133]	GSWAP[132]	GSWAP[131]	GSWAP[130]	GSWAP[129]	GSWAP[128]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

21th parameter	1	↑	↑	GSWAP[143]	GSWAP[142]	GSWAP[141]	GSWAP[140]	GSWAP[139]	GSWAP[138]	GSWAP[137]	GSWAP[136]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
22th parameter	1	↑	↑	GSWAP[151]	GSWAP[150]	GSWAP[149]	GSWAP[148]	GSWAP[147]	GSWAP[146]	GSWAP[145]	GSWAP[144]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
23th parameter	1	↑	↑	GSWAP[159]	GSWAP[158]	GSWAP[157]	GSWAP[156]	GSWAP[155]	GSWAP[154]	GSWAP[153]	GSWAP[152]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
24th parameter	1	↑	↑	0	DSPODR1[2]	DSPODR1[1]	DSPODR1[0]	0	DSPODR0[2]	DSPODR0[1]	DSPODR0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
25th parameter	1	↑	↑	0	DSPODR3[2]	DSPODR3[1]	DSPODR3[0]	0	DSPODR2[2]	DSPODR2[1]	DSPODR2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
26th parameter	1	↑	↑	0	DSPODR5[2]	DSPODR5[1]	DSPODR5[0]	0	DSPODR4[2]	DSPODR4[1]	DSPODR4[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
27th parameter	1	↑	↑	0	DSPODR7[2]	DSPODR7[1]	DSPODR7[0]	0	DSPODR6[2]	DSPODR6[1]	DSPODR6[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
28th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
29th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
30th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
31th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
32th parameter	1	↑	↑	0	0	0	0	0	0	1	0	xx
init	-	-	-	0	0	0	0	0	0	1	0	02
33th parameter	1	↑	↑	0	0	0	0	0	0	1	0	xx
init	-	-	-	0	0	0	0	0	0	1	0	02
34th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

Note) GSWAP, DSPODRn registers are described in Appendix.

SS1

Description

This register controls output shift direction of source driver.
Register's value reflects when data are written to line buffer.

Function Table

SS0	Source output direction	
	BGR1=0	BGR1=1
0	S1→Sn “R”, “G”, “B”	S1→Sn “B”, “G”, “R”
1	Sn→S1 “R”, “G”, “B”	Sn→S1 “B”, “G”, “R”

Restriction -

BGR1**Description**

This register controls data order when display data are written to line buffer.
Please set the suitable value of color filter.

Function Table

BGR1	Order of RGB data when data are written to line buffer
0	(R) (G) (B) → (R) (G) (B)
1	(R) (G) (B) → (B) (G) (R)

Restriction -**REV****Description**

This register controls source output level of display period in Normal.
And this register defines the relation of display data and source level.

Function Table

< Column/Dot inversion >			
REV	Input Data	Source output level in display period	
		Positive polarity	Negative polarity
0	24'h000000	VP255	VN255
	: 24'hFFFFFF	: VP0	: VN0
1	24'h000000	VP0	VN0
	: 24'hFFFFFF	: VP255	: VN255

Restriction -**BLREV, BLS****Description**

This register controls source output level of blank period in Normal.

Function Table

< Column/Dot inversion >				Source Amp. operation in blank period	
BLREV	BLS	Source output level of blank period			
		Positive polarity	Negative polarity		
0	0	V255P	V255N	ON	
	1	GND	GND	OFF	
1	0	V0P	V0N	ON	
	1	HiZ	HiZ	OFF	

Restriction -

HRE1**Description**

This register controls assignment of source output.

According to this register setting, display operation mode is defined.

Function Table

HRE1	Panel resolution control (=CABC resolution)		Assignment of Source pins
	X (HRE)	Y (NL)	
'h0	1080RGB	1920	S[1:1080]
'h1	1024RGB	1600	S[1:512], S[569:1080]
		1280	
'h2	960RGB	1280	S[1:480], S[601:1080]
'h3	900RGB	1600	S[1:450], S[631:1080]
		1440	
'h4	800RGB	1024	S[1:400], S[681:1080]
'h5	768RGB	1280	S[1:384], S[697:1080]
		1024	
'h6	720RGB	1280	S[1:360], S[721:1080]

Restriction

This register is setted in sleep in mode. Please do not change in sleep out mode.

Please set `set_column_address` and `set_page_address` again after releasing HWRESET, releasing DSTB, changing HRE1.

GMMD**Description**

This register controls operation mode of gamma setting register.

Function Table

GMMD	Operation mode	Gamma Set A	Gamma Set B	Gamma Set C
'h0	Separate Gamma	srcsw(a)	srcsw(b)	srcsw(c)
'h1	4 Gamma mode (common sub-pixels)	26h:GC0 srcsw(a-c)	26h:GC1 srcsw(a-c)	26h:GC2 26h:GC3 srcsw(a-c)

Note1: "srcsw" is defined as follows.

The relationship of Gamma set and Display data is below.

	sub-pixel1 srcsw(a)	sub-pixel2 srcsw(b)	sub-pixel3 srcsw(c)
24bpp display data	[23:16]	[15:8]	[7:0]

Restriction -

- *Display Setting 2 : C2h*

C2h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	0	C2
1st parameter	1	↑	↑	0	0	1	1	0	0	0	0	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
2nd parameter	1	↑	↑	LINEINVA[3]	LINEINVA[2]	LINEINVA[1]	LINEINVA[0]	PNSET	NL[10]	NL[9]	NL[8]	xx
init	-	-	-	0	0	0	0	0	1	1	1	07
3rd parameter	1	↑	↑	NL[7]	NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
4th parameter	1	↑	↑	0	0	0	BP[4]	BP[3]	BP[2]	BP[1]	BP[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
5th parameter	1	↑	↑	0	0	0	0	1	0	0	0	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

Note) Other registers are described in Appendix.

PNSET

Description

This register sets a dot inversion method.

Details are described in a paragraph “LINEINVA”, please refer it.

Function Table

PNSET	Method
'h0	Spetial configuration mode 1
'h1	Spetial configuration mode 2

Restriction

This register setting is not usable at the time of 1-line, 3-line, over 14-line and Column inversion.

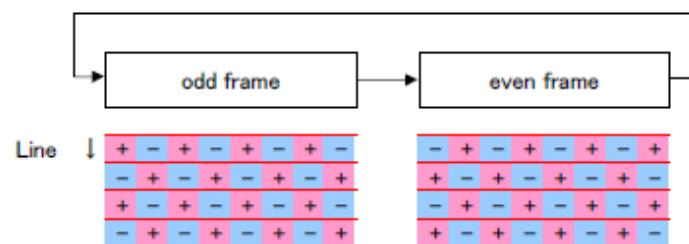
LINEINVA**Description**

This register sets a dot inversion method.

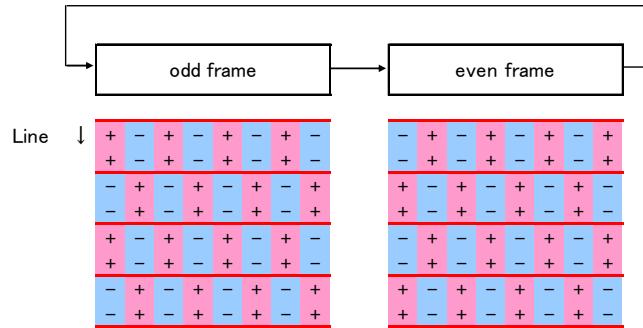
Function Table

LINEINVA	Method
'h0	1-line inversion drive
'h1	2-line inversion drive
'h2	3-line inversion drive
'h3	4-line inversion drive
'h4	6-line inversion drive
'h5	8-line inversion drive
'h6	10-line inversion drive
'h7	12-line inversion drive
'h8	14-line inversion drive
'h9	16-line inversion drive
'hA	24-line inversion drive
'hB	32-line inversion drive
'hC	48-line inversion drive
'hD	64-line inversion drive
'hE	Setting inhibited
'hF	Column inversion

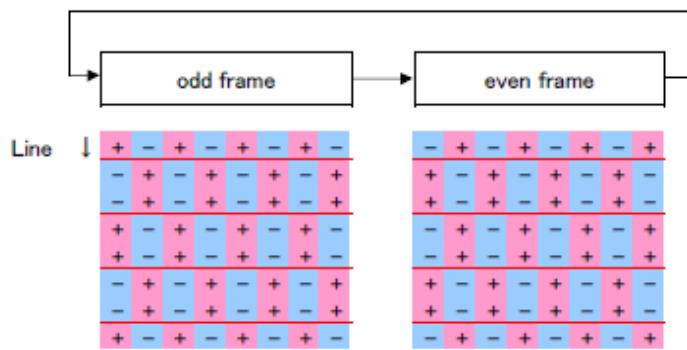
1line inversion drive [spatial configuration mode1] (LINEINVA='h0, PNSET=Don't care)



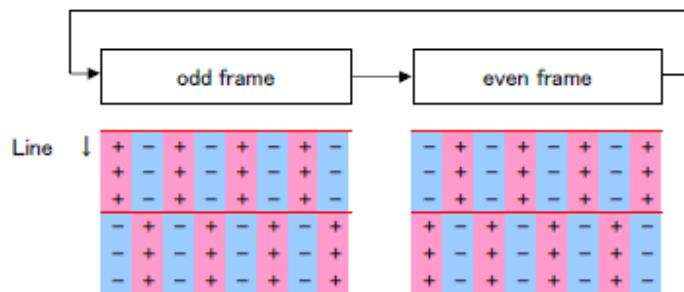
2-line inversion drive [spatial configuration mode1] (LINEINVA ='h1, PNSET='h0)



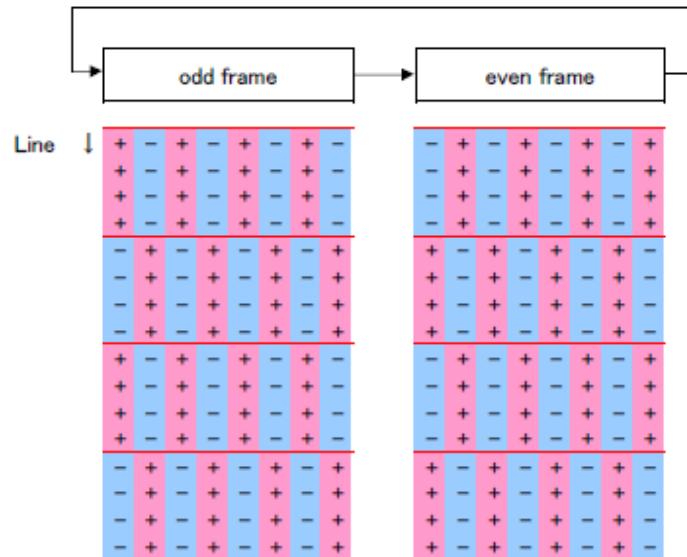
2-line inversion drive [spatial configuration mode2] (LINEINVA ='h1, PNSET='h1)



3-line inversion drive [spatial configuration mode1] (LINEINVA ='h2, PNSET=Don't care)



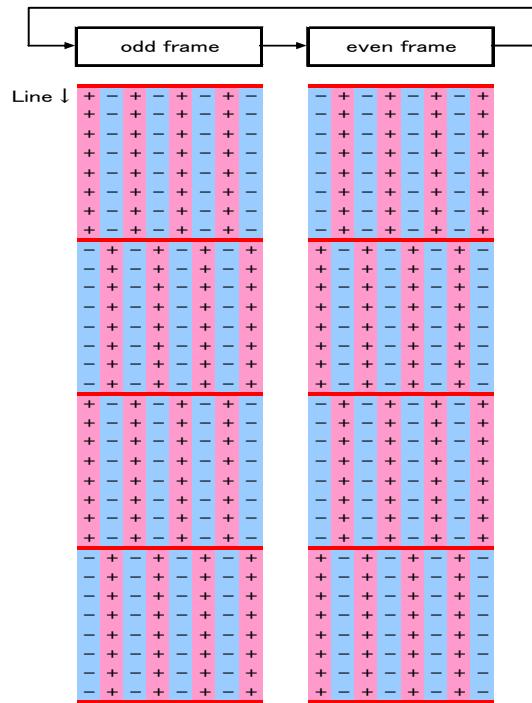
4-line inversion drive [spatial configuration mode1] (LINEINVA ='h3, PNSET='h0)



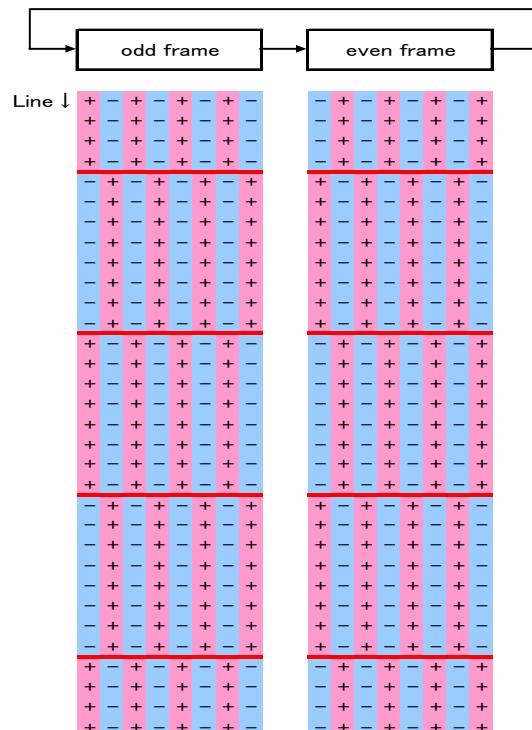
4-line inversion drive [spatial configuration mode2] (LINEINVA ='h3, PNSET='h1)



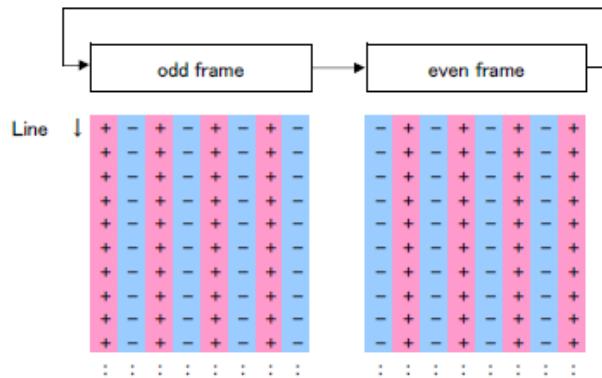
8-line inversion drive [spatial configuration mode1] (LINEINVA ='h5, PNSET='h0)



8-line inversion drive [spatial configuration mode2] (LINEINVA ='h5, PNSET='h1)



Column inversion

**Restriction** -**NL****Description**

This register controls the number of lines to drive panel.

Function Table

NL	Number of lines [line]
'h400	1024 lines
'h500	1280 lines
'h556	1366 lines
'h5A0	1440 lines
'h640	1600 lines
'h780	1920 lines

Restriction -**BP****Description**

This register controls the number of line of back porch.

Function Table

BP	Number of line of back porch[line]
n<2	Setting inhibit
'h2	2 lines
'h3	3 lines
:	:
n	n lines
:	:
'h1F	31 lines

Restriction

Please refer to Appendix data sheet.

• ***Touch Panel Sync Function : C3h***

C3h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	1	C3
1st parameter	1	↑	↑	0	0	VSOD[1]	VSOD[0]	HSOM[1]	HSOM[0]	0	TPSYNEN	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	HSOD[6]	HSOD[5]	HSOD[4]	HSOD[3]	HSOD[2]	HSOD[1]	HSOD[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	HSOHW[7]	HSOHW[6]	HSOHW[5]	HSOHW[4]	HSOHW[3]	HSOHW[2]	HSOHW[1]	HSOHW[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

TPSYNEN

Description

This register set to enable VSOUT, HSOUT output.

Function Table

TPSYNEN	VSOUT, HSOUT output
'h0	OFF (Fixed Low)
'h1	ON (Active)

Restriction

HSOM

Description

This register set the HSOUT output timing.

Refer to "Synchronization signal Output for touch panel controller" for details.

Function Table

HSOM	HSOUT output period		
	Back porach (BP)	Display period (NL)	Front poarch (FP)
'h0	Output	Output	Output
'h1	Fixed low	Output	Fixed Low
'h2	Output	Fixed low	Output
'h3	Setting inhibited		

Restriction

VSOD**Description**

This register set the VSOUT output timing.
Refer to "Synchronization signal Output for touch panel controller" for details.

Function Table

VSOD	VSOUT output timing
'h0	0 line (First line of back porch)
'h1	+1 line
'h2	+2 line
'h3	+3 line

Restriction -**HSOD****Description**

This register set the HSOUT output timing

Function Table

HSOD	HSOUT output timing
'h0	0clk
'h1	1clk
'h2	2clk
:	:
n	n clk
:	:
'h7F	127clk

(1clk=1RCLK)

Restriction -**HSOHW****Description**

This register set the high period of HSOUT.

Function Table

HSOHW	HSOUT high period
'h0	0clk
'h1	1clk
'h2	2clk
:	:
n	n clk
:	:
'hFF	255 clk

(1clk=1RCLK)

Restriction -

• *Source Timing Setting : C4h*

													P	Please refer to Application Note
													P	Please refer to Appendix
C4h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	1	1	0	0	0	1	0	0	C4		
1st parameter	1	↑	↑	0	1	1	1	0	0	0	0	xx		
init	-	-	-	0	1	1	1	0	0	0	0	70		
2nd parameter	1	↑	↑	0	EQW1[6]	EQW1[5]	EQW1[4]	EQW1[3]	EQW1[2]	EQW1[1]	EQW1[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
3rd parameter	1	↑	↑	0	EQW2[6]	EQW2[5]	EQW2[4]	EQW2[3]	EQW2[2]	EQW2[1]	EQW2[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
4th parameter	1	↑	↑	EQM 4	0	EQW3[5]	EQW3[4]	EQW3[3]	EQW3[2]	EQW3[1]	EQW3[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
5th parameter	1	↑	↑	EQM 5[1]	EQM 5[0]	EQW5[5]	EQW5[4]	EQW5[3]	EQW5[2]	EQW5[1]	EQW5[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
6th parameter	1	↑	↑	0	0	EQW6[5]	EQW6[4]	EQW6[3]	EQW6[2]	EQW6[1]	EQW6[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
7th parameter	1	↑	↑	EQM 7[1]	EQM 7[0]	EQW7[5]	EQW7[4]	EQW7[3]	EQW7[2]	EQW7[1]	EQW7[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
8th parameter	1	↑	↑	0	0	EQW8[5]	EQW8[4]	EQW8[3]	EQW8[2]	EQW8[1]	EQW8[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
9th parameter	1	↑	↑	EQM 9[1]	EQM 9[0]	EQW9[5]	EQW9[4]	EQW9[3]	EQW9[2]	EQW9[1]	EQW9[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
10th parameter	1	↑	↑	SNT1[7]	SNT1[6]	SNT1[5]	SNT1[4]	SNT1[3]	SNT1[2]	SNT1[1]	SNT1[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
11th parameter	1	↑	↑	0	SNT2[6]	SNT2[5]	SNT2[4]	SNT2[3]	SNT2[2]	SNT2[1]	SNT2[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
12th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
13th parameter	1	↑	↑	0	EQWA1[6]	EQWA1[5]	EQWA1[4]	EQWA1[3]	EQWA1[2]	EQWA1[1]	EQWA1[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
14th parameter	1	↑	↑	0	EQWA2[6]	EQWA2[5]	EQWA2[4]	EQWA2[3]	EQWA2[2]	EQWA2[1]	EQWA2[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
15th parameter	1	↑	↑	0	0	EQWA3[5]	EQWA3[4]	EQWA3[3]	EQWA3[2]	EQWA3[1]	EQWA3[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
16th parameter	1	↑	↑	0	0	EQWA5[5]	EQWA5[4]	EQWA5[3]	EQWA5[2]	EQWA5[1]	EQWA5[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
17th parameter	1	↑	↑	0	0	EQWA6[5]	EQWA6[4]	EQWA6[3]	EQWA6[2]	EQWA6[1]	EQWA6[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
18th parameter	1	↑	↑	0	0	EQWA7[5]	EQWA7[4]	EQWA7[3]	EQWA7[2]	EQWA7[1]	EQWA7[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
19th parameter	1	↑	↑	0	0	EQWA8[5]	EQWA8[4]	EQWA8[3]	EQWA8[2]	EQWA8[1]	EQWA8[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		
20th parameter	1	↑	↑	0	0	EQWA9[5]	EQWA9[4]	EQWA9[3]	EQWA9[2]	EQWA9[1]	EQWA9[0]	xx		
init	-	-	-	0	0	0	0	0	0	0	0	00		

21st parameter	1	\uparrow	\uparrow	SNTA1[7]	SNTA1[6]	SNTA1[5]	SNTA1[4]	SNTA1[3]	SNTA1[2]	SNTA1[1]	SNTA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
22nd parameter	1	\uparrow	\uparrow	0	SNTA2[6]	SNTA2[5]	SNTA2[4]	SNTA2[3]	SNTA2[2]	SNTA2[1]	SNTA2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

Note) A detail of following registers and EQMx registers are described in Appendix.

SNTx, SNTAx

Description

These registers set s source output delay.

See Appendix for detail of panel control signal timing.

Function Table

SNT1,SNTA1	Delay	SNT2,SNTA2	Timing
'h00	1clk	'h0	1clk
'h01	2clk	'h1	2clk
'h02	3clk	'h2	3clk
'h03	4clk	'h3	4clk
:	:	:	:
n	n clk	n	n clk
:	:	:	:
'hFF	254clk	'h7F	126clk

(1clk = 1RCLK)

Please refer to Appendix for detail.

Restriction

-

EQWx, EQWAx**Description**

These registers set the horizontal period of pre-charge,equalize operation.

EQW1/2,EQWA1/2 : sets a source pre-charge period.

EQW3,EQWA3: sets a SOUTx pre-charge(GND) period. SOUT2,3,4,5,28,29,30,31

EQW5,EQWA5: sets a SOUTx pre-charge(VSP/VSN) period. SOUT2,3,4,5,28,29,30,31

EQW6,EQWA6: sets a SOUTx pre-charge(GND) period. SOUT14,15,16,17,18,19

EQW7,EQWA7: sets a SOUTx pre-charge(VSP/VSN) period. SOUT14,15,16,17,18,19

EQW8,EQWA8: sets a SOUTx pre-charge(GND) period. SOUT11,12,13,20,21,22

EQW9,EQWA9: sets a SOUTx pre-charge(VSP/VSN) period. SOUT11,12,13,20,21,22

See Appendix for detail of panel control signal timing.

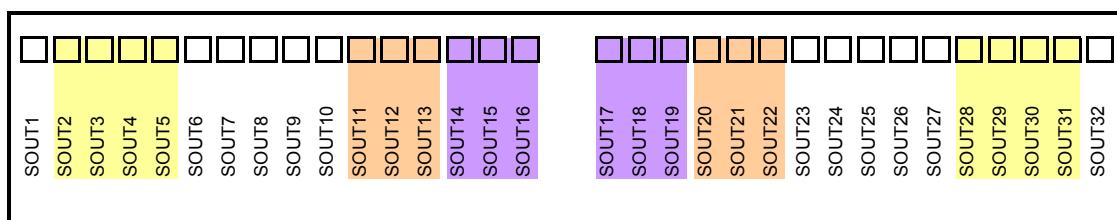
Function Table

EQW1/2, EQWA1/2	Period
'h00	0clk
'h01	1clk
'h02	2clk
'h03	3clk
:	:
n	n clk
:	:
'h7F	127clk

EQW3/5/6/7/8/9 EQWA3/5/6/7/8/9	Period
'h0	0clk
'h1	1clk
'h2	2clk
'h3	3clk
:	:
n	n clk
:	:
'h3F	63clk

(1clk = 1RCLK)

Please refer to Appendix for detail.

Restriction -

- [Yellow Box] SOUT 2,3,4,5,28,29,30,31 EQW3/3A,EQW5/A5
- [Purple Box] SOUT14,15,16,17,18,19 EQW6/6A,EQW7/A7
- [Orange Box] SOUT11,12,13,20,21,22 EQW8/8A,EQW9/A9
- [White Box] SOUT1,6,7,8,9,10,23,24,25,26,27,32 no pre-charge

• *LTPS Timing Setting : C6h*

	Please refer to Application Note									
	Please refer to Appendix									

C6h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	1	1	0	C6
1st parameter	1	↑	↑	0	ST1[6]	ST1[5]	ST1[4]	ST1[3]	ST1[2]	ST1[1]	ST1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	SW1[7]	SW1[6]	SW1[5]	SW1[4]	SW1[3]	SW1[2]	SW1[1]	SW1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	ST2[6]	ST2[5]	ST2[4]	ST2[3]	ST2[2]	ST2[1]	ST2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	SW2[7]	SW2[6]	SW2[5]	SW2[4]	SW2[3]	SW2[2]	SW2[1]	SW2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	ST3[6]	ST3[5]	ST3[4]	ST3[3]	ST3[2]	ST3[1]	ST3[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	SW3[7]	SW3[6]	SW3[5]	SW3[4]	SW3[3]	SW3[2]	SW3[1]	SW3[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	ST4[6]	ST4[5]	ST4[4]	ST4[3]	ST4[2]	ST4[1]	ST4[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	SW4[7]	SW4[6]	SW4[5]	SW4[4]	SW4[3]	SW4[2]	SW4[1]	SW4[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	0	ST5[6]	ST5[5]	ST5[4]	ST5[3]	ST5[2]	ST5[1]	ST5[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	SW5[7]	SW5[6]	SW5[5]	SW5[4]	SW5[3]	SW5[2]	SW5[1]	SW5[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
11th parameter	1	↑	↑	0	ST6[6]	ST6[5]	ST6[4]	ST6[3]	ST6[2]	ST6[1]	ST6[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
12th parameter	1	↑	↑	SW6[7]	SW6[6]	SW6[5]	SW6[4]	SW6[3]	SW6[2]	SW6[1]	SW6[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
13th parameter	1	↑	↑	0	ST7[6]	ST7[5]	ST7[4]	ST7[3]	ST7[2]	ST7[1]	ST7[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
14th parameter	1	↑	↑	SW7[7]	SW7[6]	SW7[5]	SW7[4]	SW7[3]	SW7[2]	SW7[1]	SW7[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
15th parameter	1	↑	↑	0	ST8[6]	ST8[5]	ST8[4]	ST8[3]	ST8[2]	ST8[1]	ST8[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
16th parameter	1	↑	↑	SW8[7]	SW8[6]	SW8[5]	SW8[4]	SW8[3]	SW8[2]	SW8[1]	SW8[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
17th parameter	1	↑	↑	0	PSWT1[6]	PSWT1[5]	PSWT1[4]	PSWT1[3]	PSWT1[2]	PSWT1[1]	PSWT1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
18th parameter	1	↑	↑	PSWW1[7]	PSWW1[6]	PSWW1[5]	PSWW1[4]	PSWW1[3]	PSWW1[2]	PSWW1[1]	PSWW1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
19th parameter	1	↑	↑	0	0	PSWG1[5]	PSWG1[4]	PSWG1[3]	PSWG1[2]	PSWG1[1]	PSWG1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
20th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

21th parameter	1	↑	↑	0	0	0	0	0	0	0	1	xx
init	-	-	-	0	0	0	0	0	0	0	1	01
22th parameter	1	↑	↑	0	STA1[6]	STA1[5]	STA1[4]	STA1[3]	STA1[2]	STA1[1]	STA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
23th parameter	1	↑	↑	SWA1[7]	SWA1[6]	SWA1[5]	SWA1[4]	SWA1[3]	SWA1[2]	SWA1[1]	SWA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
24th parameter	1	↑	↑	0	STA2[6]	STA2[5]	STA2[4]	STA2[3]	STA2[2]	STA2[1]	STA2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
25th parameter	1	↑	↑	SWA2[7]	SWA2[6]	SWA2[5]	SWA2[4]	SWA2[3]	SWA2[2]	SWA2[1]	SWA2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
26th parameter	1	↑	↑	0	STA3[6]	STA3[5]	STA3[4]	STA3[3]	STA3[2]	STA3[1]	STA3[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
27th parameter	1	↑	↑	SWA3[7]	SWA3[6]	SWA3[5]	SWA3[4]	SWA3[3]	SWA3[2]	SWA3[1]	SWA3[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
28th parameter	1	↑	↑	0	STA4[6]	STA4[5]	STA4[4]	STA4[3]	STA4[2]	STA4[1]	STA4[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
29th parameter	1	↑	↑	SWA4[7]	SWA4[6]	SWA4[5]	SWA4[4]	SWA4[3]	SWA4[2]	SWA4[1]	SWA4[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
30th parameter	1	↑	↑	0	STA5[6]	STA5[5]	STA5[4]	STA5[3]	STA5[2]	STA5[1]	STA5[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
31th parameter	1	↑	↑	SWA5[7]	SWA5[6]	SWA5[5]	SWA5[4]	SWA5[3]	SWA5[2]	SWA5[1]	SWA5[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
32th parameter	1	↑	↑	0	STA6[6]	STA6[5]	STA6[4]	STA6[3]	STA6[2]	STA6[1]	STA6[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
33th parameter	1	↑	↑	SWA6[7]	SWA6[6]	SWA6[5]	SWA6[4]	SWA6[3]	SWA6[2]	SWA6[1]	SWA6[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
34th parameter	1	↑	↑	0	STA7[6]	STA7[5]	STA7[4]	STA7[3]	STA7[2]	STA7[1]	STA7[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
35th parameter	1	↑	↑	SWA7[7]	SWA7[6]	SWA7[5]	SWA7[4]	SWA7[3]	SWA7[2]	SWA7[1]	SWA7[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
36th parameter	1	↑	↑	0	STA8[6]	STA8[5]	STA8[4]	STA8[3]	STA8[2]	STA8[1]	STA8[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
37th parameter	1	↑	↑	SWA8[7]	SWA8[6]	SWA8[5]	SWA8[4]	SWA8[3]	SWA8[2]	SWA8[1]	SWA8[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
38th parameter	1	↑	↑	0	PSWTA1[6]	PSWTA1[5]	PSWTA1[4]	PSWTA1[3]	PSWTA1[2]	PSWTA1[1]	PSWTA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
39th parameter	1	↑	↑	PSWWA1[7]	PSWWA1[6]	PSWWA1[5]	PSWWA1[4]	PSWWA1[3]	PSWWA1[2]	PSWWA1[1]	PSWWA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
40th parameter	1	↑	↑	0	0	PSWGA1[5]	PSWGA1[4]	PSWGA1[3]	PSWGA1[2]	PSWGA1[1]	PSWGA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

Note) A detail of following registers and other registers are described in Appendix.

**STx, SWx, PSWTx, PWWx, PSWGx,
STAx, SWAx, PSWTAx, PWWAx, PSWGAx**

Description

The output timing of each panel control signal is set.

STx, STAx: Sets the Rising or Falling position of the SOUT signal.

SWx, SWAx: Sets the High or Low period of the SOUT signal.

PSWTx, PSWTAx: Sets the Rising or Falling position of the SOUT signal.

PWWx, PWWAx: Sets the High or Low period of the SOUT signal.

PSWGx, PSWGAx: Sets the Non-overlap period of the SOUT signal

See Appendix for detail of panel control signal timing.

Function Table

SWx, PSWWx, SWAx, SWWAx	Timing	STx,PSWTx, STAx,PSWTAx	Timing	PSWGx, PSWGAx	Timing
'h00	Setting inhibit	'h0	Setting inhibit	'h0	Setting inhibit
'h01	1clk	'h1	1clk	'h1	1clk
'h02	2clk	'h2	2clk	'h2	2clk
'h03	3clk	'h3	3clk	'h3	3clk
:	:	:	:	:	:
n	n clk	n	n clk	n	n clk
:	:	:	:	:	:
'hFF	255clk	'h7F	127clk	'h3F	63clk

(1clk = 1RCLK)

Please refer to Appendix for detail.

Restriction -

• *Gamma Setting A set : C7h*

C7h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	1	1	1	C7
1st parameter	1	↑	↑	0	VGMAP0[6]	VGMAP0[5]	VGMAP0[4]	VGMAP0[3]	VGMAP0[2]	VGMAP0[1]	VGMAP0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	VGMAP1[6]	VGMAP1[5]	VGMAP1[4]	VGMAP1[3]	VGMAP1[2]	VGMAP1[1]	VGMAP1[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
3rd parameter	1	↑	↑	0	VGMAP2[6]	VGMAP2[5]	VGMAP2[4]	VGMAP2[3]	VGMAP2[2]	VGMAP2[1]	VGMAP2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
4th parameter	1	↑	↑	0	VGMAP3[6]	VGMAP3[5]	VGMAP3[4]	VGMAP3[3]	VGMAP3[2]	VGMAP3[1]	VGMAP3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
5th parameter	1	↑	↑	0	VGMAP4[6]	VGMAP4[5]	VGMAP4[4]	VGMAP4[3]	VGMAP4[2]	VGMAP4[1]	VGMAP4[0]	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
6th parameter	1	↑	↑	0	VGMAP5[6]	VGMAP5[5]	VGMAP5[4]	VGMAP5[3]	VGMAP5[2]	VGMAP5[1]	VGMAP5[0]	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
7th parameter	1	↑	↑	0	VGMAP6[6]	VGMAP6[5]	VGMAP6[4]	VGMAP6[3]	VGMAP6[2]	VGMAP6[1]	VGMAP6[0]	xx
init	-	-	-	0	0	1	0	1	1	1	1	2F
8th parameter	1	↑	↑	0	VGMAP7[6]	VGMAP7[5]	VGMAP7[4]	VGMAP7[3]	VGMAP7[2]	VGMAP7[1]	VGMAP7[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
9th parameter	1	↑	↑	0	VGMAP8[6]	VGMAP8[5]	VGMAP8[4]	VGMAP8[3]	VGMAP8[2]	VGMAP8[1]	VGMAP8[0]	xx
init	-	-	-	0	1	0	0	1	1	1	1	4F
10th parameter	1	↑	↑	0	VGMAP9[6]	VGMAP9[5]	VGMAP9[4]	VGMAP9[3]	VGMAP9[2]	VGMAP9[1]	VGMAP9[0]	xx
init	-	-	-	0	1	0	1	0	1	1	1	57
11th parameter	1	↑	↑	0	VGMAP10[6]	VGMAP10[5]	VGMAP10[4]	VGMAP10[3]	VGMAP10[2]	VGMAP10[1]	VGMAP10[0]	xx
init	-	-	-	0	1	0	1	1	1	1	1	5F
12th parameter	1	↑	↑	0	VGMAP11[6]	VGMAP11[5]	VGMAP11[4]	VGMAP11[3]	VGMAP11[2]	VGMAP11[1]	VGMAP11[0]	xx
init	-	-	-	0	1	1	0	0	1	1	1	67
13th parameter	1	↑	↑	0	VGMAN0[6]	VGMAN0[5]	VGMAN0[4]	VGMAN0[3]	VGMAN0[2]	VGMAN0[1]	VGMAN0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
14th parameter	1	↑	↑	0	VGMAN1[6]	VGMAN1[5]	VGMAN1[4]	VGMAN1[3]	VGMAN1[2]	VGMAN1[1]	VGMAN1[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
15th parameter	1	↑	↑	0	VGMAN2[6]	VGMAN2[5]	VGMAN2[4]	VGMAN2[3]	VGMAN2[2]	VGMAN2[1]	VGMAN2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
16th parameter	1	↑	↑	0	VGMAN3[6]	VGMAN3[5]	VGMAN3[4]	VGMAN3[3]	VGMAN3[2]	VGMAN3[1]	VGMAN3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
17th parameter	1	↑	↑	0	VGMAN4[6]	VGMAN4[5]	VGMAN4[4]	VGMAN4[3]	VGMAN4[2]	VGMAN4[1]	VGMAN4[0]	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
18th parameter	1	↑	↑	0	VGMAN5[6]	VGMAN5[5]	VGMAN5[4]	VGMAN5[3]	VGMAN5[2]	VGMAN5[1]	VGMAN5[0]	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
19th parameter	1	↑	↑	0	VGMAN6[6]	VGMAN6[5]	VGMAN6[4]	VGMAN6[3]	VGMAN6[2]	VGMAN6[1]	VGMAN6[0]	xx
init	-	-	-	0	0	1	0	1	1	1	1	2F
20th parameter	1	↑	↑	0	VGMAN7[6]	VGMAN7[5]	VGMAN7[4]	VGMAN7[3]	VGMAN7[2]	VGMAN7[1]	VGMAN7[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F

21st parameter	1	↑	↑	0	VGMAN8[6]	VGMAN8[5]	VGMAN8[4]	VGMAN8[3]	VGMAN8[2]	VGMAN8[1]	VGMAN8[0]	xx
init	-	-	-	0	1	0	0	1	1	1	1	4F
22nd parameter	1	↑	↑	0	VGMAN9[6]	VGMAN9[5]	VGMAN9[4]	VGMAN9[3]	VGMAN9[2]	VGMAN9[1]	VGMAN9[0]	xx
init	-	-	-	0	1	0	1	0	1	1	1	57
23rd parameter	1	↑	↑	0	VGMAN10[6]	VGMAN10[5]	VGMAN10[4]	VGMAN10[3]	VGMAN10[2]	VGMAN10[1]	VGMAN10[0]	xx
init	-	-	-	0	1	0	1	1	1	1	1	5F
24th parameter	1	↑	↑	0	VGMAN11[6]	VGMAN11[5]	VGMAN11[4]	VGMAN11[3]	VGMAN11[2]	VGMAN11[1]	VGMAN11[0]	xx
init	-	-	-	0	1	1	0	0	1	1	1	67

VGMAPy, VGMANy**Description**

This registers are applied to source pins.

See "Gamma Correction Function" for detailed description of the parameters.

Function Table -**Restriction** -

• *Gamma Setting B set : C8h*

C8h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	0	0	C8
1st parameter	1	↑	↑	0	VGMBP0[6]	VGMBP0[5]	VGMBP0[4]	VGMBP0[3]	VGMBP0[2]	VGMBP0[1]	VGMBP0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	VGMBP1[6]	VGMBP1[5]	VGMBP1[4]	VGMBP1[3]	VGMBP1[2]	VGMBP1[1]	VGMBP1[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
3rd parameter	1	↑	↑	0	VGMBP2[6]	VGMBP2[5]	VGMBP2[4]	VGMBP2[3]	VGMBP2[2]	VGMBP2[1]	VGMBP2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
4th parameter	1	↑	↑	0	VGMBP3[6]	VGMBP3[5]	VGMBP3[4]	VGMBP3[3]	VGMBP3[2]	VGMBP3[1]	VGMBP3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
5th parameter	1	↑	↑	0	VGMBP4[6]	VGMBP4[5]	VGMBP4[4]	VGMBP4[3]	VGMBP4[2]	VGMBP4[1]	VGMBP4[0]	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
6th parameter	1	↑	↑	0	VGMBP5[6]	VGMBP5[5]	VGMBP5[4]	VGMBP5[3]	VGMBP5[2]	VGMBP5[1]	VGMBP5[0]	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
7th parameter	1	↑	↑	0	VGMBP6[6]	VGMBP6[5]	VGMBP6[4]	VGMBP6[3]	VGMBP6[2]	VGMBP6[1]	VGMBP6[0]	xx
init	-	-	-	0	0	1	0	1	1	1	1	2F
8th parameter	1	↑	↑	0	VGMBP7[6]	VGMBP7[5]	VGMBP7[4]	VGMBP7[3]	VGMBP7[2]	VGMBP7[1]	VGMBP7[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
9th parameter	1	↑	↑	0	VGMBP8[6]	VGMBP8[5]	VGMBP8[4]	VGMBP8[3]	VGMBP8[2]	VGMBP8[1]	VGMBP8[0]	xx
init	-	-	-	0	1	0	0	1	1	1	1	4F
10th parameter	1	↑	↑	0	VGMBP9[6]	VGMBP9[5]	VGMBP9[4]	VGMBP9[3]	VGMBP9[2]	VGMBP9[1]	VGMBP9[0]	xx
init	-	-	-	0	1	0	1	0	1	1	1	57
11th parameter	1	↑	↑	0	VGMBP10[6]	VGMBP10[5]	VGMBP10[4]	VGMBP10[3]	VGMBP10[2]	VGMBP10[1]	VGMBP10[0]	xx
init	-	-	-	0	1	0	1	1	1	1	1	5F
12th parameter	1	↑	↑	0	VGMBP11[6]	VGMBP11[5]	VGMBP11[4]	VGMBP11[3]	VGMBP11[2]	VGMBP11[1]	VGMBP11[0]	xx
init	-	-	-	0	1	1	0	0	1	1	1	67
13th parameter	1	↑	↑	0	VGMBN0[6]	VGMBN0[5]	VGMBN0[4]	VGMBN0[3]	VGMBN0[2]	VGMBN0[1]	VGMBN0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
14th parameter	1	↑	↑	0	VGMBN1[6]	VGMBN1[5]	VGMBN1[4]	VGMBN1[3]	VGMBN1[2]	VGMBN1[1]	VGMBN1[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
15th parameter	1	↑	↑	0	VGMBN2[6]	VGMBN2[5]	VGMBN2[4]	VGMBN2[3]	VGMBN2[2]	VGMBN2[1]	VGMBN2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
16th parameter	1	↑	↑	0	VGMBN3[6]	VGMBN3[5]	VGMBN3[4]	VGMBN3[3]	VGMBN3[2]	VGMBN3[1]	VGMBN3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
17th parameter	1	↑	↑	0	VGMBN4[6]	VGMBN4[5]	VGMBN4[4]	VGMBN4[3]	VGMBN4[2]	VGMBN4[1]	VGMBN4[0]	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
18th parameter	1	↑	↑	0	VGMBN5[6]	VGMBN5[5]	VGMBN5[4]	VGMBN5[3]	VGMBN5[2]	VGMBN5[1]	VGMBN5[0]	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
19th parameter	1	↑	↑	0	VGMBN6[6]	VGMBN6[5]	VGMBN6[4]	VGMBN6[3]	VGMBN6[2]	VGMBN6[1]	VGMBN6[0]	xx
init	-	-	-	0	0	1	0	1	1	1	1	2F
20th parameter	1	↑	↑	0	VGMBN7[6]	VGMBN7[5]	VGMBN7[4]	VGMBN7[3]	VGMBN7[2]	VGMBN7[1]	VGMBN7[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F

21st parameter	1	↑	↑	0	VGM BN8[6]	VGM BN8[5]	VGM BN8[4]	VGM BN8[3]	VGM BN8[2]	VGM BN8[1]	VGM BN8[0]	xx
init	-	-	-	0	1	0	0	1	1	1	1	4F
22nd parameter	1	↑	↑	0	VGM BN9[6]	VGM BN9[5]	VGM BN9[4]	VGM BN9[3]	VGM BN9[2]	VGM BN9[1]	VGM BN9[0]	xx
init	-	-	-	0	1	0	1	0	1	1	1	57
23rd parameter	1	↑	↑	0	VGM BN10[6]	VGM BN10[5]	VGM BN10[4]	VGM BN10[3]	VGM BN10[2]	VGM BN10[1]	VGM BN10[0]	xx
init	-	-	-	0	1	0	1	1	1	1	1	5F
24th parameter	1	↑	↑	0	VGM BN11[6]	VGM BN11[5]	VGM BN11[4]	VGM BN11[3]	VGM BN11[2]	VGM BN11[1]	VGM BN11[0]	xx
init	-	-	-	0	1	1	0	0	1	1	1	67

VGMBP_y, VGMBN_y**Description**

This registers are applied to source pins.

See "Gamma Correction Function" for detailed description of the parameters.

Function Table -**Restriction** -

• *Gamma Setting C set : C9h*

C9h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	0	1	C9
1st parameter	1	↑	↑	0	VGMCP0[6]	VGMCP0[5]	VGMCP0[4]	VGMCP0[3]	VGMCP0[2]	VGMCP0[1]	VGMCP0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	VGMCP1[6]	VGMCP1[5]	VGMCP1[4]	VGMCP1[3]	VGMCP1[2]	VGMCP1[1]	VGMCP1[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
3rd parameter	1	↑	↑	0	VGMCP2[6]	VGMCP2[5]	VGMCP2[4]	VGMCP2[3]	VGMCP2[2]	VGMCP2[1]	VGMCP2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
4th parameter	1	↑	↑	0	VGMCP3[6]	VGMCP3[5]	VGMCP3[4]	VGMCP3[3]	VGMCP3[2]	VGMCP3[1]	VGMCP3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
5th parameter	1	↑	↑	0	VGMCP4[6]	VGMCP4[5]	VGMCP4[4]	VGMCP4[3]	VGMCP4[2]	VGMCP4[1]	VGMCP4[0]	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
6th parameter	1	↑	↑	0	VGMCP5[6]	VGMCP5[5]	VGMCP5[4]	VGMCP5[3]	VGMCP5[2]	VGMCP5[1]	VGMCP5[0]	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
7th parameter	1	↑	↑	0	VGMCP6[6]	VGMCP6[5]	VGMCP6[4]	VGMCP6[3]	VGMCP6[2]	VGMCP6[1]	VGMCP6[0]	xx
init	-	-	-	0	0	1	0	1	1	1	1	2F
8th parameter	1	↑	↑	0	VGMCP7[6]	VGMCP7[5]	VGMCP7[4]	VGMCP7[3]	VGMCP7[2]	VGMCP7[1]	VGMCP7[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
9th parameter	1	↑	↑	0	VGMCP8[6]	VGMCP8[5]	VGMCP8[4]	VGMCP8[3]	VGMCP8[2]	VGMCP8[1]	VGMCP8[0]	xx
init	-	-	-	0	1	0	0	1	1	1	1	4F
10th parameter	1	↑	↑	0	VGMCP9[6]	VGMCP9[5]	VGMCP9[4]	VGMCP9[3]	VGMCP9[2]	VGMCP9[1]	VGMCP9[0]	xx
init	-	-	-	0	1	0	1	0	1	1	1	57
11th parameter	1	↑	↑	0	VGMCP10[6]	VGMCP10[5]	VGMCP10[4]	VGMCP10[3]	VGMCP10[2]	VGMCP10[1]	VGMCP10[0]	xx
init	-	-	-	0	1	0	1	1	1	1	1	5F
12th parameter	1	↑	↑	0	VGMCP11[6]	VGMCP11[5]	VGMCP11[4]	VGMCP11[3]	VGMCP11[2]	VGMCP11[1]	VGMCP11[0]	xx
init	-	-	-	0	1	1	0	0	1	1	1	67
13th parameter	1	↑	↑	0	VGMCN0[6]	VGMCN0[5]	VGMCN0[4]	VGMCN0[3]	VGMCN0[2]	VGMCN0[1]	VGMCN0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
14th parameter	1	↑	↑	0	VGMCN1[6]	VGMCN1[5]	VGMCN1[4]	VGMCN1[3]	VGMCN1[2]	VGMCN1[1]	VGMCN1[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
15th parameter	1	↑	↑	0	VGMCN2[6]	VGMCN2[5]	VGMCN2[4]	VGMCN2[3]	VGMCN2[2]	VGMCN2[1]	VGMCN2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
16th parameter	1	↑	↑	0	VGMCN3[6]	VGMCN3[5]	VGMCN3[4]	VGMCN3[3]	VGMCN3[2]	VGMCN3[1]	VGMCN3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
17th parameter	1	↑	↑	0	VGMCN4[6]	VGMCN4[5]	VGMCN4[4]	VGMCN4[3]	VGMCN4[2]	VGMCN4[1]	VGMCN4[0]	xx
init	-	-	-	0	0	1	1	0	0	0	0	30
18th parameter	1	↑	↑	0	VGMCN5[6]	VGMCN5[5]	VGMCN5[4]	VGMCN5[3]	VGMCN5[2]	VGMCN5[1]	VGMCN5[0]	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
19th parameter	1	↑	↑	0	VGMCN6[6]	VGMCN6[5]	VGMCN6[4]	VGMCN6[3]	VGMCN6[2]	VGMCN6[1]	VGMCN6[0]	xx
init	-	-	-	0	0	1	0	1	1	1	1	2F
20th parameter	1	↑	↑	0	VGMCN7[6]	VGMCN7[5]	VGMCN7[4]	VGMCN7[3]	VGMCN7[2]	VGMCN7[1]	VGMCN7[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F

21st parameter	1	↑	↑	0	VGM CN8[6]	VGM CN8[5]	VGM CN8[4]	VGM CN8[3]	VGM CN8[2]	VGM CN8[1]	VGM CN8[0]	xx
init	-	-	-	0	1	0	0	1	1	1	1	4F
22nd parameter	1	↑	↑	0	VGM CN9[6]	VGM CN9[5]	VGM CN9[4]	VGM CN9[3]	VGM CN9[2]	VGM CN9[1]	VGM CN9[0]	xx
init	-	-	-	0	1	0	1	0	1	1	1	57
23rd parameter	1	↑	↑	0	VGM CN10[6]	VGM CN10[5]	VGM CN10[4]	VGM CN10[3]	VGM CN10[2]	VGM CN10[1]	VGM CN10[0]	xx
init	-	-	-	0	1	0	1	1	1	1	1	5F
24th parameter	1	↑	↑	0	VGM CN11[6]	VGM CN11[5]	VGM CN11[4]	VGM CN11[3]	VGM CN11[2]	VGM CN11[1]	VGM CN11[0]	xx
init	-	-	-	0	1	1	0	0	1	1	1	67

VGMCPy, VGMCNy**Description**

This registers are applied to source pins.

See "Gamma Correction Function" for detailed description of the parameters.

Function Table -**Restriction** -

• **Color Enhancement Function (RSP lcd driver IP) : CAh**

	Please refer to Application Note									
	Please refer to Appendix									

CAh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	0	CA
1st parameter	1	↑	↑	0	0	0	0	0	0	0	CE_ON	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	PMIN[7]	PMIN[6]	PMIN[5]	PMIN[4]	PMIN[3]	PMIN[2]	PMIN[1]	PMIN[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
3rd parameter	1	↑	↑	PMAX_R[7]	PMAX_R[6]	PMAX_R[5]	PMAX_R[4]	PMAX_R[3]	PMAX_R[2]	PMAX_R[1]	PMAX_R[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
4th parameter	1	↑	↑	PMAX_Y[7]	PMAX_Y[6]	PMAX_Y[5]	PMAX_Y[4]	PMAX_Y[3]	PMAX_Y[2]	PMAX_Y[1]	PMAX_Y[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
5th parameter	1	↑	↑	PMAX_G[7]	PMAX_G[6]	PMAX_G[5]	PMAX_G[4]	PMAX_G[3]	PMAX_G[2]	PMAX_G[1]	PMAX_G[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
6th parameter	1	↑	↑	PMAX_C[7]	PMAX_C[6]	PMAX_C[5]	PMAX_C[4]	PMAX_C[3]	PMAX_C[2]	PMAX_C[1]	PMAX_C[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
7th parameter	1	↑	↑	PMAX_B[7]	PMAX_B[6]	PMAX_B[5]	PMAX_B[4]	PMAX_B[3]	PMAX_B[2]	PMAX_B[1]	PMAX_B[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
8th parameter	1	↑	↑	PMAX_M[7]	PMAX_M[6]	PMAX_M[5]	PMAX_M[4]	PMAX_M[3]	PMAX_M[2]	PMAX_M[1]	PMAX_M[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
9th parameter	1	↑	↑	0	0	CENH[9]	CENH[8]	CENH[7]	CENH[6]	CENH[5]	CENH[4]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
10th parameter	1	↑	↑	0	0	CENL[9]	CENL[8]	CENL[7]	CENL[6]	CENL[5]	CENL[4]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
11th parameter	1	↑	↑	SLOFS[7]	SLOFS[6]	SLOFS[5]	SLOFS[4]	SLOFS[3]	SLOFS[2]	SLOFS[1]	SLOFS[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
12th parameter	1	↑	↑	CEP[7]	CEP[6]	CEP[5]	CEP[4]	CEP[3]	CEP[2]	CEP[1]	CEP[0]	xx
init	-	-	-	1	0	0	0	0	0	0	0	80
13th parameter	1	↑	↑	CEA1[7]	CEA1[6]	CEA1[5]	CEA1[4]	CEA1[3]	CEA1[2]	CEA1[1]	CEA1[0]	xx
init	-	-	-	0	0	0	0	1	0	1	0	0A
14th parameter	1	↑	↑	CEA2[7]	CEA2[6]	CEA2[5]	CEA2[4]	CEA2[3]	CEA2[2]	CEA2[1]	CEA2[0]	xx
init	-	-	-	0	1	0	0	1	0	1	0	4A
15th parameter	1	↑	↑	CEA3[7]	CEA3[6]	CEA3[5]	CEA3[4]	CEA3[3]	CEA3[2]	CEA3[1]	CEA3[0]	xx
init	-	-	-	0	0	1	1	0	1	1	1	37
16th parameter	1	↑	↑	CEA4[7]	CEA4[6]	CEA4[5]	CEA4[4]	CEA4[3]	CEA4[2]	CEA4[1]	CEA4[0]	xx
init	-	-	-	1	0	1	0	0	0	0	0	A0
17th parameter	1	↑	↑	CEA5[7]	CEA5[6]	CEA5[5]	CEA5[4]	CEA5[3]	CEA5[2]	CEA5[1]	CEA5[0]	xx
init	-	-	-	0	1	0	1	0	1	0	1	55
18th parameter	1	↑	↑	CEA6[7]	CEA6[6]	CEA6[5]	CEA6[4]	CEA6[3]	CEA6[2]	CEA6[1]	CEA6[0]	xx
init	-	-	-	1	1	1	1	1	0	0	0	F8
19th parameter	1	↑	↑	0	0	CEP1[5]	CEP1[4]	CEP1[3]	CEP1[2]	CEP1[1]	CEP1[0]	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C
20th parameter	1	↑	↑	0	0	CEP2[5]	CEP2[4]	CEP2[3]	CEP2[2]	CEP2[1]	CEP2[0]	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C

21st parameter	1	↑	↑	0	0	CEP3[5]	CEP3[4]	CEP3[3]	CEP3[2]	CEP3[1]	CEP3[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
22nd parameter	1	↑	↑	0	0	CEP4[5]	CEP4[4]	CEP4[3]	CEP4[2]	CEP4[1]	CEP4[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
23rd parameter	1	↑	↑	0	0	CEP5[5]	CEP5[4]	CEP5[3]	CEP5[2]	CEP5[1]	CEP5[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
24th parameter	1	↑	↑	0	0	CEP6[5]	CEP6[4]	CEP6[3]	CEP6[2]	CEP6[1]	CEP6[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
25th parameter	1	↑	↑	CEC0[7]	CEC0[6]	CEC0[5]	CEC0[4]	CEC0[3]	CEC0[2]	CEC0[1]	CEC0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
26th parameter	1	↑	↑	CEC[7]	CEC[6]	CEC[5]	CEC[4]	CEC[3]	CEC[2]	CEC[1]	CEC[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
27th parameter	1	↑	↑	0	0	CEC1[5]	CEC1[4]	CEC1[3]	CEC1[2]	CEC1[1]	CEC1[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
28th parameter	1	↑	↑	0	0	CEC2[5]	CEC2[4]	CEC2[3]	CEC2[2]	CEC2[1]	CEC2[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
29th parameter	1	↑	↑	0	0	CEC3[5]	CEC3[4]	CEC3[3]	CEC3[2]	CEC3[1]	CEC3[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
30th parameter	1	↑	↑	0	0	CEC4[5]	CEC4[4]	CEC4[3]	CEC4[2]	CEC4[1]	CEC4[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
31st parameter	1	↑	↑	0	0	CEC5[5]	CEC5[4]	CEC5[3]	CEC5[2]	CEC5[1]	CEC5[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F
32nd parameter	1	↑	↑	0	0	CEC6[5]	CEC6[4]	CEC6[3]	CEC6[2]	CEC6[1]	CEC6[0]	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F

Note) Please refer to Application Note for Color Enhancement Function.

• *Panel PIN Control : CBh*

	Please refer to Application Note
	Please refer to Appendix

CBh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	1	CB
1st parameter	1	↑	↑	SOUTEN8	SOUTEN7	SOUTEN6	SOUTEN5	SOUTEN4	SOUTEN3	SOUTEN2	SOUTEN1	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
2nd parameter	1	↑	↑	SOUTEN16	SOUTEN15	SOUTEN14	SOUTEN13	SOUTEN12	SOUTEN11	SOUTEN10	SOUTEN0	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
3rd parameter	1	↑	↑	SOUTEN24	SOUTEN23	SOUTEN22	SOUTEN21	SOUTEN20	SOUTEN19	SOUTEN18	SOUTEN17	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
4th parameter	1	↑	↑	SOUTEN32	SOUTEN31	SOUTEN30	SOUTEN29	SOUTEN28	SOUTEN27	SOUTEN26	SOUTEN25	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
5th parameter	1	↑	↑	SOUTPL8	SOUTPL7	SOUTPL6	SOUTPL5	SOUTPL4	SOUTPL3	SOUTPL2	SOUTPL1	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	SOUTPL16	SOUTPL15	SOUTPL14	SOUTPL13	SOUTPL12	SOUTPL11	SOUTPL10	SOUTPL9	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	SOUTPL24	SOUTPL23	SOUTPL22	SOUTPL21	SOUTPL20	SOUTPL19	SOUTPL18	SOUTPL17	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	SOUTPL32	SOUTPL31	SOUTPL30	SOUTPL29	SOUTPL28	SOUTPL27	SOUTPL26	SOUTPL25	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	1	1	0	0	0	0	0	0	0
init	-	-	-	1	1	0	0	0	0	0	0	C0

Note) Please refer to Appendix.

• *Panel Interface Control : CCh*

	Please refer to Application Note										
	Please refer to Appendix										

CCh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	0	0	CC
1st parameter	1	↑	↑	0	0	LIM[5]	LIM[4]	LIM[3]	LIM[2]	LIM[1]	LIM[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

LIM

Description

This register controls Panel Interface Mode.

Please select suitable setting for each panel according to Panel Interface Specification.

Function Table

LIM	LCD Panel interface Mode
n	Please refer to the Appendix data sheet.

Restriction

LIM is defined by the Panel Specification. Please refer to the Appendix data sheet.

- *Test : CDh*

CDh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	0	1	CD
1st parameter	1	↑	1	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	1	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	1	1	1	1	1	1	1	1	1	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF

• *Backlight Control 6 : CEh*

	Please refer to Application Note
	Please refer to Appendix

CEh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	1	0	CE
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	PWM_DIV[7]	PWM_DIV[6]	PWM_DIV[5]	PWM_DIV[4]	PWM_DIV[3]	PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	xx
init	-	-	-	0	0	0	0	0	0	0	1	01
3rd parameter	1	↑	↑	PWM_WM	LEDPWMPO_L	PWM_DIMM_METHOD_HIDDEN	PWM_DIMM_INTRPT	PWM_LOWER_MASK[2]	PWM_LOWER_MASK[1]	PWM_LOWER_MASK[0]	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	1	1	0	0	0	0	0	PWM_CYCL_E[8]	xx
init	-	-	-	1	1	0	0	0	0	0	1	C1
5th parameter	1	↑	↑	PWM_CYCL_E[7]	PWM_CYCL_E[6]	PWM_CYCL_E[5]	PWM_CYCL_E[4]	PWM_CYCL_E[3]	PWM_CYCL_E[2]	PWM_CYCL_E[1]	PWM_CYCL_E[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	PWM_DIMM_METHOD	PWM_DIMM_PERIOD[6]	PWM_DIMM_PERIOD[5]	PWM_DIMM_PERIOD[4]	PWM_DIMM_PERIOD[3]	PWM_DIMM_PERIOD[2]	PWM_DIMM_PERIOD[1]	PWM_DIMM_PERIOD[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	PWM_DIMM_PRESCA[6]	PWM_DIMM_PRESCA[5]	PWM_DIMM_PRESCA[4]	PWM_DIMM_PRESCA[3]	PWM_DIMM_PRESCA[2]	PWM_DIMM_PRESCA[1]	PWM_DIMM_PRESCA[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

Note) Please refer to Application Note for CABC Function.

- General Purpose Output Control : CFh*

CFh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	1	1	CF
1st parameter	1	↑	↑	PBCTLB2[1]	PBCTLB2[0]	PBCTLB1[1]	PBCTLB1[0]	PBCTLA2[1]	PBCTLA2[0]	PBCTLA1[1]	PBCTLA1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	PBAMPPON	0	0	0	PBON	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	PBHLVL[3]	PBHLVL[2]	PBHLVL[1]	PBHLVL[0]	0	0	0	1	xx
init	-	-	-	1	1	0	0	0	0	0	1	C1
4th parameter	1	↑	↑	0	0	0	0	0	PBDIV[2]	PBDIV[1]	PBDIV[0]	xx
init	-	-	-	0	0	0	0	0	1	0	1	05
5th parameter	1	↑	↑	0	0	1	1	1	1	1	1	xx
init	-	-	-	0	0	1	1	1	1	1	1	3F

PBCTLA1, PBCTLA2, PBCTLB1, PBCTLB2

Description

This register controls output of PBCTLA1(B1), PBCTLA2(B2) signals.

PBCTLA1 control PBCTLA1 signal.

PBCTLA2 control PBCTLA2 signal.

PBCTLB1 control PBCTLB1 signal.

PBCTLB2 control PBCTLB2 signal.

Function Table

PBCTLA1(B1), PBCTLA2(B2)	OutPut
'h0	Disable (Fixed Low: GND)
'h1	Enable (Inversion is Off)
'h2	Enable (Inversion is On)
'h3	Setting Inhibit

Restriction -

PBON

Description

This register controls output of PBCTLA1(B1), PBCTLA2(B2).

These signals output after entering exit_sleep_mode command, and these signals are independent output of display operation.

Function Table

State	PBON	Output
Sleep in	*	Disable (Fixed Low)
Sleep out	0	Disable (Fixed Low)
	1	Enable

Restriction -

PBAMPON

Description

This register controls high level circuit of PBCTLA1(B1), PBCTLA2(B2).
This circuit operate after entering exit_sleep_mode command.

Function Table

PBAMPON	High level circuit of PBCTLA1(B1), PBCTLA2(B2)
0	Halt
1	Operate

Restriction -

PBHLVL

Description

This register controls high level of PBCTLA1(B1), PBCTLA2(B2).
(Low level is GND.)

Function Table

PBHLVL	High level voltage (High)
'h0	Setting Inhibit
'h1	3.0V
'h2	3.2V
'h3	3.4V
'h4	3.6V
'h5	3.8V
'h6	4.0V
'h7	4.2V
'h8	4.4V
'h9	4.6V
'hA	4.8V
'hB	5.0V
'hC	5.2V
'hD	5.4V
'hE	5.6V
'hF	Setting Inhibit

Restriction

Make sure that voltage level is under (VSP-0.3)V.

PBDIV**Description**

This register controls the frequency of PBCTLA1(B1), PBCTLA2(B2).

Function Table

PBDIV	PBCTLA1(B1), PBCTLA2(B2). frequency (fosc=14MHz)
'h0	30Hz
'h1	40Hz
'h2	50Hz
'h3	60Hz
'h4	70Hz
'h5	80Hz
'h6	90Hz
'h7	100Hz

Restriction -

Power Setting (Charge Pump Setting) : D0h

D0h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	0	DD
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	BT3	0	0	0	BT2	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	1	1	0	0	1	xx
init	-	-	-	0	0	0	1	1	0	0	1	19
4th parameter	1	↑	↑	0	0	0	1	1	0	0	0	xx
init	-	-	-	0	0	0	1	1	0	0	0	18
5th parameter	1	↑	↑	1	0	0	1	1	0	0	1	xx
init	-	-	-	1	0	0	1	1	0	0	1	99
6th parameter	1	↑	↑	1	0	0	1	1	DC2[2]	DC2[1]	DC2[0]	xx
init	-	-	-	1	0	0	1	1	0	0	1	99
7th parameter	1	↑	↑	0	0	0	1	1	DC3[2]	DC3[1]	DC3[0]	xx
init	-	-	-	0	0	0	1	1	0	0	1	19
8th parameter	1	↑	↑	0	0	0	0	0	0	0	1	xx
init	-	-	-	0	0	0	0	0	0	0	1	01
9th parameter	1	↑	↑	1	0	0	0	1	DC4[2]	DC4[1]	DC4[0]	xx
init	-	-	-	1	0	0	0	1	0	0	1	89
10th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
11th parameter	1	↑	↑	VLM1M[3]	VLM1M[2]	VLM1M[1]	VLM1M[0]	VLM1[3]	VLM1[2]	VLM1[1]	VLM1[0]	xx
init	-	-	-	1	0	1	1	1	0	1	1	BB
12th parameter	1	↑	↑	0	VLM2E	VLM2[5]	VLM2[4]	VLM2[3]	VLM2[2]	VLM2[1]	VLM2[0]	xx
init	-	-	-	0	1	0	0	1	0	1	1	4B
13th parameter	1	↑	↑	1	VLM3E	VLM3[5]	VLM3[4]	VLM3[3]	VLM3[2]	VLM3[1]	VLM3[0]	xx
init	-	-	-	1	1	0	0	1	1	1	0	CE
14th parameter	1	↑	↑	0	0	0	0	0	0	0	1	xx
init	-	-	-	0	0	0	0	0	0	0	1	01

BT2**Description**

This register controls boost ratio of VGH.

Function Table

BT2	Boost ratio
	VGH boost ratio
'h0	VCI2×2
'h1	VCI2×2-VSN

Restriction

This command will control when power on/off sequence.

BT3**Description**

This register controls boost ratio of VGL.

Function Table

BT3	Boost ratio
	VGL boost ratio
'h0	VSN—VCI3
'h1	VSN×2—VCI3

Restriction

This command will control when power on/off sequence.

DC2**Description**

This register controls divide ration of boost clock frequency for VGH..

Function Table

DC2	Divide ratio
'h0	Setting inhibited
'h1	210division
'h2	240division
'h3	280 division
'h4	330division
'h5	410 division
'h6	Setting inhibited
'h7	Setting inhibited

Note : $f_{CLK_DC2} = f_{osc} * 1 / n$

f_{CLK_DC2} : CLK_DC2 clock (VGH Step-up frequency)

f_{osc} : OSC clock

n : DC2 divided ratio (in table)

Restriction

This command will control when power on/off sequence..

DC3**Description**

This register controls divide ration of boost clock frequency for VGL.

Function Table

DC3	Divide ratio
'h0	Setting inhibited
'h1	210division
'h2	240division
'h3	280 division
'h4	330division
'h5	410 division
'h6	Setting inhibited
'h7	Setting inhibited

Note : $f_{CLK_DC3} = f_{OSC} * 1/n$

f_{CLK_DC3} : CLK_DC3 clock (VGL Step-up frequency)

f_{OSC} : OSC clock

n : DC3 divided ratio (in table)

Restriction -**DC4****Description**

This register controls divide ration of boost clock frequency for VCL.

Function Table

DC4	Divide ratio
'h0	Setting inhibited
'h1	210division
'h2	240division
'h3	280 division
'h4	330division
'h5	410 division
'h6	Setting inhibited
'h7	Setting inhibited

Note : $f_{CLK_DC4} = f_{OSC} * 1/n$

f_{CLK_DC4} : CLK_DC4 clock (VCL Step-up frequency)

f_{OSC} : OSC clock

n : DC4 divided ratio (in table)

Restriction

This register's value is effective only using charge pump,

VLM1**Description**

This register controls VSP output voltage level.

Function Table

VLM1	VSP level
'h0	4.5V
'h1	4.6V
'h2	4.7V
'h3	4.8V
'h4	4.9V
'h5	5.0V
'h6	5.1V
'h7	5.2V
'h8	5.3V
'h9	5.4V
'hA	5.5V
'hB	5.6V
'hC	5.7V
'hD	5.8V
'hE	5.9V
'hF	6.0V

Restriction -

VLM1M**Description**

This register controls VSN output voltage level

Function Table

VLM1M	VSN level
'h0	-4.5V
'h1	-4.6V
'h2	-4.7V
'h3	-4.8V
'h4	-4.9V
'h5	-5.0V
'h6	-5.1V
'h7	-5.2V
'h8	-5.3V
'h9	-5.4V
'hA	-5.5V
'hB	-5.6V
'hC	-5.7V
'hD	-5.8V
'hE	-5.9V
'hF	-6.0V

Restriction -

VLM2**Description**

This register controls output level of GVDD(VGH).

Function Table

VLM2	GVDD(VGH) level
'h00	Setting inhibited
'h01	Setting inhibited
'h02	Setting inhibited
'h03	Setting inhibited
'h04	Setting inhibited
'h05	5.0V
'h06	5.2V
'h07	5.4V
'h08	5.6V
'h09	5.8V
'h0A	6.0V
'h0B	6.2V
'h0C	6.4V
'h0D	6.6V
'h0E	6.8V
'h0F	7.0V

VLM2	GVDD(VGH) level
'h10	7.2V
'h11	7.4V
'h12	7.6V
'h13	7.8V
'h14	8.0V
'h15	8.2V
'h16	8.4V
'h17	8.6V
'h18	8.8V
'h19	9.0V
'h1A	9.2V
'h1B	9.4V
'h1C	9.6V
'h1D	9.8V
'h1E	10.0V
'h1F	10.2V

VLM2	GVDD(VGH) level
'h20	10.4V
'h21	10.6V
'h22	10.8V
'h23	11.0V
'h24	11.2V
'h25	11.4V
'h26	11.6V
'h27	11.8V
'h28	12.0V
'h29	12.2V
'h2A	12.4V
'h2B	12.6V
'h2C	12.8V
'h2D	13.0V
'h2E	Setting inhibited
'h2F	Setting inhibited

Restriction -

VLM2E**Description**

This register controls the output specification of VGH/GVDD.

Function Table

VLM2E	GVDDDRCT	VGH setup	GVDD setup	Note.
0	0	BT2 register	VLM2 register	GVDD regulator output
	1	-	-	Setting inhibited
1	0	-	-	Setting inhibited
	1	VLM2 register	VLM2 register	VGH=GVDD

Restriction -

VLM3**Description**

This register controls output voltage level of GVSS(VGL).

Function Table

VLM3	GVSS(VGL) level	VLM3	GVSS(VGL) level	VLM3	GVSS(VGL) level
'h00	Setting inhibited	'h10	-7.2V	'h20	-10.4V
'h01	Setting inhibited	'h11	-7.4V	'h21	-10.6V
'h02	Setting inhibited	'h12	-7.6V	'h22	-10.8V
'h03	Setting inhibited	'h13	-7.8V	'h23	-11.0V
'h04	Setting inhibited	'h14	-8.0V	'h24	-11.2V
'h05	-5.0V	'h15	-8.2V	'h25	-11.4V
'h06	-5.2V	'h16	-8.4V	'h26	-11.6V
'h07	-5.4V	'h17	-8.6V	'h27	-11.8V
'h08	-5.6V	'h18	-8.8V	'h28	-12.0V
'h09	-5.8V	'h19	-9.0V	'h29	Setting inhibited
'h0A	-6.0V	'h1A	-9.2V	'h2A	Setting inhibited
'h0B	-6.2V	'h1B	-9.4V	'h2B	Setting inhibited
'h0C	-6.4V	'h1C	-9.6V	'h2C	Setting inhibited
'h0D	-6.6V	'h1D	-9.8V	'h2D	Setting inhibited
'h0E	-6.8V	'h1E	-10.0V	'h2E	Setting inhibited
'h0F	-7.0V	'h1F	-10.2V	'h2F	Setting inhibited

Restriction -

VLM3E**Description**

This register controls the output specification of VGL/GVSS.

Function Table

VLM3E	GVSSDRCT	VGL setup	GVSS setup	Note.
0	0	BT3 register	VLM3 register	GVSS regulator output
	1	-	-	Setting inhibited
1	0	-	-	Setting inhibited
	1	VLM3 register	VLM3 register	VGL=GVSS

Restriction -

• Power Setting (Switching regulator Setting) : D1h

D1h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	1	D1
1st parameter	1	↑	↑	0	DC1SP[6]	DC1SP[5]	DC1SP[4]	DC1SP[3]	DC1SP[2]	DC1SP[1]	DC1SP[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	DC1SPHA[5]	DC1SPHA[4]	DC1SPHA[3]	DC1SPHA[2]	DC1SPHA[1]	DC1SPHA[0]	xx
init	-	-	-	0	0	0	0	0	1	0	0	04
5th parameter	1	↑	↑	0	0	DC1SPHB[5]	DC1SPHB[4]	DC1SPHB[3]	DC1SPHB[2]	DC1SPHB[1]	DC1SPHB[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
6th parameter	1	↑	↑	0	0	DC1SPHC[5]	DC1SPHC[4]	DC1SPHC[3]	DC1SPHC[2]	DC1SPHC[1]	DC1SPHC[0]	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C
7th parameter	1	↑	↑	0	0	DC1SPHD[5]	DC1SPHD[4]	DC1SPHD[3]	DC1SPHD[2]	DC1SPHD[1]	DC1SPHD[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
8th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
11th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
12th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
13th parameter	1	↑	↑	0	0	1	1	1	1	0	0	xx
init	-	-	-	0	0	1	1	1	1	0	0	3C
14th parameter	1	↑	↑	0	0	0	0	0	1	0	0	xx
init	-	-	-	0	0	0	0	0	1	0	0	04
15th parameter	1	↑	↑	0	DC1SM[6]	DC1SM[5]	DC1SM[4]	DC1SM[3]	DC1SM[2]	DC1SM[1]	DC1SM[0]	xx
init	-	-	-	0	0	1	0	0	0	0	0	20
16th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
17th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
18th parameter	1	↑	↑	0	0	DC1SMHA[5]	DC1SMHA[4]	DC1SMHA[3]	DC1SMHA[2]	DC1SMHA[1]	DC1SMHA[0]	xx
init	-	-	-	0	0	0	0	0	1	0	0	04
19th parameter	1	↑	↑	0	0	DC1SMHB[5]	DC1SMHB[4]	DC1SMHB[3]	DC1SMHB[2]	DC1SMHB[1]	DC1SMHB[0]	xx
init	-	-	-	0	0	0	0	1	0	0	0	08
20th parameter	1	↑	↑	0	0	DC1SMHC[5]	DC1SMHC[4]	DC1SMHC[3]	DC1SMHC[2]	DC1SMHC[1]	DC1SMHC[0]	xx
init	-	-	-	0	0	0	0	1	1	0	0	0C

21th parameter	1	↑	↑	0	0	DC1SMHD[5]	DC1SMHD[4]	DC1SMHD[3]	DC1SMHD[2]	DC1SMHD[1]	DC1SMHD[0]	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
22th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
23th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
24th parameter	1	↑	↑	0	0	1	1	1	1	0	0	xx
init	-	-	-	0	0	1	1	1	1	0	0	3C
25th parameter	1	↑	↑	0	0	0	0	0	1	1	0	xx
init	-	-	-	0	0	0	0	0	1	1	0	06
26th parameter	1	↑	↑	0	1	0	0	0	0	0	0	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
27th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
28th parameter	1	↑	↑	0	0	1	1	0	0	1	0	xx
init	-	-	-	0	0	1	1	0	0	1	0	32
29th parameter	1	↑	↑	0	0	1	1	0	0	0	1	xx
init	-	-	-	0	0	1	1	0	0	0	1	31

DC1SP

Description

This register controls clock period of CLK_DC1SP. (CLK_DC1SP is switching clock of VSP.)

Function Table

DC1SP	CLK_DC1SP period
'h0	Setting inhibited
'h1	1 clock
'h2	2 clock
'h3	3 clock
:	:
'h7F	127 clock

1clock = fosc

Restriction

This register's value is effective only using switching regulator.

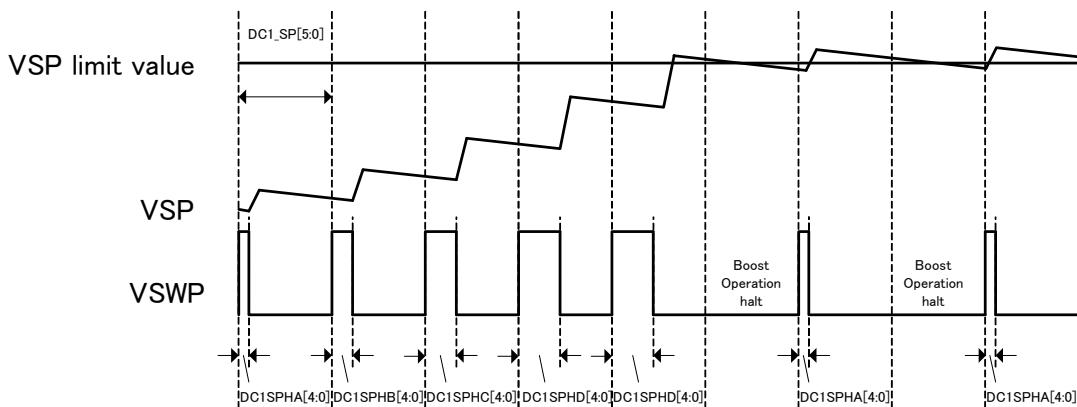
DC1SPHA , DC1SPHB , DC1SPHC , DC1SPHD

Description

This register controls high level width of CLK_DC1SP. (CLK_DC1SP is switchning clock of VSP)

Operation of switching regulator

When VSP is lower than VSP limit voltage, VSWP outputs the clocks set by DC1SPHA, DC1SPHB, DC1SPHC, and DC1SPHD in order according to the cycle of DC1SP and performs boost operation. The boost operation continues according to the setting of DC1SPHD until VSP reaches the VSP limit voltage. When VSP is higher than the VSP limit voltage, the VSWP output, and then, boost operation halt. The above operation applies to VSN and VSN limit voltage.



Function Table

DC1SPH	CLK_DC1SP high level width
'h0	0 clock
'h1	1 clock
'h2	2 clock
'h3	3 clock
:	:
'h3F	63 clock

1clock = fosc

Restriction

This register's value is effective only using switching regulator.

DC1SM**Description**

This register controls clock period of CLK_DC1SM. (CLK_DC1SM is switching clock of VSN.)

Function Table

DC1SM	CLK_DC1SM period
'h0	Setting inhibited
'h1	1 clock
'h2	2 clock
'h3	3 clock
:	:
'h7F	127 clock

1clock = fosc

Restriction

This register's value is effective only using switching regulator. (SWRPON=1, SWRMON=1)

DC1SMHA , DC1SMHB , DC1SMHC , DC1SMHD**Description**

This register controls high level width of CLK_DC1SM. (CLK_DC1SM is switching clock of VSM.).

Function Table

DC1SMH	CLK_DC1SM high peirod
'h0	Setting inhibited
'h1	1 clock
'h2	2 clock
'h3	3 clock
:	:
'h3F	63 clock

1clock = fosc

Restriction

This register's value is effective only using switching regulator.

Test : D2h

D2h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	0	D2
1st parameter	1	↑	↑	0	1	0	1	1	1	0	0	xx
init	-	-	-	0	1	0	1	1	1	0	0	5C
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

Power Setting for Internal Power : D3h

	Please refer to Application Note									
	Please refer to Appendix									

D3h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	1	D3
1st parameter	1	↑	↑	0	0	0	1	1	0	1	1	xx
init	-	-	-	0	0	0	1	1	0	1	1	1B
2nd parameter	1	↑	↑	0	0	1	1	0	0	1	1	xx
init	-	-	-	0	0	1	1	0	0	1	1	33
3rd parameter	1	↑	↑	1	0	1	1	1	0	1	1	xx
init	-	-	-	1	0	1	1	1	0	1	1	BB
4th parameter	1	↑	↑	1	APSGP2[2]	APSGP2[1]	APSGP2[0]	1	APSGP1[2]	APSGP1[1]	APSGP1[0]	xx
init	-	-	-	1	0	1	1	1	0	1	1	BB
5th parameter	1	↑	↑	1	APSGN2[2]	APSGN2[1]	APSGN2[0]	0	APSGN1[2]	APSGN1[1]	APSGN1[0]	xx
init	-	-	-	1	0	1	1	0	0	1	1	B3
6th parameter	1	↑	↑	0	0	1	1	0	0	1	1	xx
init	-	-	-	0	0	1	1	0	0	1	1	33
7th parameter	1	↑	↑	0	0	1	1	0	0	1	1	xx
init	-	-	-	0	0	1	1	0	0	1	1	33
8th parameter	1	↑	↑	0	0	1	1	0	0	1	1	xx
init	-	-	-	0	0	1	1	0	0	1	1	33
9th parameter	1	↑	↑	SEQGND2 [3]	SEQGND2 [2]	SEQGND2 [1]	SEQGND2 [0]	SEQGND1 [3]	SEQGND1 [2]	SEQGND1 [1]	SEQGND1 [0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	0	0	0	0	0	0	0	1	xx
init	-	-	-	0	0	0	0	0	0	0	1	01
11th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
12th parameter	1	↑	↑	1	VC1[2]	VC1[1]	VC1[0]	0	0	0	0	xx
init	-	-	-	1	0	1	0	0	0	0	0	A0
13th parameter	1	↑	↑	VC2[3]	VC2[2]	VC2[1]	VC2[0]	1	0	0	0	xx
init	-	-	-	1	1	0	1	1	0	0	0	D8
14th parameter	1	↑	↑	1	0	1	0	0	0	0	0	xx
init	-	-	-	1	0	1	0	0	0	0	0	A0
15th parameter	1	↑	↑	0	0	0	0	VC3[3]	VC3[2]	VC3[1]	VC3[0]	xx
init	-	-	-	0	0	0	0	1	1	0	1	0D
16th parameter	1	↑	↑	0	VPL[6]	VPL[5]	VPL[4]	VPL[3]	VPL[2]	VPL[1]	VPL[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
17th parameter	1	↑	↑	0	0	1	1	0	0	1	1	xx
init	-	-	-	0	0	1	1	0	0	1	1	33
18th parameter	1	↑	↑	0	APAP[2]	APAP[1]	APAP[0]	0	APAN[2]	APAN[1]	APAN[0]	xx
init	-	-	-	0	0	1	1	0	0	1	1	33
19th parameter	1	↑	↑	0	0	1	0	0	0	1	0	xx
init	-	-	-	0	0	1	0	0	0	1	0	22
20th parameter	1	↑	↑	0	1	1	1	0	0	0	0	xx
init	-	-	-	0	1	1	1	0	0	0	0	70

21st parameter	1	↑	↑	0	0	0	0	0	0	1	0	xx
init	-	-	-	0	0	0	0	0	0	1	0	02
22nd parameter	1	↑	↑	0	VNL[6]	VNL[5]	VNL[4]	VNL[3]	VNL[2]	VNL[1]	VNL[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
23rd parameter	1	↑	↑	GVDDDRCT[1]	0GVDDDRCT[0]	GVSSDRCT[1]	GVSSDRCT[0]	0	0	1	1	xx
init	-	-	-	0	0	0	0	0	0	1	1	03
24th parameter	1	↑	↑	0	0	1	1	1	1	0	1	xx
init	-	-	-	0	0	1	1	1	1	0	1	3D
25th parameter	1	↑	↑	1	0	1	1	1	1	1	1	xx
init	-	-	-	1	0	1	1	1	1	1	1	BF
26th parameter	1	↑	↑	SVS[3]	SVS[2]	SVS[1]	SVS[0]	SVD[3]	SVD[2]	SVD[1]	SVD[0]	xx
init	-	-	-	1	0	0	1	1	0	0	1	99

Note) SEQGND1,SEQGND2 registers are described in Appendix.

APSGP1/2,APSGN1/2

Description

This register controls source bias current.

Function Table

APSGP1/2	Source bias current (Positive)	APSGN1/2	Source bias current (Negative)
'h0	100%	'h0	100%
'h1	125%	'h1	125%
'h2	150%	'h2	150%
'h3	175%	'h3	175%
'h4	200%	'h4	200%
'h5	225%	'h5	225%
'h6	250%	'h6	250%
'h7	275%	'h7	275%

Restriction

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VC1**Description**

This register controls output voltage of VCI1 regulator. VCI1 is internal voltage for generating VCL.

Function Table

VC1	VCI1 regulator output voltage
'h0	2.3V
'h1	2.4V
'h2	2.5V
'h3	2.6V
'h4	2.7V
'h5	2.8V
'h6	2.9V
'h7	3.0V

Restriction

This command will control when power on/off sequence.

VC2**Description**

This register controls output voltage of VCI2 regulator. VCI2 is internal voltage for generateing VGH.

Function Table

VC2	VCI2 regulator output voltage
'h0	2.4V
'h1	2.6V
'h2	2.8V
'h3	3.0V
'h4	3.2V
'h5	3.4V
'h6	3.6V
'h7	3.8V
'h8	4.0V
'h9	4.2V
'hA	4.4V
'hB	4.6V
'hC	4.8V
'hD	5.0V
'hE	5.2V
'hF	5.4V

Restriction

This command will control when power on/off sequence.

VC3

Description

This register controls output voltage of VCI3 regulator. VCI3 is internal volgtage for generating VGL.

Function Table

VC3	VCI3 regulator output voltage
'h0	2.4V
'h1	2.6V
'h2	2.8V
'h3	3.0V
'h4	3.2V
'h5	3.4V
'h6	3.6V
'h7	3.8V
'h8	4.0V
'h9	4.2V
'hA	4.4V
'hB	4.6V
'hC	4.8V
'hD	5.0V
'hE	5.2V
'hF	5.4V

Restriction

This command will control when power on/off sequence.

VPL**Description**

This register controls output voltage of positive gray scale reference level.

Function Table

VPL	VPLVL [V]	VPL	VPLVL [V]	VPL	VPLVL [V]	VPL	VPLVL [V]
'h00	Setting inhibited	'h20	3.325	'h40	4.125	'h60	4.925
'h01		'h21	3.350	'h41	4.150	'h61	4.950
'h02		'h22	3.375	'h42	4.175	'h62	4.975
'h03		'h23	3.400	'h43	4.200	'h63	5.000
'h04		'h24	3.425	'h44	4.225	'h64	5.025
'h05		'h25	3.450	'h45	4.250	'h65	5.050
'h06		'h26	3.475	'h46	4.275	'h66	5.075
'h07		'h27	3.500	'h47	4.300	'h67	5.100
'h08		'h28	3.525	'h48	4.325	'h68	5.125
'h09		'h29	3.550	'h49	4.350	'h69	5.150
'h0A		'h2A	3.575	'h4A	4.375	'h6A	5.175
'h0B		'h2B	3.600	'h4B	4.400	'h6B	5.200
'h0C		'h2C	3.625	'h4C	4.425	'h6C	5.225
'h0D		'h2D	3.650	'h4D	4.450	'h6D	5.250
'h0E		'h2E	3.675	'h4E	4.475	'h6E	5.275
'h0F		'h2F	3.700	'h4F	4.500	'h6F	5.300
'h10		'h30	3.725	'h50	4.525	'h70	5.325
'h11		'h31	3.750	'h51	4.550	'h71	5.350
'h12		'h32	3.775	'h52	4.575	'h72	5.375
'h13	3.000	'h33	3.800	'h53	4.600	'h73	5.400
'h14	3.025	'h34	3.825	'h54	4.625	'h74	5.425
'h15	3.050	'h35	3.850	'h55	4.650	'h75	5.450
'h16	3.075	'h36	3.875	'h56	4.675	'h76	5.475
'h17	3.100	'h37	3.900	'h57	4.700	'h77	5.500
'h18	3.125	'h38	3.925	'h58	4.725	'h78	5.525
'h19	3.150	'h39	3.950	'h59	4.750	'h79	5.550
'h1A	3.175	'h3A	3.975	'h5A	4.775	'h7A	5.575
'h1B	3.200	'h3B	4.000	'h5B	4.800	'h7B	5.600
'h1C	3.225	'h3C	4.025	'h5C	4.825	'h7C	5.625
'h1D	3.250	'h3D	4.050	'h5D	4.850	'h7D	5.650
'h1E	3.275	'h3E	4.075	'h5E	4.875	'h7E	5.675
'h1F	3.300	'h3F	4.100	'h5F	4.900	'h7F	5.700

Restriction -

APAN**Description**

This register controls reference current of Source amp and Gamma circuit for negative polarity.

Function Table

APAP	Current consumption
'h0	Setting inhibited
'h1	50%
'h2	75%
'h3	100%
'h4	125%
'h5	Setting inhibited
'h6	Setting inhibited
'h7	Setting inhibited

Restriction -

APAP**Description**

This register controls reference current of Source amp and Gamma circuit positive output.

Function Table

APAP	Current consumption
'h0	Setting inhibited
'h1	50%
'h2	75%
'h3	100%
'h4	125%
'h5	Setting inhibited
'h6	Setting inhibited
'h7	Setting inhibited

Restriction -

VNL**Description**

This register controls output voltage of negative gray scale reference level.

Function Table

VNL	VNLVL [V]	VNL	VNLVL [V]	VNL	VNLVL [V]	VNL	VNLVL [V]
'h00	Setting inhibited	'h20	-3.325	'h40	-4.125	'h60	-4.925
'h01		'h21	-3.350	'h41	-4.150	'h61	-4.950
'h02		'h22	-3.375	'h42	-4.175	'h62	-4.975
'h03		'h23	-3.400	'h43	-4.200	'h63	-5.000
'h04		'h24	-3.425	'h44	-4.225	'h64	-5.025
'h05		'h25	-3.450	'h45	-4.250	'h65	-5.050
'h06		'h26	-3.475	'h46	-4.275	'h66	-5.075
'h07		'h27	-3.500	'h47	-4.300	'h67	-5.100
'h08		'h28	-3.525	'h48	-4.325	'h68	-5.125
'h09		'h29	-3.550	'h49	-4.350	'h69	-5.150
'h0A		'h2A	-3.575	'h4A	-4.375	'h6A	-5.175
'h0B		'h2B	-3.600	'h4B	-4.400	'h6B	-5.200
'h0C		'h2C	-3.625	'h4C	-4.425	'h6C	-5.225
'h0D		'h2D	-3.650	'h4D	-4.450	'h6D	-5.250
'h0E		'h2E	-3.675	'h4E	-4.475	'h6E	-5.275
'h0F		'h2F	-3.700	'h4F	-4.500	'h6F	-5.300
'h10		'h30	-3.725	'h50	-4.525	'h70	-5.325
'h11		'h31	-3.750	'h51	-4.550	'h71	-5.350
'h12		'h32	-3.775	'h52	-4.575	'h72	-5.375
'h13	-3.000	'h33	-3.800	'h53	-4.600	'h73	-5.400
'h14	-3.025	'h34	-3.825	'h54	-4.625	'h74	-5.425
'h15	-3.050	'h35	-3.850	'h55	-4.650	'h75	-5.450
'h16	-3.075	'h36	-3.875	'h56	-4.675	'h76	-5.475
'h17	-3.100	'h37	-3.900	'h57	-4.700	'h77	-5.500
'h18	-3.125	'h38	-3.925	'h58	-4.725	'h78	-5.525
'h19	-3.150	'h39	-3.950	'h59	-4.750	'h79	-5.550
'h1A	-3.175	'h3A	-3.975	'h5A	-4.775	'h7A	-5.575
'h1B	-3.200	'h3B	-4.000	'h5B	-4.800	'h7B	-5.600
'h1C	-3.225	'h3C	-4.025	'h5C	-4.825	'h7C	-5.625
'h1D	-3.250	'h3D	-4.050	'h5D	-4.850	'h7D	-5.650
'h1E	-3.275	'h3E	-4.075	'h5E	-4.875	'h7E	-5.675
'h1F	-3.300	'h3F	-4.100	'h5F	-4.900	'h7F	-5.700

Restriction -

GVDDDRCT**Description**

This register controls the output specification of GVDD.

Function Table

GVDDDRCT	GVDD
'h0	Amplifier output
'h1	VGH short
'h2	Setting inhibited
'h3	Setting inhibited

Restriction -**GVSSDRCT****Description**

This register controls the output specification of GVSS.

Function Table

GVSSDRCT	GVSS
'h0	Amplifier output
'h1	VGL short
'h2	Setting inhibited
'h3	Setting inhibited

Restriction -

SVD**Description**

This register controls the output voltage of SVDD.

Function Table

SVD	SVDD[V] (case of VSP=6.0V)
'h0	4.5
'h1	4.6
'h2	4.7
'h3	4.8
'h4	4.9
'h5	5.0
'h6	5.1
'h7	5.2
'h8	5.3
'h9	5.4
'hA	5.5
'hB	5.6
'hC	5.7
'hD	5.8
'hE	Setting inhibited
'hF	Setting inhibited

The setting range of SVDD is 4.5V to VSP-0.2V

Restriction -

SVS**Description**

This register controls the output voltage of SVSS.

Function Table

SVS	SVSS[V] (case of VSN=-6.0V)
'h0	-4.5
'h1	-4.6
'h2	-4.7
'h3	-4.8
'h4	-4.9
'h5	-5.0
'h6	-5.1
'h7	-5.2
'h8	-5.3
'h9	-5.4
'hA	-5.5
'hB	-5.6
'hC	-5.7
'hD	-5.8
'hE	Setting inhibited
'hF	Setting inhibited

The setting range of SVSS is -4.5V to VSN+0.2V

Restriction -

VCOM Setting : D5h

D5h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	1	0	1	D5
1st parameter	1	↑	↑	0	0	0	0	0	WCVDC	WCVDCB	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	0	0	0	0	0	VDC[8]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	VDC[7]	VDC[6]	VDC[5]	VDC[4]	VDC[3]	VDC[2]	VDC[1]	VDC[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	VDCB[8]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	VDCB[7]	VDCB[6]	VDCB[5]	VDCB[4]	VDCB[3]	VDCB[2]	VDCB[1]	VDCB[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

WCVDCB**Description**

This register controls access to VCOM adjustment register(VDCB).
Please use this register in case of adjustment.

Function Table

WCVDCB	Operation
0	Register access is disable. VDC is kept initial value from NVM data.
1	Register access is enable. If user wants to re-write NVM data, please set WCVDCB=1 before NVM re-write sequence.

Restriction -

WCVDC**Description**

This register controls access to VCOM adjustment register(VDC).
Please use this register in case of VCOM adjustment.

Function Table

WCVDC	Operation
0	Register access is disable. VDC is kept initial value from NVM data.
1	Register access is enable. If user wants to re-write NVM data, please set WCVDC=1 before NVM re-write sequence.

Restriction -

VDC**Description**

This register controls VCOMDC output level. VDC is effective on forward scan.

$$\text{VCOMDC}[V] = \text{VPLVL} - (\text{VPLVL}-\text{VNLVL}) \times [\text{Setting Value}]$$

Note : Refer to the appendix for scan mode.

Function Table

VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC
'h0	Setting inhibited	'h20	Setting inhibited	'h40	Setting inhibited	'h60	x 0.3727
'h1		'h21		'h41		'h61	x 0.3735
'h2		'h22		'h42		'h62	x 0.3742
'h3		'h23		'h43		'h63	x 0.3750
'h4		'h24		'h44		'h64	x 0.3758
'h5		'h25		'h45		'h65	x 0.3765
'h6		'h26		'h46		'h66	x 0.3773
'h7		'h27		'h47		'h67	x 0.3780
'h8		'h28		'h48	x 0.3545	'h68	x 0.3788
'h9		'h29		'h49	x 0.3553	'h69	x 0.3795
'hA		'h2A		'h4A	x 0.3561	'h6A	x 0.3803
'hB		'h2B		'h4B	x 0.3568	'h6B	x 0.3811
'hC		'h2C		'h4C	x 0.3576	'h6C	x 0.3818
'hD		'h2D		'h4D	x 0.3583	'h6D	x 0.3826
'hE		'h2E		'h4E	x 0.3591	'h6E	x 0.3833
'hF		'h2F		'h4F	x 0.3598	'h6F	x 0.3841
'h10		'h30		'h50	x 0.3606	'h70	x 0.3848
'h11		'h31		'h51	x 0.3614	'h71	x 0.3856
'h12		'h32		'h52	x 0.3621	'h72	x 0.3864
'h13		'h33		'h53	x 0.3629	'h73	x 0.3871
'h14		'h34		'h54	x 0.3636	'h74	x 0.3879
'h15		'h35		'h55	x 0.3644	'h75	x 0.3886
'h16		'h36		'h56	x 0.3652	'h76	x 0.3894
'h17		'h37		'h57	x 0.3659	'h77	x 0.3902
'h18		'h38		'h58	x 0.3667	'h78	x 0.3909
'h19		'h39		'h59	x 0.3674	'h79	x 0.3917
'h1A		'h3A		'h5A	x 0.3682	'h7A	x 0.3924
'h1B		'h3B		'h5B	x 0.3689	'h7B	x 0.3932
'h1C		'h3C		'h5C	x 0.3697	'h7C	x 0.3939
'h1D		'h3D		'h5D	x 0.3705	'h7D	x 0.3947
'h1E		'h3E		'h5E	x 0.3712	'h7E	x 0.3955
'h1F		'h3F		'h5F	x 0.3720	'h7F	x 0.3962

(continued)

VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC
'h80	x 0.3970	'hA0	x 0.4212	'hC0	x 0.4455	'hE0	x 0.4697
'h81	x 0.3977	'hA1	x 0.4220	'hC1	x 0.4462	'hE1	x 0.4705
'h82	x 0.3985	'hA2	x 0.4227	'hC2	x 0.4470	'hE2	x 0.4712
'h83	x 0.3992	'hA3	x 0.4235	'hC3	x 0.4477	'hE3	x 0.4720
'h84	x 0.4000	'hA4	x 0.4242	'hC4	x 0.4485	'hE4	x 0.4727
'h85	x 0.4008	'hA5	x 0.4250	'hC5	x 0.4492	'hE5	x 0.4735
'h86	x 0.4015	'hA6	x 0.4258	'hC6	x 0.4500	'hE6	x 0.4742
'h87	x 0.4023	'hA7	x 0.4265	'hC7	x 0.4508	'hE7	x 0.4750
'h88	x 0.4030	'hA8	x 0.4273	'hC8	x 0.4515	'hE8	x 0.4758
'h89	x 0.4038	'hA9	x 0.4280	'hC9	x 0.4523	'hE9	x 0.4765
'h8A	x 0.4045	'hAA	x 0.4288	'hCA	x 0.4530	'hEA	x 0.4773
'h8B	x 0.4053	'hAB	x 0.4295	'hCB	x 0.4538	'hEB	x 0.4780
'h8C	x 0.4061	'hAC	x 0.4303	'hCC	x 0.4545	'hEC	x 0.4788
'h8D	x 0.4068	'hAD	x 0.4311	'hCD	x 0.4553	'hED	x 0.4795
'h8E	x 0.4076	'hAE	x 0.4318	'hCE	x 0.4561	'hEE	x 0.4803
'h8F	x 0.4083	'hAF	x 0.4326	'hCF	x 0.4568	'hEF	x 0.4811
'h90	x 0.4091	'hB0	x 0.4333	'hD0	x 0.4576	'hF0	x 0.4818
'h91	x 0.4098	'hB1	x 0.4341	'hD1	x 0.4583	'hF1	x 0.4826
'h92	x 0.4106	'hB2	x 0.4348	'hD2	x 0.4591	'hF2	x 0.4833
'h93	x 0.4114	'hB3	x 0.4356	'hD3	x 0.4598	'hF3	x 0.4841
'h94	x 0.4121	'hB4	x 0.4364	'hD4	x 0.4606	'hF4	x 0.4848
'h95	x 0.4129	'hB5	x 0.4371	'hD5	x 0.4614	'hF5	x 0.4856
'h96	x 0.4136	'hB6	x 0.4379	'hD6	x 0.4621	'hF6	x 0.4864
'h97	x 0.4144	'hB7	x 0.4386	'hD7	x 0.4629	'hF7	x 0.4871
'h98	x 0.4152	'hB8	x 0.4394	'hD8	x 0.4636	'hF8	x 0.4879
'h99	x 0.4159	'hB9	x 0.4402	'hD9	x 0.4644	'hF9	x 0.4886
'h9A	x 0.4167	'hBA	x 0.4409	'hDA	x 0.4652	'hFA	x 0.4894
'h9B	x 0.4174	'hBB	x 0.4417	'hDB	x 0.4659	'hFB	x 0.4902
'h9C	x 0.4182	'hBC	x 0.4424	'hDC	x 0.4667	'hFC	x 0.4909
'h9D	x 0.4189	'hBD	x 0.4432	'hDD	x 0.4674	'hFD	x 0.4917
'h9E	x 0.4197	'hBE	x 0.4439	'hDE	x 0.4682	'hFE	x 0.4924
'h9F	x 0.4205	'hBF	x 0.4447	'hDF	x 0.4689	'hFF	x 0.4932

(continued)

VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC
'h100	x 0.4939	'h120	x 0.5182	'h140	x 0.5424	'h160	x 0.5667
'h101	x 0.4947	'h121	x 0.5189	'h141	x 0.5432	'h161	x 0.5674
'h102	x 0.4955	'h122	x 0.5197	'h142	x 0.5439	'h162	x 0.5682
'h103	x 0.4962	'h123	x 0.5205	'h143	x 0.5447	'h163	x 0.5689
'h104	x 0.4970	'h124	x 0.5212	'h144	x 0.5455	'h164	x 0.5697
'h105	x 0.4977	'h125	x 0.5220	'h145	x 0.5462	'h165	x 0.5705
'h106	x 0.4985	'h126	x 0.5227	'h146	x 0.5470	'h166	x 0.5712
'h107	x 0.4992	'h127	x 0.5235	'h147	x 0.5477	'h167	x 0.5720
'h108	x 0.5000	'h128	x 0.5242	'h148	x 0.5485	'h168	x 0.5727
'h109	x 0.5008	'h129	x 0.5250	'h149	x 0.5492	'h169	x 0.5735
'h10A	x 0.5015	'h12A	x 0.5258	'h14A	x 0.5500	'h16A	x 0.5742
'h10B	x 0.5023	'h12B	x 0.5265	'h14B	x 0.5508	'h16B	x 0.5750
'h10C	x 0.5030	'h12C	x 0.5273	'h14C	x 0.5515	'h16C	x 0.5758
'h10D	x 0.5038	'h12D	x 0.5280	'h14D	x 0.5523	'h16D	x 0.5765
'h10E	x 0.5045	'h12E	x 0.5288	'h14E	x 0.5530	'h16E	x 0.5773
'h10F	x 0.5053	'h12F	x 0.5295	'h14F	x 0.5538	'h16F	x 0.5780
'h110	x 0.5061	'h130	x 0.5303	'h150	x 0.5545	'h170	x 0.5788
'h111	x 0.5068	'h131	x 0.5311	'h151	x 0.5553	'h171	x 0.5795
'h112	x 0.5076	'h132	x 0.5318	'h152	x 0.5561	'h172	x 0.5803
'h113	x 0.5083	'h133	x 0.5326	'h153	x 0.5568	'h173	x 0.5811
'h114	x 0.5091	'h134	x 0.5333	'h154	x 0.5576	'h174	x 0.5818
'h115	x 0.5098	'h135	x 0.5341	'h155	x 0.5583	'h175	x 0.5826
'h116	x 0.5106	'h136	x 0.5348	'h156	x 0.5591	'h176	x 0.5833
'h117	x 0.5114	'h137	x 0.5356	'h157	x 0.5598	'h177	x 0.5841
'h118	x 0.5121	'h138	x 0.5364	'h158	x 0.5606	'h178	x 0.5848
'h119	x 0.5129	'h139	x 0.5371	'h159	x 0.5614	'h179	x 0.5856
'h11A	x 0.5136	'h13A	x 0.5379	'h15A	x 0.5621	'h17A	x 0.5864
'h11B	x 0.5144	'h13B	x 0.5386	'h15B	x 0.5629	'h17B	x 0.5871
'h11C	x 0.5152	'h13C	x 0.5394	'h15C	x 0.5636	'h17C	x 0.5879
'h11D	x 0.5159	'h13D	x 0.5402	'h15D	x 0.5644	'h17D	x 0.5886
'h11E	x 0.5167	'h13E	x 0.5409	'h15E	x 0.5652	'h17E	x 0.5894
'h11F	x 0.5174	'h13F	x 0.5417	'h15F	x 0.5659	'h17F	x 0.5902

(continued)

VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC	VDC	VCOMDC
'h180	x 0.5909	'h1A0	x 0.6152	'h1C0	x 0.6394	'h1E0	
'h181	x 0.5917	'h1A1	x 0.6159	'h1C1	x 0.6402	'h1E1	
'h182	x 0.5924	'h1A2	x 0.6167	'h1C2	x 0.6409	'h1E2	
'h183	x 0.5932	'h1A3	x 0.6174	'h1C3	x 0.6417	'h1E3	
'h184	x 0.5939	'h1A4	x 0.6182	'h1C4	x 0.6424	'h1E4	
'h185	x 0.5947	'h1A5	x 0.6189	'h1C5	x 0.6432	'h1E5	
'h186	x 0.5955	'h1A6	x 0.6197	'h1C6	x 0.6439	'h1E6	
'h187	x 0.5962	'h1A7	x 0.6205	'h1C7	x 0.6447	'h1E7	
'h188	x 0.5970	'h1A8	x 0.6212	'h1C8	x 0.6455	'h1E8	
'h189	x 0.5977	'h1A9	x 0.6220	'h1C9		'h1E9	
'h18A	x 0.5985	'h1AA	x 0.6227	'h1CA		'h1EA	
'h18B	x 0.5992	'h1AB	x 0.6235	'h1CB		'h1EB	
'h18C	x 0.6000	'h1AC	x 0.6242	'h1CC		'h1EC	
'h18D	x 0.6008	'h1AD	x 0.6250	'h1CD		'h1ED	
'h18E	x 0.6015	'h1AE	x 0.6258	'h1CE		'h1EE	
'h18F	x 0.6023	'h1AF	x 0.6265	'h1CF		'h1EF	
'h190	x 0.6030	'h1B0	x 0.6273	'h1D0		'h1F0	
'h191	x 0.6038	'h1B1	x 0.6280	'h1D1		'h1F1	
'h192	x 0.6045	'h1B2	x 0.6288	'h1D2		'h1F2	
'h193	x 0.6053	'h1B3	x 0.6295	'h1D3		'h1F3	
'h194	x 0.6061	'h1B4	x 0.6303	'h1D4		'h1F4	
'h195	x 0.6068	'h1B5	x 0.6311	'h1D5		'h1F5	
'h196	x 0.6076	'h1B6	x 0.6318	'h1D6		'h1F6	
'h197	x 0.6083	'h1B7	x 0.6326	'h1D7		'h1F7	
'h198	x 0.6091	'h1B8	x 0.6333	'h1D8		'h1F8	
'h199	x 0.6098	'h1B9	x 0.6341	'h1D9		'h1F9	
'h19A	x 0.6106	'h1BA	x 0.6348	'h1DA		'h1FA	
'h19B	x 0.6114	'h1BB	x 0.6356	'h1DB		'h1FB	
'h19C	x 0.6121	'h1BC	x 0.6364	'h1DC		'h1FC	
'h19D	x 0.6129	'h1BD	x 0.6371	'h1DD		'h1FD	
'h19E	x 0.6136	'h1BE	x 0.6379	'h1DE		'h1FE	
'h19F	x 0.6144	'h1BF	x 0.6386	'h1DF		'h1FF	

Restriction

Make sure that voltage level is (-2.0 ~ +2.0)V in setting.

VDCB**Description**

This register controls VCOMDC output level. VDCB is effective on backward scan.

$$\text{VCOMDC}[V] = \text{VPLVL} - (\text{VPLVL}-\text{VNLVL}) \times [\text{Setting Value}]$$

Note : Refer to the appendix for scan mode.

Function Table

VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC
'h0	Setting inhibited	'h20	Setting inhibited	'h40	Setting inhibited	'h60	x 0.3727
'h1		'h21		'h41		'h61	x 0.3735
'h2		'h22		'h42		'h62	x 0.3742
'h3		'h23		'h43		'h63	x 0.3750
'h4		'h24		'h44		'h64	x 0.3758
'h5		'h25		'h45		'h65	x 0.3765
'h6		'h26		'h46		'h66	x 0.3773
'h7		'h27		'h47		'h67	x 0.3780
'h8		'h28		'h48	x 0.3545	'h68	x 0.3788
'h9		'h29		'h49	x 0.3553	'h69	x 0.3795
'hA		'h2A		'h4A	x 0.3561	'h6A	x 0.3803
'hB		'h2B		'h4B	x 0.3568	'h6B	x 0.3811
'hC		'h2C		'h4C	x 0.3576	'h6C	x 0.3818
'hD		'h2D		'h4D	x 0.3583	'h6D	x 0.3826
'hE		'h2E		'h4E	x 0.3591	'h6E	x 0.3833
'hF		'h2F		'h4F	x 0.3598	'h6F	x 0.3841
'h10		'h30		'h50	x 0.3606	'h70	x 0.3848
'h11		'h31		'h51	x 0.3614	'h71	x 0.3856
'h12		'h32		'h52	x 0.3621	'h72	x 0.3864
'h13		'h33		'h53	x 0.3629	'h73	x 0.3871
'h14		'h34		'h54	x 0.3636	'h74	x 0.3879
'h15		'h35		'h55	x 0.3644	'h75	x 0.3886
'h16		'h36		'h56	x 0.3652	'h76	x 0.3894
'h17		'h37		'h57	x 0.3659	'h77	x 0.3902
'h18		'h38		'h58	x 0.3667	'h78	x 0.3909
'h19		'h39		'h59	x 0.3674	'h79	x 0.3917
'h1A		'h3A		'h5A	x 0.3682	'h7A	x 0.3924
'h1B		'h3B		'h5B	x 0.3689	'h7B	x 0.3932
'h1C		'h3C		'h5C	x 0.3697	'h7C	x 0.3939
'h1D		'h3D		'h5D	x 0.3705	'h7D	x 0.3947
'h1E		'h3E		'h5E	x 0.3712	'h7E	x 0.3955
'h1F		'h3F		'h5F	x 0.3720	'h7F	x 0.3962

(continued)

VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC
'h80	x 0.3970	'hA0	x 0.4212	'hC0	x 0.4455	'hE0	x 0.4697
'h81	x 0.3977	'hA1	x 0.4220	'hC1	x 0.4462	'hE1	x 0.4705
'h82	x 0.3985	'hA2	x 0.4227	'hC2	x 0.4470	'hE2	x 0.4712
'h83	x 0.3992	'hA3	x 0.4235	'hC3	x 0.4477	'hE3	x 0.4720
'h84	x 0.4000	'hA4	x 0.4242	'hC4	x 0.4485	'hE4	x 0.4727
'h85	x 0.4008	'hA5	x 0.4250	'hC5	x 0.4492	'hE5	x 0.4735
'h86	x 0.4015	'hA6	x 0.4258	'hC6	x 0.4500	'hE6	x 0.4742
'h87	x 0.4023	'hA7	x 0.4265	'hC7	x 0.4508	'hE7	x 0.4750
'h88	x 0.4030	'hA8	x 0.4273	'hC8	x 0.4515	'hE8	x 0.4758
'h89	x 0.4038	'hA9	x 0.4280	'hC9	x 0.4523	'hE9	x 0.4765
'h8A	x 0.4045	'hAA	x 0.4288	'hCA	x 0.4530	'hEA	x 0.4773
'h8B	x 0.4053	'hAB	x 0.4295	'hCB	x 0.4538	'hEB	x 0.4780
'h8C	x 0.4061	'hAC	x 0.4303	'hCC	x 0.4545	'hEC	x 0.4788
'h8D	x 0.4068	'hAD	x 0.4311	'hCD	x 0.4553	'hED	x 0.4795
'h8E	x 0.4076	'hAE	x 0.4318	'hCE	x 0.4561	'hEE	x 0.4803
'h8F	x 0.4083	'hAF	x 0.4326	'hCF	x 0.4568	'hEF	x 0.4811
'h90	x 0.4091	'hB0	x 0.4333	'hD0	x 0.4576	'hF0	x 0.4818
'h91	x 0.4098	'hB1	x 0.4341	'hD1	x 0.4583	'hF1	x 0.4826
'h92	x 0.4106	'hB2	x 0.4348	'hD2	x 0.4591	'hF2	x 0.4833
'h93	x 0.4114	'hB3	x 0.4356	'hD3	x 0.4598	'hF3	x 0.4841
'h94	x 0.4121	'hB4	x 0.4364	'hD4	x 0.4606	'hF4	x 0.4848
'h95	x 0.4129	'hB5	x 0.4371	'hD5	x 0.4614	'hF5	x 0.4856
'h96	x 0.4136	'hB6	x 0.4379	'hD6	x 0.4621	'hF6	x 0.4864
'h97	x 0.4144	'hB7	x 0.4386	'hD7	x 0.4629	'hF7	x 0.4871
'h98	x 0.4152	'hB8	x 0.4394	'hD8	x 0.4636	'hF8	x 0.4879
'h99	x 0.4159	'hB9	x 0.4402	'hD9	x 0.4644	'hF9	x 0.4886
'h9A	x 0.4167	'hBA	x 0.4409	'hDA	x 0.4652	'hFA	x 0.4894
'h9B	x 0.4174	'hBB	x 0.4417	'hDB	x 0.4659	'hFB	x 0.4902
'h9C	x 0.4182	'hBC	x 0.4424	'hDC	x 0.4667	'hFC	x 0.4909
'h9D	x 0.4189	'hBD	x 0.4432	'hDD	x 0.4674	'hFD	x 0.4917
'h9E	x 0.4197	'hBE	x 0.4439	'hDE	x 0.4682	'hFE	x 0.4924
'h9F	x 0.4205	'hBF	x 0.4447	'hDF	x 0.4689	'hFF	x 0.4932

(continued)

VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC
'h100	x 0.4939	'h120	x 0.5182	'h140	x 0.5424	'h160	x 0.5667
'h101	x 0.4947	'h121	x 0.5189	'h141	x 0.5432	'h161	x 0.5674
'h102	x 0.4955	'h122	x 0.5197	'h142	x 0.5439	'h162	x 0.5682
'h103	x 0.4962	'h123	x 0.5205	'h143	x 0.5447	'h163	x 0.5689
'h104	x 0.4970	'h124	x 0.5212	'h144	x 0.5455	'h164	x 0.5697
'h105	x 0.4977	'h125	x 0.5220	'h145	x 0.5462	'h165	x 0.5705
'h106	x 0.4985	'h126	x 0.5227	'h146	x 0.5470	'h166	x 0.5712
'h107	x 0.4992	'h127	x 0.5235	'h147	x 0.5477	'h167	x 0.5720
'h108	x 0.5000	'h128	x 0.5242	'h148	x 0.5485	'h168	x 0.5727
'h109	x 0.5008	'h129	x 0.5250	'h149	x 0.5492	'h169	x 0.5735
'h10A	x 0.5015	'h12A	x 0.5258	'h14A	x 0.5500	'h16A	x 0.5742
'h10B	x 0.5023	'h12B	x 0.5265	'h14B	x 0.5508	'h16B	x 0.5750
'h10C	x 0.5030	'h12C	x 0.5273	'h14C	x 0.5515	'h16C	x 0.5758
'h10D	x 0.5038	'h12D	x 0.5280	'h14D	x 0.5523	'h16D	x 0.5765
'h10E	x 0.5045	'h12E	x 0.5288	'h14E	x 0.5530	'h16E	x 0.5773
'h10F	x 0.5053	'h12F	x 0.5295	'h14F	x 0.5538	'h16F	x 0.5780
'h110	x 0.5061	'h130	x 0.5303	'h150	x 0.5545	'h170	x 0.5788
'h111	x 0.5068	'h131	x 0.5311	'h151	x 0.5553	'h171	x 0.5795
'h112	x 0.5076	'h132	x 0.5318	'h152	x 0.5561	'h172	x 0.5803
'h113	x 0.5083	'h133	x 0.5326	'h153	x 0.5568	'h173	x 0.5811
'h114	x 0.5091	'h134	x 0.5333	'h154	x 0.5576	'h174	x 0.5818
'h115	x 0.5098	'h135	x 0.5341	'h155	x 0.5583	'h175	x 0.5826
'h116	x 0.5106	'h136	x 0.5348	'h156	x 0.5591	'h176	x 0.5833
'h117	x 0.5114	'h137	x 0.5356	'h157	x 0.5598	'h177	x 0.5841
'h118	x 0.5121	'h138	x 0.5364	'h158	x 0.5606	'h178	x 0.5848
'h119	x 0.5129	'h139	x 0.5371	'h159	x 0.5614	'h179	x 0.5856
'h11A	x 0.5136	'h13A	x 0.5379	'h15A	x 0.5621	'h17A	x 0.5864
'h11B	x 0.5144	'h13B	x 0.5386	'h15B	x 0.5629	'h17B	x 0.5871
'h11C	x 0.5152	'h13C	x 0.5394	'h15C	x 0.5636	'h17C	x 0.5879
'h11D	x 0.5159	'h13D	x 0.5402	'h15D	x 0.5644	'h17D	x 0.5886
'h11E	x 0.5167	'h13E	x 0.5409	'h15E	x 0.5652	'h17E	x 0.5894
'h11F	x 0.5174	'h13F	x 0.5417	'h15F	x 0.5659	'h17F	x 0.5902

(continued)

VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC	VDCB	VCOMDC
'h180	x 0.5909	'h1A0	x 0.6152	'h1C0	x 0.6394	'h1E0	
'h181	x 0.5917	'h1A1	x 0.6159	'h1C1	x 0.6402	'h1E1	
'h182	x 0.5924	'h1A2	x 0.6167	'h1C2	x 0.6409	'h1E2	
'h183	x 0.5932	'h1A3	x 0.6174	'h1C3	x 0.6417	'h1E3	
'h184	x 0.5939	'h1A4	x 0.6182	'h1C4	x 0.6424	'h1E4	
'h185	x 0.5947	'h1A5	x 0.6189	'h1C5	x 0.6432	'h1E5	
'h186	x 0.5955	'h1A6	x 0.6197	'h1C6	x 0.6439	'h1E6	
'h187	x 0.5962	'h1A7	x 0.6205	'h1C7	x 0.6447	'h1E7	
'h188	x 0.5970	'h1A8	x 0.6212	'h1C8	x 0.6455	'h1E8	
'h189	x 0.5977	'h1A9	x 0.6220	'h1C9		'h1E9	
'h18A	x 0.5985	'h1AA	x 0.6227	'h1CA		'h1EA	
'h18B	x 0.5992	'h1AB	x 0.6235	'h1CB		'h1EB	
'h18C	x 0.6000	'h1AC	x 0.6242	'h1CC		'h1EC	
'h18D	x 0.6008	'h1AD	x 0.6250	'h1CD		'h1ED	
'h18E	x 0.6015	'h1AE	x 0.6258	'h1CE		'h1EE	
'h18F	x 0.6023	'h1AF	x 0.6265	'h1CF		'h1EF	
'h190	x 0.6030	'h1B0	x 0.6273	'h1D0		'h1F0	
'h191	x 0.6038	'h1B1	x 0.6280	'h1D1		'h1F1	
'h192	x 0.6045	'h1B2	x 0.6288	'h1D2		'h1F2	
'h193	x 0.6053	'h1B3	x 0.6295	'h1D3		'h1F3	
'h194	x 0.6061	'h1B4	x 0.6303	'h1D4		'h1F4	
'h195	x 0.6068	'h1B5	x 0.6311	'h1D5		'h1F5	
'h196	x 0.6076	'h1B6	x 0.6318	'h1D6		'h1F6	
'h197	x 0.6083	'h1B7	x 0.6326	'h1D7		'h1F7	
'h198	x 0.6091	'h1B8	x 0.6333	'h1D8		'h1F8	
'h199	x 0.6098	'h1B9	x 0.6341	'h1D9		'h1F9	
'h19A	x 0.6106	'h1BA	x 0.6348	'h1DA		'h1FA	
'h19B	x 0.6114	'h1BB	x 0.6356	'h1DB		'h1FB	
'h19C	x 0.6121	'h1BC	x 0.6364	'h1DC		'h1FC	
'h19D	x 0.6129	'h1BD	x 0.6371	'h1DD		'h1FD	
'h19E	x 0.6136	'h1BE	x 0.6379	'h1DE		'h1FE	
'h19F	x 0.6144	'h1BF	x 0.6386	'h1DF		'h1FF	

Restriction

Make sure that voltage level is (-2.0 ~ +2.0)V in setting.

- Sequencer Test Control : D6h**

D6h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	1	1	0	D6
1st parameter	1	↑	↑	T_SLPOUT	0	0	0	0	0	0	1	xx
init	-	-	-	1	0	0	0	0	0	0	1	81

T_SLPOUT

Description

This register controls NVM Load at the time of exit_sleep_mode.

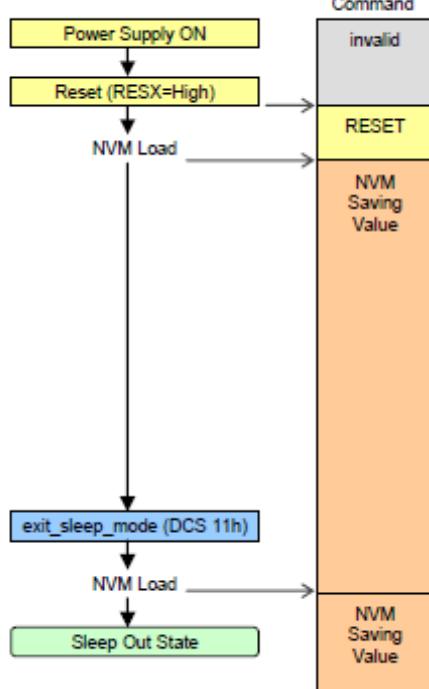
Function Table

T_SLPOUT	Operation
0	NVM is not loaded.
1	NVM is loaded.

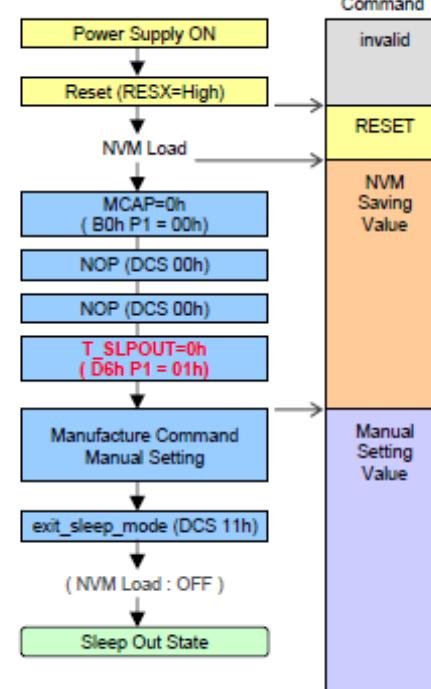
Restriction

Sequence Example

(1) T_SLPOUT=1h example



(2) T_SLPOUT=0h example



• ***Test : D7h***

D7h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	1	1	1	D7
1st parameter	1	↑	↑	1	0	0	0	0	1	0	0	xx
init	-	-	-	1	0	0	0	0	1	0	0	84
2nd parameter	1	↑	↑	1	1	1	0	0	0	0	0	xx
init	-	-	-	1	1	1	0	0	0	0	0	E0
3rd parameter	1	↑	↑	0	1	1	1	1	1	1	1	xx
init	-	-	-	0	1	1	1	1	1	1	1	7F
4th parameter	1	↑	↑	1	0	1	0	1	0	0	0	xx
init	-	-	-	1	0	1	0	1	0	0	0	A8
5th parameter	1	↑	↑	1	1	0	0	1	1	1	0	xx
init	-	-	-	1	1	0	0	1	1	1	0	CE
6th parameter	1	↑	↑	0	0	1	1	1	0	0	0	xx
init	-	-	-	0	0	1	1	1	0	0	0	38
7th parameter	1	↑	↑	1	1	1	1	1	1	0	0	xx
init	-	-	-	1	1	1	1	1	1	0	0	FC
8th parameter	1	↑	↑	1	1	0	0	0	0	0	0	xx
init	-	-	-	1	1	0	0	0	0	0	1	C1
9th parameter	1	↑	↑	1	0	0	0	0	0	1	1	xx
init	-	-	-	1	0	0	0	0	0	1	1	83
10th parameter	1	↑	↑	1	1	1	0	0	1	1	1	xx
init	-	-	-	1	1	1	0	0	1	1	1	E7
11th parameter	1	↑	↑	1	0	0	0	1	1	1	1	xx
init	-	-	-	1	0	0	0	1	1	1	1	8F
12th parameter	1	↑	↑	0	0	0	1	1	1	1	1	xx
init	-	-	-	0	0	0	1	1	1	1	1	1F
13th parameter	1	↑	↑	0	0	1	1	1	1	0	0	xx
init	-	-	-	0	0	1	1	1	1	0	0	3C
14th parameter	1	↑	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
15th parameter	1	↑	↑	1	1	1	1	1	0	1	0	xx
init	-	-	-	1	1	1	1	1	0	1	0	FA
16th parameter	1	↑	↑	1	1	0	0	0	0	1	1	xx
init	-	-	-	1	1	0	0	0	0	1	1	C3
17th parameter	1	↑	↑	0	0	0	0	1	1	1	1	xx
init	-	-	-	0	0	0	0	1	1	1	1	0F
18th parameter	1	↑	↑	0	0	0	0	0	1	0	0	xx
init	-	-	-	0	0	0	0	0	1	0	0	04
19th parameter	1	↑	↑	0	1	0	0	0	0	0	1	xx
init	-	-	-	0	1	0	0	0	0	0	1	41
20th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

• *Auto Contrast Optimization : D8h*

	Please refer to Application Note
	Please refer to Appendix

D8h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	0	0	D8
1st parameter	1	↑	↑	0	0	0	0	0	0	0	ACO_ON	xx
Init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	SPEED_HI[7]	SPEED_HI[6]	SPEED_HI[5]	SPEED_HI[4]	SPEED_HI[3]	SPEED_HI[2]	SPEED_HI[1]	SPEED_HI[0]	xx
Init	-	-	-	1	0	0	0	0	0	0	0	80
3rd parameter	1	↑	↑	SPEED_LO[7]	SPEED_LO[6]	SPEED_LO[5]	SPEED_LO[4]	SPEED_LO[3]	SPEED_LO[2]	SPEED_LO[1]	SPEED_LO[0]	xx
Init	-	-	-	1	1	1	1	1	1	1	1	80
4th parameter	1	↑	↑	SPEED_JX_T_H[7]	SPEED_JX_T_H[6]	SPEED_JX_T_H[5]	SPEED_JX_T_H[4]	SPEED_JX_T_H[3]	SPEED_JX_T_H[2]	SPEED_JX_T_H[1]	SPEED_JX_T_H[0]	xx
Init	-	-	-	0	1	0	0	0	0	0	0	40
5th parameter	1	↑	↑	MODE_JX_TOB_V0_V255	ACO_MASK	0	0	SPEED_BX_T_H[3]	SPEED_BX_T_H[2]	SPEED_BX_T_H[1]	SPEED_BX_T_H[0]	xx
Init	-	-	-	0	1	0	0	0	0	1	0	42
6th parameter	1	↑	↑	BASE_INTEN_S[3]	BASE_INTEN_S[2]	BASE_INTEN_S[1]	BASE_INTEN_S[0]	BIN_INTENS[3]	BIN_INTENS[2]	BIN_INTENS[1]	BIN_INTENS[0]	xx
Init	-	-	-	0	0	1	0	0	0	0	1	21

Note) Please refer to Application Note for ACO Function.

- **Test : D9h**

D9h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	0	1	D9
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- Outline Sharpening Control : DDh*

 Please refer to Application Note
 Please refer to Appendix

DDh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	1	DD
1st parameter	1	↑	↑	0	0	EGE_MODE[9]	EGE_MODE[8]	0	0	0	EGE_ON	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
2nd parameter	1	↑	↑	EGE_MODE[7]	EGE_MODE[6]	EGE_MODE[5]	EGE_MODE[4]	EGE_MODE[3]	EGE_MODE[2]	EGE_MODE[1]	EGE_MODE[0]	xx
init	-	-	-	1	0	0	0	1	1	0	0	8C

Note) Please refer to Application Note for Outline Sharpening Control Function.

- *Test Image Generator : DEh*

DEh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	1	0	DE
1st parameter	1	↑	↑	0	0	0	0	0	0	0	TIGON	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	TIP[7]	TIP[6]	TIP[5]	TIP[4]	TIP[3]	TIP[2]	TIP[1]	TIP[0]	xx
init	-	-	-	1	1	1	1	1	1	1	1	FF
3rd parameter	1	↑	↑	0	0	TIGCYC[1]	TIGCYC[0]	0	TIP[10]	TIP[9]	TIP[8]	xx
init	-	-	-	0	0	0	0	0	1	1	1	07
4th parameter	1	↑	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10
5th parameter	1	↑	↑	0	0	0	0	0	0	0	RTN[8]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	RTN[7]	RTN[6]	RTN[5]	RTN[4]	RTN[3]	RTN[2]	RTN[1]	RTN[0]	xx
init	-	-	-	0	1	1	1	0	1	1	1	77

TIGON

Description

This IC supports the test free-running mode function. When TIGON is set to "1", this IC operates in synchronization with the internal oscillation clock.

Enables the Test Image Generation function.

Function Table

TIGON	Test Image Generator
0	Off
1	On

Restriction

- In Built-in TCON Display Mode (DM = 'h0) only, TIGON can set to 1.

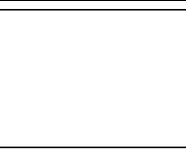
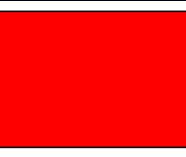
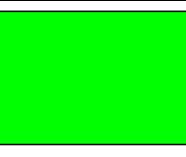
TIP**Description**

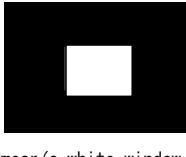
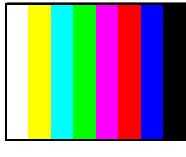
Setting each of the TIP[10:0] registers to 1 allows images to be displayed in the free-running mode. The following are the relationships between the registers and display images.

Function Table

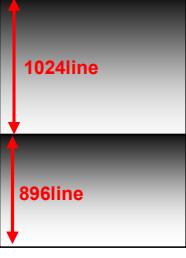
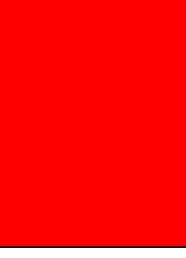
Register	Display image
TIP[0]	Middle Gray 127
TIP[1]	Horizontal grayscale
TIP[2]	Vertical grayscale
TIP[3]	White 255
TIP[4]	Red 255
TIP[5]	Green 255
TIP[6]	Blue 255
TIP[7]	Black
TIP[8]	SMEAR (a white window against a dark background)
TIP[9]	Color bar
TIP[10]	DCF (aligned dot check)

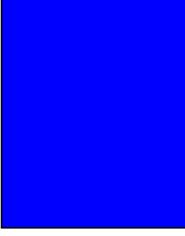
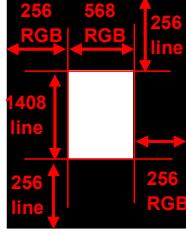
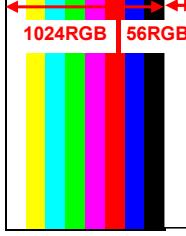
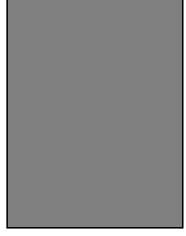
1024RGB × 1024

TIP[0]	TIP[1]	TIP[2]	TIP[3]	TIP[4]	TIP[5]
					
Middle Gray 127	Horizontal Grayscale	Vertical Grayscale	White 255	Red 255	Green 255

TIP[6]	TIP[7]	TIP[8]	TIP[9]	TIP[10]
				
Blue 255	Black	Smear (a white window against a black background)	Color bar	DCF (aligned dot check)

1080RGB × 1920

TIP[0]	TIP[1]	TIP[2]	TIP[3]	TIP[4]	TIP[5]
					
Middle Gray 127	Horizontal Grayscale	Vertical Grayscale	White 255	Red 255	Green 255

TIP[6]	TIP[7]	TIP[8]	TIP[9]	TIP[10]
				
Blue 255	Black	Smear (a white window against a black background)	Color bar	DCF (aligned dot check)

Restriction

Display image TIP[1], TIP[2] , and TIP[9] may be repeated in a screen according to the size. The central

white window size in display image TIP[8] varies according to the display image size.

TIGCYC

Description

TIGCYC can change the display cycle of the selected image.

Function Table

TIGCYC	Display cycle
'h0	64 frames
'h1	128 frames
'h2	256 frames
'h3	512 frames
'h4	1024 frames

Restriction -

RTN

Description

Sets 1H (line) period.

Only "Test Image Generation(DM='h0&TIGON=1)" is effective.

Test Image Generation, frame frequency is adjusted by BP and RTN.

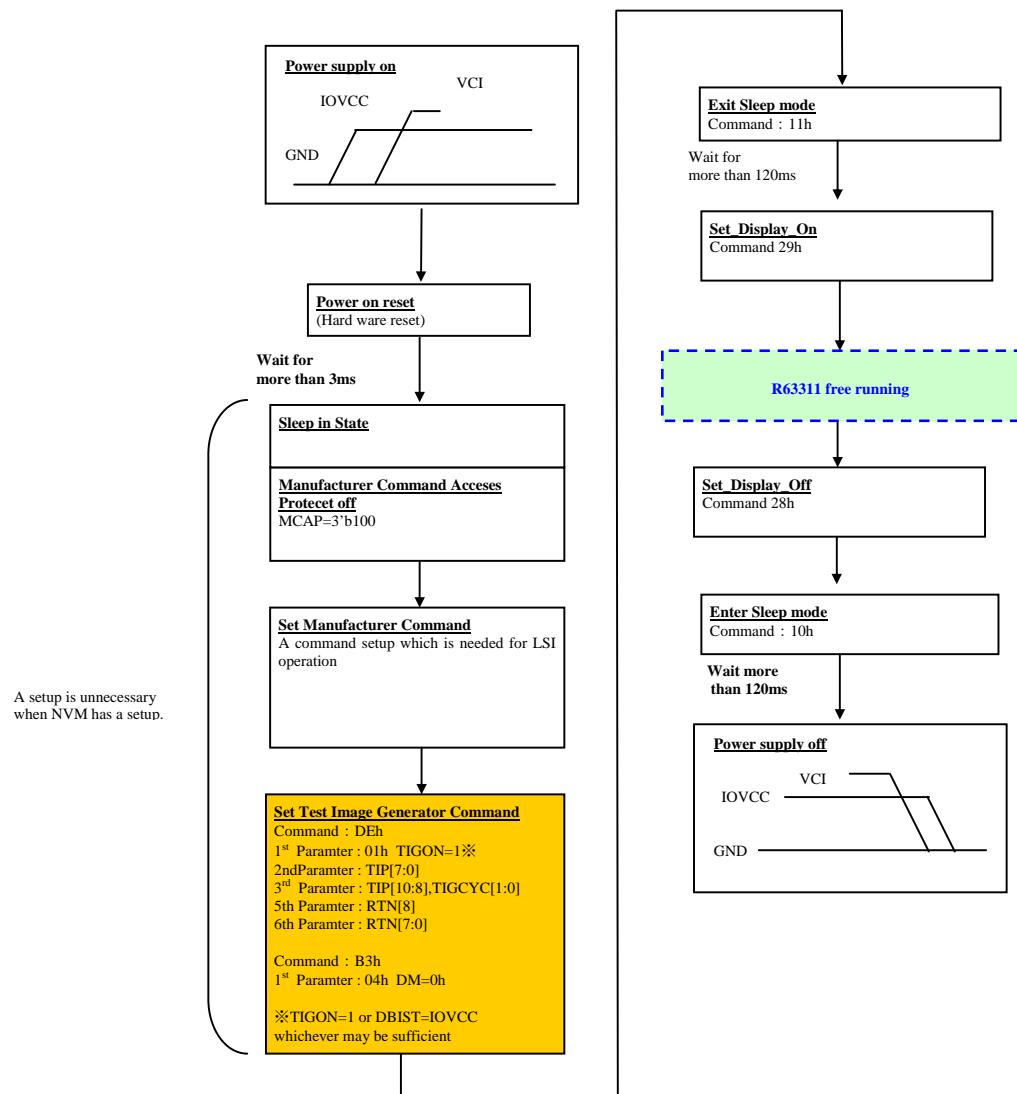
Function Table

RTN	Clocks per Line
'h60 >	Setting inhibited(96clk)
'h61	97clk
'h62	98 clk
:	:
n	n clk
:	:
'hFF	255 clk

(1clk=1RCLK)

Restriction -

Test Image Generator Flow



• **NVM Function : E0h**

E0h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	0	0	E0
1st parameter	1	↑	↑	0	0	0	TEM[0]	0	0	0	NVMAEN	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	NVMFTT	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	NVMVFFLGW/NVMVFLGE		xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

NVMAEN

Description

This register controls NVM accessibility. Refer to "NVM Control" for detail.

Function Table

NVMAEN		NV Memory Access
0		Disable
1		Enable

Restriction

TEM

Description

This register controls output data from LEDPWM.

Function Table

TEM	LEDPEM output
'h0	LEDPWM
'h1	NVM automatical write data verification result. LEDPWM = 0 Verification result is NG LEDPWM = 1 Verification result is OK

Restriction

NVMFTT**Description**

This register controls NVM re-write sequence.
If NVMAEN=1 & NVMFTT=1, NVM start re-write (erase and write) sequence.

Function Table

NVMFTT		NV Memory re-write & Verify operation
0→1		Sequence start
(1→0)		Return to "0" when sequence finish

Restriction**NVMVFFLGER****Description**

NVM execute erase verify operation after NVM erase operation, and return write verify result.
(Erase operation is executed 1st step of NVM re-write sequence.)
This register is read-only, and can not write data.

Function Table

NVMVFFLGER		NV Memory Erase Verification Result
0		Fail
1		Pass

Restriction**NVMVFFLGWR****Description**

NVM execute write verify operation after NVM write operation, and return write verify result.
(Write operation is executed following erase operation.)
This register is read-only, and can not write data.

Function Table

NVMVFFLGWR		NVM Write Verification Result
0		Fail
1		Pass

Restriction

- set_DDB write control : E1h*

E1h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	0	1	E1
1st parameter	1	↑	↑	0	0	0	0	0	0	WCIFID	WCDDDB	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	DDB0[7]	DDB0[6]	DDB0[5]	DDB0[4]	DDB0[3]	DDB0[2]	DDB0[1]	DDB0[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	DDB1[7]	DDB1[6]	DDB1[5]	DDB1[4]	DDB1[3]	DDB1[2]	DDB1[1]	DDB1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	DDB2[7]	DDB2[6]	DDB2[5]	DDB2[4]	DDB2[3]	DDB2[2]	DDB2[1]	DDB2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	DDB3[7]	DDB3[6]	DDB3[5]	DDB3[4]	DDB3[3]	DDB3[2]	DDB3[1]	DDB3[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	DDB4[7]	DDB4[6]	DDB4[5]	DDB4[4]	DDB4[3]	DDB4[2]	DDB4[1]	DDB4[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	DDB5[7]	DDB5[6]	DDB5[5]	DDB5[4]	DDB5[3]	DDB5[2]	DDB5[1]	DDB5[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	0	IFID[6]	IFID[5]	IFID[4]	IFID[3]	IFID[2]	IFID[1]	IFID[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

WCDDDB

Description

This register controls accessibility of A1h: read_DDB_Start register.

Function Table

WCDDDB	Notes
0	DDB access is disable. *Please set WCDDDB=0 except NVM writing
1	DDB access is enable. *Data setted DDB register are written to NVM.

Restriction

WCIFID**Description**

This register set the write control of IFID register.

Function Table

WCIFID	Operation
0	This register disables write to IFID. Values loaded from NVM are retained even if this parameter is written.
1	This register enables write to IFID. To set NVM write data, write 1 in WCIFID.

Restriction -

DDB0, DDB1, DDB2, DDB3, DDB4, DDB5**Description**

This register is to store A1h: read_DDB_Start and 04h: RDDIDIF. Setted data to this register are read by A1h: read_DDB_Start command and 04h: RDDIDIF command.

Function Table

The parameter order of A1h: read_DDB_start and DDBx and 04h: RDDIDIF.

A1h: read_DDB_start 04h: RDDIDIF	DDBx register
Dummy parameter	-
1 st parameter: ID1[15:8]	DDB0
2 nd parameter: ID1[7:0]	DDB1
3 rd parameter: ID2[15:8]	DDB2
4 th parameter: ID2[7:0]	DDB3
5 th parameter: ID3[7:0]	DDB4
6 th parameter: ID4[7:0]	DDB5
7 th parameter: IFID[6:0]	-
8 th parameter: 8'hFF	-

Restriction -

IFID**Description**

This register is for setting Slave address of I²C.

Function Table

IFIDEN	IFID	I2C Slave Address
0	*	don't care
1	IFID	IFID

Restriction

If any data are written to NVM, value of this register is "0"
(Do not corresponded General Call Address)

- *ReadID write control : E2h*

E2h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	1	0	E2
1st parameter	1	↑	↑	0	0	0	0	0	0	0	WCRDID	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	RDID1[7]	RDID1[6]	RDID1[5]	RDID1[4]	RDID1[3]	RDID1[2]	RDID1[1]	RDID1[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	RDID2[7]	RDID2[6]	RDID2[5]	RDID2[4]	RDID2[3]	RDID2[2]	RDID2[1]	RDID2[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	RDID3[7]	RDID3[6]	RDID3[5]	RDID3[4]	RDID3[3]	RDID3[2]	RDID3[1]	RDID3[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

WCRDID

Description

This register controls access to RDIDx register.

Please use this register in case of skipping NVM re-write.

Function Table

WCEXTID	Operation
0	NVM re-write is disable. If value written to NVM and load from NVM, RDIDx value is kept.
1	NVM re-write is enable. If user wants to re-write NVM data, please set WCRDID=1 before NVM re-write sequence.

Restriction

RDID1,RDID2,RDID3

Description

This register is to store DAh,DBh,DCh. Setted data to this register are read by DAh,DBh,DCh.

Function Table

Read register	Write register(E2h)
DAh : RDID1	RDID1
DBh : RDID2	RDID2
DCh : RDID3	RDID3

Restriction

- NV Memory Load Control : E3h

E3h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	1	1	E3
1st parameter	1	↑	↑	NVMLD[7]	NVMLD[6]	NVMLD[5]	NVMLD[4]	NVMLD[3]	NVMLD[2]	NVMLD[1]	NVMLD[0]	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

NVMLD

Description

These registers set commands used to load data from NVM during each sequence.

Function Table

NVMLD[x]	Operation
0	Data is not loaded from NVM by command. The setting values before data is loaded are not updated.
1	Data is loaded from NVM by command. The setting values before data is loaded are updated.

Assignment of Command controlled by NVMLD command

NVMLD command	command controlled NVM load	
Unconditional	E3h	
NVMLD[0]	B3h, B4h, B6h, E1h, E2h,E9h	ID Read, IF Setting
NVMLD[1]	B8h, B9h, BAh, BBh, CAh, CEh, CFh, D8h,D9h,DDh	BLC, TIG , GPO , Outline Sharpening Control. Color enhancement Control, Contrast Optimize
NVMLD[2]	C0h, C1h, C2h, C3h, C4h, C6h, CBh, CCh	Panel Driving, Panel I/F Setting
NVMLD[3]	C7h, C8h, C9h	Gamma Setting
NVMLD[4]	D0h, D1h, D2h, D3h, D6h, D7h	Power Setting
NVMLD[5]	D5h	VCOM/VREG Setting
NVMLD[6]	DEh	Test Omage Generator Setting
NVMLD[7]	ECh,EDh,EEh,EFh	Special function setting

Restriction

- *Test : E4h*

E4h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	0	0	E4
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : E4h*

E5h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	0	1	E5
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	1	0	0	0	1	0	xx
init	-	-	-	0	0	1	0	0	0	1	0	22
3rd parameter	1	↑	↑	1	0	1	0	1	0	1	0	xx
init	-	-	-	1	0	1	0	1	0	1	0	AA
4th parameter	1	↑	1	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : E6h*

E6h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	1	0	E6
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : E7h*

E7h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	1	1	E7
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : E8h*

E8h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	0	0	E8
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
11th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : E9h*

E9h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	0	1	E9
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : ECh*

ECh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	0	0	EC
1st parameter	1	↑	↑	0	1	0	0	0	0	0	0	xx
init	-	-	-	0	1	0	0	0	0	0	0	40
2nd parameter	1	↑	↑	0	0	0	1	0	0	0	0	xx
init	-	-	-	0	0	0	1	0	0	0	0	10

- *Test : EDh*

EDh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	0	1	ED
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : EEh*

EEh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	1	0	EE
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	1	1	0	0	1	0	xx
init	-	-	-	0	0	1	1	0	0	1	0	32

- Test : EFh

EFh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	1	1	EF
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
10th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
11th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
12th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- Test : F3h

F3h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	1	F3
1st parameter	1	↑	↑	0	0	0	0	0	0	1	0	xx
init	-	-	-	0	0	0	0	0	0	1	0	02
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	1	0	0	1	0	0	xx
init	-	-	-	0	0	1	0	0	1	0	0	24
4th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : FAh*

FAh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FA
1st parameter	1	↑	1	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : FBh*

FBh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	1	FB
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : FDh*

FDh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	1	FD
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

- *Test : FEh*

FEh	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	1	0	FE
1st parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
5th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
6th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
7th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
8th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00
9th parameter	1	↑	↑	0	0	0	0	0	0	0	0	xx
init	-	-	-	0	0	0	0	0	0	0	0	00

System Interface Configuration (MIPI DBI Type C)

Outline

The RSP LCD driver supports serial interface DBI Type C (Option 1 and Option 3). Nine/Eight bit data, transmitted from host processor to the RSP LCD driver is stored in command register(CDR) or parameter register(PR), and then the RSP LCD driver start internal operation.

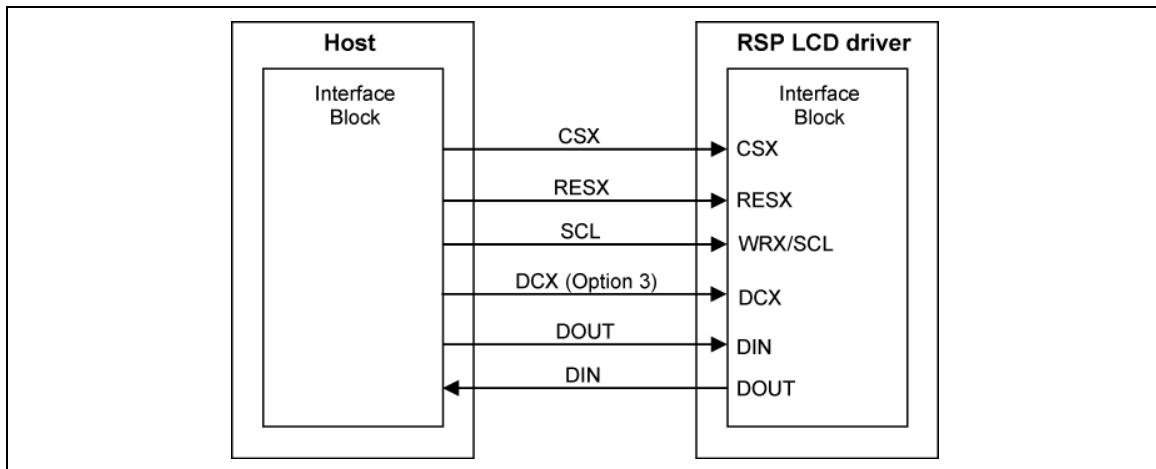
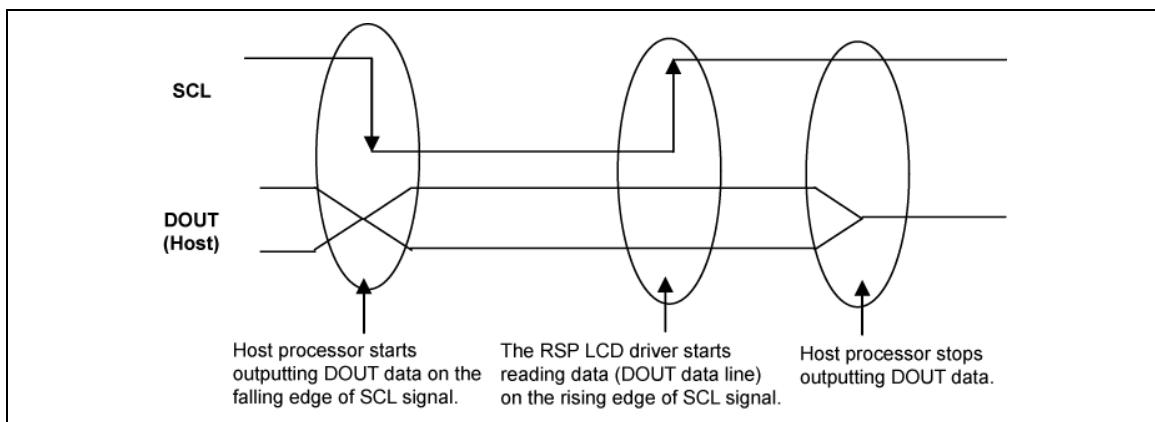


Figure 18 Example of DBI Type C

Write Cycle Sequence

In write cycle, data and/or command are written to the RSP LCD driver via the interface with the host processor. Each step of write cycle sequence (SCL high, SCL low, SCL high) comprises two or three control signals (CSX, SCL, (DCX)) and DOUT data. During a write cycle sequence, the host processor outputs data while the RSP LCD driver accepts data at the rising edge of SCL. See next figures for write cycle sequence.

When DCX is “0” (Option 3), DOUT data is command. When DCX is “1” (Option 3), DOUT data is command parameter. See the figure below for the write cycle sequences.



Note: SCL is not a synchronous signal (can be halted).

Figure 19 Write Cycle Sequence

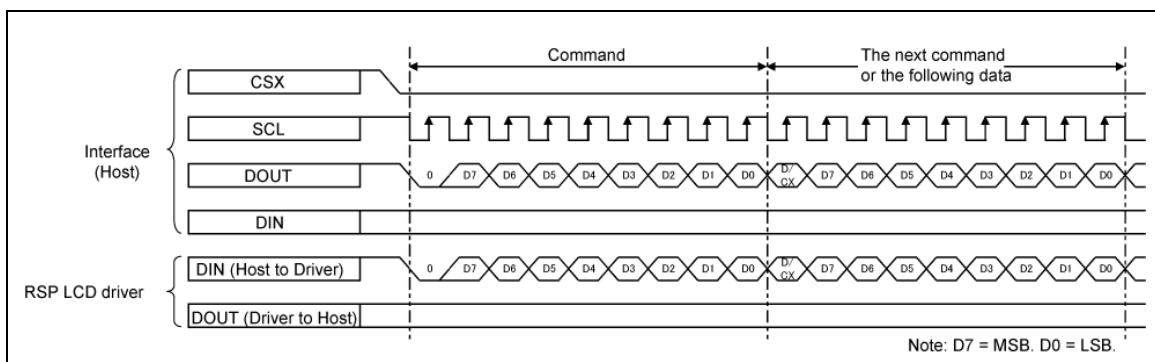


Figure 20 Example of Serial Interface Write Sequence (Option 1)

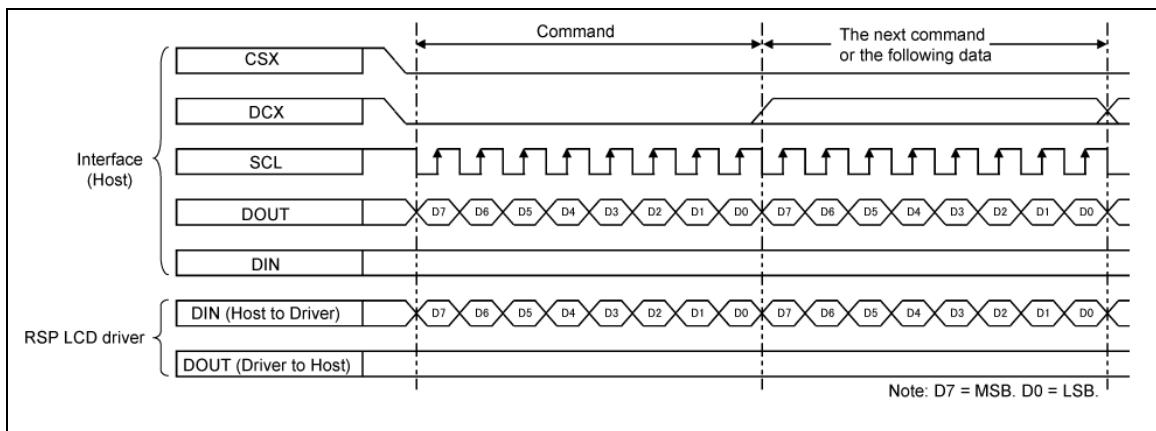
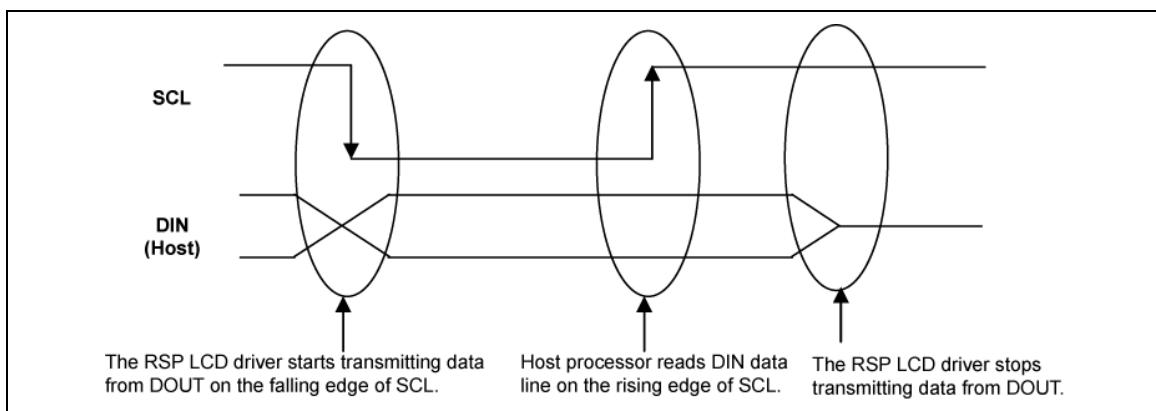


Figure 21 Example of Serial Interface Write Sequence (Option 3)

Read Cycle Sequence

In read cycle, data and/or commands are read from the RSP LCD driver via the interface with the host processor. The RSP LCD driver transmits data from DOUT to the host processor on the falling edge of SCL. The host processor reads the data on the rising edge of SCL. See next figure for the read cycle sequence.



Note: SCL is not a synchronous signal (can be halted).

Figure 22 Read Cycle Sequence

DCS Read Command

The first byte of read data following a command is dummy data irrespective of parameter. A pause can end the read cycle sequence.

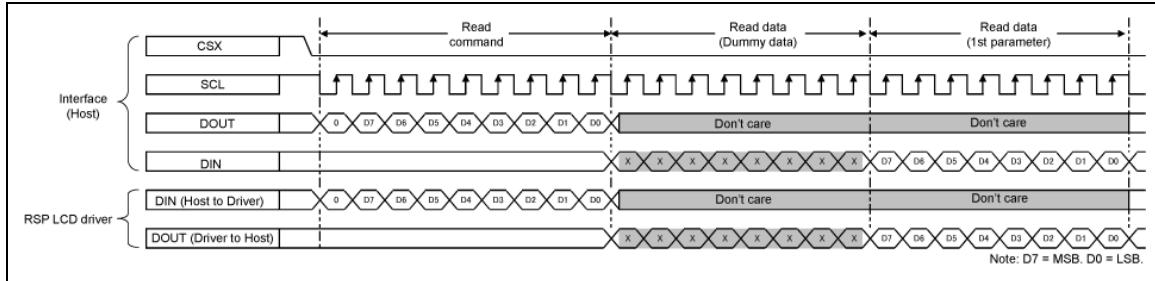


Figure 23 Example of MIPI DBI Type C Read Cycle Sequence (Option 1)

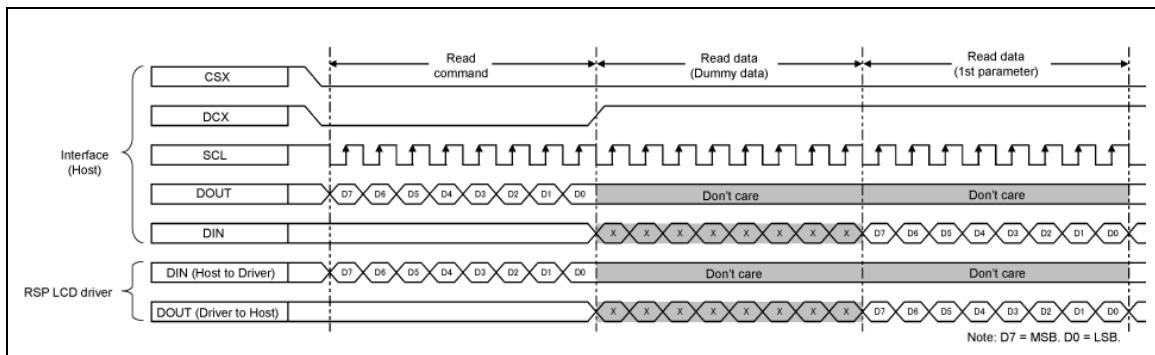


Figure 24 Example of MIPI DBI Type C Read Cycle Sequence (Option 3)

Manufacturer Command Read (Using Read Mode In and read Mode Out Command)

The first byte of read data following a command is dummy data irrespective of parameter. After a pause, inoutting Read Mode Out command (F6h) can end the read cycle sequence.

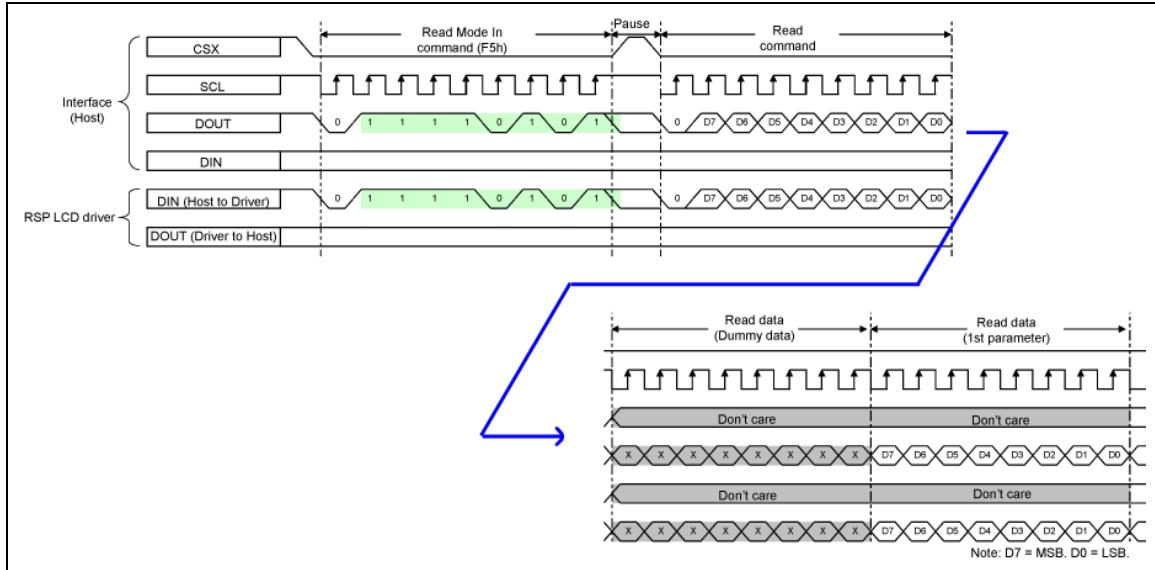


Figure 25 Example of MIPI DBI Type C Read Cycle Sequence Using Read Mode In Command (Option 1)

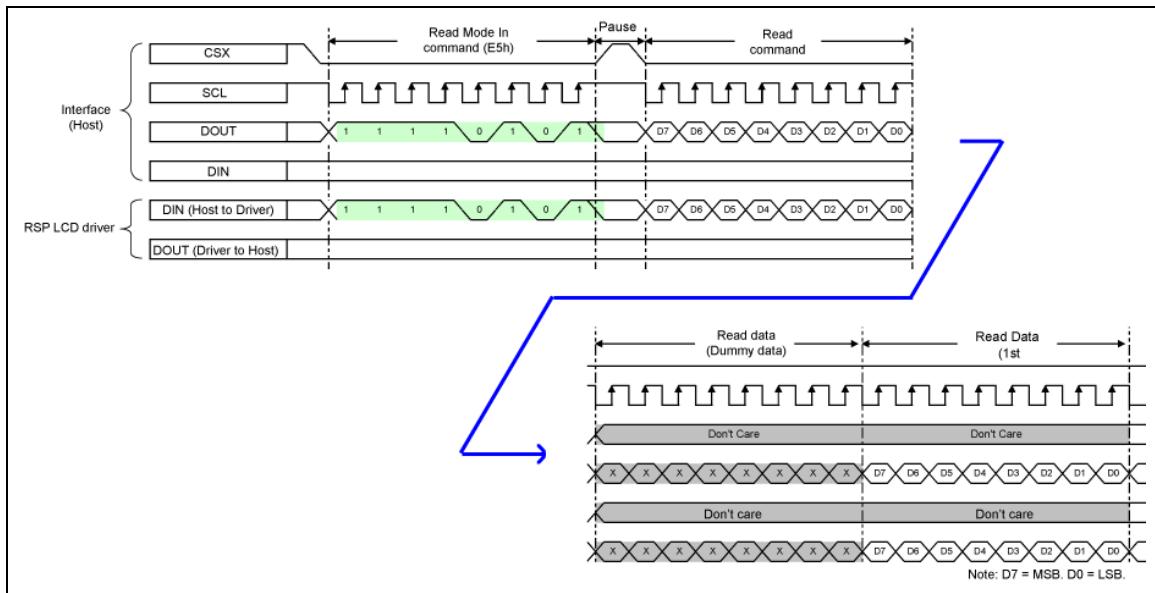


Figure 26 Example of MIPI DBI Type C Read Cycle Sequence Using Read Mode In Command (Option 3)

Data Transfer Break/Pause

Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the RSP LCD driver, the command parameters sent to the RSP LCD driver before the break occurs are stored in the register of the RSP LCD driver when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the RSP LCD driver. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupt command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

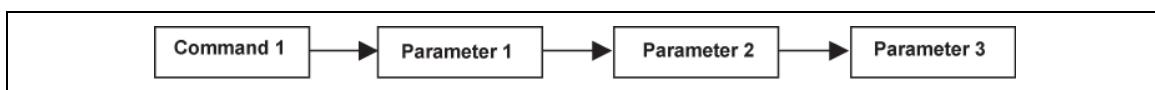


Figure 27 Normal Data Transfer

While parameter commands are being sent, if a break occurs before sending the last parameter, those parameters sent after the break are disregarded. For example, a break is caused by other command input.

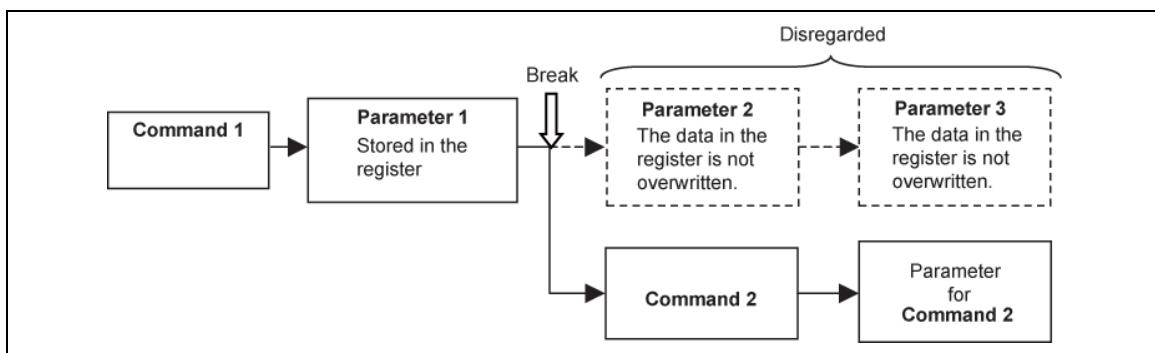


Figure 28 Broken Data Transfer

Data Transfer Pause

The RSP LCD driver does not support pause operation during the Type C write sequence and read sequence. After transfer of command/parameter ends, write operation resumes from command/parameter right before a stop of transfer if transfer is stopped by setting CSX to “High.” Next transfer should start with command (CSX is “Low”).

Data Format

For the color formats supported by the RSP LCD driver, see “Data Format.”

System Interface Configuration (I²C)

The RSP LCD driver supports I²C bus interface as serial interface. Data is transferred via serial transmit/receive data bus (DIN) and serial transfer clock line (SCL). In the I²C bus system, the RSP LCD driver is a bidirectional slave device.

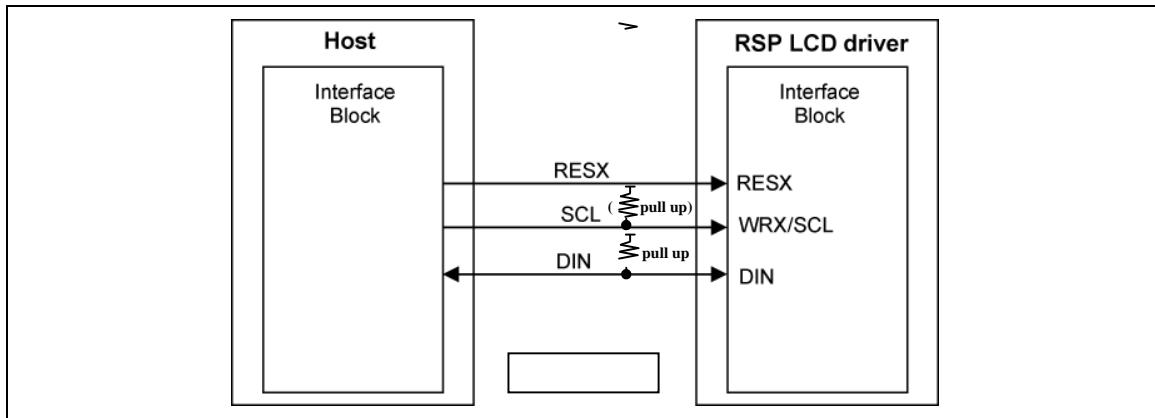


Figure 29 Example of I²C

Note: To connect the interface bus to a device, start data transfer according to a slave address from one specified in other devices.

First Byte of I²C Bus

Table 54

First byte	Start	1	2	3	4	5	6	7	8	9
		I ² C slave address							R/W	ACK
When an ID code default is written	0	0	0	0	0	0	0	0	R/W	ACK/NACK
When an ID code is used	Start	I2CID [6]	I2CID [5]	I2CID [4]	I2CID [3]	I2CID [2]	I2CID [1]	I2CID [0]	R/W	ACK/NACK

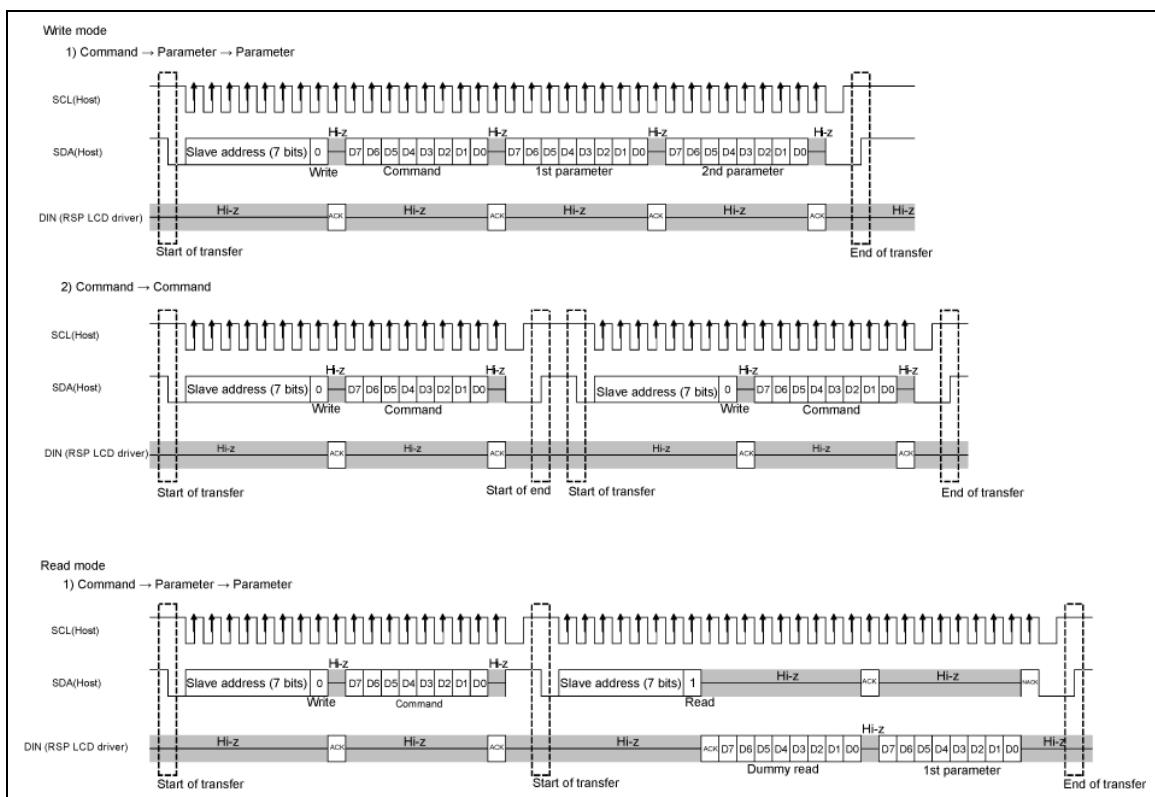
Table 55

R/W	Function
0	Command write
1	Command read

Table 56

ACK	Function
0	ACK
Hi-Z	NACK

The 7-bit data after the start of transfer is treated as an I²C slave address. An ID code (I2CID) stored in NVM beforehand is used as a slave address. If a slave address transferred by host corresponds to the ID code, the subsequent data transfer is treated as access to the RSP LCD driver. The RSP LCD driver returns ACK to host by setting the ninth bit to “L” (ACK operation). If a slave address transferred by host does not correspond to the ID code, the RSP LCD driver does not set the ninth bit to “L”. The bit is set to “H” by an external pull-up resistor.

**Figure 30 Serial Data Transfer via I²C Bus Interface**

System Interface Configuration (MIPI DSI)

The DSI incorporated in the RSP LCD driver complies with the following standards:

MIPI DSI: Version 1.01.00r11 21-Feb-2008

MIPI D-PHY: Version 1.00.00 14-May-2009

MIPI DCS: Version 1.01.00

(1) Basic DSI Specification

- Video Mode supported
- One line data must be sent by one packed pixel stream packet.

Note: For the number of lanes and the data rate, see “Block Function” and “Electrical Characteristics.”

(2) DSI System Configuration

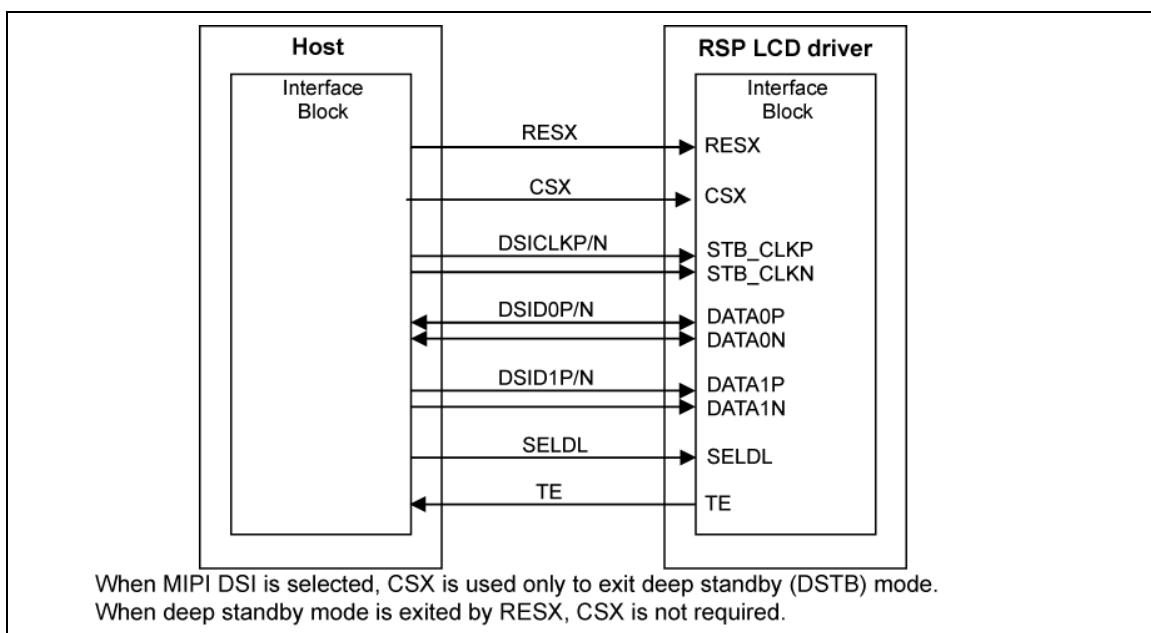


Figure 31 Example of DSI

Table 57 Interface Type (IM Setting) – Color Format

Type	IM2-0	Data pin	Color format	MIPI Spec.	RSP LCD driver support
DSI	110	D0+/-, D1+/-	16bpp	Yes	Yes
			18bpp	Yes	Yes
			24bpp	Yes	Yes

Yes: Supported

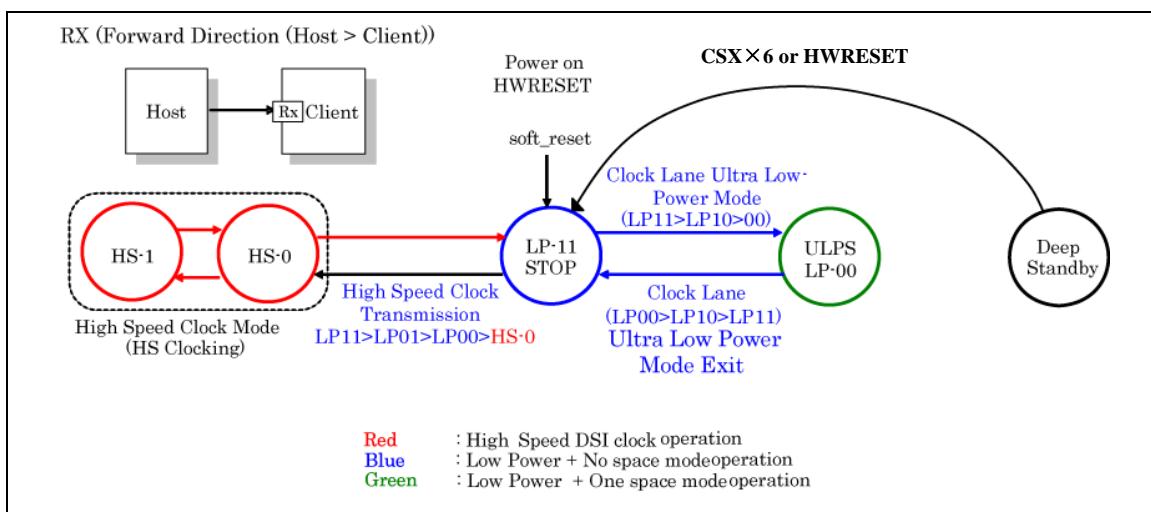
No: Unsupported

(3) Lane State Definition**Table 58 Lane State Description**

State code	Line voltage levels		High speed	Low power	
	Dp-line	Dn-line		Burst mode	Control mode
HS-0	HS Low	HS High	Differential-0	1	1
HS-1	HS High	HS Low	Differential-1	1	1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	2

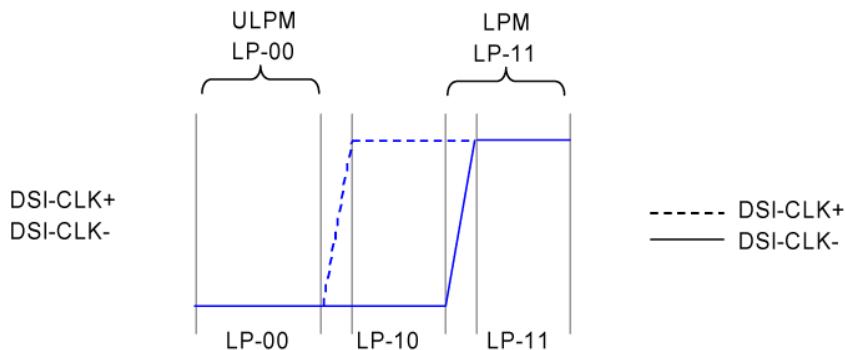
Notes:

1. During high-speed transmission, the low power receivers observe LP-00 on the lines.
2. If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11).

(4) DSI-CLK Lane**Figure 32 Clock Lane State Diagram**

1) Low Power Mode (LP-11: STOP)

- Power on, HWREST
The data lanes and clock lane should be in LP-11 state during power on and HWRESET sequences.
- ULPM →(LP00>LP10>LP11) → LP-11(LPM)



- High Speed Clock Mode (HSCM) → (HS-0) → LP-11(LPM)

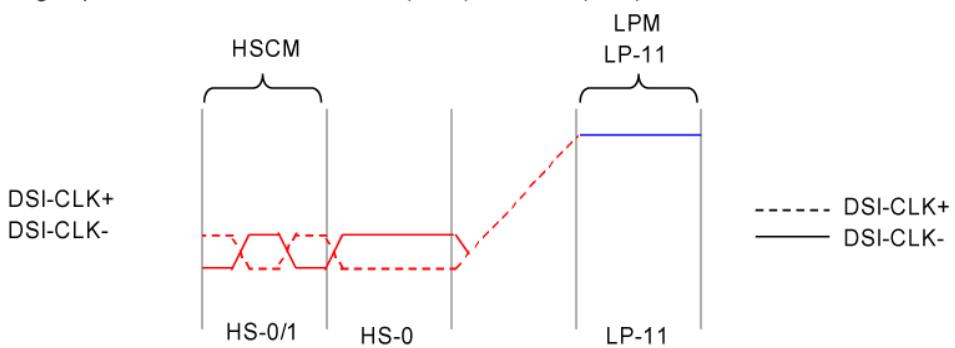


Figure 33 Switching the Clock Lane between Clock Transmission and Low Power Mode 1

2) Ultra Low Power Mode (LP-00: ULPM)

- Ultra Low Power Mode (LP-00:ULPM)
 - LP-11(LPM) → LP-10 → LP-00(ULPM)

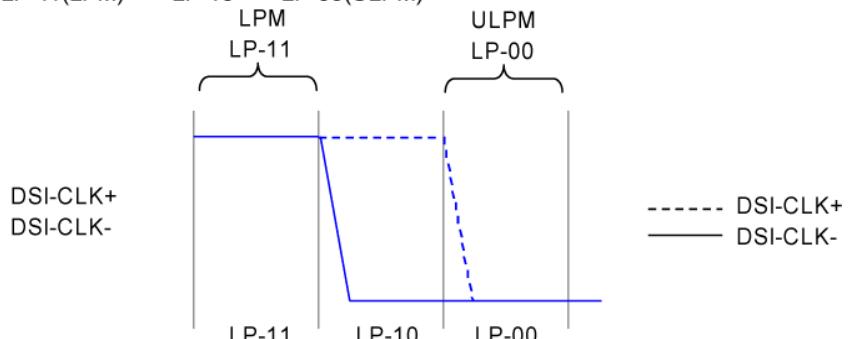


Figure 34 Switching the Clock Lane between Clock Transmission and Low Power Mode 2

3) High Speed Clock Mode

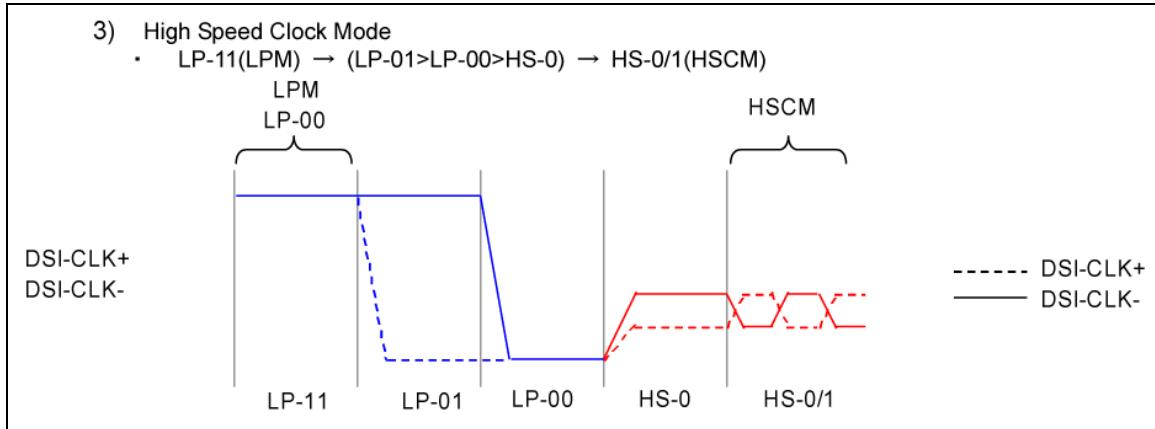


Figure 35 Switching the Clock Lane between Clock Transmission and Low Power Mode 3

4) High Speed Clock Burst

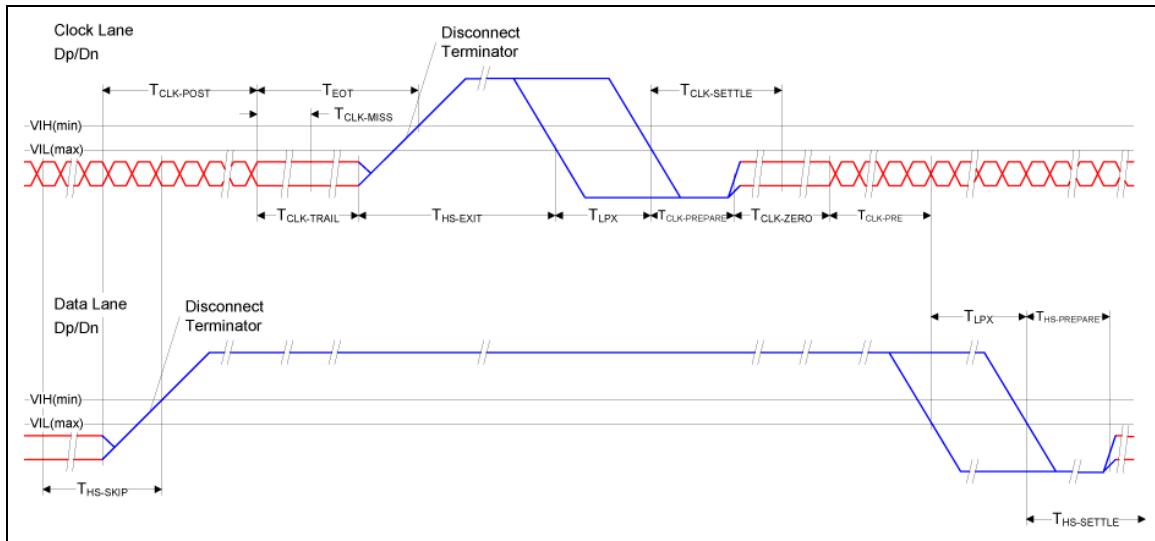


Figure 36 Switching the Clock Lane between Clock Transmission and Low Power Mode 4

(5) DSI-D0 Data Lane

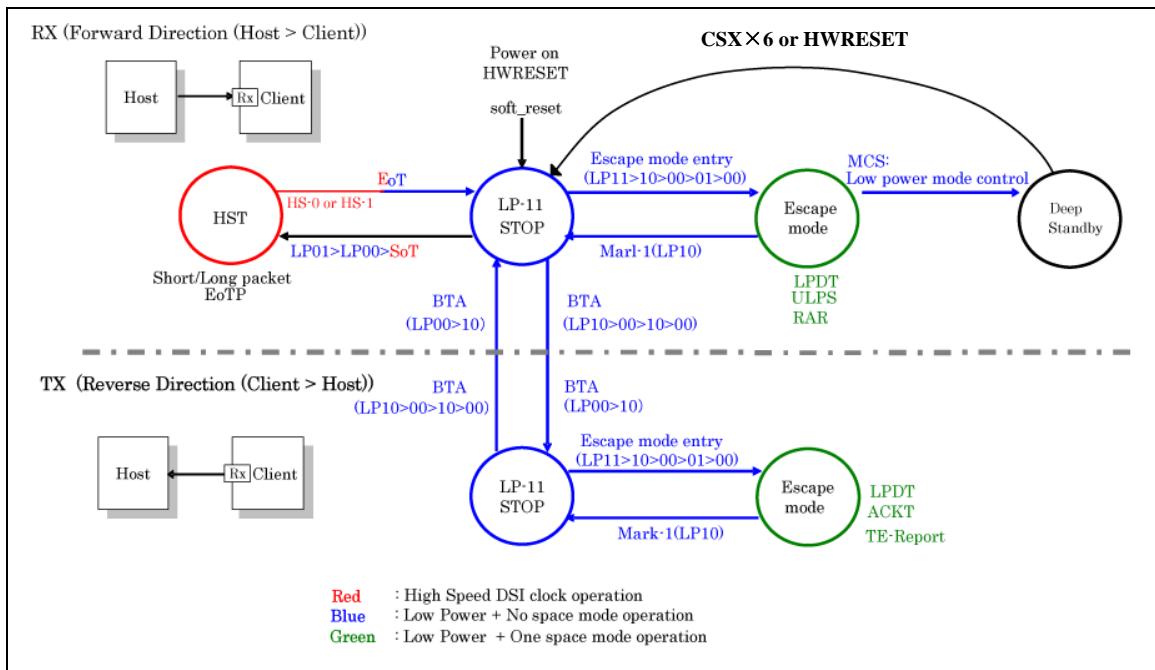


Figure 37 DSI-D0 Data Lane State Diagram

Table 59 Data Lane Operating Modes

No.	Description	Operation code	Note
1	High Speed Data Transmission Burst	LP-11 > L-P01 > LP-00	
2	Escape mode entry	LP-11 > LP-10 > LP-00 > LP-01 > LP-00	
3	Turnaround	LP-11 > LP-10 > LP-00 > LP-10 > LP-00	1
4	Exit Escape mode (Mark-1)	L-10	
5	Deep Standby Mode	DSTB=1	2
6	Exit Deep Standby Mode	CSX x 6 or HWRESET	3

- Note:
1. Before Turnaround operation, DBI Packet must be sent.
 2. DSTB must be sent by Escape mode in Sleep mode.
 3. After exiting from the Deep Standby Mode, all of commands are reset.

1) Power On, HWRESET → LP-11

The data lanes and clock lane should be in the LP-11 state during power-on, HWRESET, and soft_reset sequences.

2) Escape Mode

- Escape mode entry
- Mark-1 (exit Escape mode)

Table 60 Escape Entry Code

No.	Symbol	Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)	R63311 implementation		Note
					LP-RX	LP-TX	
1	LPDT	Low Power Data Transmission	Mode	1110_0001	Yes	Yes	
2	ULPS	Ultra-Low Power State	Mode	0001_1110	Yes	No	
3	UDF1	Undefined-1	Mode	1001_1111	No	No	
4	UDF2	Undefined-2	Mode	1101_1110	No	No	
5	RAR	Remote Application Reset	Trigger	0110_0010	Yes	No	See note.
6	TER	TE-Report	Trigger	0101_1101	No	No	
7	ACKT	Unknown-4 (Acknowledge Trigger)	Trigger	0010_0001	No	Yes	
8	UNK5	Unknown-5	Trigger	1010_0000	No	No	

Note: DSI circuit is reset by Remote Application Reset.

3) Escape Mode (Host >Client): Low Power Data Transmission (LPDT)

An example of DSI read sequence by LPDT is shown below.

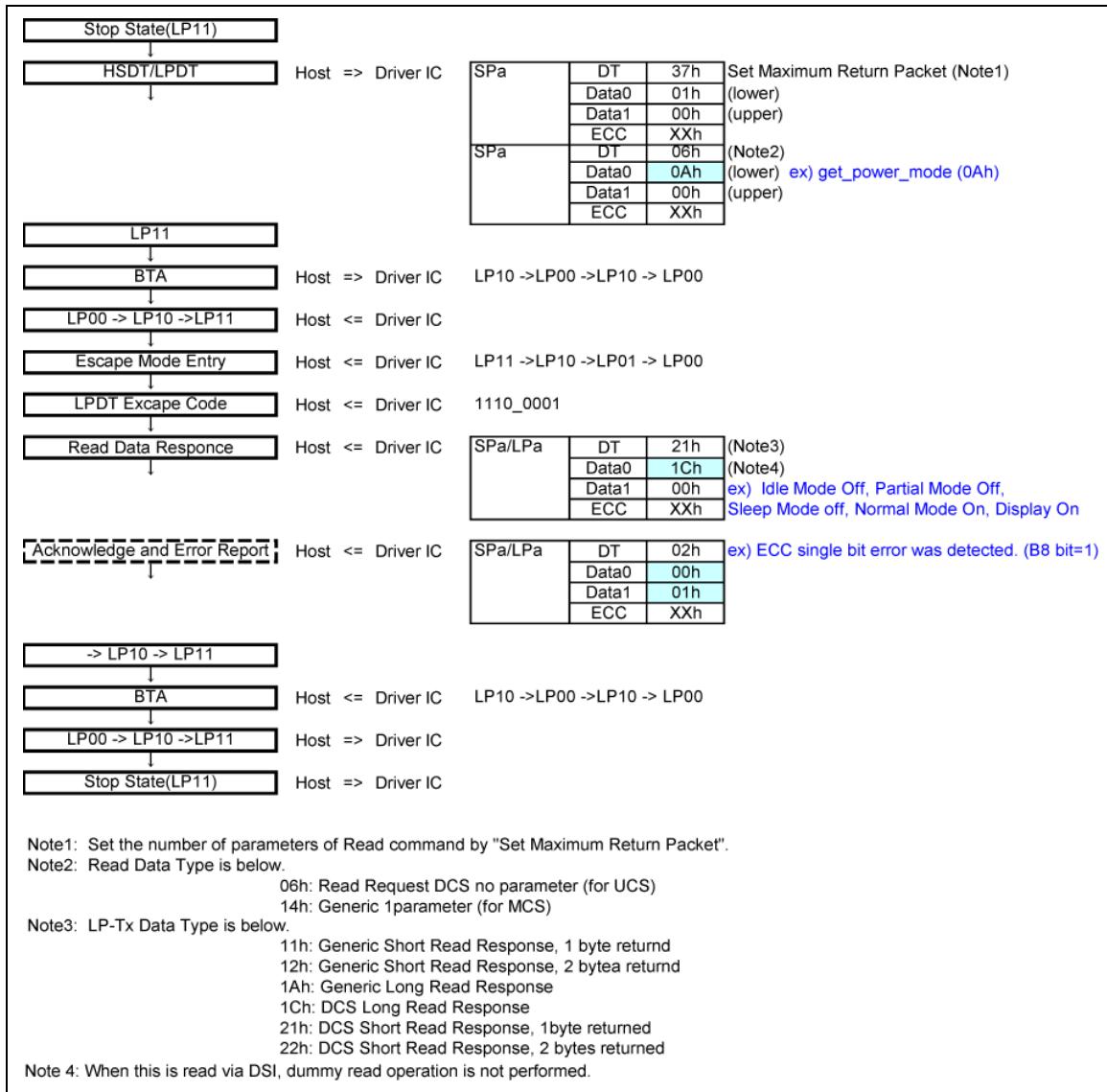


Figure 38

4) Escape Mode (Host>Client): Ultra Low Power State (ULPS)**5) Escape Mode (Host>Client): Remote Application Reset (RAR)****6) Escape Mode (Client>Host): Tearing Report (TER)**

The RSP LCD driver supports TE Report function. Procedures are as follows:

Host to Client: send set_tear_on of DCS

Host to Client: send BTA

Client to Host: send Acknowledge Trigger

Client to Host: send BTA

Host check Error Report

Host to Client: send BTA

Client to Host: send TE Report when TE occurred at the line of set_scan_line

Client to Host: send BTA

Host to Client: send image data by HST

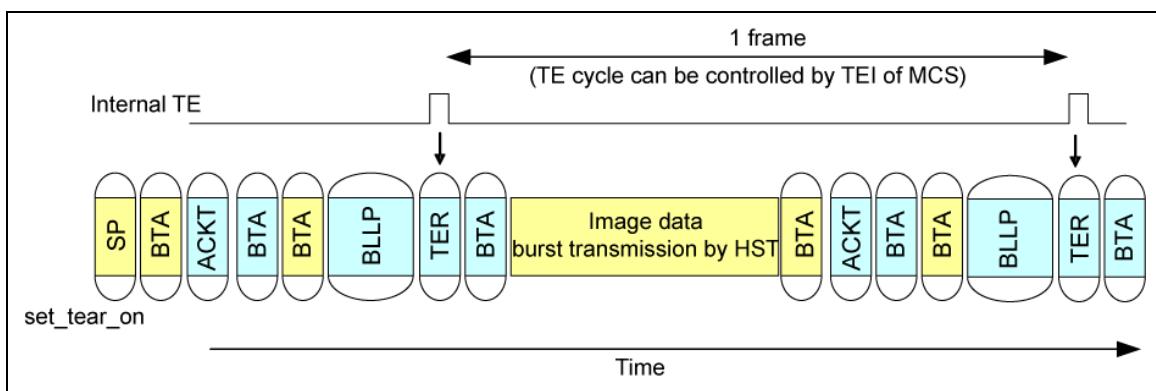


Figure 39

7) Escape Mode (Client > Host): Acknowledge Trigger (ACKT)**8) High Speed Data Transmission (HST)****9) Bus Turnaround (Host>Client) (BTA)****10) Bus Turnaround (Client>Host) (BTA)**

(6) Packet Level Communication

1) Short Packet (SPa) Structure

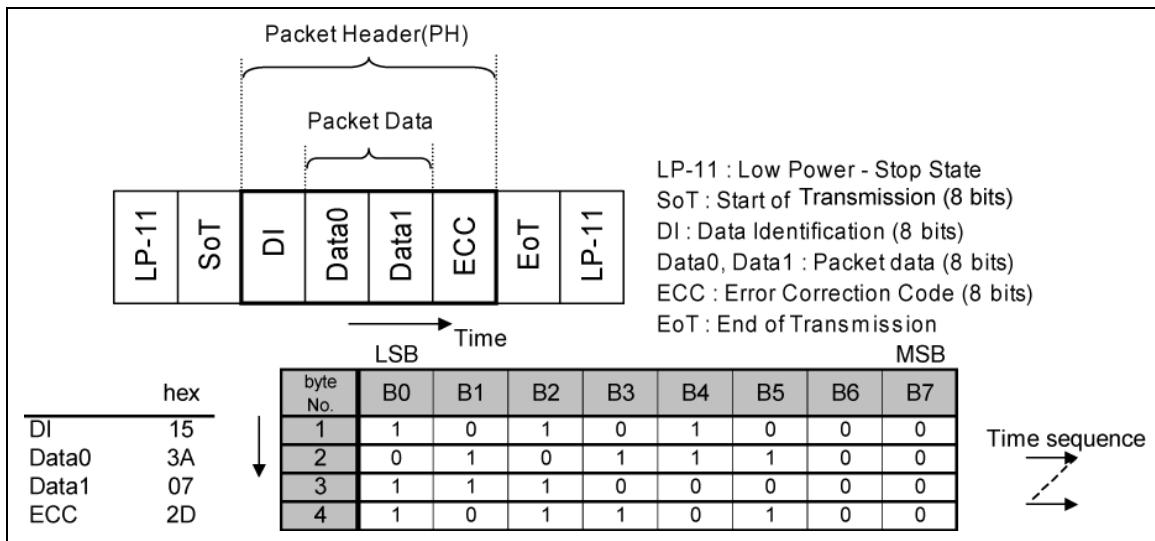


Figure 40 Example of Short Packet (SPa) (DCS WRITE, 1 Parameter)

2) Long Packet (LPa) Structure

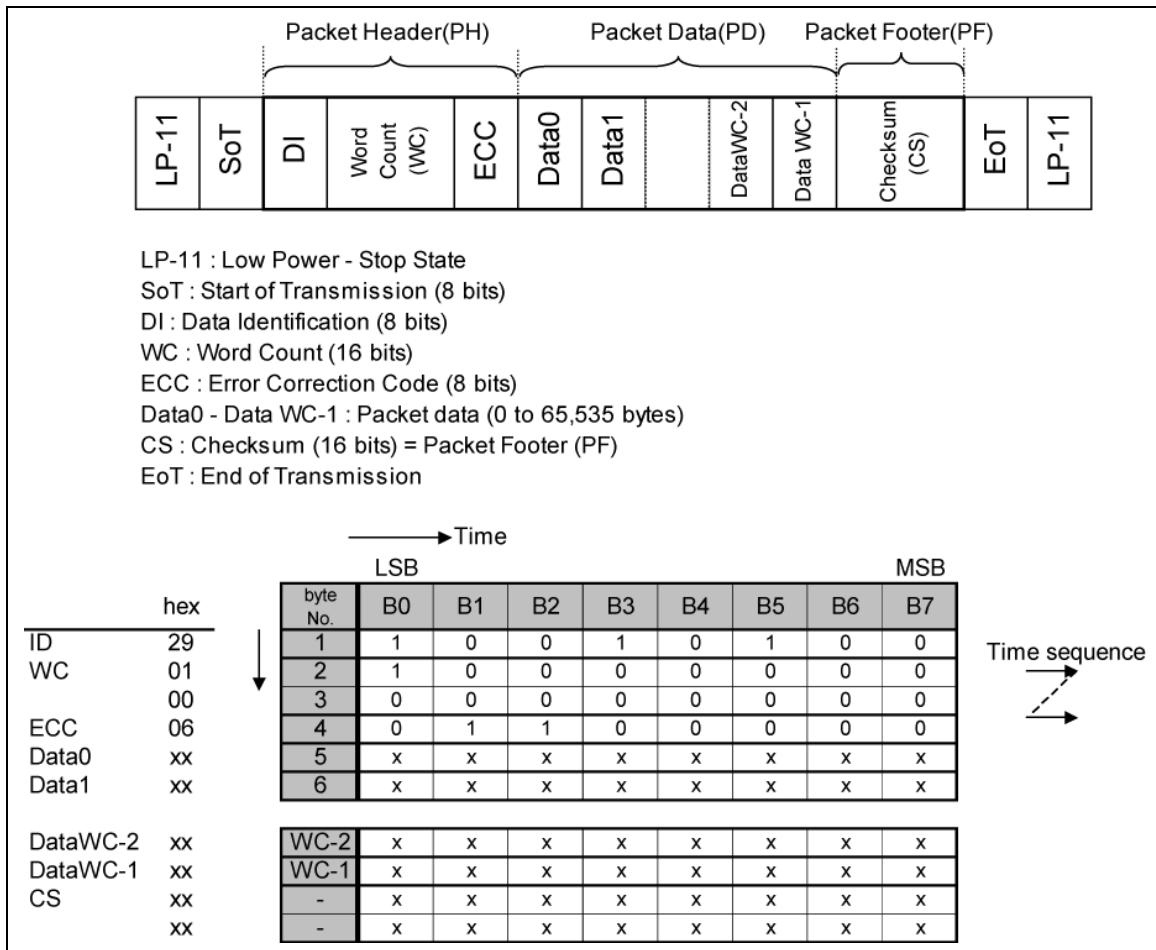


Figure 41

3) Multiple Packet Sending

In LP-11 state, multiple Short Packets (SPa) and Long Packets (LPa) can be received between SoT and EoT.

LP-11 → SoT → SPa → SPa → EoT

LP-11 → SoT → SPa → LPa → EoT

LP-11 → SoT → LPa → LPa → EoT

LP-11 → SoT → LPa → SPa → EoT

LP-11 → SoT → Combination of the above methods → EoT

(7) Data Identification (DI)**1) Virtual Channel (VC)**

The RSP LCD driver supports Virtual Channel(VC). The data of VC is setting by 2bits, and refer data of DSIVC[1:0]. The data of DSIVC[1:0] are stored to NVM.

2) Data Type (DT)

If Data Type undefined in the MIPI DSI specification is received, the subsequent data cannot be received. Transmit data again after checking that the RSP LCD driver is in LP-11 state by Error Report. If Data Type unsupported in the RSP LCD driver is received, it is regarded as NOP, and the result is not reflected on the Error Report.

Table 61

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
B7 (0)	B6 (0)	B5	B4	B3	B2	B1	B0

Table 62 RSP LCD Driver Rx Data Type List

Data Type	Description	Packet size	DBI packet	DPI packet	Command mode Implementation	Video mode Implementation	Note
01h	Sync Event, V Sync Start	Short		Yes	No	Yes	4
11h	Sync Event, V Sync End	Short		Yes	No	No	4
21h	Sync Event, H Sync Start	Short		Yes	No	Yes	4
31h	Sync Event, H Sync End	Short		Yes	No	No	4
08h	End of Transmission packet (EoT)	Short			Yes	Yes	
02h	Color Mode (CM) Off Command	Short		Yes	No	No	4
12h	Color Mode (CM) On Command	Short		Yes	No	No	4
22h	Shut Down Peripheral Command	Short		Yes	No	Yes	
32h	Turn On Peripheral Command	Short		Yes	No	Yes	
03h	Generic Short WRITE, no parameters	Short	Yes		No	No	4
13h	Generic Short WRITE, 1 parameter	Short	Yes		Yes	Yes	1, 2
23h	Generic Short WRITE, 2 parameters	Short	Yes		Yes	Yes	1, 2
04h	Generic READ, no parameters	Short	Yes		No	No	1, 4
14h	Generic READ, 1 parameter	Short	Yes		Yes	Yes	
24h	Generic READ, 2 parameters	Short	Yes		Yes	Yes	1, 2
05h	DCS WRITE, no parameters	Short	Yes		Yes	Yes	1, 2
15h	DCS WRITE, 1 parameter	Short	Yes		Yes	Yes	1, 2
06h	DCS READ, no parameters	Short	Yes		Yes	Yes	1, 2
37h	Set Maximum Return Packet Size (default 0001h)	Short	Yes		Yes	Yes	
09h	Null Packet, no data	Long			Yes	Yes	
19h	Blanking Packet, no data	Long		Yes	No	Yes	4
29h	Generic Long Write	Long	Yes		Yes	Yes	
39h	DCS Long Write/write_LUT Command Packet	Long	Yes		Yes	Yes	
0Eh	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long		Yes	No	No	3
1Eh	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	No	No	3
2Eh	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	No	Yes	3
3Eh	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long		Yes	No	Yes	3
other	All unspecified codes are reserved	-	-	-	-	-	

Table 63 RSP LCD Driver LP-Tx Data Type List

Data Type	Description	Packet size	RSP LCD driver (LP-Tx) Implementation	Note
00h-01h	Reserved	—	—	
02h	Acknowledge with Error Report	Short	Yes	
03h-07h	Reserved	—	—	
08h	End of Transmission packet (EoT)	Short	No	5
09h-10h	Reserved	—	—	
11h	Generic Short READ Response, 1 byte returned	Short	Yes	
12h	Generic Short READ Response, 2 bytes returned	Short	Yes	
13h-18h	Reserved	—	—	
1Ah	Generic Long READ Response	Long	Yes	
1Bh	Reserved	—	—	
1Ch	DCS Long READ Response	Long	Yes	
1Dh-20h	Reserved	—	—	
21h	DCS Short READ Response, 1 byte returned	Short	Yes	
22h	DCS Short READ Response, 2 bytes returned	Short	Yes	
23h-28h	Reserved	—	—	
29h-3Fh	Reserved	—	—	

- Notes:
1. Generic Command is Manufacturer Command.
DCS Command is User Command.
 2. Generic XXX 1 parameter is Manufacturer Command + 1 byte (all "0").
Generic XXX 2 parameter is Manufacturer Command + 1 parameter.
DCS XXX no parameter is User Command + 1 byte (all "0").
DCS XXX 1 parameter is User Command + 1 parameter.
 3. Line data must be sent by one packet.
 4. Any packet with data type that MIPI Specification defines and the RSP LCD driver doesn't support is treated as NOP.
 5. Defined in MIPI DSI Specification (used for HS transmission).
 6. Note that the RSP LCD driver will stop to receive as soon as it detects any packet with data type that the MIPI Specification doesn't define.
 7. Using DSI Data Type (22h and 32h) with DCS Commands (11h, 10h, 28h, and 29h) is prohibited.

(8) Word Count (WC) on Long Packet (LPa)

Word Count (WC) = 2 bytes: The number of packet data on Long Packet (0 to 65,535 bytes)

(9) Error Correction Code (ECC)

ECC detects 1-bit errors or multiple-bit errors in each Packet Header. ECC is performed on the following:

- Short Packet: DI, Data0, Data1, and ECC
 - Long Packet: DI, WC (2 bytes), and ECC

(10) Command Mode Pixel Data Format (PD)

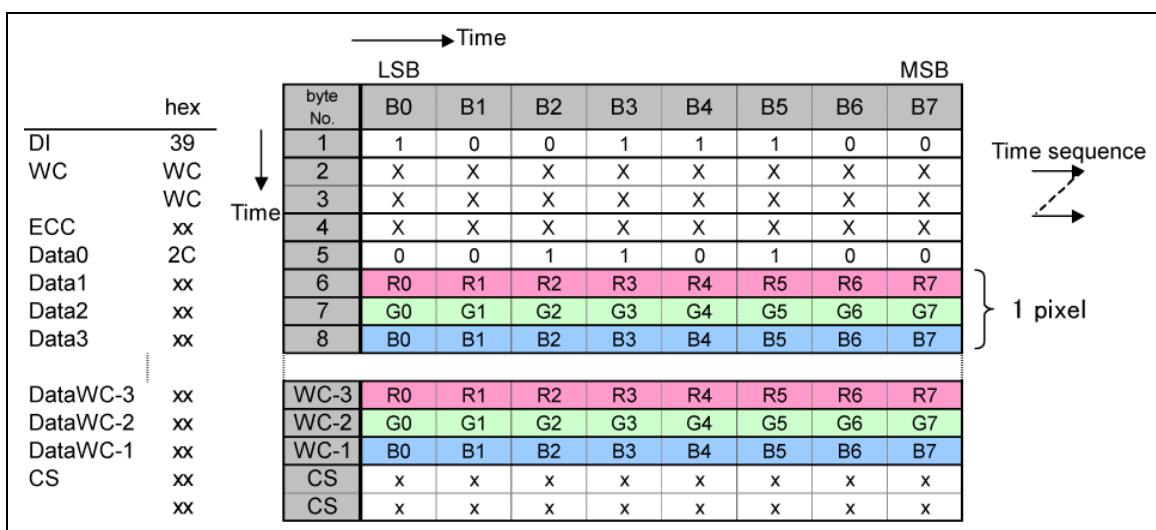


Figure 42 24bpp Pixel Data Format on the Long Packet (3Ah: set_pixel_format D2-0 = 111)

→ Time

	hex	byte No.	B0	B1	B2	B3	B4	B5	B6	B7	
DI	39	1	1	0	0	1	1	1	0	0	
WC	WC	2	X	X	X	X	X	X	X	X	
WC	WC	3	X	X	X	X	X	X	X	X	
ECC	xx	4	X	X	X	X	X	X	X	X	
Data0	2C	5	0	0	1	1	0	1	0	0	
Data1	xx	6	X	X	R0	R1	R2	R3	R4	R5	
Data2	xx	7	X	X	G0	G1	G2	G3	G4	G5	
Data3	xx	8	X	X	B0	B1	B2	B3	B4	B5	
DataWC-3	xx	WC-3	X	X	R0	R1	R2	R3	R4	R5	
DataWC-2	xx	WC-2	X	X	G0	G1	G2	G3	G4	G5	
DataWC-1	xx	WC-1	X	X	B0	B1	B2	B3	B4	B5	
CS	xx	CS	x	x	x	x	x	x	x	x	
		CS	x	x	x	x	x	x	x	x	

Figure 43 18bpp Pixel Data Format on the Long Packet (3Ah: set_pixel_format D2-0 = 110)

→ Time

	hex	byte No.	B0	B1	B2	B3	B4	B5	B6	B7	
DI	39	1	1	0	0	1	1	1	0	0	
WC	WC	2	X	X	X	X	X	X	X	X	
WC	WC	3	X	X	X	X	X	X	X	X	
ECC	xx	4	X	X	X	X	X	X	X	X	
Data0	2C	5	0	0	1	1	0	1	0	0	
Data1	xx	6	G3	G4	G5	R0	R1	R2	R3	R4	
Data2	xx	7	B0	B1	B2	B3	B4	G0	G1	G2	
DataWC-2	xx	WC-2	G3	G4	G5	R0	R1	R2	R3	R4	
DataWC-1	xx	WC-1	B0	B1	B2	B3	B4	G0	G1	G2	
CS	xx	CS	x	x	x	x	x	x	x	x	
		CS	x	x	x	x	x	x	x	x	

Figure 44 16bpp Pixel Data Format on the Long Packet (3Ah: set_pixel_format D2-0 = 101)

(11) Packet Footer on Long Packet (LPa)

In the Long Packet, Packet Footer is added after Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

- Checksum (2 bytes) = CRC (Packet Data): $CRC = X^{16} + X^{12} + X^5 + X^0$

(12) Acknowledge with Error Report (AwER)**Table 64**

Bit	Description	RSP LCD driver implementation	Note
0	SoT Error	No	
1	SoT Sync Error	No	
2	EoT Sync Error	No	
3	Escape Mode Entry Command Error	Yes	1
4	Low-Power Transmit Sync Error	Yes	1
5	HS Receive Timeout Error	No	
6	False Control Error	No	
7	Reserved	-	
8	ECC Error, single-bit (detected, and corrected)	Yes	
9	ECC Error, multi-bit (detected, not corrected)	Yes	
10	Checksum Error (Long packet only)	Yes	
11	DSI Data Type Not Recognized	Yes	
12	DSI VC ID Invalid	Yes	
13	Invalid Transmission Length	No	
14	Reserved	-	
15	DSI Protocol Violation	No	

Note: Detail error report condition is defined by RSP LCD driver (based on MIPI description).

(13) DCS, MCS, and Data Type List

The following tables show available data type of each command (DCS and MCS).

Table 65 DCS Data Type List

Command/Parameter		W/R	Host to RSP LCD driver Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
		DCS para	DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size
00h	nop	C	Yes	No	Yes	No	No	No	No	No	No	-
01h	soft_reset	C	Yes	No	Yes	No	No	No	No	No	No	-
04h	read_DDB_start	16	No	No	No	No	No	No	No	No	Yes	16'h10
05h	read_Number_of_the_Errors_on_DSI	1	No	No	No	No	No	No	No	No	Yes	16'h1
06h	get_red_channel	1	No	No	No	No	No	No	No	No	Yes	
07h	get_green_channel	1	No	No	No	No	No	No	No	No	Yes	
08h	get_blue_channel	1	No	No	No	No	No	No	No	No	Yes	
0Ah	get_power_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Bh	get_address_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Ch	get_pixel_format	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Dh	get_display_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Eh	get_signal_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Fh	get_diagnostic_result	1	No	No	No	No	No	No	No	No	Yes	16'h1
10h	enter_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
11h	exit_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
20h	exit_invert_mode	C	YES	NO	YES	No	No	No	No	No	No	-
21h	enter_invert_mode	C	YES	NO	YES	No	No	No	No	No	No	-
26h	set_gamma_curve	1	No	Yes	Yes	No	No	No	No	No	No	-
28h	set_display_off	C	Yes	No	Yes	No	No	No	No	No	No	-
29h	set_display_on	C	Yes	No	Yes	No	No	No	No	No	No	-

Table 66 DCS and Data Type List (continued)

DCS Command/Parameter		W/R	Host to RSP LCD driver Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
		DCS para	DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size
34h	set_tear_off	C	Yes	No	Yes	No	No	No	No	No	No	-
35h	set_tear_on	1	No	Yes	Yes	No	No	No	No	No	No	-
36h	set_address_mode	1	No	Yes	Yes	No	No	No	No	No	No	-
3Ah	set_pixel_format	1	No	Yes	Yes	No	No	No	No	No	No	-
44h	set_tear_scanline	2	No	Yes	Yes	No	No	No	No	No	No	-
51h	write_display_brightness	2	No	Yes	Yes	No	No	No	No	No	No	-
52h	read_display_brightness — value	2	No	No	No	No	No	No	No	No	Yes	16'h1
55h	write_content_adaptive_brightness_control	1	No	Yes	Yes	No	No	No	No	No	No	-
56h	read_content_adaptive_brightness_control	1	No	No	No	No	No	No	No	No	Yes	16'h1
5Eh	write_CABC_minimum_brightness	2	No	Yes	Yes	No	No	No	No	No	No	-
5Fh	read_CABC_minimum_brightness	2	No	No	No	No	No	No	No	No	Yes	16'h1
68h	read_automatic_brightness_control_self-diagnostic_result	1	No	No	No	No	No	No	No	No	No	16'h1
A1h	read_DDB_start (Note1)	16	No	No	No	No	No	No	No	No	Yes	16'h10
A8h	read_DDB_continue (Note1)	N	No	No	No	No	No	No	No	No	Yes	16'h10
DAh	Read ID1	1	No	No	No	No	No	No	No	No	Yes	-
DBh	Read ID2	1	No	No	No	No	No	No	No	No	Yes	-
DCh	Read ID3	1	No	No	No	No	No	No	No	No	Yes	-

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Note1: maximum return packet size ≥ 2

Table 67 MCS and Data Type List

MCS Command/Parameter	W/R	Host to RSP LCD driver Data Type (RX)									
		Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	37'h
	MCS para	DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size
MCS Read only command	1	No	No	No	No	No	No	Yes	No	No	16'h1
MCS write/read command	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
MCS write/read command	1 < n	No	No	No	No	No	Yes	Yes	No	No	16'hn

(14) Video Mode

The RSP LCD driver supports Video Mode for moving pictures. There are three formats of transmission packet sequences. The RSP LCD driver supports two of these formats. See the following table.

Table 68

Transmission packet sequence in video mode	RSP LCD driver implementation
Non-burst mode with sync pulses	Not supported
Non-burst mode with sync events	Supported
Burst mode	Supported

1) Display Timing (Video Mode)

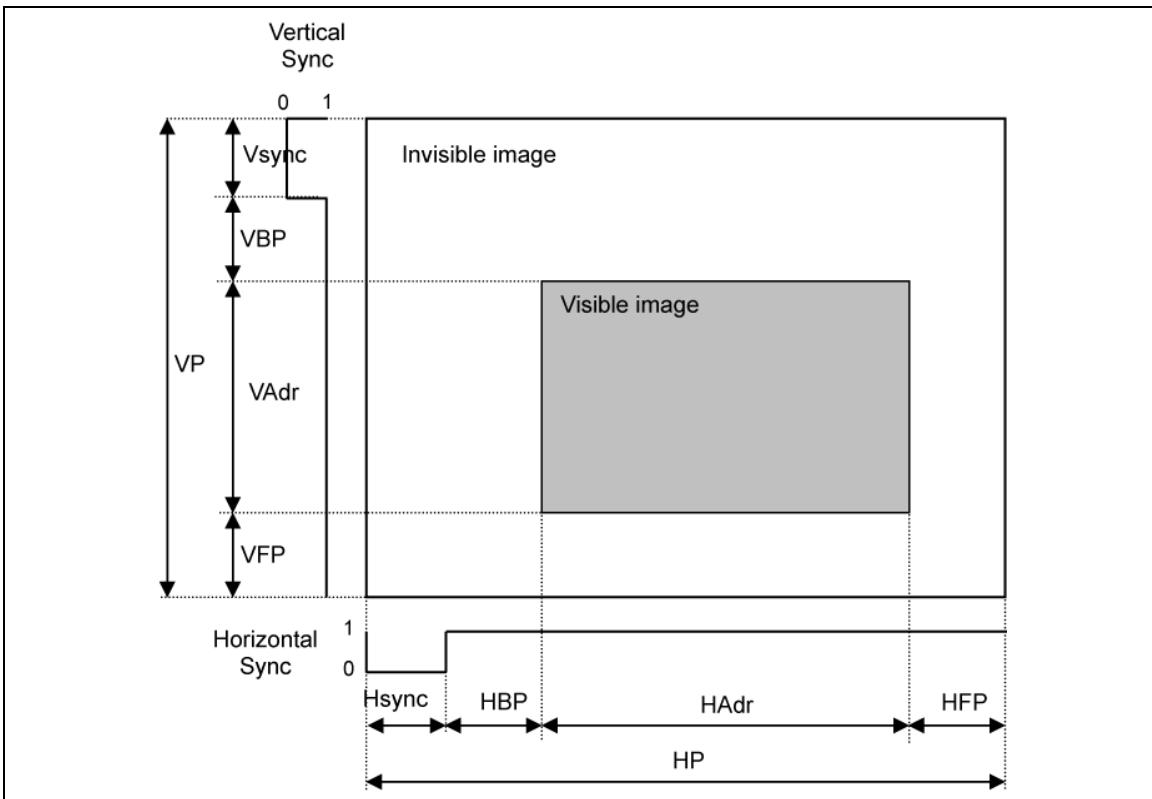


Figure 45

2) Vertical Display Timing (VideoMode)

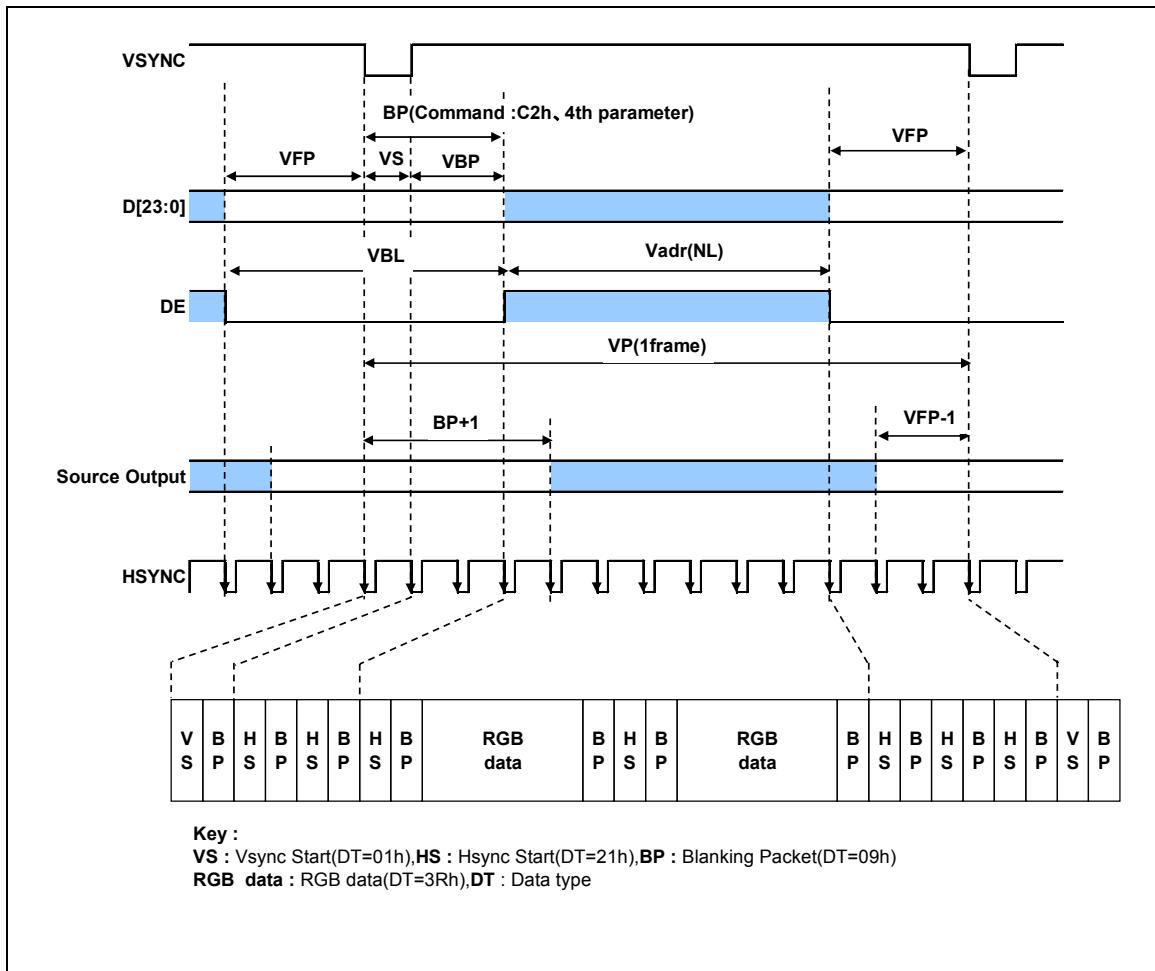


Figure 46

3) Horizontal Display Timing (Video Mode)

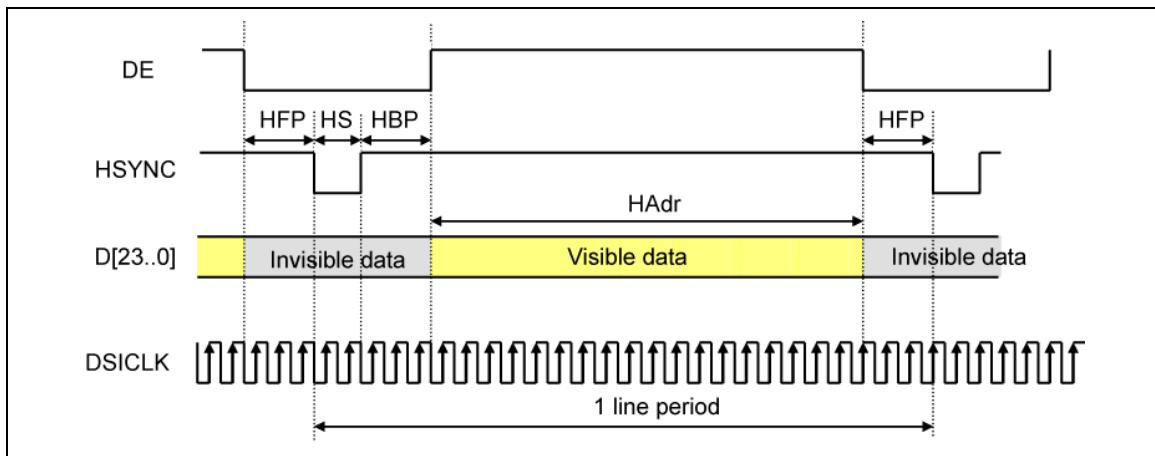


Figure 47

Table 69 Vertical Display Timing (Video Mode, DM = 1h)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line	1286	-	-	
Vertical low pulse width	VS		Line	1	-	-	
Vertical front porch	VFP		Line	2	-	-	
Vertical back porch	VBP		Line	2	-	-	
Vertical data start point	-	BP	Line	4	-	-	See
Vertical blanking period	VBL	VFP+BP	Line	6	-	-	
Vertical active area	Vadr		Line	1280	1920	1920	

Note: "BP" is set as back porch by BP register.

1 line : prescribed by HSYNC (when DM = 4'h1)

Table 70 Horizontal Display Timing (Video Mode, DM = 1h)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock	4lane:70 3lane:95 2lane:140	-	-	
Horizontal data start point	-	HS+HBP	ByteClock	45	-	-	
Horizontal active area	Hadr		Pixel	720		1080	

Note: fByteClock = (1/4) * fDSICLK. fByteClock = frequency of ByteClock.

5) Packet Footer on Long Packet (LPa)

In the Long Packet, Packet Footer is added after Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

Checksum (2 bytes) = CRC (Packet Data): $CRC = X^{16} + X^{12} + X^5 + X^0$

6) Line Contention Detection

The Low-Power receiver and a separate contention detector shall be used in a bi-directional data Lane to monitor the line voltage on each low-power signal. The low-power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than V_{IL} . The contention detector shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD} . An LP low fault shall not be detected when the pin voltage is less than V_{ILCD} .

The LP-CD threshold voltages (V_{ILCD} and V_{IHCD}) are shown along with the normal signaling voltages as below.

After contention has been detected, the protocol shall take proper measures to resolve the situation.

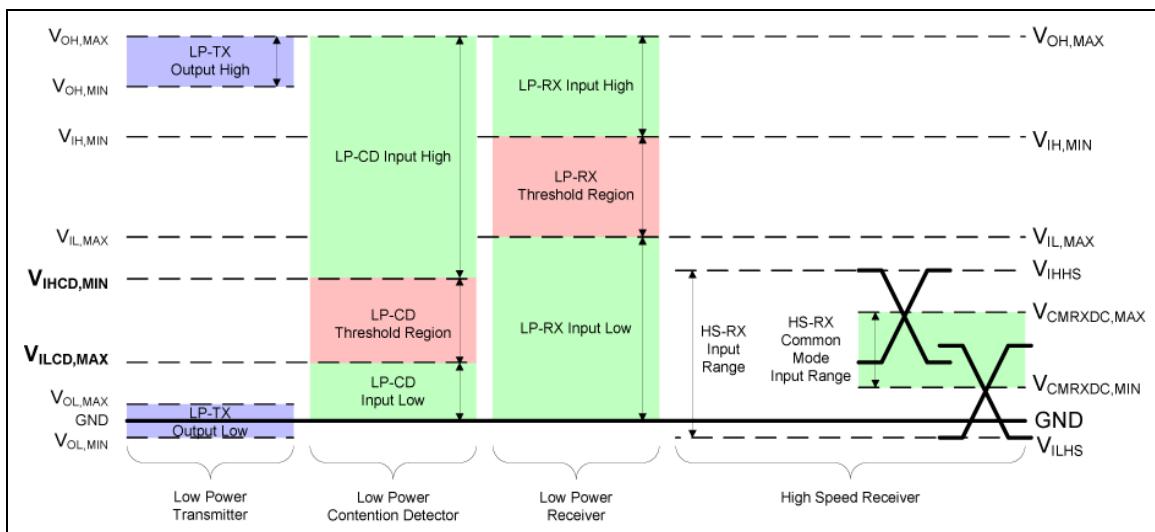


Figure 48 Signaling and Contention Voltage Levels

Display Mode

The RSP LCD driver supports display operations synchronized with the internal oscillation clock and with the external clock. The DM register changes display modes.

Table 71

DM	Display Mode	Display clock	Display Sync	Data latch clock	cABC PWM
'h0	built-in TCON	OSC	OSC	OSC	OSC
'h1	DSI-Video-Burst	OSC	DSI	DSI (*)	OSC
'h2	Setting inhibited	-	-	-	-
'h3	Setting inhibited	-	-	-	-
'h4	Setting inhibited	-	-	-	-
'h5	Setting inhibited	-	-	-	-
'h6	Setting inhibited	-	-	-	-
'h7	Setting inhibited	-	-	-	-
'h8	Setting inhibited	-	-	-	-
'h9	Setting inhibited	-	-	-	-
'hA	Setting inhibited	-	-	-	-
'hB	Setting inhibited	-	-	-	-
'hC	Setting inhibited	-	-	-	-
'hD	Setting inhibited	-	-	-	-
'hE	Setting inhibited	-	-	-	-
'hF	Setting inhibited	-	-	-	-

Note: Data latch clock is changed to the clock based on OSC during blank period.

The DM register setting cannot be changed during display operation. Change this register setting during Sleep In. As shown below, input display clock via each interface before issuing exit_sleep_mode.

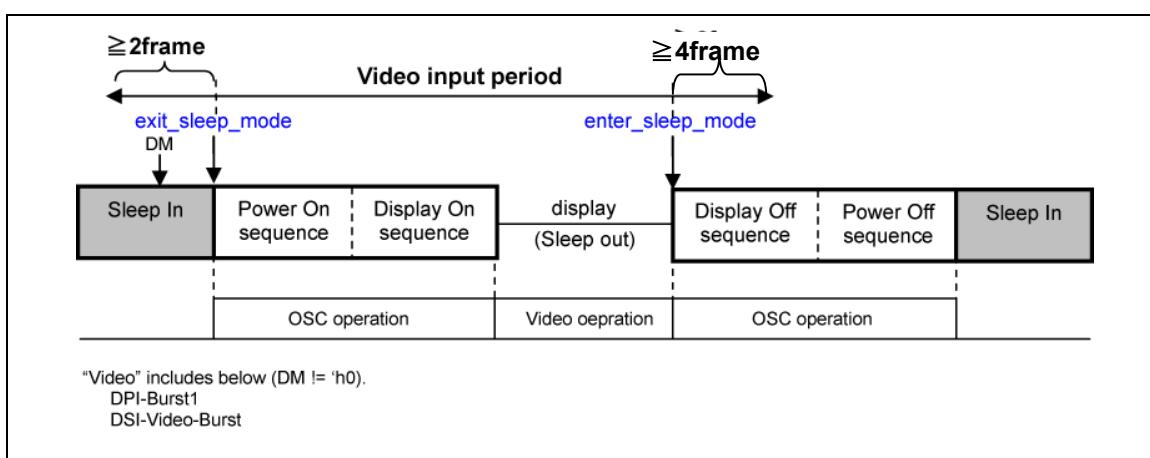


Figure 49

Data Format

The RSP LCD driver supports the following data formats.

DPI Data Format															supported by DB pins										
SIM	DPIDL	set_pixel_format D[6:4]	Transfer Mode	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	Access Type	Notes					
				23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
c1000	0	3h5	16bpp	1times	1st	N/A	N/A	N/A	N/A	N/A	R41	R42	R43	R44	G51	G52	G53	G54	B41	B42	B43	B44	DSPW	1	
		3h6	18bpp	1times	1st	N/A	N/A	N/A	N/A	N/A	R51	R52	R53	R54	G51	G52	G53	G54	B51	B52	B53	B54	DSPW	No	
		3h7	24bpp	1times	1st	R71	R76	R51	R41	R31	R21	R11	R01	G71	G76	G51	G52	G53	G54	B71	B76	B51	B41	DSPW	No
	1	3h5	16bpp	1times	1st	N/A	N/A	N/A	R41	R31	R21	R11	R01	N/A	N/A	G51	G52	G53	G54	B51	B52	B53	B54	DSPW	No
		3h6	18bpp	1times	1st	N/A	N/A	R51	R41	R31	R21	R11	R01	G51	G52	G53	G54	B51	B52	B53	B54	DSPW	No		
		3h7	24bpp	1times	1st	R71	R76	R51	R41	R31	R21	R11	R01	G71	G76	G51	G52	G53	G54	B71	B76	B51	B41	DSPW	No

Note1. only Secondary IF

Note A supported data format range depends on the number of DB pins in the product.

DSPW : Display Data Write

Figure 50

Internal Reference Clock Generating Function

The following figure shows the generation of reference clock (RCLK) used in the RSP LCD driver. RCLK is a minimum unit of a clock used for register setting. RCLK is generated from a divider ("1/2" in the figure) divides an internal oscillation clock. Set display timing according to use conditions.

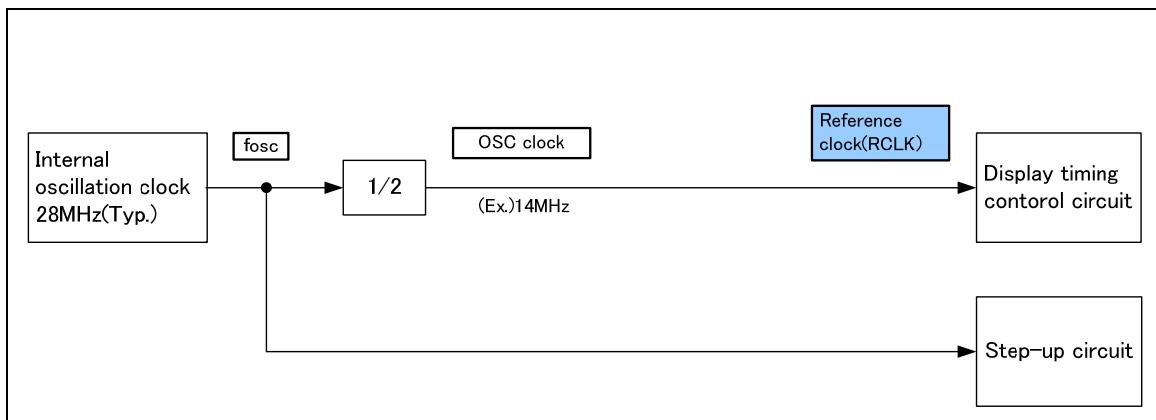


Figure 51 Internal Reference Clock Generation

Output Waveform Mode of Panel Control Signals

For the specifications for panel control signals, see the appendix.

TE Pin Output Signal

Tearing Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

Table 72

TEON (represents status of 35h command)	TELOM (35h1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

Tearing Effect signal mode is defined by TELOM (D0 in parameter of set_tear_on (35h)). Write TELOM=0 when using DSI TE report function.

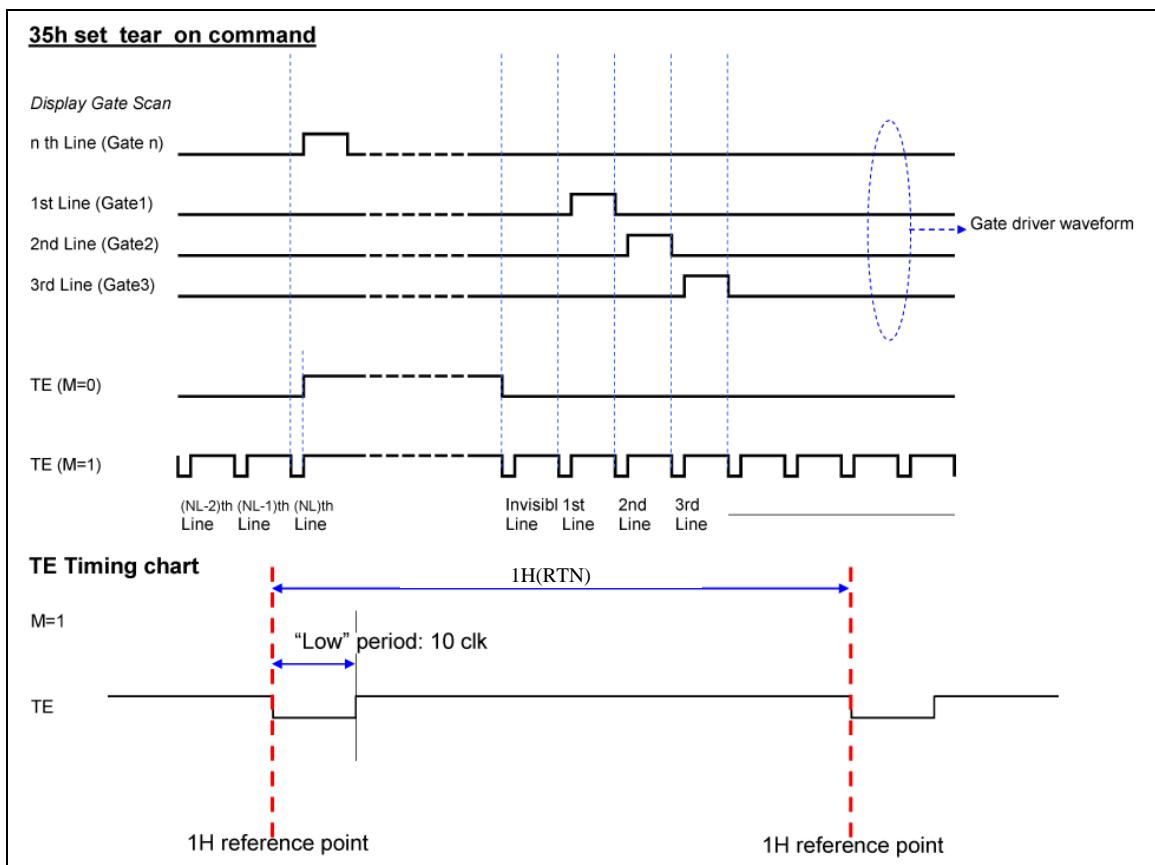


Figure 52

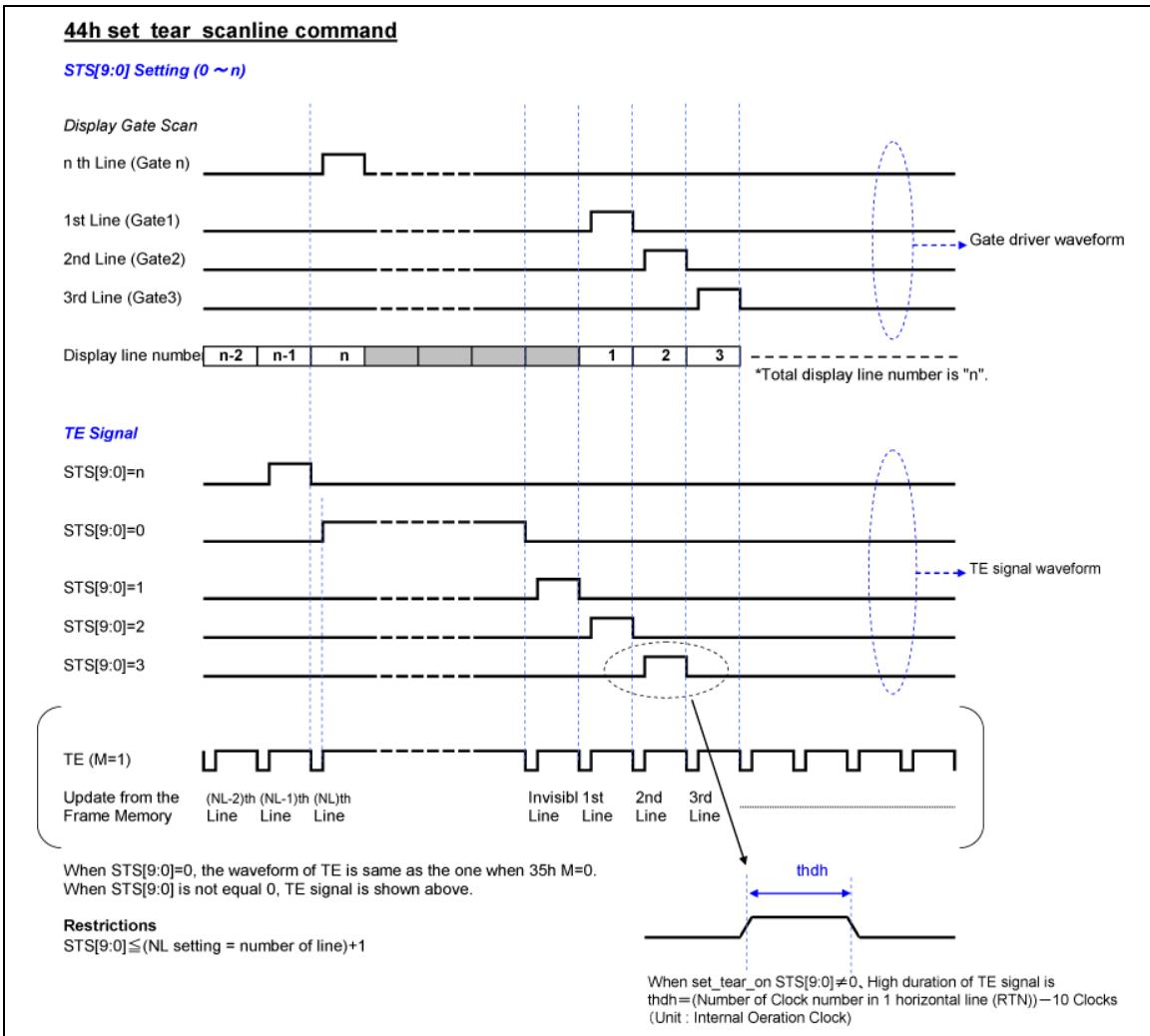


Figure 53

Self-Diagnostic Function

The RSP LCD driver supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D6 bit according to the following flow chart.

note1) This function operate except "External VSP/VSN Supply mode".

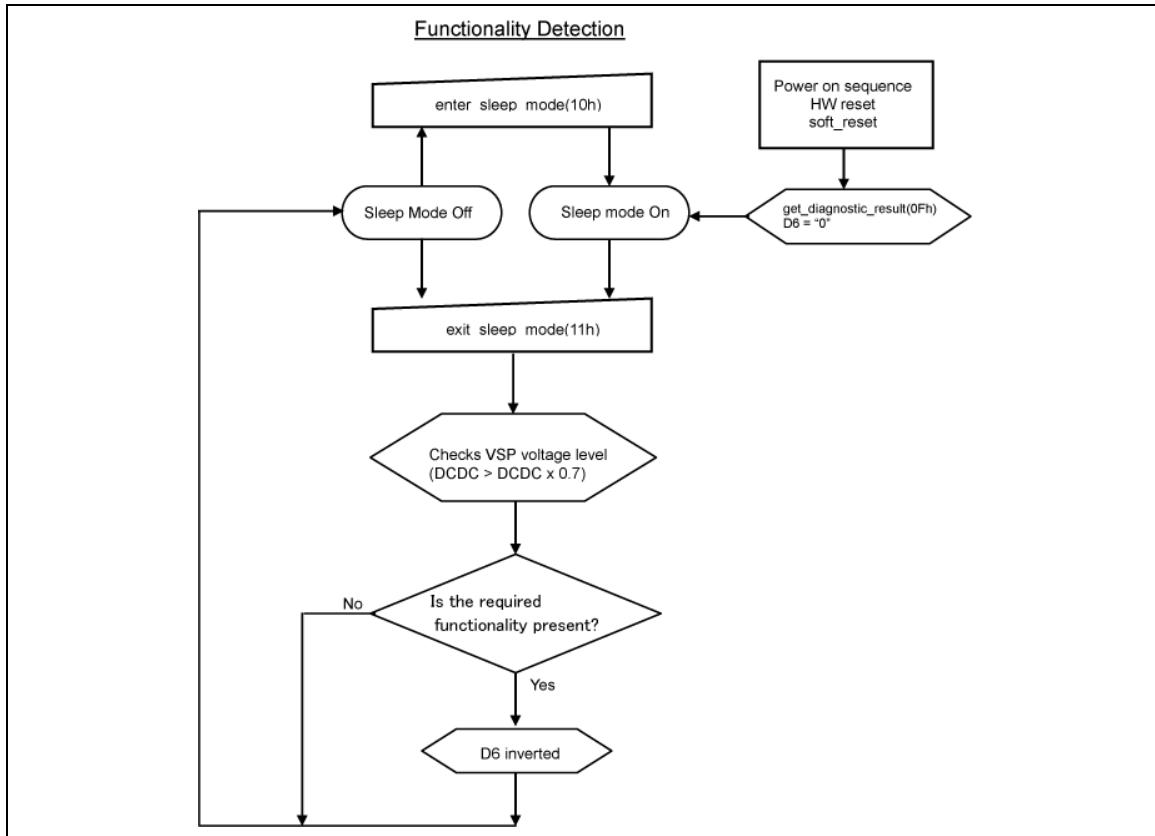


Figure 54 Functionality Detection

Content Adaptive Brightness Control (Dynamic Backlight Control Function)

The RSP LCD driver supports a CABC (Content Adaptive Brightness Control) function to control backlight brightness and process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The CABC function analyzes the histogram of brightness of image data, and determines whether the image is bright image, dark image, middle image, or GUI image. Parameters are calculated for each of the above image data so that image processing and backlight dimming are optimized. By processing image and dimming backlight for each frame, backlight is reduced according to display image. An area that a histogram analysis result significantly changes is regarded as an area that a video scene changes. Then, image processing and backlight dimming are performed on the area instantly. In an area that a video scene does not change, backlight brightness is changed slowly to avoid flicker.

- Control backlight dynamically according to the image histogram.
- PWM pin(LEDPWM) for LED brightness
- PWM signal control register set by the host processor. Backlight dimmer is adjusted by calculating internally decided PWM value and maximum PWM value from the host processor.

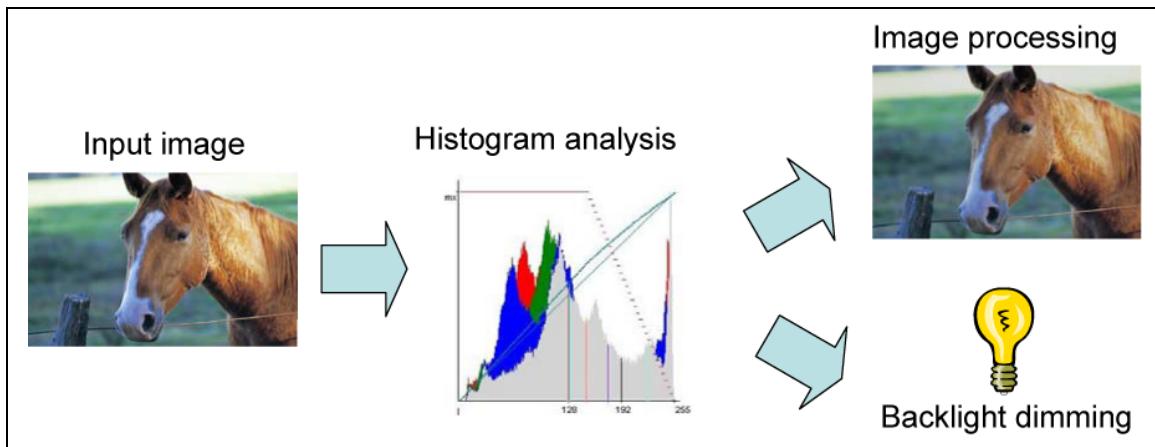


Figure 55

- Notes:
1. The CABC function is enabled by 55h command (write_content_adaptive_brightness_control).
 2. The effects of CABC function on power efficiency and display quality depend on image data and the setting. Check display quality on the panel.

Restriction on Content Adaptive Brightness Control function

The RSP LCD driver cannot use Auto Contrast Optimization function and Content Adaptive Brightness Control function at the same time.

System Configuration

1. The PWM signal is used to directly control the RSP LCD driver and LED driver IC. The LED driver IC is controlled entirely via the RSP LCD driver.

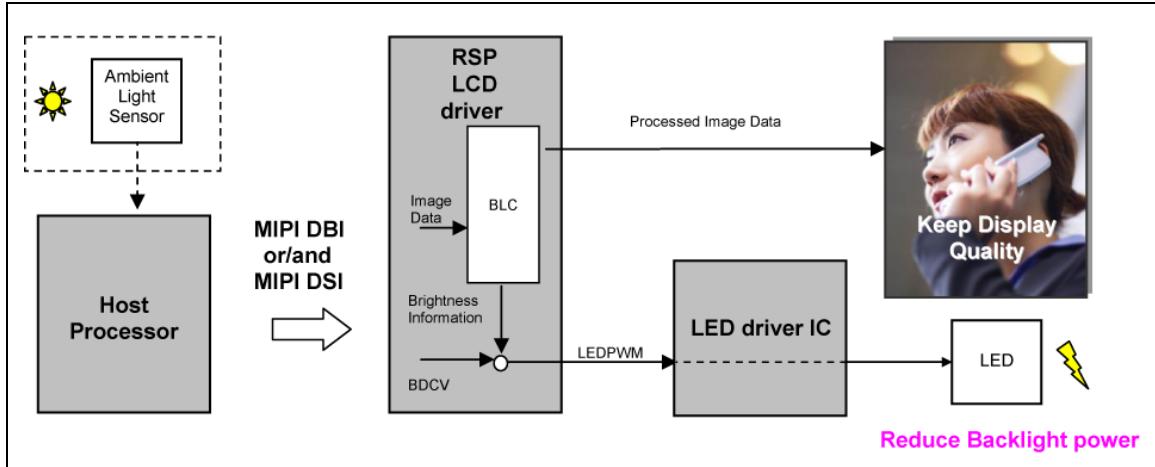


Figure 56

2. The host processor reads LED brightness information internally generated by CABC processing from the RSP LCD driver via MIPI DBI/DSI. Then, the LED driver IC is controlled from the host processor. There is the time difference between adjusting brightness by PWM and displaying data processed from the RSP LCD driver. Check the effect on the image.

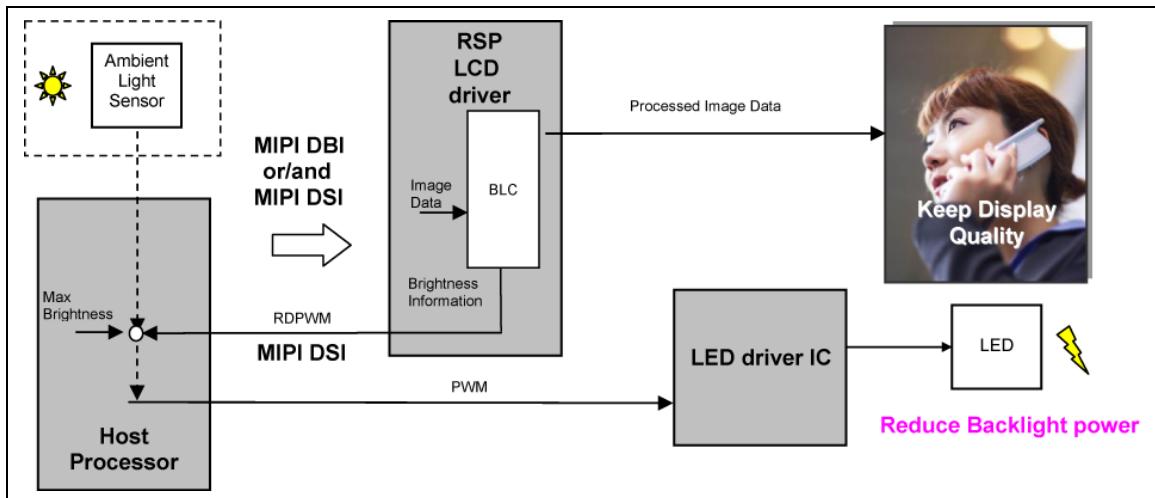


Figure 57

Auto Contrast Optimization

(1) Overview

The Auto Contrast Optimization (ACO) function enhances a contrast suitable for the input image by determining an enhancement parameter according to the input image histogram. This function enhances image quality by applying a CABC image processing method.

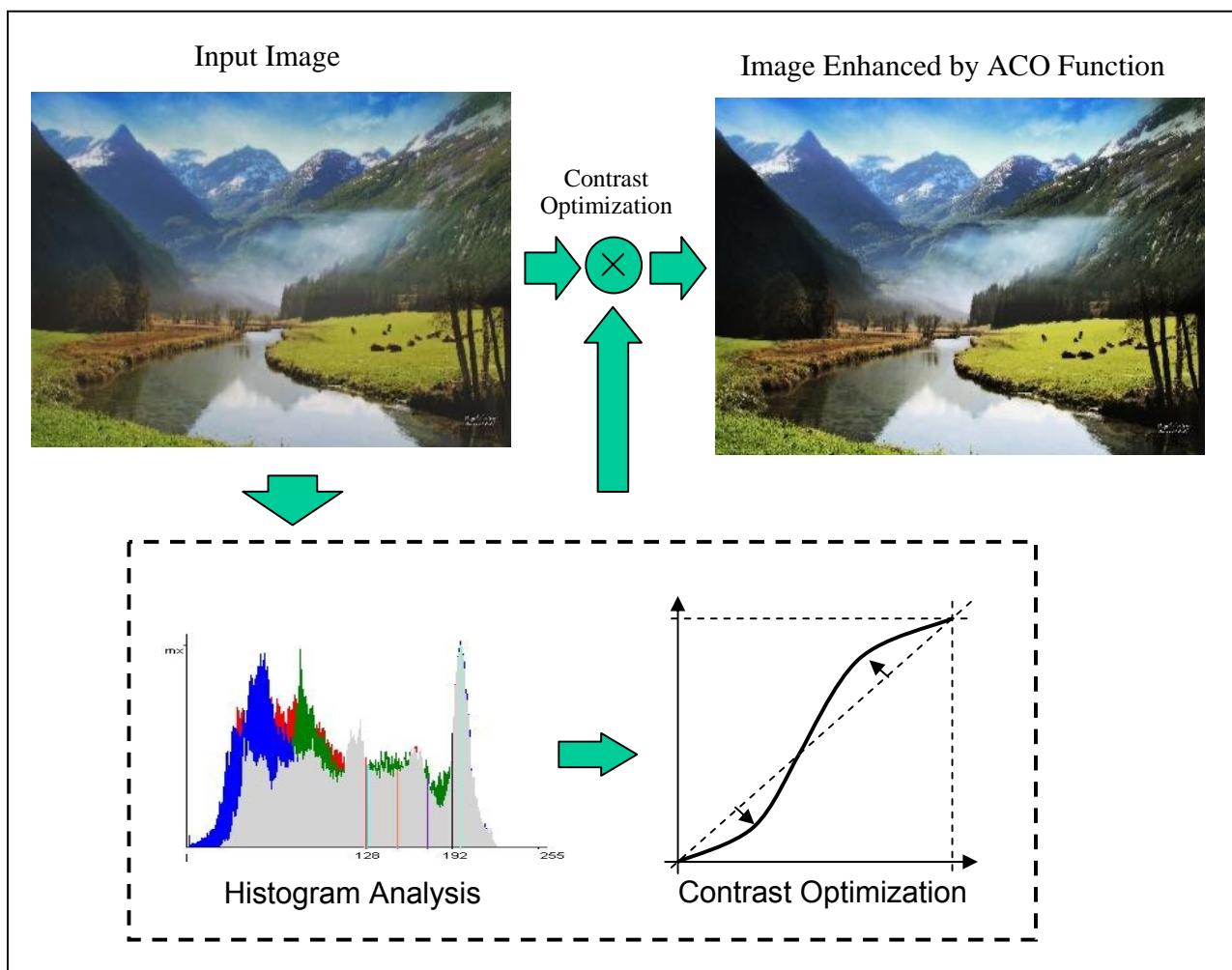


Figure 58

The ACO function adjusts an enhancement parameter according to the input image. When the image subtly changes, the parameter may rapidly change. To prevent flickering caused by the rapid parameter change, this function slows the parameter change (caused by the input image change).

Outline Sharpening Function

(1) Overview

The RSP LCD driver supports outline sharpening function. Image can be clearly displayed by sharpening outlines of the image tone.

This function operates calculating data of pixels, images with sharp outlines can be realized regardless of moving or still images.

The characteristics of algorithm used in this function may not fit some types of data to realize desirable result. Please confirm images after outline sharpening operation.

The following figure shows how the each stages of operational sequence interact.

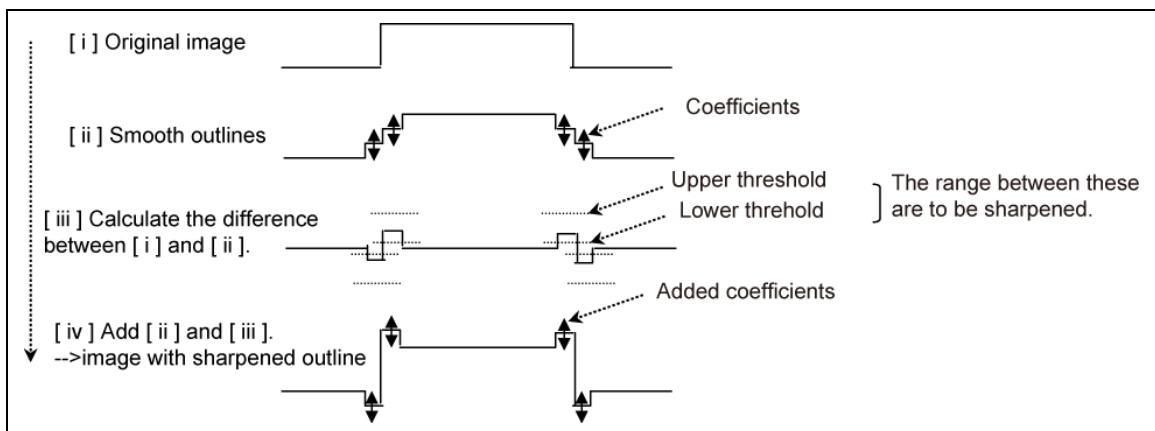


Figure 59

Example of Image with Outline Sharpened



Figure 60

Restriction on Outline Sharpening Function

1. One pixel at the end of original data will not be sharpened.

Color Enhancement Function

(1) Overview

The RSP LCD driver supports a color enhancement function, which enhances saturation by calculating image data. This function enhances the saturation of the image displayed on the liquid crystal panel and displays image with color enhanced.

- The function enhances color and makes pixel colors more vivid.

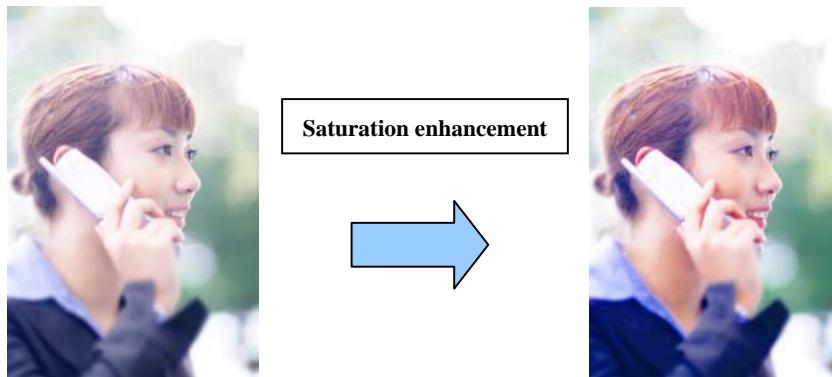


Figure 61

- When the saturation enhancement coefficients of the input image are 1.0 or more, the display image with color enhanced is generated.

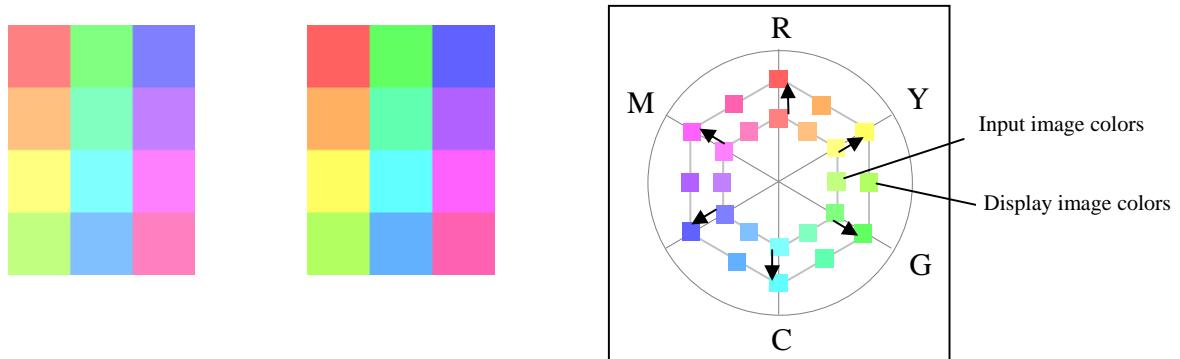


Figure 62

See the saturation diagram right above. The colors of the input image are enhanced. (The polygon showing the colors of the input image is enlarged)

- When the saturation enhancement coefficients of red, yellow, green, cyan, blue, and magenta are set independently. Here the saturation enhancement coefficients of only red and yellow are set.

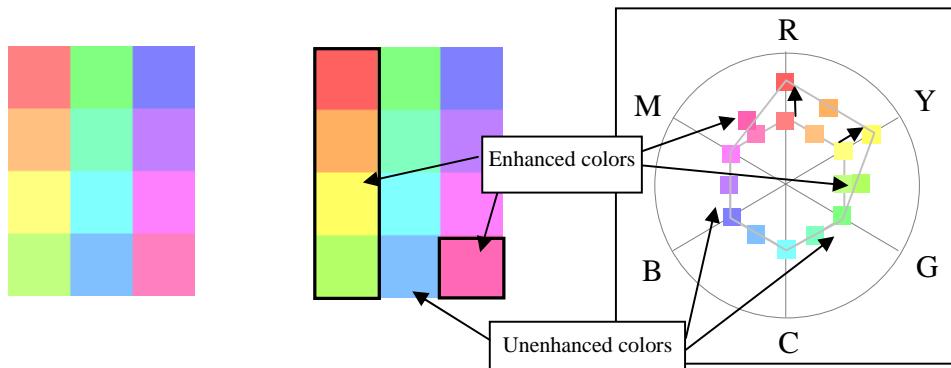


Figure 63

See the saturation diagram right above. Green, cyan, blue, and magenta are not enhanced. The colors mixed with red or yellow and the mixed colors of red and yellow are enhanced.

- The skin color independent adjustment function displays natural skin color.

Input image

Output image:

Output image:

No skin color adjustment areas are set. Skin color adjustment areas are set.



- To adjust the skin color after saturation enhancement, this function adjusts the skin hues independently from the other hues.

Output image:

The hues have changed
from yellowish to reddish.

Output image :

The hues remain unchanged.

Output image:

The hues have changed
from reddish to yellowish.



Restriction on Auto Contrast Optimization function

The RSP LCD driver cannot use Auto Contrast Optimization function and Content Adaptive Brightness Control function at the same time.

Multi Interface

The RSP LCD driver supports multi interface. A primary interface is set by the IM pins. A secondary interface is set by the SIMEN and SIM registers.

(1) Interface Setting

The primary interface or the secondary interface can be chosen arbitrarily. After the RSP LCD driver is accessed via the primary interface, values set in the SIM register are stored in NVM.

(2) Interface Switching

The interfaces can be switched by issuing the nop command. They cannot be switched without issuing the command. Issue the command to switch them. Also, the primary interface and the second interface cannot be used at the same time.

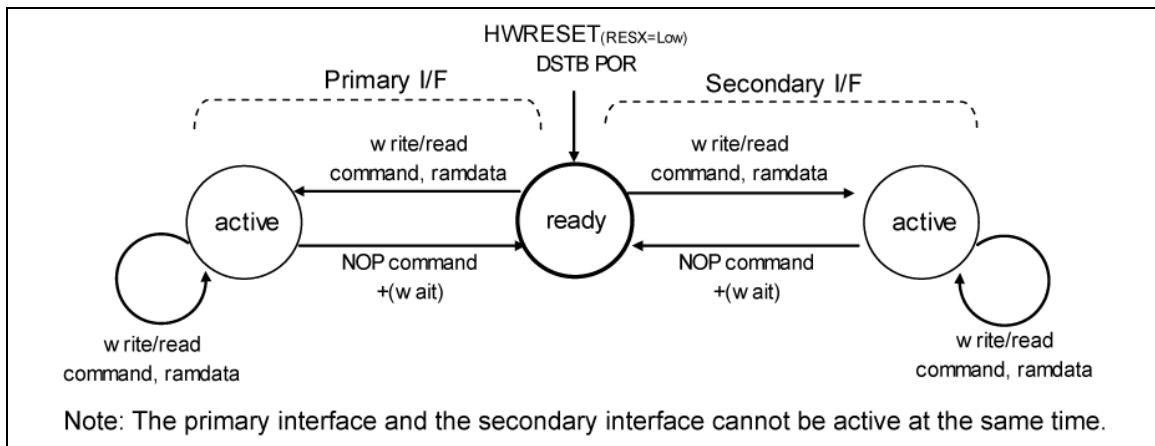


Figure 64 Multi Interface State Transition

(3) Interface Switching Sequence

The RSP LCD driver supports the following interface switching sequences.

Table 73

- DSI \longleftrightarrow I²C Multi interface (Primary: DSI)
- DSI \longleftrightarrow DBI Type C (Option 1) Multi interface (Primary: DSI)
- DSI \longleftrightarrow DBI Type C (Option 3) Multi interface (Primary: DSI)

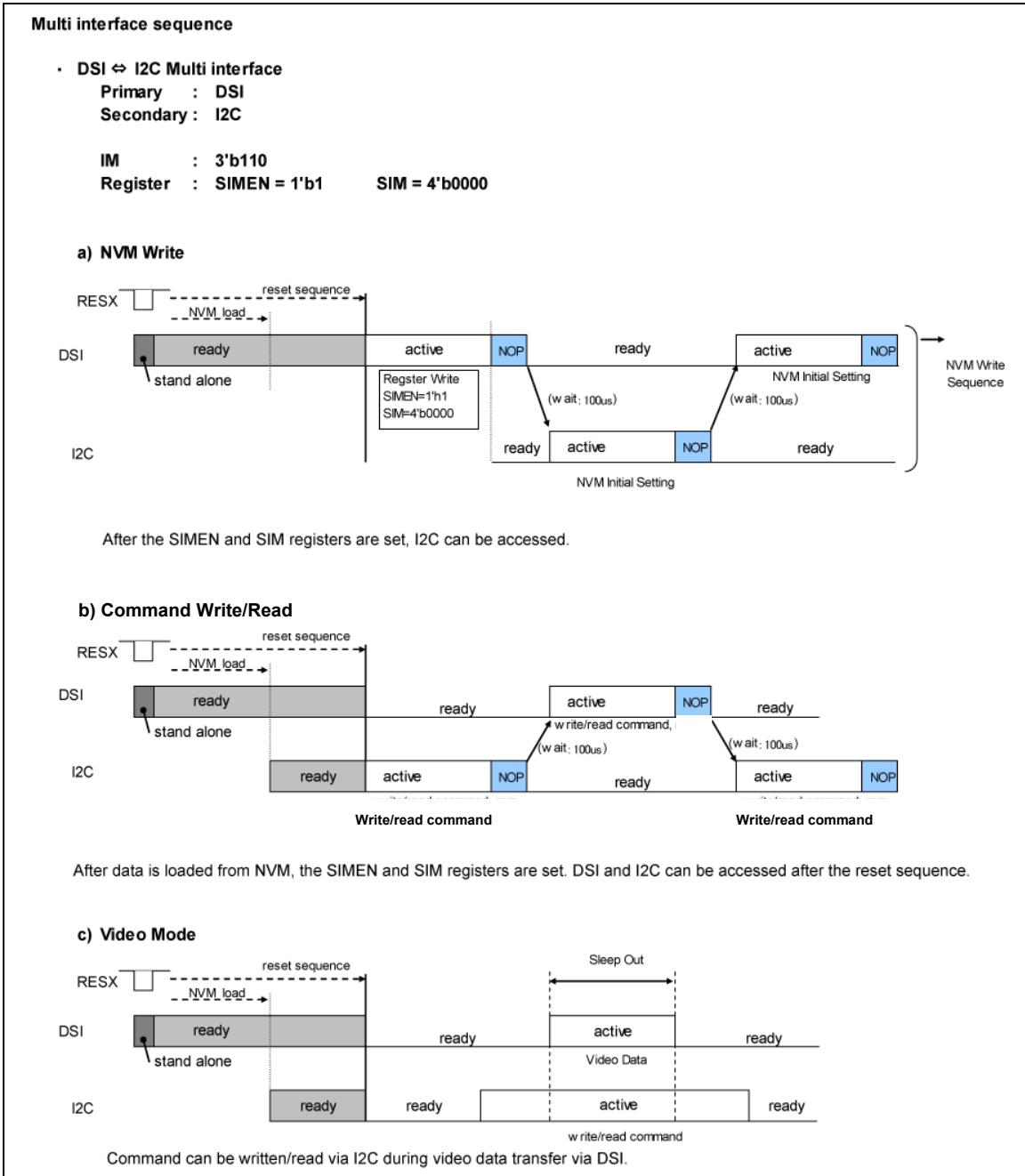


Figure 65

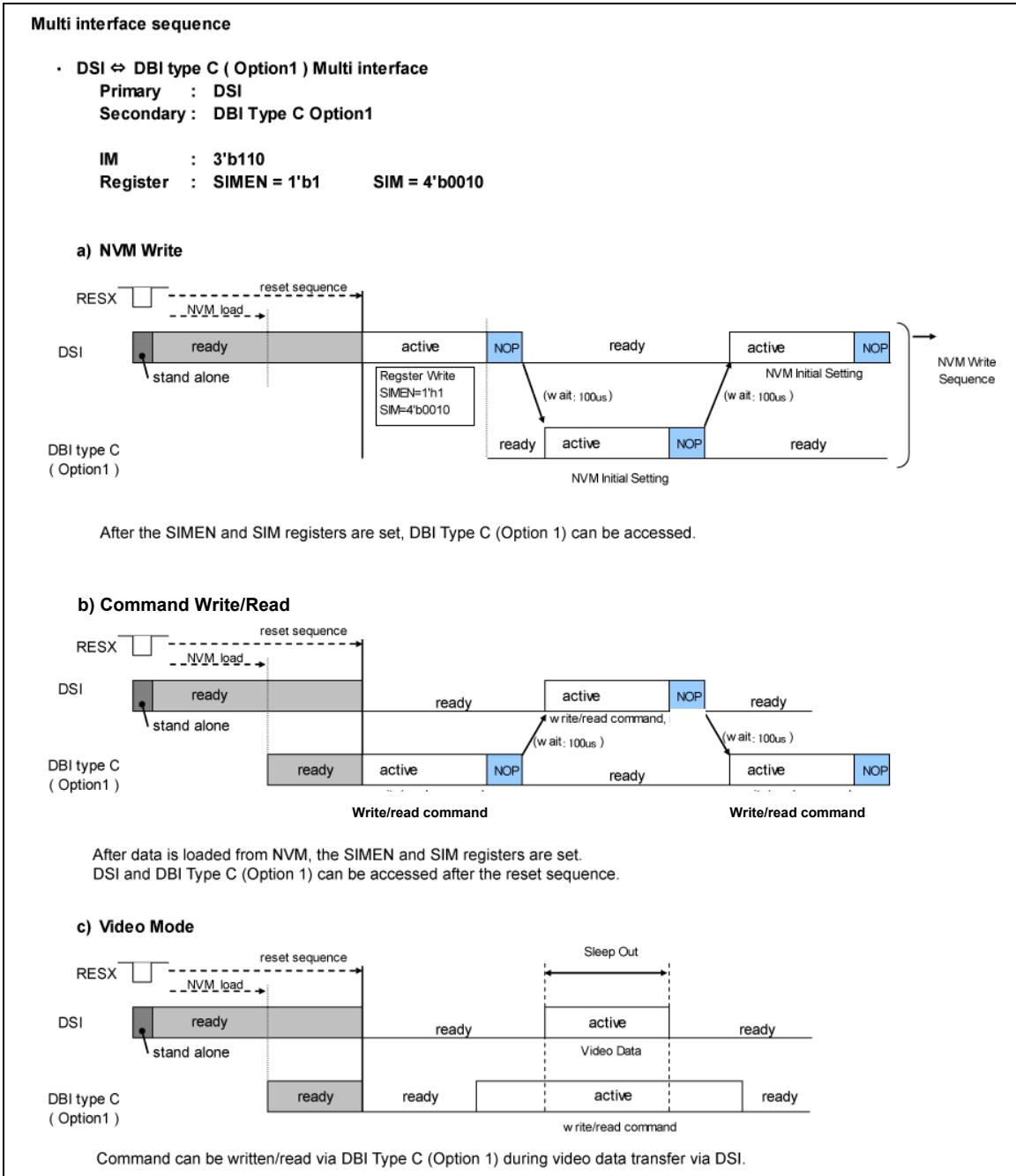


Figure 66

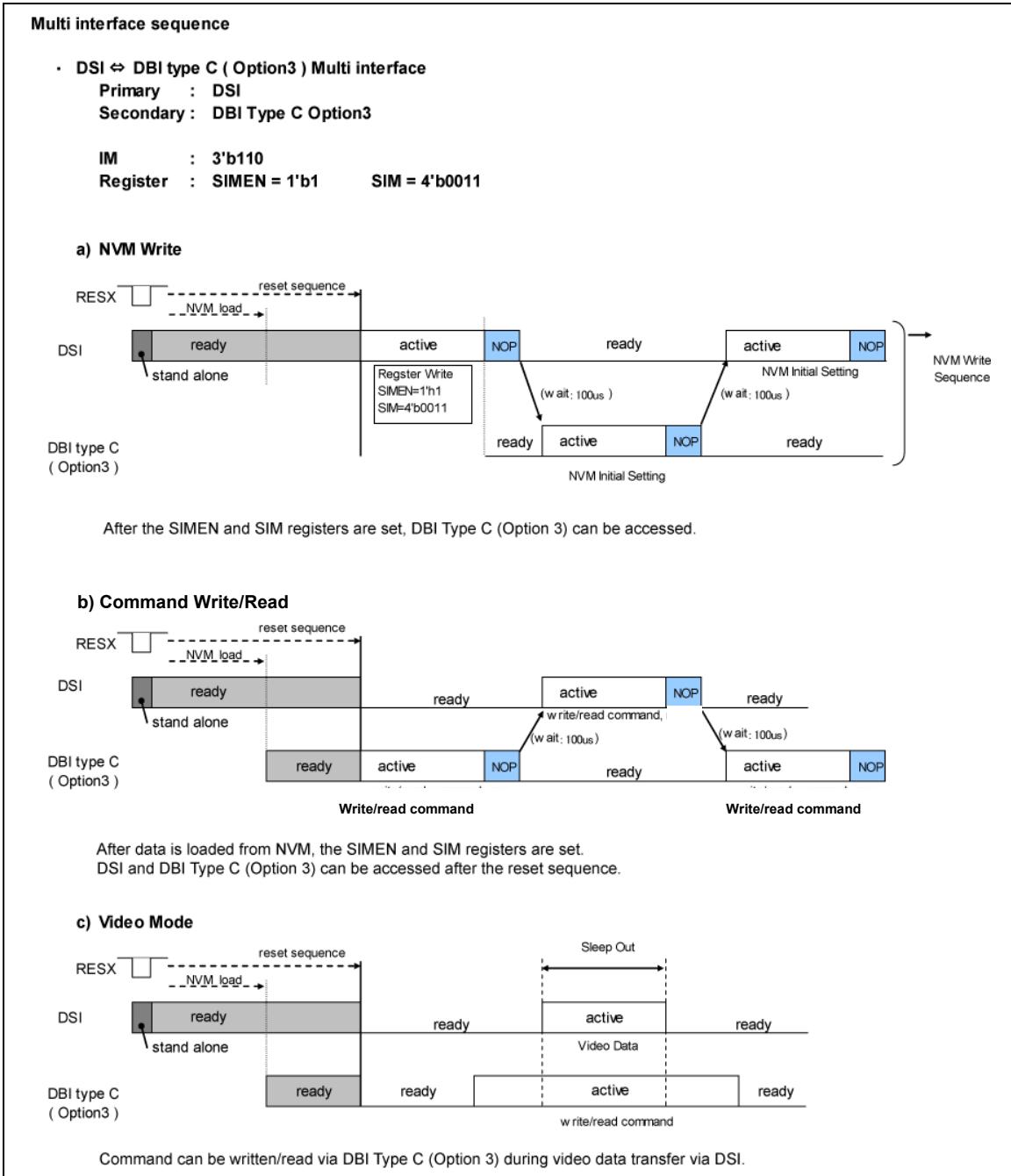


Figure 67

General Purpose Output (GPO) : TN Liquid Crystal Drive Signal Output

The RSP LCD driver can output the signals to drive TN liquid crystal panel different from the display liquid crystal panel.

There are four output pins for the control signals. These pins can change the output of alternating signals. So, four drive systems, a left-to-right system and a top-to-bottom system, are supported.

Also, the alternating signal cycles and output voltages can be changed by register setting.

(1) Output Timing

Control signals are output by setting the PBON register to 1. The control signals and the alternating signals do not synchronize with display data and display VCOM.

(2) Signal Output Pins to Drive Crystal Panel

The RSP LCD driver has PBCTLA1, PBCTLA2, PBCTLB1 and PBCTLB2 as control signal output pins. PBCTLA1(B1) and PBCTLA2(B2) output the control signals at a level between GND and voltage set by PBHLVL register (drive voltage setting register).

When the PBON register is set to 0, the output level of each pin is GND.

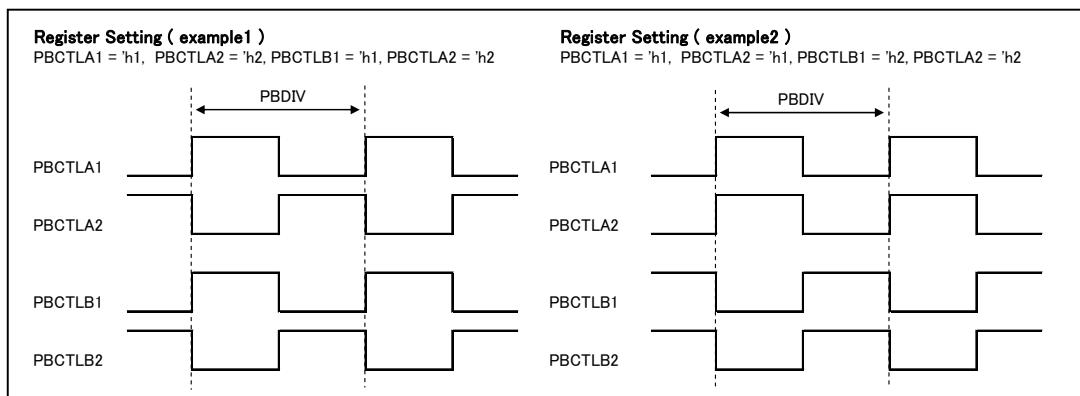


Figure 68

(3) Drive Frequency Setting

The PBDIV register can change the drive frequencies of the control signals.

(4) Drive Voltage Setting

The PBHLVL register can change the drive voltages of the control signals.

Synchronization signal Output for touch panel controller

The RSP LCD driver can output the synchronization signals to capture touch sensing signal for touch panel controller. To use these signals, touch panel controller can capture touch sensing signal while avoiding display changing noise.

These signals are consist of vertical synchronization signal: VSOUT and horizontal synchronization signal: HSOUT. The level of output voltage is IOVCC to GND. Each signal can adjust output timing for internal synchronization signal. The high level width of VSOUT is 1 line, and the high level width is adjustable.

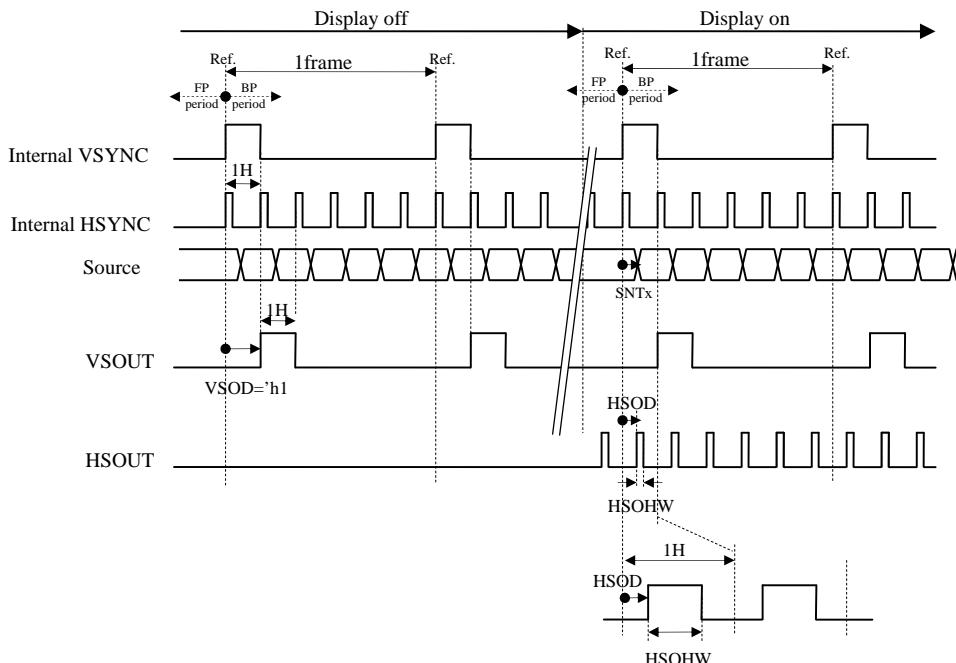
Enable/disable of these signals is controlled by TPSYNEN register. VSOUT is outputted always, but HSOUT is outputted during displaying only.

(1) VSOUT output Timing

VSOUT is outputted that internal VSYNC is starting point. VSOUT output timing can adjust by VSOD register. Unit is 1H.

(2) HSOUT output Timing

HSOUT is outputted that internal source output timing is starting point. HSOUT output timing can adjust by HSOD register. And HSOUT high level width can adjust by HSOHW register.



State Transition Diagram (Display Mode)

(1) Definition of Display Modes

The state transition of the RSP LCD driver (display modes) compliant with MIPI DCS is as follows:

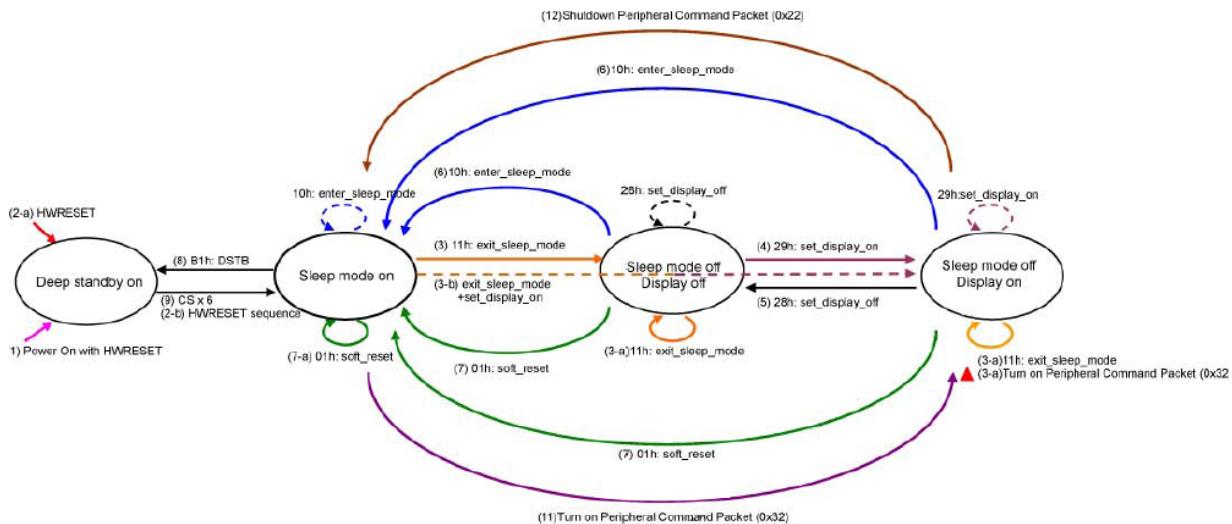


Figure 69

- Notes:
1. A specified sequence is executed during each state transition. For details, see the description of each sequence.
 2. Do not transit to states not defined.
 3. Turn on Peripheral Command Packet and Shutdown Peripheral Command Packet are supported in only DSI Video mode.

Table 74 Operation Mode Transition Sequence

Sequence		Command	State	
			From	To
(1)	Power On sequence with HWRESET	-	-	Sleep mode on
(2-a)	HWRESET	(RESX=Low)	-	Sleep mode on
(2-b)	HWRESET sequence	(RESX= Low ->High)	Deep stand by	Sleep mode on
(3)	exit_sleep_mode sequence	11h:exit_sleep_mode	Sleep mode on	Sleep out Display off
(3-a)		11h:exit_sleep_mode	Sleep mode off Display off/on	Sleep mode off Display off/on
		Turn on Peripheral Command DSI : Data Type=0x32		
(3-b)	exit_sleep_mode+ display_on sequence	11h:exit_sleep_mode	Sleep mode on	Sleep mode off Display on
(4)	set_display_on sequence	29h:set_display_on	Sleep mode off Display off	Sleep mode off Display on
(5)	set_display_off sequence	28h:set_display_off	Sleep mode off Display on	Sleep mode off Display off
(6)	enter_sleep_mode sequence	10h:enter_sleep_mode	Sleep mode off Display off/on	Sleep mode on
(7)	soft_reset sequence	01h:soft_reset	Sleep out Display off/on	Sleep mode on
(7-a)			Sleep mode on	Sleep mode on
(8)	Deep standby mode on sequence	B1h: DSTB	Sleep mode on	Deep standby on
(9)	Deep standby mode off sequence	CSX x 6	Deep standby on	Sleep mode on
(11)	Turn on Sequence	Turn on Peripheral Command DSI : Data Type=0x32	Sleep mode on	Sleep mode off Display on
(12)	Shutdown Sequence	Shutdown Peripheral Command DSI : Data Type=0x22	Sleep mode off Display on	Sleep mode on

(2) Power/Display On/Off Sequence

A power/display on/off sequence is shown below.

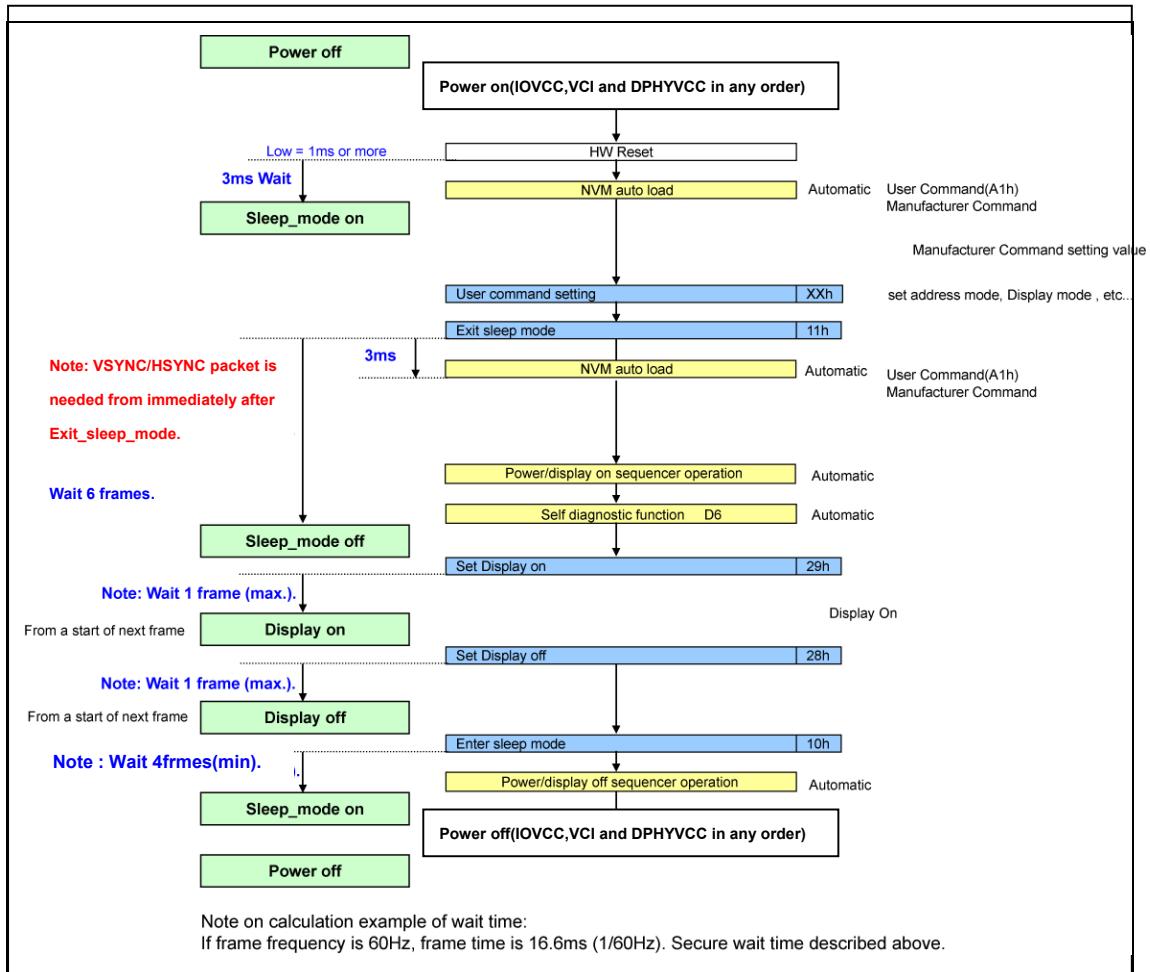


Figure 70

Deep Standby Mode On/Off Sequence

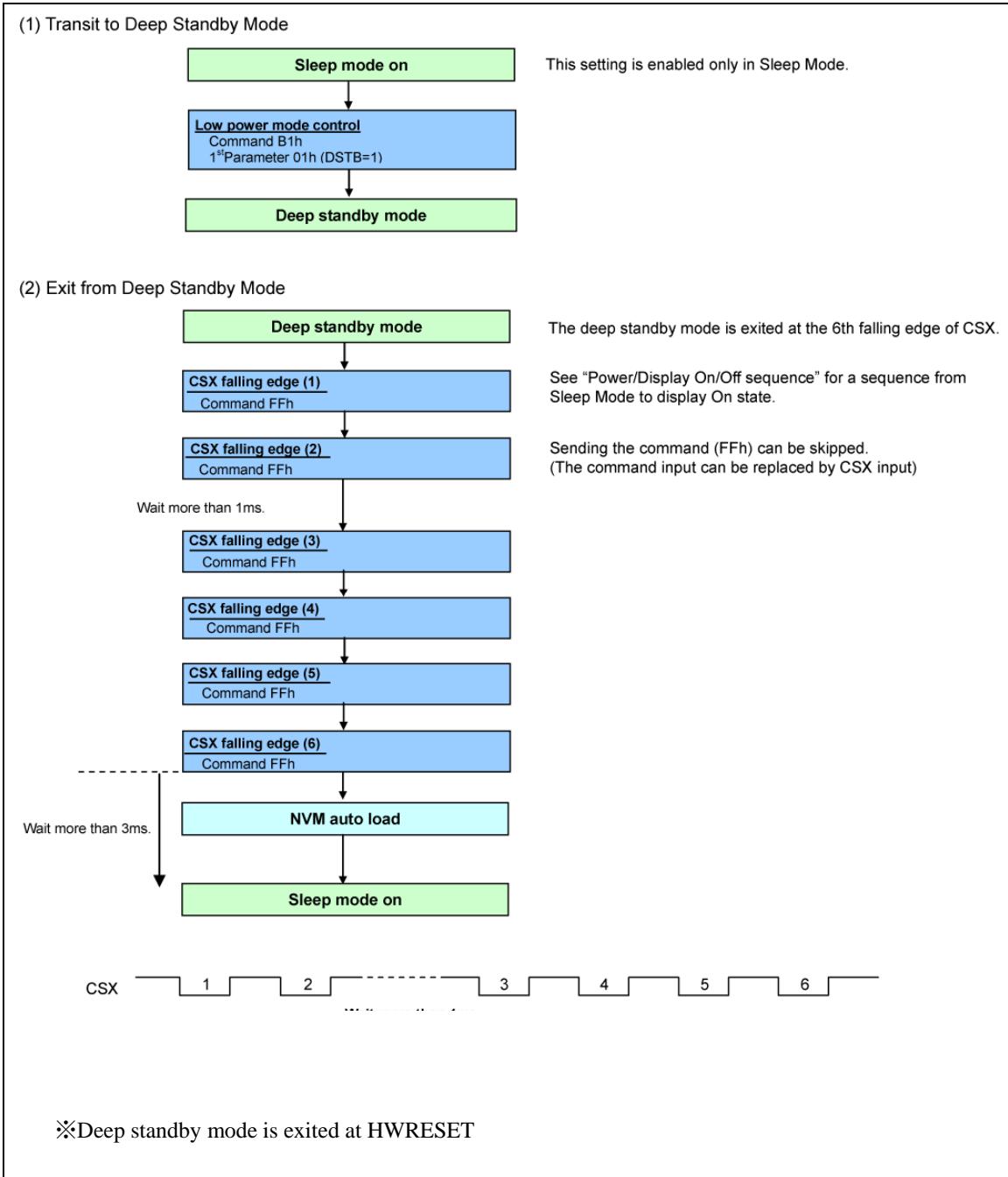


Figure 71

Gamma Correction Function

The RSP LCD driver supports gamma correction function to make the optimal colors according to the characteristics of the panel. The RSP LCD driver has registers for positive and negative polarities (Gamma Setting A Set, Gamma Setting B Set, and Gamma Setting C Set) to allow different settings for R, G, and B dots.

Gamma Correction Circuit

The following figure shows a gamma correction circuit. Two ends of the 168-step ladder resistors for positive grayscale are connected to VPLVL and VGS. Those for negative grayscale are connected to VGS (GND) and VNLVL.

Vx0, Vx4, Vx8, Vx15, Vx31, Vx79, Vx176, Vx224, Vx240, Vx247, Vx251, and Vx255 are grayscale reference levels. The reference levels can be adjusted by register. Voltage between VPLVL and VGS (GND), and voltage between VGS (GND) and VNLVL is divided by ladder resistors. The divided voltage is selected by selectors, and then, grayscale reference levels are output. For other grayscale levels, see “Grayscale Voltage Calculation Formula.” The amplifiers for the selectors are divided into three kinds: ones for R dots, ones for G dots, and ones for B dots.

Note: Vx0 to Vx255 mean positive grayscale voltages VP0 to VP255 and negative grayscale voltages VN0 to VN255.

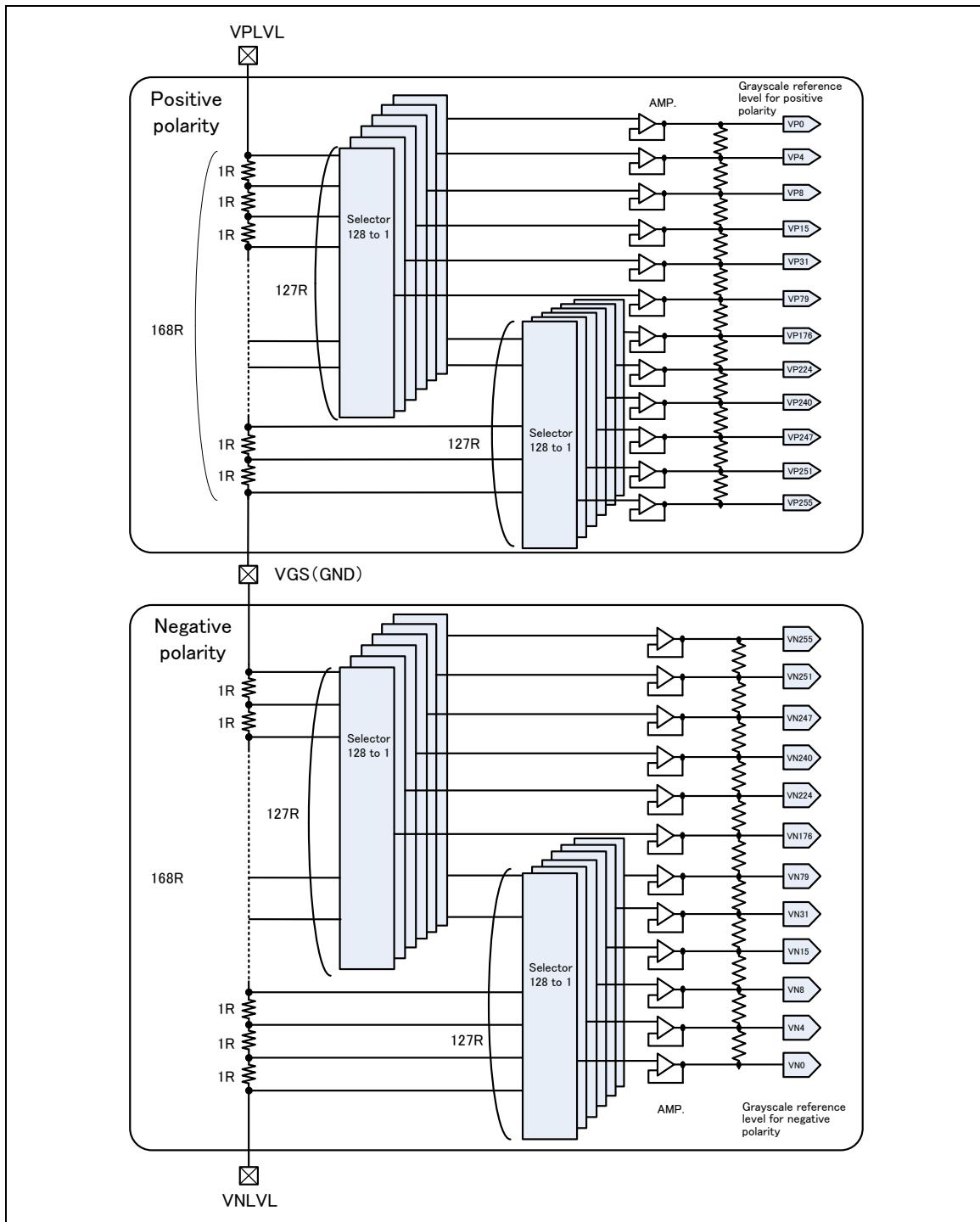


Figure 72

Gamma Correction Registers

A table below shows grayscale reference levels to be adjusted. Each reference level is set by a 7-bit gamma correction register that generates a grayscale reference level. Each of the gamma correction registers for positive polarity and negative polarity consists of twelve 7-bit registers (total: 84 bits).

Table 75

Grayscale reference level	Gamma correction register	
	Positive polarity	Negative polarity
Vx0	VGMxP0[6:0]	VGMxN0[6:0]
Vx4	VGMxP1[6:0]	VGMxN1[6:0]
Vx8	VGMxP2[6:0]	VGMxN2[6:0]
Vx15	VGMxP3[6:0]	VGMxN3[6:0]
Vx31	VGMxP4[6:0]	VGMxN4[6:0]
Vx79	VGMxP5[6:0]	VGMxN5[6:0]
Vx176	VGMxP6[6:0]	VGMxN6[6:0]
Vx224	VGMxP7[6:0]	VGMxN7[6:0]
Vx240	VGMxP8[6:0]	VGMxN8[6:0]
Vx247	VGMxP9[6:0]	VGMxN9[6:0]
Vx251	VGMxP10[6:0]	VGMxN10[6:0]
Vx255	VGMxP11[6:0]	VGMxN11[6:0]

Note: 'X' in register name VGMx indicates 'A' of "Gamma Setting A Set", 'B' of "Gamma Setting B Set," or 'C' of "Gamma Setting C Set."

Relationship between Gamma Correction Register and Voltage

Tables below shows relationships between values set in gamma correction registers and voltage.

Table 76

Register	Value	Voltage
VGMxP0[6:0]	7'h00	$\Delta V \times (1-0/168)$
VGMxP1[6:0]	7'h01	$\Delta V \times (1-1/168)$
VGMxP2[6:0]	7'h02	$\Delta V \times (1-2/168)$
VGMxP3[6:0]	7'h03	$\Delta V \times (1-3/168)$
VGMxP4[6:0]	7'h04	$\Delta V \times (1-4/168)$
VGMxP5[6:0]	7'h05	$\Delta V \times (1-5/168)$
	:	:
	:	:
VGMxN0[6:0]	7'h7A	$\Delta V \times (1-122/168)$
VGMxN1[6:0]	7'h7B	$\Delta V \times (1-123/168)$
VGMxN2[6:0]	7'h7C	$\Delta V \times (1-124/168)$
VGMxN3[6:0]	7'h7D	$\Delta V \times (1-125/168)$
VGMxN4[6:0]	7'h7E	$\Delta V \times (1-126/168)$
VGMxN5[6:0]	7'h7F	$\Delta V \times (1-127/168)$

Note: ‘ ΔV ’ indicates VPLVL-VGS (positive polarity) or VGS-VNLVL (negative polarity).

Table 77

Register	Value	Voltage
VGMxP6[6:0]	7'h00	$\Delta V \times (1-41/168)$
VGMxP7[6:0]	7'h01	$\Delta V \times (1-42/168)$
VGMxP8[6:0]	7'h02	$\Delta V \times (1-43/168)$
VGMxP9[6:0]	7'h03	$\Delta V \times (1-44/168)$
VGMxP10[6:0]	7'h04	$\Delta V \times (1-45/168)$
VGMxP11[6:0]	7'h05	$\Delta V \times (1-46/168)$
	:	:
	:	:
VGMxN6[6:0]	7'h7A	$\Delta V \times (1-163/168)$
VGMxN7[6:0]	7'h7B	$\Delta V \times (1-164/168)$
VGMxN8[6:0]	7'h7C	$\Delta V \times (1-165/168)$
VGMxN9[6:0]	7'h7D	$\Delta V \times (1-166/168)$
VGMxN10[6:0]	7'h7E	$\Delta V \times (1-167/168)$
VGMxN11[6:0]	7'h7F	$\Delta V \times (1-168/168)$

Note: ‘ ΔV ’ indicates VPLVL-VGS (positive polarity) or VGS-VNLVL (negative polarity).

Grayscale Voltage Calculation Formula**Table 78**

Grayscale voltage	Calculation formula	Grayscale voltage	Calculation formula
V0	See Table - Table .	V32	(V31*3+V35)/4
V1	(V0-V4)*18/26+V4	V33	(V31*2+V35*2)/4
V2	(V0-V4)*11/26+V4	V34	(V31+V35*3)/4
V3	(V0-V4)*5/26+V4	V35	(V31-V79)*24/27+V79
V4	See Table - Table .	V36	(V35*3+V39)/4
V5	(V4-V8)*10/14+V8	V37	(V35*2+V39*2)/4
V6	(V4-V8)*6/14+V8	V38	(V35+V39*3)/4
V7	(V4-V8)*3/14+V8	V39	(V31-V79)*21/27+V79
V8	See Table - Table .	V40	(V39*3+V43)/4
V9	(V8-V15)*13/16+V15	V41	(V39*2+V43*2)/4
V10	(V8-V15)*10/16+V15	V42	(V39+V43*3)/4
V11	(V8-V15)*8/16+V15	V43	(V31-V79)*18/27+V79
V12	(V8-V15)*6/16+V15	V44	(V43*3+V47)/4
V13	(V8-V15)*4/16+V15	V45	(V43*2+V47*2)/4
V14	(V8-V15)*2/16+V15	V46	(V43+V47*3)/4
V15	See Table - Table .	V47	(V31-V79)*15.5/27+V79
V16	(V15*3+V19)/4	V48	(V47*3+V51)/4
V17	(V15*2+V19*2)/4	V49	(V47*2+V51*2)/4
V18	(V15+V19*3)/4	V50	(V47+V51*3)/4
V19	(V15-V31)*12/17+V31	V51	(V31-V79)*13/27+V79
V20	(V19*3+V23)/4	V52	(V51*3+V55)/4
V21	(V19*2+V23*2)/4	V53	(V51*2+V55*2)/4
V22	(V19+V23*3)/4	V54	(V51+V55*3)/4
V23	(V15-V31)*7/17+V31	V55	(V31-V79)*10.5/27+V79
V24	(V23*3+V27)/4	V56	(V55*3+V59)/4
V25	(V23*2+V27*2)/4	V57	(V55*2+V59*2)/4
V26	(V23+V27*3)/4	V58	(V55+V59*3)/4
V27	(V15-V31)*3/17+V31	V59	(V31-V79)*8.5/27+V79
V28	(V27*3+V31)/4	V60	(V59*3+V63)/4
V29	(V27*2+V31*2)/4	V61	(V59*2+V63*2)/4
V30	(V27+V31*3)/4	V62	(V59+V63*3)/4
V31	See Table - Table .	V63	(V31-V79)*6.5/27+V79

Table 79

Grayscale voltage	Calculation formula	Grayscale voltage	Calculation formula
V64	(V63*3+V67)/4	V96	(V95*3+V99)/4
V65	(V63*2+V67*2)/4	V97	(V95*2+V99*2)/4
V66	(V63+V67*3)/4	V98	(V95+V99*3)/4
V67	(V31-V79)*4.5/27+V79	V99	(V79-V176)*19.25/24.25+V176
V68	(V67*3+V71)/4	V100	(V99*3+V103)/4
V69	(V67*2+V71*2)/4	V101	(V99*2+V103*2)/4
V70	(V67+V71*3)/4	V102	(V99+V103*3)/4
V71	(V31-V79)*3/27+V79	V103	(V79-V176)*18.25/24.25+V176
V72	(V71*3+V75)/4	V104	(V103*3+V107)/4
V73	(V71*2+V75*2)/4	V105	(V103*2+V107*2)/4
V74	(V71+V75*3)/4	V106	(V103+V107*3)/4
V75	(V31-V79)*1.5/27+V79	V107	(V79-V176)*17.25/24.25+V176
V76	(V75*3+V79)/4	V108	(V107*3+V111)/4
V77	(V75*2+V79*2)/4	V109	(V107*2+V111*2)/4
V78	(V75+V79*3)/4	V110	(V107+V111*3)/4
V79	See Table - Table .	V111	(V79-V176)*16.25/24.25+V176
V80	(V79*3+V83)/4	V112	(V111*3+V115)/4
V81	(V79*2+V83*2)/4	V113	(V111*2+V115*2)/4
V82	(V79+V83*3)/4	V114	(V111+V115*3)/4
V83	(V79-V176)*23.25/24.25+V176	V115	(V79-V176)*15.25/24.25+V176
V84	(V83*3+V87)/4	V116	(V115*3+V119)/4
V85	(V83*2+V87*2)/4	V117	(V115*2+V119*2)/4
V86	(V83+V87*3)/4	V118	(V115+V119*3)/4
V87	(V79-V176)*22.25/24.25+V176	V119	(V79-V176)*14.25/24.25+V176
V88	(V87*3+V91)/4	V120	(V119*3+V123)/4
V89	(V87*2+V91*2)/4	V121	(V119*2+V123*2)/4
V90	(V87+V91*3)/4	V122	(V119+V123*3)/4
V91	(V79-V176)*21.25/24.25+V176	V123	(V79-V176)*13.25/24.25+V176
V92	(V91*3+V95)/4	V124	(V123*3+V127)/4
V93	(V91*2+V95*2)/4	V125	(V123*2+V127*2)/4
V94	(V91+V95*3)/4	V126	(V123+V127*3)/4
V95	(V79-V176)*20.25/24.25+V176	V127	(V79-V176)*12.25/24.25+V176

Table 80

Grayscale voltage	Calculation formula	Grayscale voltage	Calculation formula
V128	(V79-176)*12/24.25+V176	V160	(V79-176)*4/24.25+V176
V129	(V128*3+V132)/4	V161	(V160*3+V164)/4
V130	(V128*2+V132*2)/4	V162	(V160*2+V164*2)/4
V131	(V128+V132*3)/4	V163	(V160+V164*3)/4
V132	(V79-176)*11/24.25+V176	V164	(V79-176)*3/24.25+V176
V133	(V132*3+V136)/4	V165	(V164*3+V168)/4
V134	(V132*2+V136*2)/4	V166	(V164*2+V168*2)/4
V135	(V132+V136*3)/4	V167	(V164+V168*3)/4
V136	(V79-176)*10/24.25+V176	V168	(V79-176)*2/24.25+V176
V137	(V136*3+V140)/4	V169	(V168*3+V172)/4
V138	(V136*2+V140*2)/4	V170	(V168*2+V172*2)/4
V139	(V136+V140*3)/4	V171	(V168+V172*3)/4
V140	(V79-176)*9/24.25+V176	V172	(V79-176)*1/24.25+V176
V141	(V140*3+V144)/4	V173	(V172*3+V176)/4
V142	(V140*2+V144*2)/4	V174	(V172*2+V176*2)/4
V143	(V140+V144*3)/4	V175	(V172+V176*3)/4
V144	(V79-176)*8/24.25+V176	V176	See Table - Table .
V145	(V144*3+V148)/4	V177	(V176*3+V180)/4
V146	(V144*2+V148*2)/4	V178	(V176*2+V180*2)/4
V147	(V144+V148*3)/4	V179	(V176+V180*3)/4
V148	(V79-176)*7/24.25+V176	V180	(V176-V224)*25.5/27+V224
V149	(V148*3+V152)/4	V181	(V180*3+V184)/4
V150	(V148*2+V152*2)/4	V182	(V180*2+V184*2)/4
V151	(V148+V152*3)/4	V183	(V180+V184*3)/4
V152	(V79-176)*6/24.25+V176	V184	(V176-V224)*24/27+V224
V153	(V152*3+V156)/4	V185	(V184*3+V188)/4
V154	(V152*2+V156*2)/4	V186	(V184*2+V188*2)/4
V155	(V152+V156*3)/4	V187	(V184+V188*3)/4
V156	(V79-176)*5/24.25+V176	V188	(V176-V224)*22.5/27+V224
V157	(V156*3+V160)/4	V189	(V188*3+V192)/4
V158	(V156*2+V160*2)/4	V190	(V188*2+V192*2)/4
V159	(V156+V160*3)/4	V191	(V188+V192*3)/4

Table 81

Grayscale voltage	Calculation formula	Grayscale voltage	Calculation formula
V192	$(V176-V224)*20.5/27+V224$	V224	See tables 114 and 115.
V193	$(V192*3+V196)/4$	V225	$(V224*3+V228)/4$
V194	$(V192*2+V196*2)/4$	V226	$(V224*2+V228*2)/4$
V195	$(V192+V196*3)/4$	V227	$(V224+V228*3)/4$
V196	$(V176-V224)*18.5/27+V224$	V228	$(V224-V240)*14/17+V240$
V197	$(V197*3+V200)/4$	V229	$(V228*3+V232)/4$
V198	$(V197*2+V200*2)/4$	V230	$(V228*2+V232*2)/4$
V199	$(V197+V200*3)/4$	V231	$(V228+V232*3)/4$
V200	$(V176-V224)*16.5/27+V224$	V232	$(V224-V240)*10/17+V240$
V201	$(V200*3+V204)/4$	V233	$(V232*3+V236)/4$
V202	$(V200*2+V204*2)/4$	V234	$(V232*2+V236*2)/4$
V203	$(V200+V204*3)/4$	V235	$(V232+V236*3)/4$
V204	$(V176-V224)*14/27+V224$	V236	$(V224-V240)*5/17+V240$
V205	$(V204*3+V208)/4$	V237	$(V236*3+V240)/4$
V206	$(V204*2+V208*2)/4$	V238	$(V236*2+V240*2)/4$
V207	$(V204+V208*3)/4$	V239	$(V236+V240*3)/4$
V208	$(V176-V224)*11.5/27+V224$	V240	See Table - Table .
V209	$(V208*3+V212)/4$	V241	$(V240-V247)*14/16+V247$
V210	$(V208*2+V212*2)/4$	V242	$(V240-V247)*12/16+V247$
V211	$(V208+V212*3)/4$	V243	$(V240-V247)*10/16+V247$
V212	$(V176-V224)*9/27+V224$	V244	$(V240-V247)*8/16+V247$
V213	$(V212*3+V216)/4$	V245	$(V240-V247)*6/16+V247$
V214	$(V212*2+V216*2)/4$	V246	$(V240-V247)*3/16+V247$
V215	$(V212+V216*3)/4$	V247	See Table - Table .
V216	$(V176-V224)*6/27+V224$	V248	$(V247-V251)*11/14+V251$
V217	$(V216*3+V220)/4$	V249	$(V247-V251)*8/14+V251$
V218	$(V216*2+V220*2)/4$	V250	$(V247-V251)*4/14+V251$
V219	$(V216+V220*3)/4$	V251	See Table - Table .
V220	$(V176-V224)*3/27+V224$	V252	$(V251-V255)*21/26+V255$
V221	$(V220*3+V224)/4$	V253	$(V251-V255)*15/26+V255$
V222	$(V220*2+V224*2)/4$	V254	$(V251-V255)*8/26+V255$
V223	$(V220+V224*3)/4$	V255	See Table - Table .

Gamma Correction Register Setting Example

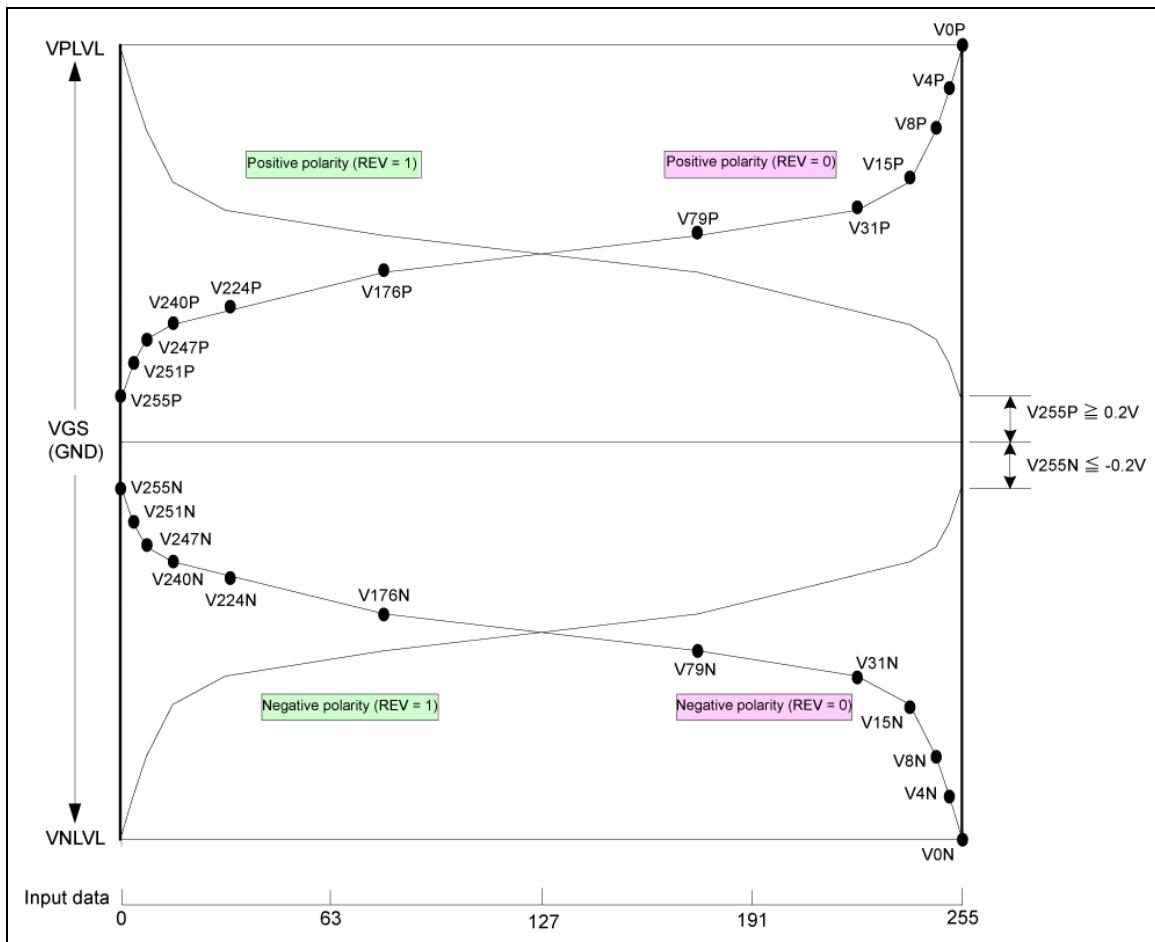


Figure 73

Notes:

1. Vx0, Vx4, Vx8, Vx15, Vx31, Vx79, Vx176, Vx224, Vx240, Vx247, Vx251, Vx255 are “reference levels” set by gamma correction registers.
2. Set gamma correction registers to satisfy the following relationship: $|Vx0| > |Vx4| > |Vx8| > |Vx15| > |Vx31| > |Vx79| > |Vx176| > |Vx224| > |Vx240| > |Vx247| > |Vx251| > |Vx255| >$
3. Set gamma correction registers to satisfy the following relationship: $V255P \geq 0.2V$. $V255N \leq -0.2V$.

Relationship between Display Data and Grayscale Voltage**Table 82 (REV bit function)**

Display Data	REV = 1		REV = 0	
	Positive polarity (PRxPxx)	Negative Polarity (PRxNxx)	Positive Polarity (PRxPxx)	Negative Polarity (PRxNxx)
8'h00	V0	V0	V255	V255
8'h01	V1	V1	V254	V254
8'h02	V2	V2	V253	V253
8'h03	V3	V3	V252	V252
8'h04	V4	V4	V251	V251
8'h05	V5	V5	V250	V250
8'h06	V6	V6	V249	V249
8'h07	V7	V7	V248	V248
8'h08	V8	V8	V247	V247
8'h09	V9	V9	V246	V246
8'h0A	V10	V10	V245	V245
8'h0B	V11	V11	V244	V244
8'h0C	V12	V12	V243	V243
8'h0D	V13	V13	V242	V242
8'h0E	V14	V14	V241	V241
8'h0F	V15	V15	V240	V240
:	:	:	:	:
8'hF0	V240	V240	V15	V15
8'hF1	V241	V241	V14	V14
8'hF2	V242	V242	V13	V13
8'hF3	V243	V243	V12	V12
8'hF4	V244	V244	V11	V11
8'hF5	V245	V245	V10	V10
8'hF6	V246	V246	V9	V9
8'hF7	V247	V247	V8	V8
8'hF8	V248	V248	V7	V7
8'hF9	V249	V249	V6	V6
8'hFA	V250	V250	V5	V5
8'hFB	V251	V251	V4	V4
8'hFC	V252	V252	V3	V3
8'hFD	V253	V253	V2	V2
8'hFE	V254	V254	V1	V1
8'hFF	V255	V255	V0	V0

NVM Control

The RSP LCD driver incorporates NVM.

- 16 bits are for Supplier ID (read by read_DDB_start command (A1h))
- 16 bits are for Supplier Elective Data (read by read_DDB_start command (A1h))
- Manufacturer Command is stored (For the Manufacturer Command stored in NVM, see “Command Stored in NVM”)

To write, read and erase data from/to the NVM, follow the sequence below. Data on the NVM is loaded to internal registers automatically when the sequences are performed. NVMLD register determines whether to update data loaded from NVM to each register.

Power On sequence
 HW RESET sequence
 exit_sleep_mode command
 soft_reset sequence
 Deep Standby Mode Off sequence

Data stored in the NVM is retained permanently even if power supply is turned off.

Table 83

Operation	Power supply voltage		Time	Temperature
Write/Erase	VCI DPHYVCC IOVCC	3.00 ~ 3.60V 1.65 ~ 3.30V 1.65~ 3.30V		
Write/Erase (External VSP/VSN supply mode)	VSP VSN DPHYVCC IOVCC	5.00 ~ 6.00V -5.00 ~ -6.00V 1.65 ~ 3.30V 1.65~ 3.30V	1.4 s or more after NVMFTT = 1	+10°C ~ +40°C

Note: NVM data rewrite (erase-write) operation should be performed up to 10 times.

NVM Write Sequence

The register values of User/Manufacturer Commands supposed to be stored in NVM are written to NVM. When “1” is written to an address, the bit of the address is set to “1”. If the data is erased from the bit, the bit is returned to “0”. The bit to which data is not written should be set to “0”.

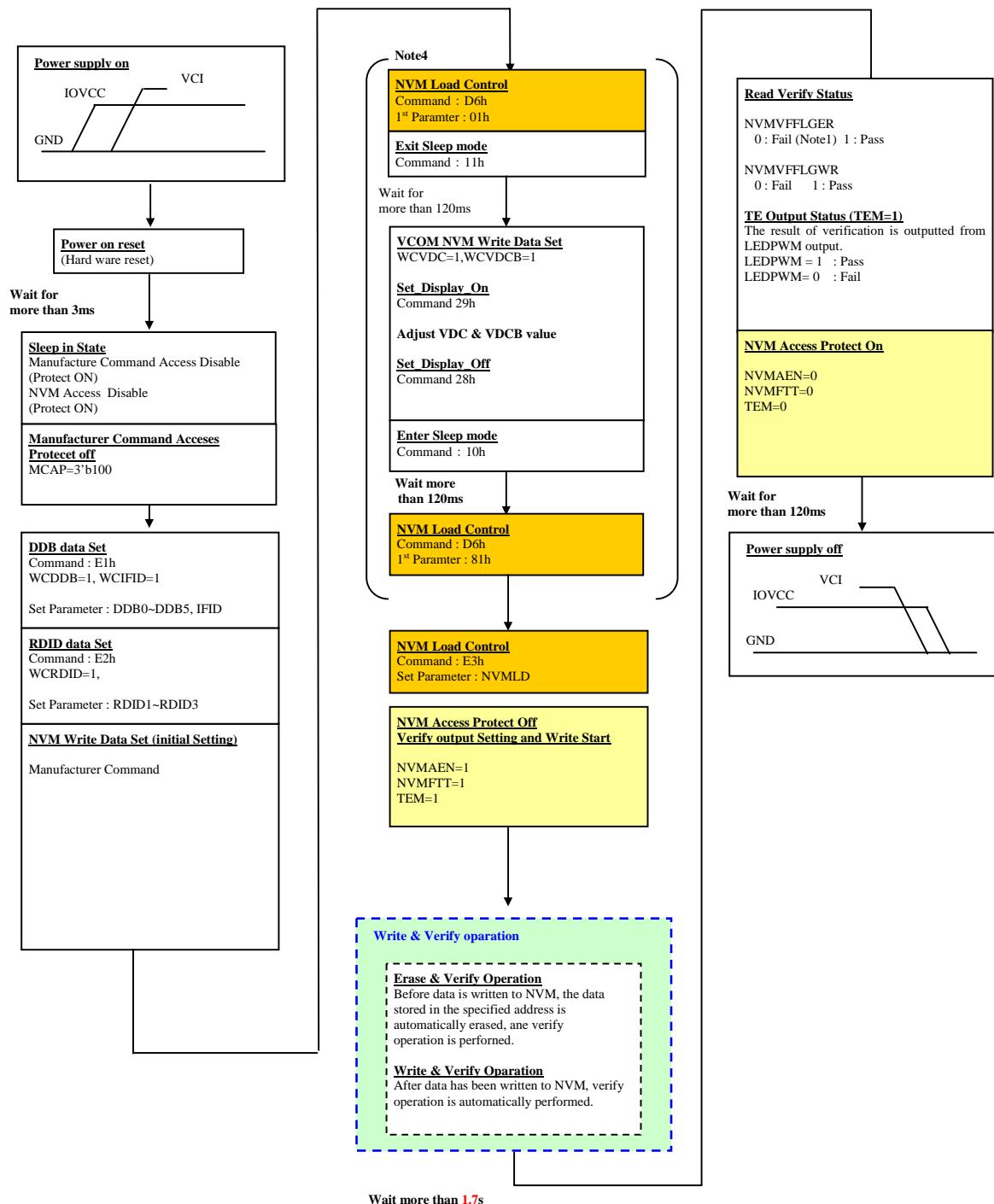
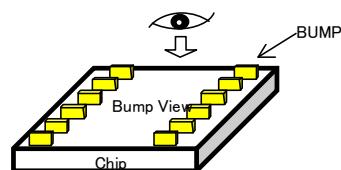
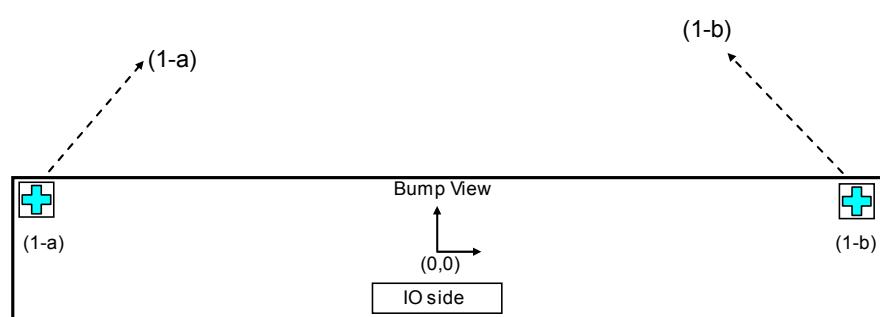
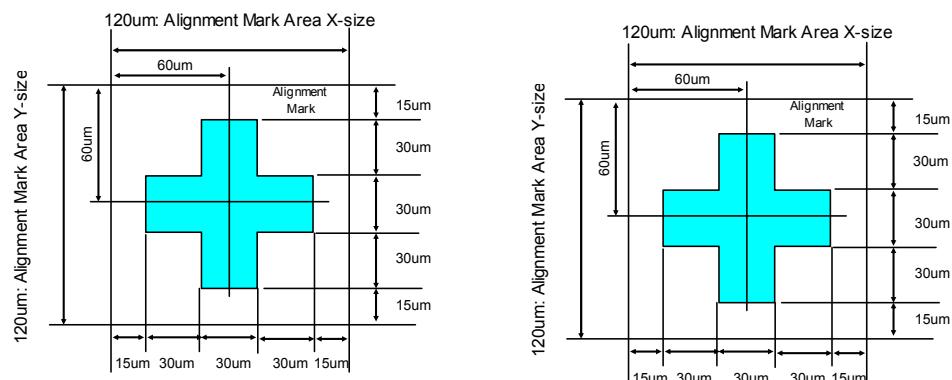


Figure 74

- Notes:
1. If verify operation to verify whether data is erased fails before write operation, write operation is not performed.
 2. If power is turned on when data has not been written, data set to “0” is loaded from NVM.
Set the defaults of all the commands at “Initial Setting” after power is turned on. Then, write the data to NVM.
 3. To change the number of lanes when data is written to NVM via DSI, execute this sequence after changing the number of lanes.
4. When VCOM is not adjusted by VDV/VDCB, this sequence is unnecessary.

Alignment Mark

- Chip size: 29.80 × 0.85mm
- Chip thickness: 170 μ m(typ.)
- Pad coordinate: Pad center
- Coordinate origin: Chip center
- Au bump pitch: Refer to Pad coordinate
- Au bump height: 15 μ m
- Alignment mark

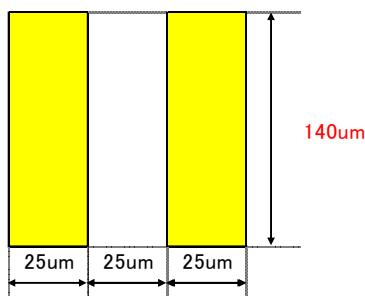


Target Die Size

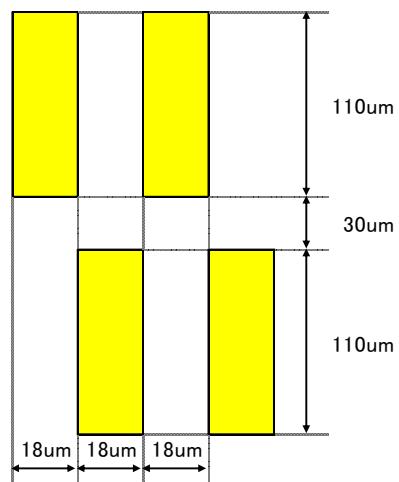
X (mm)	Y (mm)	Area (mm ²)	Aspect (X/Y)
29.80	0.85	25.33	35.06

Bump Size

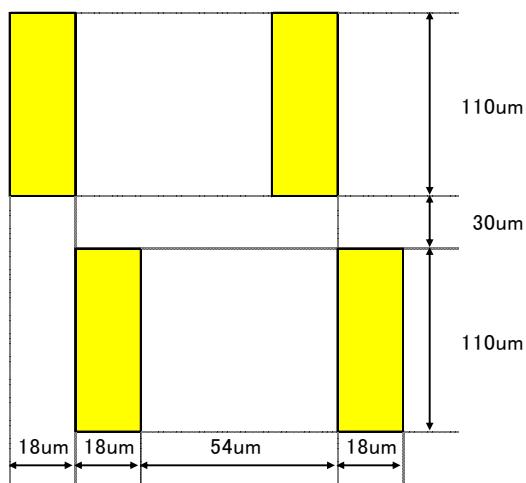
1) Input-Bump (No.1-585)



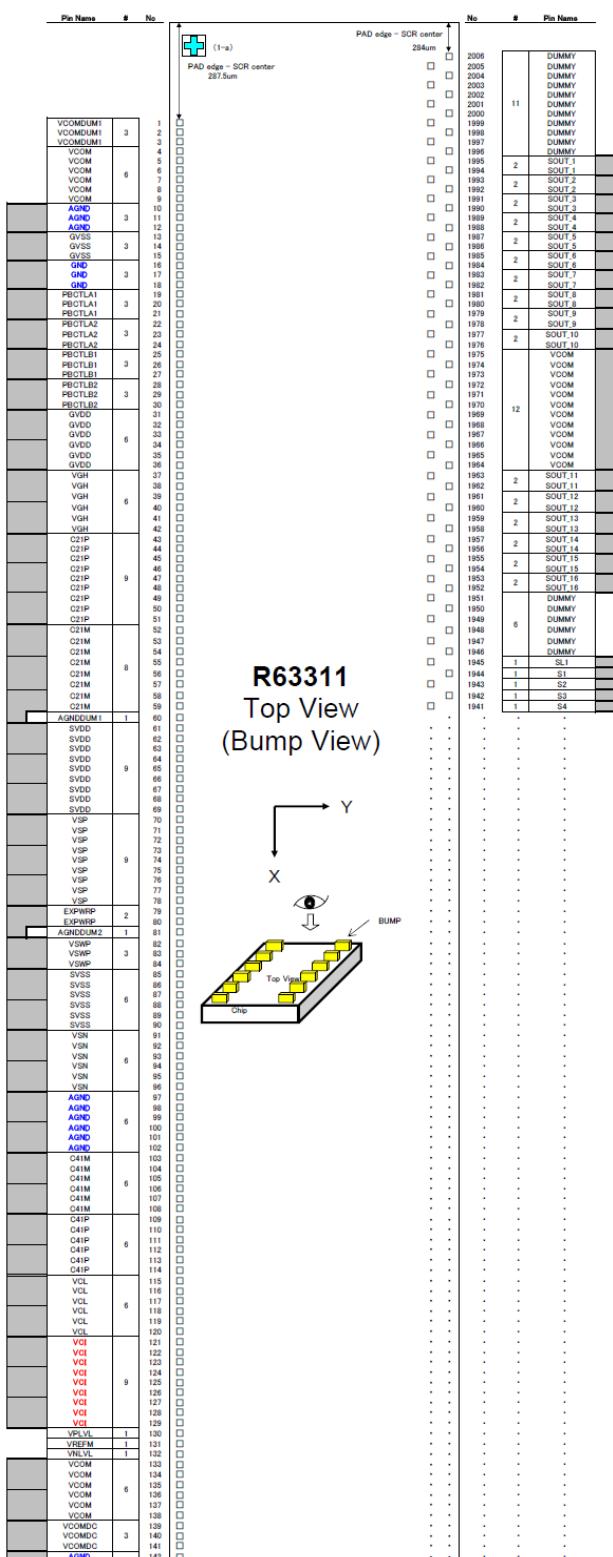
2) Output—Bump1 (No.586-1194, 1399-2006)

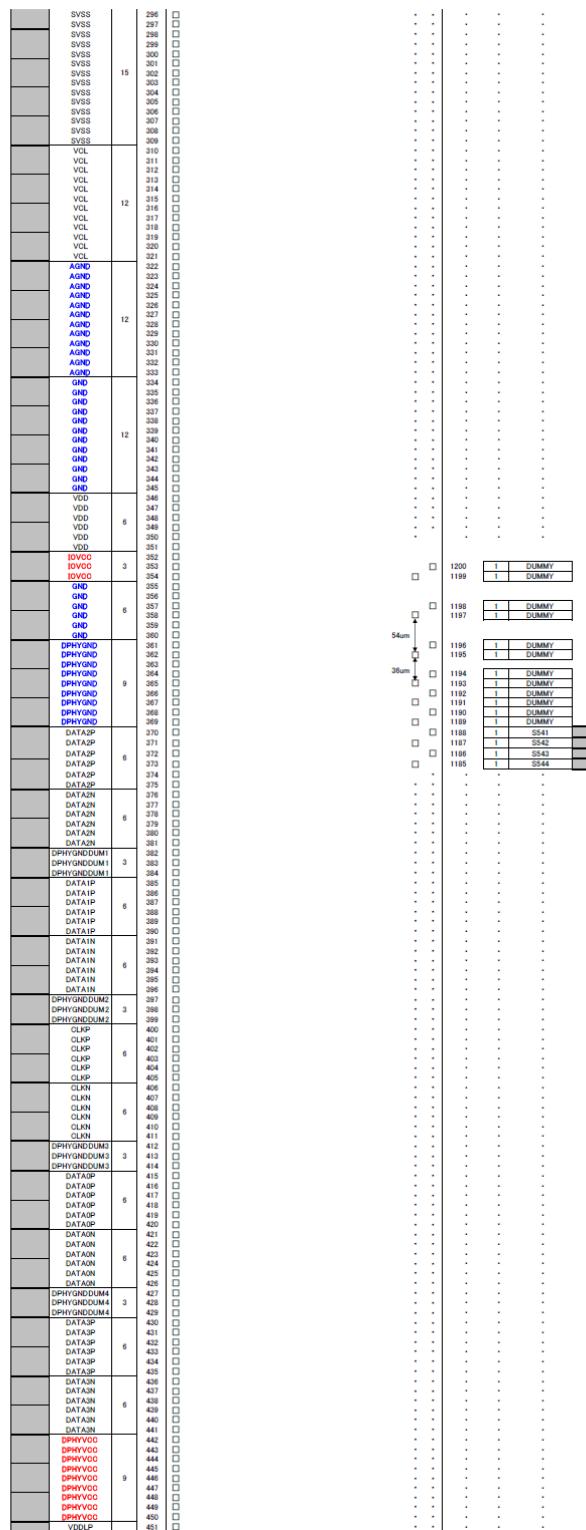


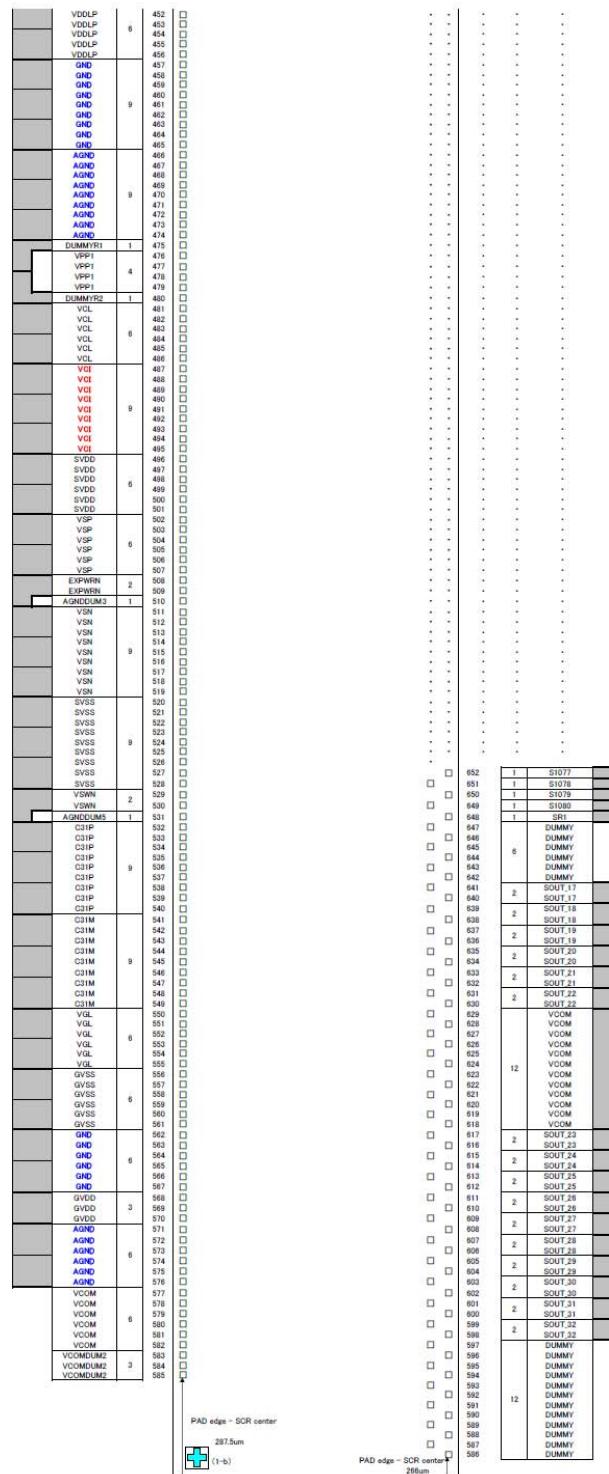
3) Output—Bump2 (No.1195-1398)



Pad Arrangement







Pad Coordinate

R63311 Pad Coordinate (No.1)(Unit: μm)

pad No	pad name	X	Y
1	VCOMDUM1	-14600	-301
2	VCOMDUM1	-14550	-301
3	VCOMDUM1	-14500	-301
4	VCOM	-14450	-301
5	VCOM	-14400	-301
6	VCOM	-14350	-301
7	VCOM	-14300	-301
8	VCOM	-14250	-301
9	VCOM	-14200	-301
10	AGND	-14150	-301
11	AGND	-14100	-301
12	AGND	-14050	-301
13	GVSS	-14000	-301
14	GVSS	-13950	-301
15	GVSS	-13900	-301
16	GND	-13850	-301
17	GND	-13800	-301
18	GND	-13750	-301
19	PBCTLA1	-13700	-301
20	PBCTLA1	-13650	-301
21	PBCTLA1	-13600	-301
22	PBCTLA2	-13550	-301
23	PBCTLA2	-13500	-301
24	PBCTLA2	-13450	-301
25	PBCTLB1	-13400	-301
26	PBCTLB1	-13350	-301
27	PBCTLB1	-13300	-301
28	PBCTLB2	-13250	-301
29	PBCTLB2	-13200	-301
30	PBCTLB2	-13150	-301
31	GVDD	-13100	-301
32	GVDD	-13050	-301
33	GVDD	-13000	-301
34	GVDD	-12950	-301
35	GVDD	-12900	-301
36	GVDD	-12850	-301
37	VGH	-12800	-301
38	VGH	-12750	-301
39	VGH	-12700	-301
40	VGH	-12650	-301
41	VGH	-12600	-301
42	VGH	-12550	-301
43	C21P	-12500	-301
44	C21P	-12450	-301
45	C21P	-12400	-301
46	C21P	-12350	-301
47	C21P	-12300	-301
48	C21P	-12250	-301
49	C21P	-12200	-301
50	C21P	-12150	-301

pad No	pad name	X	Y
51	C21P	-12100	-301
52	C21M	-12050	-301
53	C21M	-12000	-301
54	C21M	-11950	-301
55	C21M	-11900	-301
56	C21M	-11850	-301
57	C21M	-11800	-301
58	C21M	-11750	-301
59	C21M	-11700	-301
60	AGNDDUM1	-11650	-301
61	SVDD	-11600	-301
62	SVDD	-11550	-301
63	SVDD	-11500	-301
64	SVDD	-11450	-301
65	SVDD	-11400	-301
66	SVDD	-11350	-301
67	SVDD	-11300	-301
68	SVDD	-11250	-301
69	SVDD	-11200	-301
70	VSP	-11150	-301
71	VSP	-11100	-301
72	VSP	-11050	-301
73	VSP	-11000	-301
74	VSP	-10950	-301
75	VSP	-10900	-301
76	VSP	-10850	-301
77	VSP	-10800	-301
78	VSP	-10750	-301
79	EXPWRP	-10700	-301
80	EXPWRP	-10650	-301
81	AGNDDUM2	-10600	-301
82	VSWP	-10550	-301
83	VSWP	-10500	-301
84	VSWP	-10450	-301
85	SVSS	-10400	-301
86	SVSS	-10350	-301
87	SVSS	-10300	-301
88	SVSS	-10250	-301
89	SVSS	-10200	-301
90	SVSS	-10150	-301
91	VSN	-10100	-301
92	VSN	-10050	-301
93	VSN	-10000	-301
94	VSN	-9950	-301
95	VSN	-9900	-301
96	VSN	-9850	-301
97	AGND	-9800	-301
98	AGND	-9750	-301
99	AGND	-9700	-301
100	AGND	-9650	-301

R63311 Pad Coordinate (No.2)(Unit: μm)

pad No	pad name	X	Y
101	AGND	-9600	-301
102	AGND	-9550	-301
103	C41M	-9500	-301
104	C41M	-9450	-301
105	C41M	-9400	-301
106	C41M	-9350	-301
107	C41M	-9300	-301
108	C41M	-9250	-301
109	C41P	-9200	-301
110	C41P	-9150	-301
111	C41P	-9100	-301
112	C41P	-9050	-301
113	C41P	-9000	-301
114	C41P	-8950	-301
115	VCL	-8900	-301
116	VCL	-8850	-301
117	VCL	-8800	-301
118	VCL	-8750	-301
119	VCL	-8700	-301
120	VCL	-8650	-301
121	VCI	-8600	-301
122	VCI	-8550	-301
123	VCI	-8500	-301
124	VCI	-8450	-301
125	VCI	-8400	-301
126	VCI	-8350	-301
127	VCI	-8300	-301
128	VCI	-8250	-301
129	VCI	-8200	-301
130	VPLVL	-8150	-301
131	VREFM	-8100	-301
132	VNLVL	-8050	-301
133	VCOM	-8000	-301
134	VCOM	-7950	-301
135	VCOM	-7900	-301
136	VCOM	-7850	-301
137	VCOM	-7800	-301
138	VCOM	-7750	-301
139	VCOMDC	-7700	-301
140	VCOMDC	-7650	-301
141	VCOMDC	-7600	-301
142	AGND	-7550	-301
143	AGND	-7500	-301
144	AGND	-7450	-301
145	AGND	-7400	-301
146	AGND	-7350	-301
147	AGND	-7300	-301
148	VDD	-7250	-301
149	VDD	-7200	-301
150	VDD	-7150	-301

pad No	pad name	X	Y
151	VDD	-7100	-301
152	VDD	-7050	-301
153	VDD	-7000	-301
154	IOVCCRF	-6950	-301
155	IOVCCRF	-6900	-301
156	IOVCCRF	-6850	-301
157	IOVCC	-6800	-301
158	IOVCC	-6750	-301
159	IOVCC	-6700	-301
160	IOVCC	-6650	-301
161	IOVCC	-6600	-301
162	IOVCC	-6550	-301
163	IOVCC	-6500	-301
164	IOVCC	-6450	-301
165	IOVCC	-6400	-301
166	GNDRF	-6350	-301
167	GNDRF	-6300	-301
168	GNDRF	-6250	-301
169	GND	-6200	-301
170	GND	-6150	-301
171	GND	-6100	-301
172	GND	-6050	-301
173	GND	-6000	-301
174	TESTE	-5950	-301
175	VREFD	-5900	-301
176	LEDPWM	-5850	-301
177	VREF	-5800	-301
178	VREFC	-5750	-301
179	EXCK	-5700	-301
180	VDDTEST	-5650	-301
181	GNDDUM1	-5600	-301
182	DBIST	-5550	-301
183	GNDDUM2	-5500	-301
184	GNDDUM3	-5450	-301
185	LNSW1	-5400	-301
186	GNDDUM4	-5350	-301
187	GNDDUM5	-5300	-301
188	LNSW0	-5250	-301
189	GNDDUM6	-5200	-301
190	GNDDUM7	-5150	-301
191	PNSW	-5100	-301
192	GNDDUM8	-5050	-301
193	GNDDUM9	-5000	-301
194	IM2	-4950	-301
195	GNDDUM10	-4900	-301
196	GNDDUM11	-4850	-301
197	IM1	-4800	-301
198	GNDDUM12	-4750	-301
199	GNDDUM13	-4700	-301
200	IMO	-4650	-301

R63311 Pad Coordinate (No.3)(Unit: μm)

pad No	pad name	X	Y
201	VSYNC	-4600	-301
202	HSYNC	-4550	-301
203	VSOUT	-4500	-301
204	TEST6	-4450	-301
205	TEST4	-4400	-301
206	HSOUT	-4350	-301
207	PCLK	-4300	-301
208	TEST3	-4250	-301
209	TE2	-4200	-301
210	TEST2	-4150	-301
211	TEST1	-4100	-301
212	TE	-4050	-301
213	DE	-4000	-301
214	TS1	-3950	-301
215	CSX	-3900	-301
216	TS0	-3850	-301
217	DB7	-3800	-301
218	DCX	-3750	-301
219	DB6	-3700	-301
220	DB5	-3650	-301
221	WRX/SCL	-3600	-301
222	DB4	-3550	-301
223	DB3	-3500	-301
224	DOUT	-3450	-301
225	DB2	-3400	-301
226	DIN	-3350	-301
227	DIN	-3300	-301
228	DIN	-3250	-301
229	DB1	-3200	-301
230	RESX	-3150	-301
231	GNDDUM14	-3100	-301
232	IOVCC	-3050	-301
233	IOVCC	-3000	-301
234	IOVCC	-2950	-301
235	IOVCC	-2900	-301
236	IOVCC	-2850	-301
237	IOVCC	-2800	-301
238	GND	-2750	-301
239	GND	-2700	-301
240	GND	-2650	-301
241	GND	-2600	-301
242	GND	-2550	-301
243	GND	-2500	-301
244	GND	-2450	-301
245	GND	-2400	-301
246	GND	-2350	-301
247	GND	-2300	-301
248	GND	-2250	-301
249	GND	-2200	-301
250	AGND	-2150	-301

pad No	pad name	X	Y
251	AGND	-2100	-301
252	AGND	-2050	-301
253	AGND	-2000	-301
254	AGND	-1950	-301
255	AGND	-1900	-301
256	AGND	-1850	-301
257	AGND	-1800	-301
258	AGND	-1750	-301
259	AGND	-1700	-301
260	AGND	-1650	-301
261	AGND	-1600	-301
262	VCI	-1550	-301
263	VCI	-1500	-301
264	VCI	-1450	-301
265	VCI	-1400	-301
266	VCI	-1350	-301
267	VCI	-1300	-301
268	VCI	-1250	-301
269	VCI	-1200	-301
270	VCI	-1150	-301
271	VCI	-1100	-301
272	VCI	-1050	-301
273	VCI	-1000	-301
274	SVDD	-950	-301
275	SVDD	-900	-301
276	SVDD	-850	-301
277	SVDD	-800	-301
278	SVDD	-750	-301
279	SVDD	-700	-301
280	SVDD	-650	-301
281	SVDD	-600	-301
282	SVDD	-550	-301
283	SVDD	-500	-301
284	SVDD	-450	-301
285	SVDD	-400	-301
286	SVDD	-350	-301
287	SVDD	-300	-301
288	SVDD	-250	-301
289	VGS	-200	-301
290	VGS	-150	-301
291	VGS	-100	-301
292	VGS	-50	-301
293	VGS	0	-301
294	VGS	50	-301
295	SVSS	100	-301
296	SVSS	150	-301
297	SVSS	200	-301
298	SVSS	250	-301
299	SVSS	300	-301
300	SVSS	350	-301

R63311 Pad Coordinate (No.4) (Unit: μm)

pad No	pad name	X	Y
301	SVSS	400	-301
302	SVSS	450	-301
303	SVSS	500	-301
304	SVSS	550	-301
305	SVSS	600	-301
306	SVSS	650	-301
307	SVSS	700	-301
308	SVSS	750	-301
309	SVSS	800	-301
310	VCL	850	-301
311	VCL	900	-301
312	VCL	950	-301
313	VCL	1000	-301
314	VCL	1050	-301
315	VCL	1100	-301
316	VCL	1150	-301
317	VCL	1200	-301
318	VCL	1250	-301
319	VCL	1300	-301
320	VCL	1350	-301
321	VCL	1400	-301
322	AGND	1450	-301
323	AGND	1500	-301
324	AGND	1550	-301
325	AGND	1600	-301
326	AGND	1650	-301
327	AGND	1700	-301
328	AGND	1750	-301
329	AGND	1800	-301
330	AGND	1850	-301
331	AGND	1900	-301
332	AGND	1950	-301
333	AGND	2000	-301
334	GND	2050	-301
335	GND	2100	-301
336	GND	2150	-301
337	GND	2200	-301
338	GND	2250	-301
339	GND	2300	-301
340	GND	2350	-301
341	GND	2400	-301
342	GND	2450	-301
343	GND	2500	-301
344	GND	2550	-301
345	GND	2600	-301
346	VDD	2650	-301
347	VDD	2700	-301
348	VDD	2750	-301
349	VDD	2800	-301
350	VDD	2850	-301

pad No	pad name	X	Y
351	VDD	2900	-301
352	IOVCC	2950	-301
353	IOVCC	3000	-301
354	IOVCC	3050	-301
355	GND	3100	-301
356	GND	3150	-301
357	GND	3200	-301
358	GND	3250	-301
359	GND	3300	-301
360	GND	3350	-301
361	DPHYGND	3400	-301
362	DPHYGND	3450	-301
363	DPHYGND	3500	-301
364	DPHYGND	3550	-301
365	DPHYGND	3600	-301
366	DPHYGND	3650	-301
367	DPHYGND	3700	-301
368	DPHYGND	3750	-301
369	DPHYGND	3800	-301
370	DATA2P	3850	-301
371	DATA2P	3900	-301
372	DATA2P	3950	-301
373	DATA2P	4000	-301
374	DATA2P	4050	-301
375	DATA2P	4100	-301
376	DATA2N	4150	-301
377	DATA2N	4200	-301
378	DATA2N	4250	-301
379	DATA2N	4300	-301
380	DATA2N	4350	-301
381	DATA2N	4400	-301
382	DPHYGNDDUM1	4450	-301
383	DPHYGNDDUM1	4500	-301
384	DPHYGNDDUM1	4550	-301
385	DATA1P	4600	-301
386	DATA1P	4650	-301
387	DATA1P	4700	-301
388	DATA1P	4750	-301
389	DATA1P	4800	-301
390	DATA1P	4850	-301
391	DATA1N	4900	-301
392	DATA1N	4950	-301
393	DATA1N	5000	-301
394	DATA1N	5050	-301
395	DATA1N	5100	-301
396	DATA1N	5150	-301
397	DPHYGNDDUM2	5200	-301
398	DPHYGNDDUM2	5250	-301
399	DPHYGNDDUM2	5300	-301
400	CLKP	5350	-301

R63311 Pad Coordinate (No.5)(Unit: μm)

pad No	pad name	X	Y
401	CLKP	5400	-301
402	CLKP	5450	-301
403	CLKP	5500	-301
404	CLKP	5550	-301
405	CLKP	5600	-301
406	CLKN	5650	-301
407	CLKN	5700	-301
408	CLKN	5750	-301
409	CLKN	5800	-301
410	CLKN	5850	-301
411	CLKN	5900	-301
412	DPHYGNDDUM3	5950	-301
413	DPHYGNDDUM3	6000	-301
414	DPHYGNDDUM3	6050	-301
415	DATA0P	6100	-301
416	DATA0P	6150	-301
417	DATA0P	6200	-301
418	DATA0P	6250	-301
419	DATA0P	6300	-301
420	DATA0P	6350	-301
421	DATA0N	6400	-301
422	DATA0N	6450	-301
423	DATA0N	6500	-301
424	DATA0N	6550	-301
425	DATA0N	6600	-301
426	DATA0N	6650	-301
427	DPHYGNDDUM4	6700	-301
428	DPHYGNDDUM4	6750	-301
429	DPHYGNDDUM4	6800	-301
430	DATA3P	6850	-301
431	DATA3P	6900	-301
432	DATA3P	6950	-301
433	DATA3P	7000	-301
434	DATA3P	7050	-301
435	DATA3P	7100	-301
436	DATA3N	7150	-301
437	DATA3N	7200	-301
438	DATA3N	7250	-301
439	DATA3N	7300	-301
440	DATA3N	7350	-301
441	DATA3N	7400	-301
442	DPHYVCC	7450	-301
443	DPHYVCC	7500	-301
444	DPHYVCC	7550	-301
445	DPHYVCC	7600	-301
446	DPHYVCC	7650	-301
447	DPHYVCC	7700	-301
448	DPHYVCC	7750	-301
449	DPHYVCC	7800	-301
450	DPHYVCC	7850	-301

pad No	pad name	X	Y
451	VDDLP	7900	-301
452	VDDLP	7950	-301
453	VDDLP	8000	-301
454	VDDLP	8050	-301
455	VDDLP	8100	-301
456	VDDLP	8150	-301
457	GND	8200	-301
458	GND	8250	-301
459	GND	8300	-301
460	GND	8350	-301
461	GND	8400	-301
462	GND	8450	-301
463	GND	8500	-301
464	GND	8550	-301
465	GND	8600	-301
466	AGND	8650	-301
467	AGND	8700	-301
468	AGND	8750	-301
469	AGND	8800	-301
470	AGND	8850	-301
471	AGND	8900	-301
472	AGND	8950	-301
473	AGND	9000	-301
474	AGND	9050	-301
475	DUMMYR1	9100	-301
476	VPP1	9150	-301
477	VPP1	9200	-301
478	VPP1	9250	-301
479	VPP1	9300	-301
480	DUMMYR2	9350	-301
481	VCL	9400	-301
482	VCL	9450	-301
483	VCL	9500	-301
484	VCL	9550	-301
485	VCL	9600	-301
486	VCL	9650	-301
487	VCI	9700	-301
488	VCI	9750	-301
489	VCI	9800	-301
490	VCI	9850	-301
491	VCI	9900	-301
492	VCI	9950	-301
493	VCI	10000	-301
494	VCI	10050	-301
495	VCI	10100	-301
496	SVDD	10150	-301
497	SVDD	10200	-301
498	SVDD	10250	-301
499	SVDD	10300	-301
500	SVDD	10350	-301

R63311 Pad Coordinate (No.6)(Unit: μm)

pad No	pad name	X	Y
501	SVDD	10400	-301
502	VSP	10450	-301
503	VSP	10500	-301
504	VSP	10550	-301
505	VSP	10600	-301
506	VSP	10650	-301
507	VSP	10700	-301
508	EXPWRN	10750	-301
509	EXPWRN	10800	-301
510	AGNDDUM3	10850	-301
511	VSN	10900	-301
512	VSN	10950	-301
513	VSN	11000	-301
514	VSN	11050	-301
515	VSN	11100	-301
516	VSN	11150	-301
517	VSN	11200	-301
518	VSN	11250	-301
519	VSN	11300	-301
520	SVSS	11350	-301
521	SVSS	11400	-301
522	SVSS	11450	-301
523	SVSS	11500	-301
524	SVSS	11550	-301
525	SVSS	11600	-301
526	SVSS	11650	-301
527	SVSS	11700	-301
528	SVSS	11750	-301
529	VSWN	11800	-301
530	VSWN	11850	-301
531	AGNDDUM4	11900	-301
532	C31P	11950	-301
533	C31P	12000	-301
534	C31P	12050	-301
535	C31P	12100	-301
536	C31P	12150	-301
537	C31P	12200	-301
538	C31P	12250	-301
539	C31P	12300	-301
540	C31P	12350	-301
541	C31M	12400	-301
542	C31M	12450	-301
543	C31M	12500	-301
544	C31M	12550	-301
545	C31M	12600	-301
546	C31M	12650	-301
547	C31M	12700	-301
548	C31M	12750	-301
549	C31M	12800	-301
550	VGL	12850	-301

pad No	pad name	X	Y
551	VGL	12900	-301
552	VGL	12950	-301
553	VGL	13000	-301
554	VGL	13050	-301
555	VGL	13100	-301
556	GVSS	13150	-301
557	GVSS	13200	-301
558	GVSS	13250	-301
559	GVSS	13300	-301
560	GVSS	13350	-301
561	GVSS	13400	-301
562	GND	13450	-301
563	GND	13500	-301
564	GND	13550	-301
565	GND	13600	-301
566	GND	13650	-301
567	GND	13700	-301
568	GVDD	13750	-301
569	GVDD	13800	-301
570	GVDD	13850	-301
571	AGND	13900	-301
572	AGND	13950	-301
573	AGND	14000	-301
574	AGND	14050	-301
575	AGND	14100	-301
576	AGND	14150	-301
577	VCOM	14200	-301
578	VCOM	14250	-301
579	VCOM	14300	-301
580	VCOM	14350	-301
581	VCOM	14400	-301
582	VCOM	14450	-301
583	VCOMDDUM2	14500	-301
584	VCOMDDUM2	14550	-301
585	VCOMDDUM2	14600	-301
586	DUMMY	14625	316
587	DUMMY	14607	176
588	DUMMY	14589	316
589	DUMMY	14571	176
590	DUMMY	14553	316
591	DUMMY	14535	176
592	DUMMY	14517	316
593	DUMMY	14499	176
594	DUMMY	14481	316
595	DUMMY	14463	176
596	DUMMY	14445	316
597	DUMMY	14427	176
598	SOUT_32	14409	316
599	SOUT_32	14391	176
600	SOUT_31	14373	316

R63311 Pad Coordinate (No.7) (Unit: μm)

pad No	pad name	X	Y
601	SOUT_31	14355	176
602	SOUT_30	14337	316
603	SOUT_30	14319	176
604	SOUT_29	14301	316
605	SOUT_29	14283	176
606	SOUT_28	14265	316
607	SOUT_28	14247	176
608	SOUT_27	14229	316
609	SOUT_27	14211	176
610	SOUT_26	14193	316
611	SOUT_26	14175	176
612	SOUT_25	14157	316
613	SOUT_25	14139	176
614	SOUT_24	14121	316
615	SOUT_24	14103	176
616	SOUT_23	14085	316
617	SOUT_23	14067	176
618	VCOM	14049	316
619	VCOM	14031	176
620	VCOM	14013	316
621	VCOM	13995	176
622	VCOM	13977	316
623	VCOM	13959	176
624	VCOM	13941	316
625	VCOM	13923	176
626	VCOM	13905	316
627	VCOM	13887	176
628	VCOM	13869	316
629	VCOM	13851	176
630	SOUT_22	13833	316
631	SOUT_22	13815	176
632	SOUT_21	13797	316
633	SOUT_21	13779	176
634	SOUT_20	13761	316
635	SOUT_20	13743	176
636	SOUT_19	13725	316
637	SOUT_19	13707	176
638	SOUT_18	13689	316
639	SOUT_18	13671	176
640	SOUT_17	13653	316
641	SOUT_17	13635	176
642	DUMMY	13617	316
643	DUMMY	13599	176
644	DUMMY	13581	316
645	DUMMY	13563	176
646	DUMMY	13545	316
647	DUMMY	13527	176
648	SR1	13509	316
649	S1080	13491	176
650	S1079	13473	316

pad No	pad name	X	Y
651	S1078	13455	176
652	S1077	13437	316
653	S1076	13419	176
654	S1075	13401	316
655	S1074	13383	176
656	S1073	13365	316
657	S1072	13347	176
658	S1071	13329	316
659	S1070	13311	176
660	S1069	13293	316
661	S1068	13275	176
662	S1067	13257	316
663	S1066	13239	176
664	S1065	13221	316
665	S1064	13203	176
666	S1063	13185	316
667	S1062	13167	176
668	S1061	13149	316
669	S1060	13131	176
670	S1059	13113	316
671	S1058	13095	176
672	S1057	13077	316
673	S1056	13059	176
674	S1055	13041	316
675	S1054	13023	176
676	S1053	13005	316
677	S1052	12987	176
678	S1051	12969	316
679	S1050	12951	176
680	S1049	12933	316
681	S1048	12915	176
682	S1047	12897	316
683	S1046	12879	176
684	S1045	12861	316
685	S1044	12843	176
686	S1043	12825	316
687	S1042	12807	176
688	S1041	12789	316
689	S1040	12771	176
690	S1039	12753	316
691	S1038	12735	176
692	S1037	12717	316
693	S1036	12699	176
694	S1035	12681	316
695	S1034	12663	176
696	S1033	12645	316
697	S1032	12627	176
698	S1031	12609	316
699	S1030	12591	176
700	S1029	12573	316

R63311 Pad Coordinate (No.8) (Unit: μm)

pad No	pad name	X	Y
701	S1028	12555	176
702	S1027	12537	316
703	S1026	12519	176
704	S1025	12501	316
705	S1024	12483	176
706	S1023	12465	316
707	S1022	12447	176
708	S1021	12429	316
709	S1020	12411	176
710	S1019	12393	316
711	S1018	12375	176
712	S1017	12357	316
713	S1016	12339	176
714	S1015	12321	316
715	S1014	12303	176
716	S1013	12285	316
717	S1012	12267	176
718	S1011	12249	316
719	S1010	12231	176
720	S1009	12213	316
721	S1008	12195	176
722	S1007	12177	316
723	S1006	12159	176
724	S1005	12141	316
725	S1004	12123	176
726	S1003	12105	316
727	S1002	12087	176
728	S1001	12069	316
729	S1000	12051	176
730	S999	12033	316
731	S998	12015	176
732	S997	11997	316
733	S996	11979	176
734	S995	11961	316
735	S994	11943	176
736	S993	11925	316
737	S992	11907	176
738	S991	11889	316
739	S990	11871	176
740	S989	11853	316
741	S988	11835	176
742	S987	11817	316
743	S986	11799	176
744	S985	11781	316
745	S984	11763	176
746	S983	11745	316
747	S982	11727	176
748	S981	11709	316
749	S980	11691	176
750	S979	11673	316

pad No	pad name	X	Y
751	S978	11655	176
752	S977	11637	316
753	S976	11619	176
754	S975	11601	316
755	S974	11583	176
756	S973	11565	316
757	S972	11547	176
758	S971	11529	316
759	S970	11511	176
760	S969	11493	316
761	S968	11475	176
762	S967	11457	316
763	S966	11439	176
764	S965	11421	316
765	S964	11403	176
766	S963	11385	316
767	S962	11367	176
768	S961	11349	316
769	S960	11331	176
770	S959	11313	316
771	S958	11295	176
772	S957	11277	316
773	S956	11259	176
774	S955	11241	316
775	S954	11223	176
776	S953	11205	316
777	S952	11187	176
778	S951	11169	316
779	S950	11151	176
780	S949	11133	316
781	S948	11115	176
782	S947	11097	316
783	S946	11079	176
784	S945	11061	316
785	S944	11043	176
786	S943	11025	316
787	S942	11007	176
788	S941	10989	316
789	S940	10971	176
790	S939	10953	316
791	S938	10935	176
792	S937	10917	316
793	S936	10899	176
794	S935	10881	316
795	S934	10863	176
796	S933	10845	316
797	S932	10827	176
798	S931	10809	316
799	S930	10791	176
800	S929	10773	316

R63311 Pad Coordinate (No.9)(Unit: μm)

pad No	pad name	X	Y
801	S928	10755	176
802	S927	10737	316
803	S926	10719	176
804	S925	10701	316
805	S924	10683	176
806	S923	10665	316
807	S922	10647	176
808	S921	10629	316
809	S920	10611	176
810	S919	10593	316
811	S918	10575	176
812	S917	10557	316
813	S916	10539	176
814	S915	10521	316
815	S914	10503	176
816	S913	10485	316
817	S912	10467	176
818	S911	10449	316
819	S910	10431	176
820	S909	10413	316
821	S908	10395	176
822	S907	10377	316
823	S906	10359	176
824	S905	10341	316
825	S904	10323	176
826	S903	10305	316
827	S902	10287	176
828	S901	10269	316
829	S900	10251	176
830	S899	10233	316
831	S898	10215	176
832	S897	10197	316
833	S896	10179	176
834	S895	10161	316
835	S894	10143	176
836	S893	10125	316
837	S892	10107	176
838	S891	10089	316
839	S890	10071	176
840	S889	10053	316
841	S888	10035	176
842	S887	10017	316
843	S886	9999	176
844	S885	9981	316
845	S884	9963	176
846	S883	9945	316
847	S882	9927	176
848	S881	9909	316
849	S880	9891	176
850	S879	9873	316

pad No	pad name	X	Y
851	S878	9855	176
852	S877	9837	316
853	S876	9819	176
854	S875	9801	316
855	S874	9783	176
856	S873	9765	316
857	S872	9747	176
858	S871	9729	316
859	S870	9711	176
860	S869	9693	316
861	S868	9675	176
862	S867	9657	316
863	S866	9639	176
864	S865	9621	316
865	S864	9603	176
866	S863	9585	316
867	S862	9567	176
868	S861	9549	316
869	S860	9531	176
870	S859	9513	316
871	S858	9495	176
872	S857	9477	316
873	S856	9459	176
874	S855	9441	316
875	S854	9423	176
876	S853	9405	316
877	S852	9387	176
878	S851	9369	316
879	S850	9351	176
880	S849	9333	316
881	S848	9315	176
882	S847	9297	316
883	S846	9279	176
884	S845	9261	316
885	S844	9243	176
886	S843	9225	316
887	S842	9207	176
888	S841	9189	316
889	S840	9171	176
890	S839	9153	316
891	S838	9135	176
892	S837	9117	316
893	S836	9099	176
894	S835	9081	316
895	S834	9063	176
896	S833	9045	316
897	S832	9027	176
898	S831	9009	316
899	S830	8991	176
900	S829	8973	316

R63311 Pad Coordinate (No.10)(Unit: μm)

pad No	pad name	X	Y
901	S828	8955	176
902	S827	8937	316
903	S826	8919	176
904	S825	8901	316
905	S824	8883	176
906	S823	8865	316
907	S822	8847	176
908	S821	8829	316
909	S820	8811	176
910	S819	8793	316
911	S818	8775	176
912	S817	8757	316
913	S816	8739	176
914	S815	8721	316
915	S814	8703	176
916	S813	8685	316
917	S812	8667	176
918	S811	8649	316
919	S810	8631	176
920	S809	8613	316
921	S808	8595	176
922	S807	8577	316
923	S806	8559	176
924	S805	8541	316
925	S804	8523	176
926	S803	8505	316
927	S802	8487	176
928	S801	8469	316
929	S800	8451	176
930	S799	8433	316
931	S798	8415	176
932	S797	8397	316
933	S796	8379	176
934	S795	8361	316
935	S794	8343	176
936	S793	8325	316
937	S792	8307	176
938	S791	8289	316
939	S790	8271	176
940	S789	8253	316
941	S788	8235	176
942	S787	8217	316
943	S786	8199	176
944	S785	8181	316
945	S784	8163	176
946	S783	8145	316
947	S782	8127	176
948	S781	8109	316
949	S780	8091	176
950	S779	8073	316

pad No	pad name	X	Y
951	S778	8055	176
952	S777	8037	316
953	S776	8019	176
954	S775	8001	316
955	S774	7983	176
956	S773	7965	316
957	S772	7947	176
958	S771	7929	316
959	S770	7911	176
960	S769	7893	316
961	S768	7875	176
962	S767	7857	316
963	S766	7839	176
964	S765	7821	316
965	S764	7803	176
966	S763	7785	316
967	S762	7767	176
968	S761	7749	316
969	S760	7731	176
970	S759	7713	316
971	S758	7695	176
972	S757	7677	316
973	S756	7659	176
974	S755	7641	316
975	S754	7623	176
976	S753	7605	316
977	S752	7587	176
978	S751	7569	316
979	S750	7551	176
980	S749	7533	316
981	S748	7515	176
982	S747	7497	316
983	S746	7479	176
984	S745	7461	316
985	S744	7443	176
986	S743	7425	316
987	S742	7407	176
988	S741	7389	316
989	S740	7371	176
990	S739	7353	316
991	S738	7335	176
992	S737	7317	316
993	S736	7299	176
994	S735	7281	316
995	S734	7263	176
996	S733	7245	316
997	S732	7227	176
998	S731	7209	316
999	S730	7191	176
1000	S729	7173	316

R63311 Pad Coordinate (No.11)(Unit: μm)

pad No	pad name	X	Y
1001	S728	7155	176
1002	S727	7137	316
1003	S726	7119	176
1004	S725	7101	316
1005	S724	7083	176
1006	S723	7065	316
1007	S722	7047	176
1008	S721	7029	316
1009	S720	7011	176
1010	S719	6993	316
1011	S718	6975	176
1012	S717	6957	316
1013	S716	6939	176
1014	S715	6921	316
1015	S714	6903	176
1016	S713	6885	316
1017	S712	6867	176
1018	S711	6849	316
1019	S710	6831	176
1020	S709	6813	316
1021	S708	6795	176
1022	S707	6777	316
1023	S706	6759	176
1024	S705	6741	316
1025	S704	6723	176
1026	S703	6705	316
1027	S702	6687	176
1028	S701	6669	316
1029	S700	6651	176
1030	S699	6633	316
1031	S698	6615	176
1032	S697	6597	316
1033	S696	6579	176
1034	S695	6561	316
1035	S694	6543	176
1036	S693	6525	316
1037	S692	6507	176
1038	S691	6489	316
1039	S690	6471	176
1040	S689	6453	316
1041	S688	6435	176
1042	S687	6417	316
1043	S686	6399	176
1044	S685	6381	316
1045	S684	6363	176
1046	S683	6345	316
1047	S682	6327	176
1048	S681	6309	316
1049	S680	6291	176
1050	S679	6273	316

pad No	pad name	X	Y
1051	S678	6255	176
1052	S677	6237	316
1053	S676	6219	176
1054	S675	6201	316
1055	S674	6183	176
1056	S673	6165	316
1057	S672	6147	176
1058	S671	6129	316
1059	S670	6111	176
1060	S669	6093	316
1061	S668	6075	176
1062	S667	6057	316
1063	S666	6039	176
1064	S665	6021	316
1065	S664	6003	176
1066	S663	5985	316
1067	S662	5967	176
1068	S661	5949	316
1069	S660	5931	176
1070	S659	5913	316
1071	S658	5895	176
1072	S657	5877	316
1073	S656	5859	176
1074	S655	5841	316
1075	S654	5823	176
1076	S653	5805	316
1077	S652	5787	176
1078	S651	5769	316
1079	S650	5751	176
1080	S649	5733	316
1081	S648	5715	176
1082	S647	5697	316
1083	S646	5679	176
1084	S645	5661	316
1085	S644	5643	176
1086	S643	5625	316
1087	S642	5607	176
1088	S641	5589	316
1089	S640	5571	176
1090	S639	5553	316
1091	S638	5535	176
1092	S637	5517	316
1093	S636	5499	176
1094	S635	5481	316
1095	S634	5463	176
1096	S633	5445	316
1097	S632	5427	176
1098	S631	5409	316
1099	S630	5391	176
1100	S629	5373	316

R63311 Pad Coordinate (No.12) (Unit: μm)

pad No	pad name	X	Y
1101	S628	5355	176
1102	S627	5337	316
1103	S626	5319	176
1104	S625	5301	316
1105	S624	5283	176
1106	S623	5265	316
1107	S622	5247	176
1108	S621	5229	316
1109	S620	5211	176
1110	S619	5193	316
1111	S618	5175	176
1112	S617	5157	316
1113	S616	5139	176
1114	S615	5121	316
1115	S614	5103	176
1116	S613	5085	316
1117	S612	5067	176
1118	S611	5049	316
1119	S610	5031	176
1120	S609	5013	316
1121	S608	4995	176
1122	S607	4977	316
1123	S606	4959	176
1124	S605	4941	316
1125	S604	4923	176
1126	S603	4905	316
1127	S602	4887	176
1128	S601	4869	316
1129	S600	4851	176
1130	S599	4833	316
1131	S598	4815	176
1132	S597	4797	316
1133	S596	4779	176
1134	S595	4761	316
1135	S594	4743	176
1136	S593	4725	316
1137	S592	4707	176
1138	S591	4689	316
1139	S590	4671	176
1140	S589	4653	316
1141	S588	4635	176
1142	S587	4617	316
1143	S586	4599	176
1144	S585	4581	316
1145	S584	4563	176
1146	S583	4545	316
1147	S582	4527	176
1148	S581	4509	316
1149	S580	4491	176
1150	S579	4473	316

pad No	pad name	X	Y
1151	S578	4455	176
1152	S577	4437	316
1153	S576	4419	176
1154	S575	4401	316
1155	S574	4383	176
1156	S573	4365	316
1157	S572	4347	176
1158	S571	4329	316
1159	S570	4311	176
1160	S569	4293	316
1161	S568	4275	176
1162	S567	4257	316
1163	S566	4239	176
1164	S565	4221	316
1165	S564	4203	176
1166	S563	4185	316
1167	S562	4167	176
1168	S561	4149	316
1169	S560	4131	176
1170	S559	4113	316
1171	S558	4095	176
1172	S557	4077	316
1173	S556	4059	176
1174	S555	4041	316
1175	S554	4023	176
1176	S553	4005	316
1177	S552	3987	176
1178	S551	3969	316
1179	S550	3951	176
1180	S549	3933	316
1181	S548	3915	176
1182	S547	3897	316
1183	S546	3879	176
1184	S545	3861	316
1185	S544	3843	176
1186	S543	3825	316
1187	S542	3807	176
1188	S541	3789	316
1189	DUMMY	3771	176
1190	DUMMY	3753	316
1191	DUMMY	3735	176
1192	DUMMY	3717	316
1193	DUMMY	3699	176
1194	DUMMY	3681	316
1195	DUMMY	3645	176
1196	DUMMY	3627	316
1197	DUMMY	3573	176
1198	DUMMY	3555	316
1199	DUMMY	3501	176
1200	DUMMY	3483	316

R63311 Pad Coordinate (No.13)(Unit: μm)

pad No	pad name	X	Y
1201	DUMMY	3429	176
1202	DUMMY	3411	316
1203	DUMMY	3357	176
1204	DUMMY	3339	316
1205	DUMMY	3285	176
1206	DUMMY	3267	316
1207	DUMMY	3213	176
1208	DUMMY	3195	316
1209	DUMMY	3141	176
1210	DUMMY	3123	316
1211	DUMMY	3069	176
1212	DUMMY	3051	316
1213	DUMMY	2997	176
1214	DUMMY	2979	316
1215	DUMMY	2925	176
1216	DUMMY	2907	316
1217	DUMMY	2853	176
1218	DUMMY	2835	316
1219	DUMMY	2781	176
1220	DUMMY	2763	316
1221	DUMMY	2709	176
1222	DUMMY	2691	316
1223	DUMMY	2637	176
1224	DUMMY	2619	316
1225	DUMMY	2565	176
1226	DUMMY	2547	316
1227	DUMMY	2493	176
1228	DUMMY	2475	316
1229	DUMMY	2421	176
1230	DUMMY	2403	316
1231	DUMMY	2349	176
1232	DUMMY	2331	316
1233	DUMMY	2277	176
1234	DUMMY	2259	316
1235	DUMMY	2205	176
1236	DUMMY	2187	316
1237	DUMMY	2133	176
1238	DUMMY	2115	316
1239	DUMMY	2061	176
1240	DUMMY	2043	316
1241	DUMMY	1989	176
1242	DUMMY	1971	316
1243	DUMMY	1917	176
1244	DUMMY	1899	316
1245	DUMMY	1845	176
1246	DUMMY	1827	316
1247	DUMMY	1773	176
1248	DUMMY	1755	316
1249	DUMMY	1701	176
1250	DUMMY	1683	316

pad No	pad name	X	Y
1251	DUMMY	1629	176
1252	DUMMY	1611	316
1253	DUMMY	1557	176
1254	DUMMY	1539	316
1255	DUMMY	1485	176
1256	DUMMY	1467	316
1257	DUMMY	1413	176
1258	DUMMY	1395	316
1259	DUMMY	1341	176
1260	DUMMY	1323	316
1261	DUMMY	1269	176
1262	DUMMY	1251	316
1263	DUMMY	1197	176
1264	DUMMY	1179	316
1265	DUMMY	1125	176
1266	DUMMY	1107	316
1267	DUMMY	1053	176
1268	DUMMY	1035	316
1269	DUMMY	981	176
1270	DUMMY	963	316
1271	DUMMY	909	176
1272	DUMMY	891	316
1273	DUMMY	837	176
1274	DUMMY	819	316
1275	DUMMY	765	176
1276	DUMMY	747	316
1277	DUMMY	693	176
1278	DUMMY	675	316
1279	DUMMY	621	176
1280	DUMMY	603	316
1281	DUMMY	549	176
1282	DUMMY	531	316
1283	DUMMY	477	176
1284	DUMMY	459	316
1285	DUMMY	405	176
1286	DUMMY	387	316
1287	DUMMY	333	176
1288	DUMMY	315	316
1289	DUMMY	261	176
1290	DUMMY	243	316
1291	DUMMY	189	176
1292	DUMMY	171	316
1293	DUMMY	117	176
1294	DUMMY	99	316
1295	DUMMY	45	176
1296	DUMMY	27	316
1297	DUMMY	-27	176
1298	DUMMY	-45	316
1299	DUMMY	-99	176
1300	DUMMY	-117	316

R63311 Pad Coordinate (No.14)(Unit: μm)

pad No	pad name	X	Y
1301	DUMMY	-171	176
1302	DUMMY	-189	316
1303	DUMMY	-243	176
1304	DUMMY	-261	316
1305	DUMMY	-315	176
1306	DUMMY	-333	316
1307	DUMMY	-387	176
1308	DUMMY	-405	316
1309	DUMMY	-459	176
1310	DUMMY	-477	316
1311	DUMMY	-531	176
1312	DUMMY	-549	316
1313	DUMMY	-603	176
1314	DUMMY	-621	316
1315	DUMMY	-675	176
1316	DUMMY	-693	316
1317	DUMMY	-747	176
1318	DUMMY	-765	316
1319	DUMMY	-819	176
1320	DUMMY	-837	316
1321	DUMMY	-891	176
1322	DUMMY	-909	316
1323	DUMMY	-963	176
1324	DUMMY	-981	316
1325	DUMMY	-1035	176
1326	DUMMY	-1053	316
1327	DUMMY	-1107	176
1328	DUMMY	-1125	316
1329	DUMMY	-1179	176
1330	DUMMY	-1197	316
1331	DUMMY	-1251	176
1332	DUMMY	-1269	316
1333	DUMMY	-1323	176
1334	DUMMY	-1341	316
1335	DUMMY	-1395	176
1336	DUMMY	-1413	316
1337	DUMMY	-1467	176
1338	DUMMY	-1485	316
1339	DUMMY	-1539	176
1340	DUMMY	-1557	316
1341	DUMMY	-1611	176
1342	DUMMY	-1629	316
1343	DUMMY	-1683	176
1344	DUMMY	-1701	316
1345	DUMMY	-1755	176
1346	DUMMY	-1773	316
1347	DUMMY	-1827	176
1348	DUMMY	-1845	316
1349	DUMMY	-1899	176
1350	DUMMY	-1917	316

pad No	pad name	X	Y
1351	DUMMY	-1971	176
1352	DUMMY	-1989	316
1353	DUMMY	-2043	176
1354	DUMMY	-2061	316
1355	DUMMY	-2115	176
1356	DUMMY	-2133	316
1357	DUMMY	-2187	176
1358	DUMMY	-2205	316
1359	DUMMY	-2259	176
1360	DUMMY	-2277	316
1361	DUMMY	-2331	176
1362	DUMMY	-2349	316
1363	DUMMY	-2403	176
1364	DUMMY	-2421	316
1365	DUMMY	-2475	176
1366	DUMMY	-2493	316
1367	DUMMY	-2547	176
1368	DUMMY	-2565	316
1369	DUMMY	-2619	176
1370	DUMMY	-2637	316
1371	DUMMY	-2691	176
1372	DUMMY	-2709	316
1373	DUMMY	-2763	176
1374	DUMMY	-2781	316
1375	DUMMY	-2835	176
1376	DUMMY	-2853	316
1377	DUMMY	-2907	176
1378	DUMMY	-2925	316
1379	DUMMY	-2979	176
1380	DUMMY	-2997	316
1381	DUMMY	-3051	176
1382	DUMMY	-3069	316
1383	DUMMY	-3123	176
1384	DUMMY	-3141	316
1385	DUMMY	-3195	176
1386	DUMMY	-3213	316
1387	DUMMY	-3267	176
1388	DUMMY	-3285	316
1389	DUMMY	-3339	176
1390	DUMMY	-3357	316
1391	DUMMY	-3411	176
1392	DUMMY	-3429	316
1393	DUMMY	-3483	176
1394	DUMMY	-3501	316
1395	DUMMY	-3555	176
1396	DUMMY	-3573	316
1397	DUMMY	-3627	176
1398	DUMMY	-3645	316
1399	DUMMY	-3681	176
1400	DUMMY	-3699	316

R63311 Pad Coordinate (No.15) (Unit: μm)

pad No	pad name	X	Y
1401	DUMMY	-3717	176
1402	DUMMY	-3735	316
1403	DUMMY	-3753	176
1404	DUMMY	-3771	316
1405	S540	-3789	176
1406	S539	-3807	316
1407	S538	-3825	176
1408	S537	-3843	316
1409	S536	-3861	176
1410	S535	-3879	316
1411	S534	-3897	176
1412	S533	-3915	316
1413	S532	-3933	176
1414	S531	-3951	316
1415	S530	-3969	176
1416	S529	-3987	316
1417	S528	-4005	176
1418	S527	-4023	316
1419	S526	-4041	176
1420	S525	-4059	316
1421	S524	-4077	176
1422	S523	-4095	316
1423	S522	-4113	176
1424	S521	-4131	316
1425	S520	-4149	176
1426	S519	-4167	316
1427	S518	-4185	176
1428	S517	-4203	316
1429	S516	-4221	176
1430	S515	-4239	316
1431	S514	-4257	176
1432	S513	-4275	316
1433	S512	-4293	176
1434	S511	-4311	316
1435	S510	-4329	176
1436	S509	-4347	316
1437	S508	-4365	176
1438	S507	-4383	316
1439	S506	-4401	176
1440	S505	-4419	316
1441	S504	-4437	176
1442	S503	-4455	316
1443	S502	-4473	176
1444	S501	-4491	316
1445	S500	-4509	176
1446	S499	-4527	316
1447	S498	-4545	176
1448	S497	-4563	316
1449	S496	-4581	176
1450	S495	-4599	316

pad No	pad name	X	Y
1451	S494	-4617	176
1452	S493	-4635	316
1453	S492	-4653	176
1454	S491	-4671	316
1455	S490	-4689	176
1456	S489	-4707	316
1457	S488	-4725	176
1458	S487	-4743	316
1459	S486	-4761	176
1460	S485	-4779	316
1461	S484	-4797	176
1462	S483	-4815	316
1463	S482	-4833	176
1464	S481	-4851	316
1465	S480	-4869	176
1466	S479	-4887	316
1467	S478	-4905	176
1468	S477	-4923	316
1469	S476	-4941	176
1470	S475	-4959	316
1471	S474	-4977	176
1472	S473	-4995	316
1473	S472	-5013	176
1474	S471	-5031	316
1475	S470	-5049	176
1476	S469	-5067	316
1477	S468	-5085	176
1478	S467	-5103	316
1479	S466	-5121	176
1480	S465	-5139	316
1481	S464	-5157	176
1482	S463	-5175	316
1483	S462	-5193	176
1484	S461	-5211	316
1485	S460	-5229	176
1486	S459	-5247	316
1487	S458	-5265	176
1488	S457	-5283	316
1489	S456	-5301	176
1490	S455	-5319	316
1491	S454	-5337	176
1492	S453	-5355	316
1493	S452	-5373	176
1494	S451	-5391	316
1495	S450	-5409	176
1496	S449	-5427	316
1497	S448	-5445	176
1498	S447	-5463	316
1499	S446	-5481	176
1500	S445	-5499	316

R63311 Pad Coordinate (No.16) (Unit: μm)

pad No	pad name	X	Y
1501	S444	-5517	176
1502	S443	-5535	316
1503	S442	-5553	176
1504	S441	-5571	316
1505	S440	-5589	176
1506	S439	-5607	316
1507	S438	-5625	176
1508	S437	-5643	316
1509	S436	-5661	176
1510	S435	-5679	316
1511	S434	-5697	176
1512	S433	-5715	316
1513	S432	-5733	176
1514	S431	-5751	316
1515	S430	-5769	176
1516	S429	-5787	316
1517	S428	-5805	176
1518	S427	-5823	316
1519	S426	-5841	176
1520	S425	-5859	316
1521	S424	-5877	176
1522	S423	-5895	316
1523	S422	-5913	176
1524	S421	-5931	316
1525	S420	-5949	176
1526	S419	-5967	316
1527	S418	-5985	176
1528	S417	-6003	316
1529	S416	-6021	176
1530	S415	-6039	316
1531	S414	-6057	176
1532	S413	-6075	316
1533	S412	-6093	176
1534	S411	-6111	316
1535	S410	-6129	176
1536	S409	-6147	316
1537	S408	-6165	176
1538	S407	-6183	316
1539	S406	-6201	176
1540	S405	-6219	316
1541	S404	-6237	176
1542	S403	-6255	316
1543	S402	-6273	176
1544	S401	-6291	316
1545	S400	-6309	176
1546	S399	-6327	316
1547	S398	-6345	176
1548	S397	-6363	316
1549	S396	-6381	176
1550	S395	-6399	316

pad No	pad name	X	Y
1551	S394	-6417	176
1552	S393	-6435	316
1553	S392	-6453	176
1554	S391	-6471	316
1555	S390	-6489	176
1556	S389	-6507	316
1557	S388	-6525	176
1558	S387	-6543	316
1559	S386	-6561	176
1560	S385	-6579	316
1561	S384	-6597	176
1562	S383	-6615	316
1563	S382	-6633	176
1564	S381	-6651	316
1565	S380	-6669	176
1566	S379	-6687	316
1567	S378	-6705	176
1568	S377	-6723	316
1569	S376	-6741	176
1570	S375	-6759	316
1571	S374	-6777	176
1572	S373	-6795	316
1573	S372	-6813	176
1574	S371	-6831	316
1575	S370	-6849	176
1576	S369	-6867	316
1577	S368	-6885	176
1578	S367	-6903	316
1579	S366	-6921	176
1580	S365	-6939	316
1581	S364	-6957	176
1582	S363	-6975	316
1583	S362	-6993	176
1584	S361	-7011	316
1585	S360	-7029	176
1586	S359	-7047	316
1587	S358	-7065	176
1588	S357	-7083	316
1589	S356	-7101	176
1590	S355	-7119	316
1591	S354	-7137	176
1592	S353	-7155	316
1593	S352	-7173	176
1594	S351	-7191	316
1595	S350	-7209	176
1596	S349	-7227	316
1597	S348	-7245	176
1598	S347	-7263	316
1599	S346	-7281	176
1600	S345	-7299	316

R63311 Pad Coordinate (No.17) (Unit: μm)

pad No	pad name	X	Y
1601	S344	-7317	176
1602	S343	-7335	316
1603	S342	-7353	176
1604	S341	-7371	316
1605	S340	-7389	176
1606	S339	-7407	316
1607	S338	-7425	176
1608	S337	-7443	316
1609	S336	-7461	176
1610	S335	-7479	316
1611	S334	-7497	176
1612	S333	-7515	316
1613	S332	-7533	176
1614	S331	-7551	316
1615	S330	-7569	176
1616	S329	-7587	316
1617	S328	-7605	176
1618	S327	-7623	316
1619	S326	-7641	176
1620	S325	-7659	316
1621	S324	-7677	176
1622	S323	-7695	316
1623	S322	-7713	176
1624	S321	-7731	316
1625	S320	-7749	176
1626	S319	-7767	316
1627	S318	-7785	176
1628	S317	-7803	316
1629	S316	-7821	176
1630	S315	-7839	316
1631	S314	-7857	176
1632	S313	-7875	316
1633	S312	-7893	176
1634	S311	-7911	316
1635	S310	-7929	176
1636	S309	-7947	316
1637	S308	-7965	176
1638	S307	-7983	316
1639	S306	-8001	176
1640	S305	-8019	316
1641	S304	-8037	176
1642	S303	-8055	316
1643	S302	-8073	176
1644	S301	-8091	316
1645	S300	-8109	176
1646	S299	-8127	316
1647	S298	-8145	176
1648	S297	-8163	316
1649	S296	-8181	176
1650	S295	-8199	316

pad No	pad name	X	Y
1651	S294	-8217	176
1652	S293	-8235	316
1653	S292	-8253	176
1654	S291	-8271	316
1655	S290	-8289	176
1656	S289	-8307	316
1657	S288	-8325	176
1658	S287	-8343	316
1659	S286	-8361	176
1660	S285	-8379	316
1661	S284	-8397	176
1662	S283	-8415	316
1663	S282	-8433	176
1664	S281	-8451	316
1665	S280	-8469	176
1666	S279	-8487	316
1667	S278	-8505	176
1668	S277	-8523	316
1669	S276	-8541	176
1670	S275	-8559	316
1671	S274	-8577	176
1672	S273	-8595	316
1673	S272	-8613	176
1674	S271	-8631	316
1675	S270	-8649	176
1676	S269	-8667	316
1677	S268	-8685	176
1678	S267	-8703	316
1679	S266	-8721	176
1680	S265	-8739	316
1681	S264	-8757	176
1682	S263	-8775	316
1683	S262	-8793	176
1684	S261	-8811	316
1685	S260	-8829	176
1686	S259	-8847	316
1687	S258	-8865	176
1688	S257	-8883	316
1689	S256	-8901	176
1690	S255	-8919	316
1691	S254	-8937	176
1692	S253	-8955	316
1693	S252	-8973	176
1694	S251	-8991	316
1695	S250	-9009	176
1696	S249	-9027	316
1697	S248	-9045	176
1698	S247	-9063	316
1699	S246	-9081	176
1700	S245	-9099	316

R63311 Pad Coordinate (No.18)(Unit: μm)

pad No	pad name	X	Y
1701	S244	-9117	176
1702	S243	-9135	316
1703	S242	-9153	176
1704	S241	-9171	316
1705	S240	-9189	176
1706	S239	-9207	316
1707	S238	-9225	176
1708	S237	-9243	316
1709	S236	-9261	176
1710	S235	-9279	316
1711	S234	-9297	176
1712	S233	-9315	316
1713	S232	-9333	176
1714	S231	-9351	316
1715	S230	-9369	176
1716	S229	-9387	316
1717	S228	-9405	176
1718	S227	-9423	316
1719	S226	-9441	176
1720	S225	-9459	316
1721	S224	-9477	176
1722	S223	-9495	316
1723	S222	-9513	176
1724	S221	-9531	316
1725	S220	-9549	176
1726	S219	-9567	316
1727	S218	-9585	176
1728	S217	-9603	316
1729	S216	-9621	176
1730	S215	-9639	316
1731	S214	-9657	176
1732	S213	-9675	316
1733	S212	-9693	176
1734	S211	-9711	316
1735	S210	-9729	176
1736	S209	-9747	316
1737	S208	-9765	176
1738	S207	-9783	316
1739	S206	-9801	176
1740	S205	-9819	316
1741	S204	-9837	176
1742	S203	-9855	316
1743	S202	-9873	176
1744	S201	-9891	316
1745	S200	-9909	176
1746	S199	-9927	316
1747	S198	-9945	176
1748	S197	-9963	316
1749	S196	-9981	176
1750	S195	-9999	316

pad No	pad name	X	Y
1751	S194	-10017	176
1752	S193	-10035	316
1753	S192	-10053	176
1754	S191	-10071	316
1755	S190	-10089	176
1756	S189	-10107	316
1757	S188	-10125	176
1758	S187	-10143	316
1759	S186	-10161	176
1760	S185	-10179	316
1761	S184	-10197	176
1762	S183	-10215	316
1763	S182	-10233	176
1764	S181	-10251	316
1765	S180	-10269	176
1766	S179	-10287	316
1767	S178	-10305	176
1768	S177	-10323	316
1769	S176	-10341	176
1770	S175	-10359	316
1771	S174	-10377	176
1772	S173	-10395	316
1773	S172	-10413	176
1774	S171	-10431	316
1775	S170	-10449	176
1776	S169	-10467	316
1777	S168	-10485	176
1778	S167	-10503	316
1779	S166	-10521	176
1780	S165	-10539	316
1781	S164	-10557	176
1782	S163	-10575	316
1783	S162	-10593	176
1784	S161	-10611	316
1785	S160	-10629	176
1786	S159	-10647	316
1787	S158	-10665	176
1788	S157	-10683	316
1789	S156	-10701	176
1790	S155	-10719	316
1791	S154	-10737	176
1792	S153	-10755	316
1793	S152	-10773	176
1794	S151	-10791	316
1795	S150	-10809	176
1796	S149	-10827	316
1797	S148	-10845	176
1798	S147	-10863	316
1799	S146	-10881	176
1800	S145	-10899	316

R63311 Pad Coordinate (No.19)(Unit: μm)

pad No	pad name	X	Y
1801	S144	-10917	176
1802	S143	-10935	316
1803	S142	-10953	176
1804	S141	-10971	316
1805	S140	-10989	176
1806	S139	-11007	316
1807	S138	-11025	176
1808	S137	-11043	316
1809	S136	-11061	176
1810	S135	-11079	316
1811	S134	-11097	176
1812	S133	-11115	316
1813	S132	-11133	176
1814	S131	-11151	316
1815	S130	-11169	176
1816	S129	-11187	316
1817	S128	-11205	176
1818	S127	-11223	316
1819	S126	-11241	176
1820	S125	-11259	316
1821	S124	-11277	176
1822	S123	-11295	316
1823	S122	-11313	176
1824	S121	-11331	316
1825	S120	-11349	176
1826	S119	-11367	316
1827	S118	-11385	176
1828	S117	-11403	316
1829	S116	-11421	176
1830	S115	-11439	316
1831	S114	-11457	176
1832	S113	-11475	316
1833	S112	-11493	176
1834	S111	-11511	316
1835	S110	-11529	176
1836	S109	-11547	316
1837	S108	-11565	176
1838	S107	-11583	316
1839	S106	-11601	176
1840	S105	-11619	316
1841	S104	-11637	176
1842	S103	-11655	316
1843	S102	-11673	176
1844	S101	-11691	316
1845	S100	-11709	176
1846	S99	-11727	316
1847	S98	-11745	176
1848	S97	-11763	316
1849	S96	-11781	176
1850	S95	-11799	316
1851	S94	-11817	176
1852	S93	-11835	316
1853	S92	-11853	176
1854	S91	-11871	316
1855	S90	-11889	176
1856	S89	-11907	316
1857	S88	-11925	176
1858	S87	-11943	316
1859	S86	-11961	176
1860	S85	-11979	316
1861	S84	-11997	176
1862	S83	-12015	316
1863	S82	-12033	176
1864	S81	-12051	316
1865	S80	-12069	176
1866	S79	-12087	316
1867	S78	-12105	176
1868	S77	-12123	316
1869	S76	-12141	176
1870	S75	-12159	316
1871	S74	-12177	176
1872	S73	-12195	316
1873	S72	-12213	176
1874	S71	-12231	316
1875	S70	-12249	176
1876	S69	-12267	316
1877	S68	-12285	176
1878	S67	-12303	316
1879	S66	-12321	176
1880	S65	-12339	316
1881	S64	-12357	176
1882	S63	-12375	316
1883	S62	-12393	176
1884	S61	-12411	316
1885	S60	-12429	176
1886	S59	-12447	316
1887	S58	-12465	176
1888	S57	-12483	316
1889	S56	-12501	176
1890	S55	-12519	316
1891	S54	-12537	176
1892	S53	-12555	316
1893	S52	-12573	176
1894	S51	-12591	316
1895	S50	-12609	176
1896	S49	-12627	316
1897	S48	-12645	176
1898	S47	-12663	316
1899	S46	-12681	176
1900	S45	-12699	316

R63311 Pad Coordinate (No.20)(Unit: μm)

pad No	pad name	X	Y
1901	S44	-12717	176
1902	S43	-12735	316
1903	S42	-12753	176
1904	S41	-12771	316
1905	S40	-12789	176
1906	S39	-12807	316
1907	S38	-12825	176
1908	S37	-12843	316
1909	S36	-12861	176
1910	S35	-12879	316
1911	S34	-12897	176
1912	S33	-12915	316
1913	S32	-12933	176
1914	S31	-12951	316
1915	S30	-12969	176
1916	S29	-12987	316
1917	S28	-13005	176
1918	S27	-13023	316
1919	S26	-13041	176
1920	S25	-13059	316
1921	S24	-13077	176
1922	S23	-13095	316
1923	S22	-13113	176
1924	S21	-13131	316
1925	S20	-13149	176
1926	S19	-13167	316
1927	S18	-13185	176
1928	S17	-13203	316
1929	S16	-13221	176
1930	S15	-13239	316
1931	S14	-13257	176
1932	S13	-13275	316
1933	S12	-13293	176
1934	S11	-13311	316
1935	S10	-13329	176
1936	S9	-13347	316
1937	S8	-13365	176
1938	S7	-13383	316
1939	S6	-13401	176
1940	S5	-13419	316
1941	S4	-13437	176
1942	S3	-13455	316
1943	S2	-13473	176
1944	S1	-13491	316
1945	SL1	-13509	176
1946	DUMMY	-13527	316
1947	DUMMY	-13545	176
1948	DUMMY	-13563	316
1949	DUMMY	-13581	176
1950	DUMMY	-13599	316

pad No	pad name	X	Y
1951	DUMMY	-13617	176
1952	SOUT_16	-13635	316
1953	SOUT_16	-13653	176
1954	SOUT_15	-13671	316
1955	SOUT_15	-13689	176
1956	SOUT_14	-13707	316
1957	SOUT_14	-13725	176
1958	SOUT_13	-13743	316
1959	SOUT_13	-13761	176
1960	SOUT_12	-13779	316
1961	SOUT_12	-13797	176
1962	SOUT_11	-13815	316
1963	SOUT_11	-13833	176
1964	VCOM	-13851	316
1965	VCOM	-13869	176
1966	VCOM	-13887	316
1967	VCOM	-13905	176
1968	VCOM	-13923	316
1969	VCOM	-13941	176
1970	VCOM	-13959	316
1971	VCOM	-13977	176
1972	VCOM	-13995	316
1973	VCOM	-14013	176
1974	VCOM	-14031	316
1975	VCOM	-14049	176
1976	SOUT_10	-14067	316
1977	SOUT_10	-14085	176
1978	SOUT_9	-14103	316
1979	SOUT_9	-14121	176
1980	SOUT_8	-14139	316
1981	SOUT_8	-14157	176
1982	SOUT_7	-14175	316
1983	SOUT_7	-14193	176
1984	SOUT_6	-14211	316
1985	SOUT_6	-14229	176
1986	SOUT_5	-14247	316
1987	SOUT_5	-14265	176
1988	SOUT_4	-14283	316
1989	SOUT_4	-14301	176
1990	SOUT_3	-14319	316
1991	SOUT_3	-14337	176
1992	SOUT_2	-14355	316
1993	SOUT_2	-14373	176
1994	SOUT_1	-14391	316
1995	SOUT_1	-14409	176
1996	DUMMY	-14427	316
1997	DUMMY	-14445	176
1998	DUMMY	-14463	316
1999	DUMMY	-14481	176
2000	DUMMY	-14499	316

R63311 Pad Coordinate (No.21)(Unit: μm)

pad No	pad name	X	Y
2001	DUMMY	-14517	176
2002	DUMMY	-14535	316
2003	DUMMY	-14553	176
2004	DUMMY	-14571	316
2005	DUMMY	-14589	176
2006	DUMMY	-14607	316

Alignment mark	X	Y
1-a	-14780	-305
1-b	14780	-305

Revision Record

Rev.	Date	Page No	Contents of Modification
0.00	2011/12/26		First issue
0.01	2012/02/07	10	Deleted: VBAT Added: VCI
		16	Deleted: TE Added: VCI Added: GNDRF
		18	Added: VSP External Application Control Pin
		19	Added: VSN External Application Control Pin (Amplitude: AGND – VSN) Deleted: AVDDL (at Table11) Deleted: VSP2 (at Table11) Added: SVDD (at Table11) Added: SVSS (at Table11) Changed VSWP's function (at Table1) A pin to output on/off control signal of external N-channel MOSFET when VSP is generated by a switching regulator method (VBATGND amplitude). For details, see "Power Supply Generating Circuit." When power supply generated by a charge pump method is used, stops outputting the signal (VSWP is fixed to GND). →A pin to output on/off control signal of external N-channel MOSFET when VSP is generated by a switching regulator method (VCI-GND amplitude). For details, see "Power Supply Generating Circuit." When using external VSP supply, VSWP is fixed to GND. Changed: VSWN's function (at Table11) A pin to output on/off control signal of external P-channel MOSFET when VSN is generated by a switching regulator method (VBATGND amplitude). For details, see "Power Supply Generating Circuit." When power supply generated by a charge pump method is used, stops outputting the signal (VSWN is fixed to VBAT). →A pin to output on/off control signal of external P-channel MOSFET when VSN is generated by a switching regulator method (VCI-GND amplitude). For details, see "Power Supply Generating Circuit." When using external VSN supply, VSWN is fixed to VSP. Changed: GVDD (at Table11) (1)Connect to Liquid crystal panel →Connect to Liquid crystal panel Stabilizing capacitor (2)Liquid crystal drive power supply. A pin to output positive voltage for the liquid crystal panel. →Internal regulator output for liquid crystal driving power supply. A pin to output negative voltage for the liquid crystal panel (3) Open → Stabilizing capacitor
		19	Changed: GVSS (at Table11) (1)Connect to Liquid crystal panel

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			<p>→Connect to Liquid crystal panel Stabilizing capacitor (2)Liquid crystal drive power supply. A pin to output negative voltage for the liquid crystal panel. →Internal regulator output for liquid crystal driving power supply. A pin to output negative voltage for the liquid crystal panel. (3) Open →Stabilizing capacitor</p>
20			<p>Deleted (at Table11): C11P/M,C12P/M,C13P/M,C14P/M,C15P/M,C16P/M,C17P/M,C18P/M,C19P/M,C1AP/M Deleted: 42P/M (at Table11) Changed: C41P/M's function (at Table11) Connect to external capacitor for generating VCL. →Capacitor connection pins for step-up VCL generator. Changed: VCL's function (at Table11) Used for VSN reference voltage. →Internal analog power supply for VCOMDC generator.Connect to stabilizing capacitor. Changed: SL1 (at Table12) (1)Connect to Open → Connect to Liquid crystal panel (2)Not used. Leave open. →When using ZigZag inversion mode, it connects with Liquid crystal panel Changed: SR1 (at Table12) (1)Connect to Open → Connect to Liquid crystal panel (2)Not used. Leave open. →When using ZigZag inversion mode, it connects with Liquid crystal panel</p>
22			<p>Added: Clock External Application Control pin (Amplitude: IOVCC - GND) Added: DSI Pin Arrangemanet Control pin (Amplitude: IOVCC - GND)</p>
23			<p>Added: The test free-running mode Control pin (Amplitude: IOVCC - GND) Added: Other Pins (Test and Dummy)</p>
50			Changed: Power Supply Generating Circuit -Example 1-
51			Changed: Power Supply Generating Circuit -Example 2
52			Changed: Power Supply Generating Circuit -Example 3-
53			Chenged: Specifications of External Elements Connected to the Power Supply Circuit Table 20 , Table21, Table22
54			Changed: Specifications of External Elements Connected to the Power Supply Circuit Table24
55			Changed: Voltage Setting Pattern Diagram -generated bu Switching Regulator-
56			Changed: Voltage Setting Pattern Diagram -External Supply-
57			Changed: Voltage Setting Pattern Diagram -VSP: External Supply, VSN: Generated Switching Regulator-
58			Changed: Note
59			Changed: Exetral VSP/VSN Supply mode

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		61	Changed: Initial States of Input/Output Pins and Output Pins after Reset
		62	Added: Power supply voltage(4) Added: Note (High) VCI \geq VCL (Low)
		63	Changed: Power Supply Voltage Range Table26, Table27, Table28
		81	Added: B7h (Checksum and ECC Error Count Reset) Changed: C0h number of parameter Changed: C1h number of parameter Changed: C2h number of parameter Changed: C4h number of parameter Changed: C6h number of parameter Changed: D0h number of parameter Changed: D2h number of parameter Changed: D3h number of parameter
		82	Changed: D6h Command name Sequencer Control → Sequencer Test Control Added: D9h(Sequencer Control) Changed: EDh number of parameter Changed: EEh number of parameter Changed: EFh number of parameter Changed: FDh number of parameter Changed: FEh number of parameter
		96	Added: B7h (Checksum and ECC Error Count Reset) Changed: D6h Command name Sequencer Control → Sequencer Test Control Added: D9h(Sequencer Control)
		187~191	Added: Power Setting (Charge Pump Setting) BT3, BT2, DC2, DC3, DC4, VLM1, VLM1M, VLM2, VLM3
		192~194	Added: Power Setting (Swiching regulator Setting) DC1SP, DC1SPHA, DC1SPHB, DC1SPHC, DC1SPHD, DC1SM DC1SMHA, DC1SMHB, DC1SMHC, DC1SMHD
		195~199	Added: Power Setting for Internal Power VCL, VC2, VC3, VPL, APAP, APAN, VNL
		200~208	Added: VCOM Setting WCVDC, WCVDCB, VDC, VDCB
		8	Video image display interface (see Note 1) - MIPI DSI TE-reporting Deleted Analog power supply: VBAT→VCI,VSP,VSN Changed
		9	Dummy pins used to fix pin to VBAT, IOVCC, or GND (see note 2)→Dummy pins used to fix pin to IOVCC, or GND (see note 2) Changed
		10	DPHYVCC 1.65V ~ 3.30V Changed Deleted RDX

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		11	Block Diagram modified
		14	(2)Video Image Interface Deleted
		66	Note on Electrical Characteristics pin corrected
		71	I2C Serial Interface Timing Characteristics changed
		72-73	Added DPHYVCC Voltage
		118	get_signal_mode TEON/TEOM Deleted
		129	set_tear_off: 34h Deleted
		130	set_tear_on: 35h Deleted
		134	set_tear_scanline:44h Deleted
		153	TEI register Deleted
		159	Table 53 Configuration of DSITXDIV modified
		163	TIGCYC modified
		170	2-line inversion drive [spatial configuration mode1] (LINEINVA ='h1, PNSET='h0) corrected
		177	DIV Deleted
		177	RTN0, RTNA0 added comment Move Test Image Generator
		178	SNTx,SNTAx Added
		179	EQWx,EQWAx Added
		182	PBHLV corrected
		183	PBDIV frequency (fosc=28MHz)→(fosc=14MHz) changed
		208	This register controls output data from TE→LEDPWM
		166	BLREV/BLS table changed
0.02	2012/03/16	152	Changed 'h4 DSI-Video-Burst→ 'h1 DSI-Video-Burst
		163	Changed RTN0, RTNA0 → RTN
		169	Corrected LININVA → LINEINVA
		264、265、 266	Deleted 「RAM Write / Read」 function
		3、116、 124、125	Deleted enter_invert_mode、exit_invert_mode
		243	Changed Table 69 Vertical Display Timing Changed Table 70 Horizontal Display Timing
		185	Changed DC2/DC3 clock frequency
		11	Corrected Block Diagram
		226	added Exit Deep Standby Mode
		10	Corrected SOUT Level VGH - VGL→GVDD-GVSS

	22	added LNSW1/0 PNSW caption
	80,94,118,1 27,128,134	added R0Eh (TE) 、 R34h、 R35h、 R44h
	250	deleted DIV
	66	Corrected DIN
	19	Corrected EXPWRN Function
	287	Corrected NVM Write Sequence
	19	Corrected GVDD comment negative voltege→positive voltage
	52	Changed Power Supply Circuit Connection Example3
	54	Changed Table23 Transistor Specifications (33)
	55	Changed Voltage Setting Diagram(Generated by Switching Regulator)
	56	Changed Voltage Setting Diagram(External Supply)
	57	Changed VSP:External Supply,VSN:Generated by SwithingRegulator)
	58	Changed Notes1
	67	Changed VSP/VSN item
0.03	2012/04/09	Changed 'h4 『DBI.C option2』 → 『DBI.C option3』 215 Changed '『HS+HBP』 20 byteclk -> 45 byteclk 258 Changed note4 Comment 『VDV』 -> 『VDC、VDCB』 Deleted note5 255 Deleted 『per address.』 145 SOUTTR1/2, SOUTTF1/2 Added 123 ERR_CNT_RST Added 184 Corrected NVMLD Function table 184 RDID1~3 Added 151 Changed DC2,DC3,DC4 01h setting Setting inhibited→210division 126,128 TIG Display image 1080×1920 aaded. Flow added. 123 Changed DSI_THSSET T.B.D→Preset value 155 Changed VLM2 GVDD→GVDD&VGH 156 Changed VLM3 GVSS→GVSS&VGL 165 GVDDRCT/GVSSDRCT added 166 SVD<3:0>,SVS<3:0> added. 143 SNT1,SNTA1,SNT2,SNTA2 count 156 VLM2E/VLM3E added
0.04	2012/0524	Chaged Figure 5 Power supply on sequence 115 added "Notes of Manufacture Command" 176 effective on foward scan.→effective on backward scan. VDC→VDCB 216 Chaged Figure 46 218 Chaged Table 69 245 added Note:VSYNC/HSYNC packet is needed from immediately after Exit_sleep_mode.

R63311		Specification	
0.05	2012/0629	16	Deleted "By register settings, it can be used as a verify signal for NVM write. "
		36	Table29 updated VSP,VSN,VGH,VGL state updated
		39	Table29 updated IOPN/ IDST/ ICIN3/ IDST3 updated Test condition&Spec
		40	Table29 updated ICIN4/ IDST4/ ICIN5/ IDST5 updated Test condition&Spec
		41	Table30 updated $\Delta V_{O1}, \Delta V_{O2}$ added Table31 updated HIS,ILP updated Spec
		43	Table32 updated VSP,VSN,VGH,VGL,VCL1,SVDD,SVSS,GVDD,GVSS,VCL2 updated Test condition&Spec
		44	Table34 updated tRT2 updated Spec.
		45	Table35 updated tdds updated Test condition&Spec
		49	Table39 updated tSETUP ,tHOLD updated Test Spec Added Note.6
		78	Deleted 16 bits/pixel (65,536 colors)
		96	Deleted 16 bits/pixel (65,536 colors)
		99	Description of DBV is added.
		120	Deleted 16bpp(R,G,B)→24bpp(r,g,b) expansion
		166	corrected This register controls reference level → reference current(APAP) Added APSGP1/2,APSGN1/2
		172/176	corrected LPLVL→VPLVL
		183	Deleted (=VERIFLGWR & VERIFLGER)
		218	VBL condition corrected VBP+BP→VFP+BP
		245	The waiting time after a sleep mode is changed.
0.06	2012/0712	8	Corrected MIPI DSI: Version 1.01.00r11 21-Feb-2008 (Command Mode and Video Mode supported)→ (Video Mode supported)
		10	Table1 Corrected VGH 5.0V ~ 12.0V→5.0V ~ 13.0V
		32	Corrected $(VSP-VPLVL) \geq 0.3V \rightarrow (SVDD-VPLVL) \geq 0.3V$
		39	Table29 Current consumption (VCI-GND) Corrected APSGP1 = 3'h7, APSGP2 = 3'h7,APSGN1 = 3'h7, APSGN2 = 3'h7→ APSGP1 = 3'h4, APSGP2 = 3'h4,APSGN1 = 3'h4, APSGN2 = 3'h4

	40	Table29	
		Current consumption (VSP-GND)	
		Corrected APSGP1 = 3'h7, APSGP2 = 3'h7,APSGN1 = 3'h7, APSGN2 = 3'h7→ APSGP1 = 3'h4, APSGP2 = 3'h4,APSGN1 = 3'h4, APSGN2 = 3'h4	
		Current consumption (VSN-GND)	
		Corrected APSGP1 = 3'h7, APSGP2 = 3'h7,APSGN1 = 3'h7, APSGN2 = 3'h7→ APSGP1 = 3'h4, APSGP2 = 3'h4,APSGN1 = 3'h4, APSGN2 = 3'h4	
	56	Table42	
		Corrected F5h R→C	
		Corrected F6h R→C	
	57/58	Table43/44	
		Added BBh Command	
		Corrected C1h Number of parameter 31→34	
		Corrected C4h Number of parameter 14→22	
		Corrected DEh Number of parameter 5→6	
		Deleted FCh Command	
		Corrected FEh Number of parameter 8→9	
		Deleted F5h/F6h Command	
	122	I2CNCOFF is added	
	157	VLM2	
		Corrected h29 Setting inhibited→12.2V	
		Corrected h2A Setting inhibited→12.4V	
		Corrected h2B Setting inhibited→12.6V	
		Corrected h2C Setting inhibited→12.8V	
		Corrected h2D Setting inhibited→13.0V	
	221	Figure49	
		Changed video input period 2frame→4frame(after enter_sleep_mode)	
1.00	2012/09/28	11	Corrected Block Diagram(Added Test and Dummy Pin)
		13	Corrected Table 3 Function SELDL[1:0] Disabled pin CLKP/N added
		21	Corrected Table 14 TN Liquid Crystal Drive Pins PBCTL2B1→PBCTLB1,PBCTL2B2→PBCTLB2
		261	Added Alignment Mark
		262	Added Target Die Size Bump Size
		263	Aded Pad Arrangement
		267	Added Pad Coordinate
1.01	2012/11/12	'-	Added register bit map of Manufacture Command
		202	Added T_SLOUT Command

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