A Cross-Coupled CMOS Negative Capacitor for Wideband Metamaterial Applications

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***Abstract*—Non-Foster circuits can be used to provide broadband impedance matching for antennas and metamaterials. These circuits allow effective matching over a much wider bandwidth than is expected from traditional passive components. Therefore, this paper considers the design and test of a negative capacitor in a 0.5 micron CMOS process. The proposed circuit uses a cross-coupled design to allow for floating operation, and the design's simulated performance works well at high frequency. Measured results show a low-frequency capacitance of -1.7 pF and within 10% to 200 MHz, and falling to -4 pF at 230 MHz. Although the selected CMOS process is adequate to demonstrate the basic design approach, more advanced process nodes would be expected to extend performance to even higher frequencies. Results are also presented showing performance of the circuit in a metamaterial.**

***Keywords*—metamaterials, CMOS integrated circuits, impedance matching.**

I. Introduction

One emerging area of interest for negative impedance converters has been applications for wideband metamaterials [1]. Metamaterials are man-made materials that have been designed to have properties not normally shown in natural materials. They use specially-designed structures that can show properties such as a negative refractive index. For example, split ring resonators (SRRs) are used to create microwave structures that can be used for cloaking applications [2]. However, such structures are presently narrow-band due to the resonances required in these structures, and this limits their application.

Non-Foster elements such as negative capacitors and negative inductors are commonly used to eliminate narrowband resonant behavior inherent in SRRs [3]. Such circuits can be used effectively to improve impedance matching when compared to matching using passive networks.

Many of the early non-Foster circuits employed bipolar negative impedance converter designs, and industry trends for system-on-a-chip and other mixed-mode designs motivate the development of CMOS circuit approaches. CMOS generally has a lower power dissipation than bipolar designs, but has lower transconductance than bipolar, and parasitic capacitances can become a problem at higher frequencies [4].

In this paper, a CMOS implementation of a floating negative capacitor design using a cross-coupled NIC topology is presented [5]. In the proposed approach, a cross-coupled circuit is used with a 2 pF load to present an input impedance comparable to a -1.7 pF capacitor. This circuit was fabricated in 0.5 μm CMOS to allow demonstration of the proposed design. Smaller process technologies would allow operation at even higher frequencies. In addition, the proposed circuit is simulated in a metamaterial where the results show useful metamaterial characteristics even in the presence of parasitic resistance.

In Section II, a brief overview of the cross-coupled topology is given, along with the mathematical analysis of a proposed CMOS negative capacitor circuit. In Section III, simulation results in Agilent ADS are shown for the prototype circuit. In Section IV, measurement results of the fabricated circuit are shown. Finally, in Section V, the simulated and measured results are compared, and results presented for the device embedded in a metamaterial.

II. Analysis

A CMOS version of the cross-coupled negative impedance converter is first reviewed here [6]. This topology allows a floating negative impedance to be created, whereas single-ended topologies such as the Linvill NICs create a negative impedance between the input and ground [7]. A simplified view of the circuit is shown in Fig. 1. The essential circuit has two nMOS transistors where the gate of each nMOS transistor is connected to the drain of the other transistor. The transistor sources are connected to the load Z_L, and the input Z_{in} is seen looking into the drains of the transistors. Identical current sources are connected to each transistors' source and drain, to force the current seen at Z_{in} to match the current through Z_L.

Fig. 2 shows a half-circuit used for analysis. This circuit assumes that the transconductance g_m and other characteristics of the two nMOS transistors are identical. In this circuit, z_s represents half of the load impedance connected to the full circuit, and v_{in} is the differential input voltage, g_m is the transconductance, v_s is the voltage seen at the transistor source, and z_{gs}, z_{ds} and z_{gd} represent the impedances seen between the respective terminals of the nMOS device.

Note that $v_{in}/2$ represents the half of the differential input voltage connected to this half-circuit. Since the gate of this

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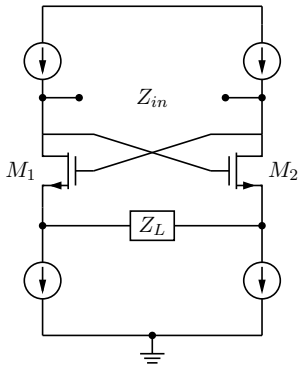

Fig. 1. Analysis circuit of the CMOS cross-coupled topology.

half-circuit is connected to the other differential input, $-v_{in}/2$ is shown at the gate connection.

The current flowing into the drain can be expressed as

$$i_d = \frac{v_{in}}{2z_{ds}} + g_m\left(-\frac{v_{in}}{2} - v_s\right) + \frac{v_{in}}{z_{gd}}, \tag{1}$$

and the current flowing out of the source can be expressed as

$$i_s = \frac{-v_{in} - 2v_s}{2z_{gs}} + g_m\left(-\frac{v_{in}}{2} - v_s\right) + \frac{v_{in}}{z_{gd}}. \tag{2}$$

Once obtaining these, the input admittance Y_{in} can be found as

$$Y_{in} = \left(y_{gd} - \frac{gm}{2} + \frac{y_{ds}}{2}\right) + \frac{(y_{ds} - g_m - y_{gs})(g_m + y_{ds})}{2(y_s + y_{gs} + g_m + y_{ds})}. \tag{3}$$

This can be further simplified, since the transconductance and the load admittance will dominate. Since $g_m >> y_{gd} + y_{ds}$, and $y_s + g_m >> y_{gs} + y_{ds}$, this can be reduced to

$$Y_{in} \approx -\frac{1}{2}\left(\frac{g_m y_s}{g_m + y_s}\right), \tag{4}$$

and can be expressed as an input impedance of

$$Z_{in} = -2z_s - \frac{2}{g_m} = -Z_L - \frac{2}{g_m}. \tag{5}$$

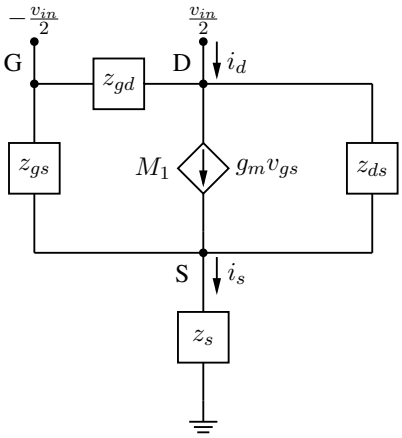

Fig. 2. Half-circuit for analysis of the CMOS cross-coupled topology.

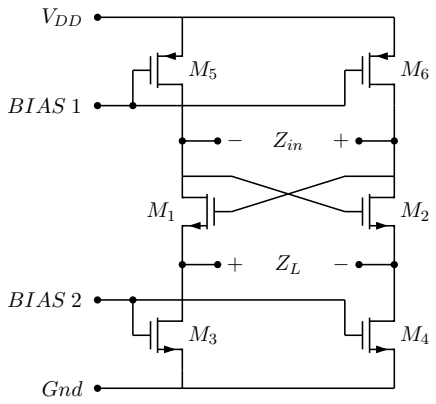

Fig. 3. Schematic of a cross-coupled circuit.

Thus, the input impedance will be approximately equal to the negative impedance of the load, if $Z_L >> \frac{1}{g_m}$.

III. Simulation Results

The prototype of the circuit shown in Fig. 3 used nMOS transistors M_1 and M_2 of 50 $\times$0.5 μm, as in an earlier design [6]. This results in values of $g_{m1} = 0.0036$ S at a bias of 378 μA. So,

$$Z_{in} = -Z_L - \frac{2}{0.0036\ S} \tag{6}$$

where $Z_L = -j\left(\frac{1}{\omega C}\right)$, and C is 2 pF, and becomes

$$Z_{in} = -556\ \Omega + j\frac{1}{\omega \cdot 2\ \text{pF}}. \tag{7}$$

The circuit was simulated in Agilent ADS, with real and imaginary parts of input impedance Z_{in} shown in Fig. 4 and the extracted capacitance shown in Fig. 5. The negative capacitance is indicated by the negative slope of the imaginary part of Z_{in} at low frequencies in Fig. 4, and corresponds to a negative capacitance of -1.8 pF, shown in Fig. 5. In addition, a negative resistance of -390 ohms was observed at

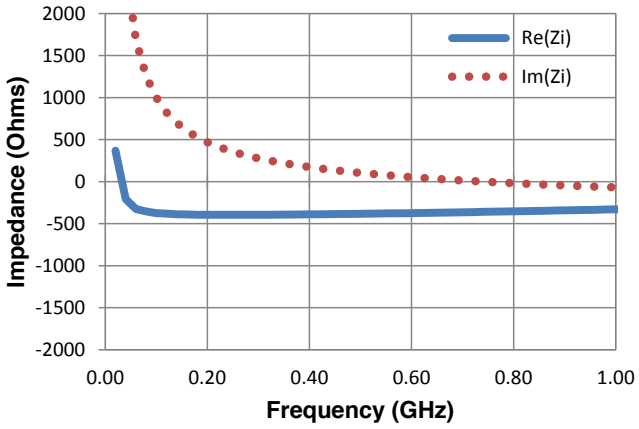

Fig. 4. Simulation results showing real part of Z_{in} (solid blue) and imaginary part of Z_{in} (dotted red).

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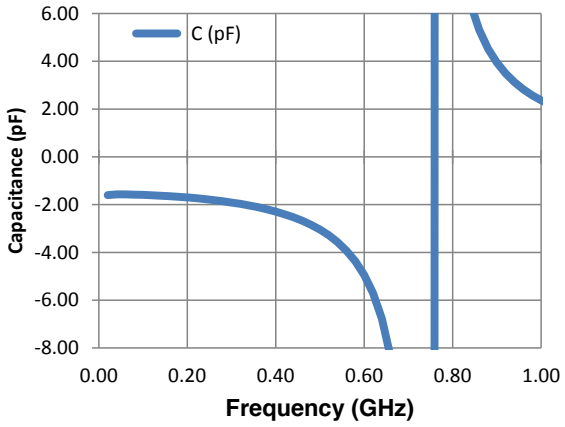

Fig. 5. Simulation results showing extracted capacitance C in pF (solid blue). The anomalous region around 0.8 GHz is due to unwanted inductance.

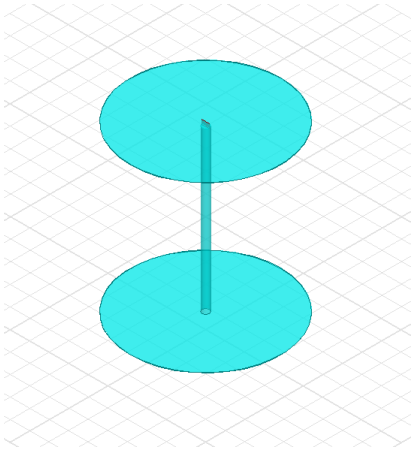

Fig. 7. Simulated EDR model in HFSS. The load is applied in a gap just under the upper disk.

low frequency. The simulated bandwidth is approximately 400 MHz for a capacitance of $\pm 10\%$, and 480 MHz for $\pm 20\%$.

It has been common with this topology to see the calculated and simulated negative capacitances differ by up to 0.5 pF. This is due to the simple model used for analysis, which does not include parasitic and pad capacitances [6]. The layout of the circuit submitted to MOSIS for fabrication is shown in Fig. 6.

Because of the series resistance shown in Fig. 4 , the performance of the capacitor in applications such as metamaterial loading may be altered. To show the effect of this resistance, an electric disk resonator (EDR) was simulated in HFSS for both the ideal case ($C = -1.7$ pF, $R = 0$) and the non-ideal case ($C = -1.7$ pF, $R = -807\ \Omega$) [3]. Fig. 7 shows the EDR under consideration. The disk radius of the simulated EDR was 19.2 mm. The post height was 42 mm, and the post radius was 0.9 mm [3]. The EDR was simulated in an ideal parallel plate waveguide. The side plates of the waveguide were defined as PMC boundaries, and the top and bottom plates were defined as PEC boundaries. The waveguide was 60 mm tall and 48 mm wide.

Fig. 8 shows the extracted values of permeability and permittivity for the simulation of the EDR loaded with the ideal -1.7 pF capacitance, and no series resistance. Fig. 9 shows the extracted values of permeability and permittivity for the simulation of the EDR loaded with -1.7 pF capacitance and a series resistance of $-807\ \Omega$ [8]. Thus, it is shown that the series resistance considerably reduces the frequency over which negative permittivity is achieved. Note that in Fig. 9, the real and imaginary parts of ϵ are approximately equal from around 0.09 GHz to 0.2 GHz. This indicates gain in the medium with an associated propagation constant of [9]

$$\gamma = \alpha + j\beta = j\omega\sqrt{\mu(\epsilon' - j\epsilon'')} = j\omega\sqrt{\mu\epsilon' e^{-j\pi/4}}. \quad (8)$$

Where gain in the metamaterial is not desired the negative resistance may be mitigated by addition of a positive resistance.

IV. Measured Results

The fabricated circuit is shown in Fig. 10. S-parameter measurements of the circuit were performed using a vector

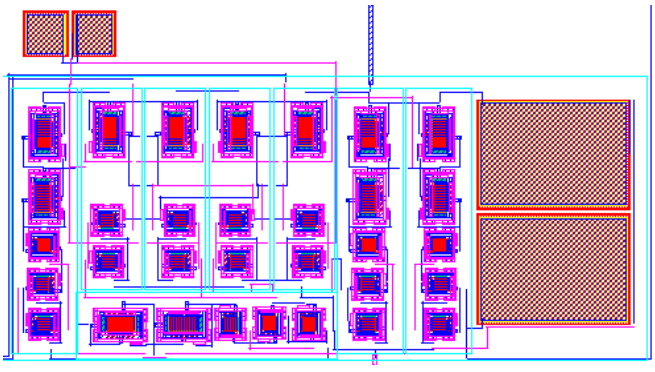

Fig. 6. Layout of cross-coupled circuit submitted to MOSIS for fabrication.

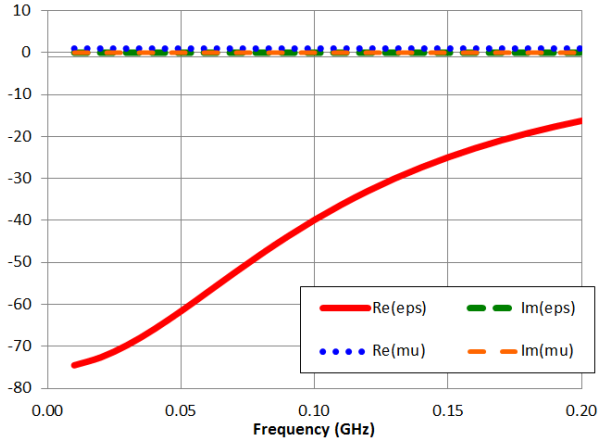

Fig. 8. Simulation results showing extracted real and imaginary parts of permeability and permittivity for the ideal loading of -1.7 pF with no series resistance.

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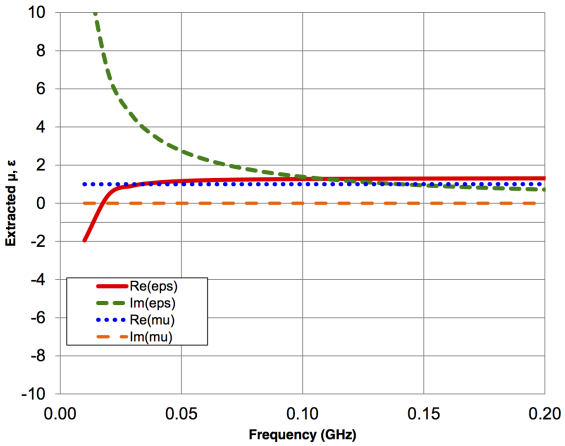

Fig. 9. Simulation results showing extracted real and imaginary parts of permeability and permittivity for the nonideal loading of -1.7 pF with -807 Ω series resistance.

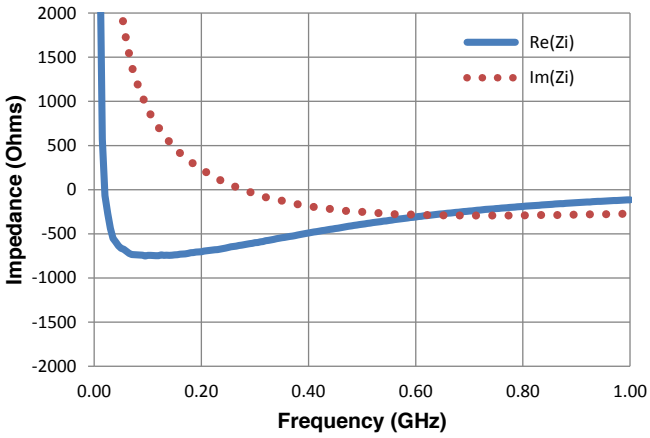

Fig. 11. Measured resistance and reactance of the fabricated circuit.

network analyzer with a bias tee providing dc bias for the circuit. These measurements were used to plot the negative reactance and resistance as shown in Fig. 11. The non-Foster behavior of the circuit is indicated by the negative slope of the reactance plot, showing a negative capacitor with some series negative resistance.

The extracted negative capacitance is shown in Fig. 12 and is observed to be -1.7 pF at low frequencies and within 20% through 200 MHz. The measured resistance of -807 Ω remains negative through 1 GHz.

V. Conclusion

A simple two-transistor negative capacitor has been analyzed, simulated and submitted for fabrication in 0.5 μm CMOS. The simulated negative capacitance and resistance values compared favorably with what was expected from the analysis. The estimated Z_{in} was -556 ohms + $j\frac{1}{\omega \cdot 2\ pF}$, the simulation yields -390 ohms + $j\frac{1}{\omega \cdot 1.7\ pF}$, and the circuit showed stability and consistent results through 200 MHz and the circuit remained useful up to 230 MHz. The measured results show the same negative capacitance but somewhat more negative resistance at -807 ohms. In applications where negative resistance may not be desired, it may be mitigated with a series resistor.

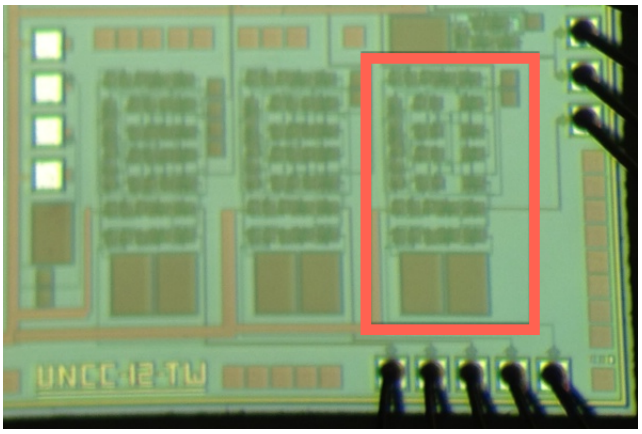

Fig. 10. Photograph of negative capacitance circuit with red box showing location of the circuit.

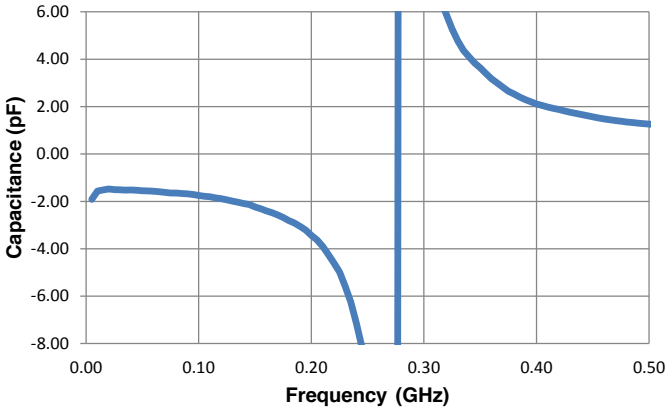

Fig. 12. Extracted capacitance of the fabricated circuit.

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