title

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this is abstract

I. INTRODUCTION

this is main.

II. METHOD

An ADTL082J was used as the Op-Amp, and IRF1010E was used for the n-channel MOSFETs. The $I-V$ characteristics of the MOSFETs where measured prior to the experimental process, in order to obtain a gating voltage and the effective resisance when the MOSFET was open. The negative resistor was designed and measured with the circuit as in Fig. , and the current was measured via a resistor in series in the negative resistor(R). The output voltage of the Op-Amp was also measured to compensate the saturation effects of the real world Op-Amp.

III. RESULT

A. Negative Resistance

Fig 1

B. Tuning Differential Resistance Slopes

Fig 2

C. Effect of Op-Amp Supply Voltage

Fig 3

D. Hysterisis Region

Fig 4

IV. CONCLUSION

Appendix A: MOSFET $I-V$ Characteristics

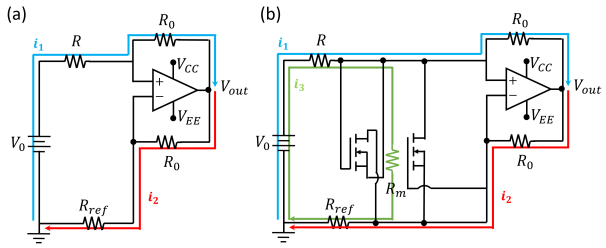
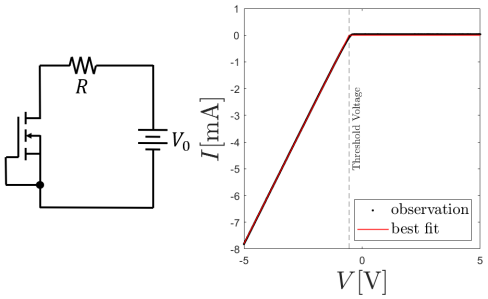


FIG. 1: The (a) capacitance and (b) resistance about the normalized deviation of phase difference.



(a) (b)

FIG. 2: (a) A schematic setup for testing MOSFET $I-V$ characteristic. (b) Experimental result of MOSFET $I-V$ characteristic. Black dots show experiment data and red line is the best fit to Eq. A1. Threshold voltage is denoted as dashed line.

In this experiment we used two MOSFETs with gate terminal and source terminal connected each other. MOSFET is open when the gate–source voltage is higher than the threshold voltage, and current through MOSFET linearly increases as gate–drain voltage increases. We can characterize this property as

$$I = \frac{V - V_{\text{th}}}{(R + R_{\text{MOS}})}\theta(V - V_{\text{th}}) \tag{A1}$$

where V_{th} is threshold voltage, R_{MOS} is effective resistance of MOSFET, and $\theta(V)$ is Heaviside step function. To test this $I-V$ characteristic, we set the circuit as Fig. 2a. We sourced

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voltage from -5.00V to +5.00V in increments of 0.01V, with a resistor of R =560 Ω. The result is plotted in Fig. 2b, where experimental data is denoted as black dots, best fit to Eq. A1 as red line, and threshold voltage as dashed line. Note that the gate–drain voltage is negative when $V_0 > 0$ and vice versa in this setup, so we put $(V - V_{\rm th}) \to -(V - V_{\rm th})$ and $I \to -I$ into the equation. Our best fit values are $V_{\rm th} = 0.5505 \pm 0.0015$ V and $R_{\rm MOS} = 10.21 \pm 0.33\,\Omega$.

Appendix B: Derivation of the theoretical $I-V$ Characteristics of the Negative Resistor

a. Op-Amp

For the

b. Op-Amp and MOSFETs

The unsaturated region of the negativer resistor using enabling MOSFETs is identical to the unsaturated region of the negative resistor without the MOSFETs, since all of the MOSFETs do not flow current. We derive a theoretical description of the differential resistance slopes for the region where a MOSFET is opened.

The three currents present after saturation are depicted in Fig. . In the saturated state, the output voltage of the Op-Amp is fixed as $V_{out} - V_{sat}$. Then the following equations can be obtained.

$$V_{sat} = V_{in} - R(i_1 + i_2) - R_0 i_1 V_{in} =$$