# Jeremiah Mahler

California State University Chico

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# Introduction



- Introduce myself by discussing a past project.
- Enthusiasm for cars and electronics.
- Before any classes on programming or embedded systems.
- Before college.

# Engine Controller



- Built a fully functional engine controller from scratch.
- Controlled both fuel and ignition.
- Four cylinder gas engine.
- Motorola 68HC12 processor.
- Developed under Linux.
- Wrote all code in C.
- Designed all circuits to and from the sensors and actuators.

# Engine Controller

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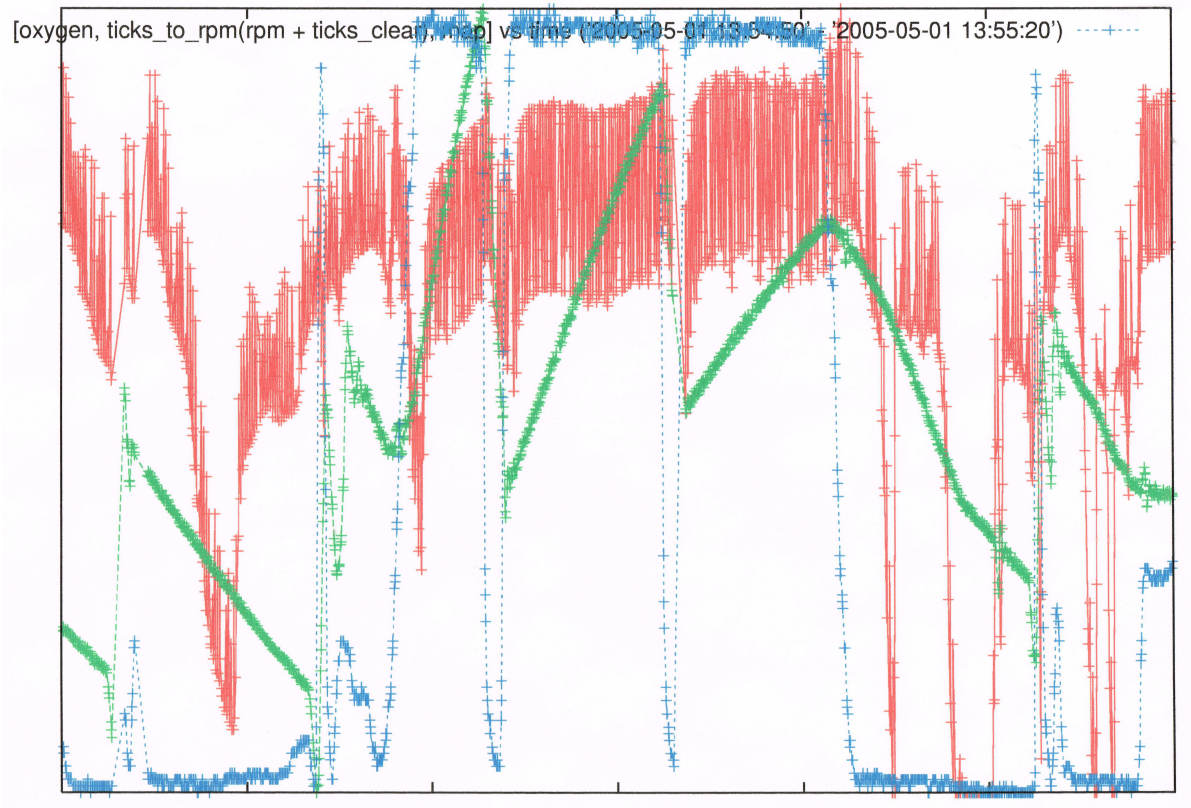
Introduction
Simulation Architecture
Synthesis Time
FPGA Errors
Buffer Underruns
Questions

- Plot from test drive.




- map sensor: blue, O2 sensor: red, rpm: green
- Full throttle, through three gears.
- 2005

# Current Projects



- California State University Chico
  - B.S. Electrical Engineering.
  - Spring 2014.
- McLeod Institute of Simulation Sciences
  - CSU Chico research project.
  - Led by Dr. Crosbie, Dr. Zenor, Dr. Kredo and others.
  - FPGA based real time simulations.
  - Grants from The Office of Naval Research.
  - Electric motor simulations for naval ships and UUV.
  - Work with three other students.

# Preview



- Introduction to one of the simulation architectures that were developed at McLeod Institute.
- Problems encountered during its development.
- Along with solutions.

# Background: Simulation Architecture

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Introduction
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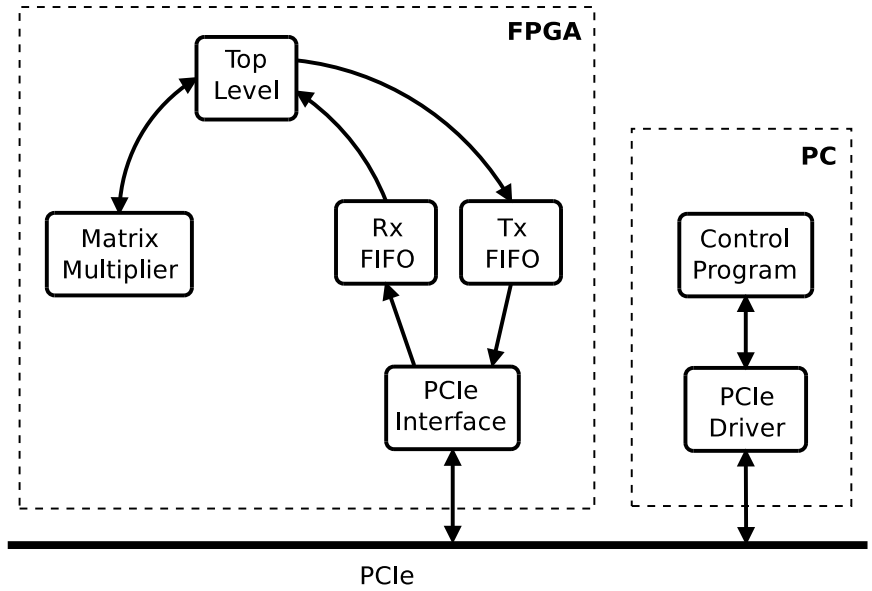


- FPGA
  - Matrix multiplier, core computation engine.
  - Top level connects the matrix multiplier to the PCIe bus.
- PC
  - Control program can be a test program or user interface such as Simulink.

# Problem: Synthesis Time

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Introduction
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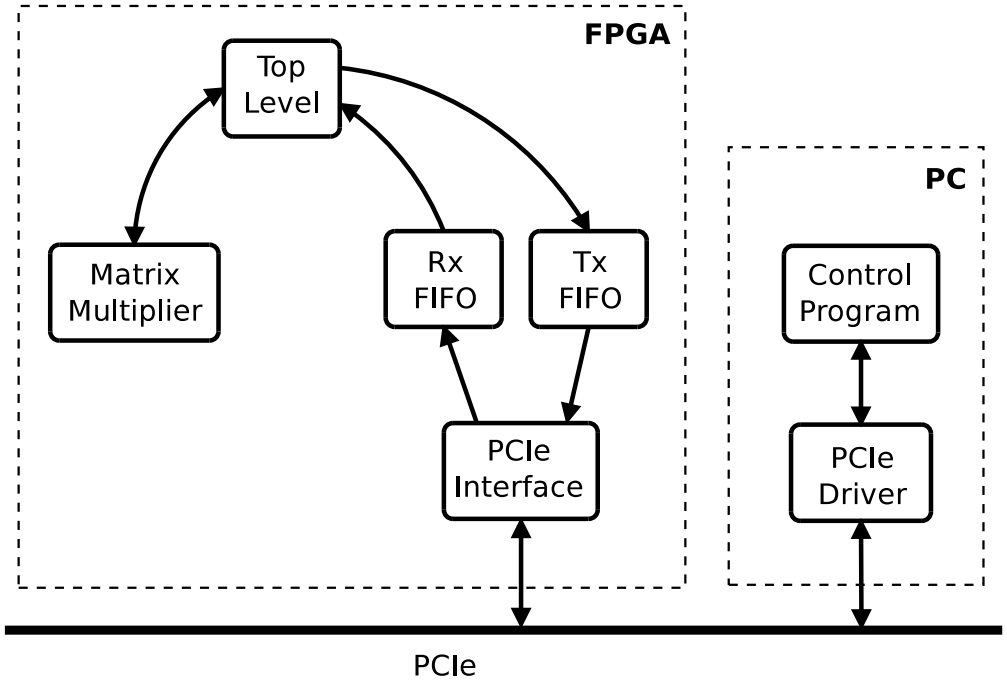


- Synthesis of HDL code with a 20x20 matrix takes two hours.
- HDL Simulation?
  - Simulation of PCIe bus?

# Solution: FIFO Simulation

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Introduction
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Buffer Underruns
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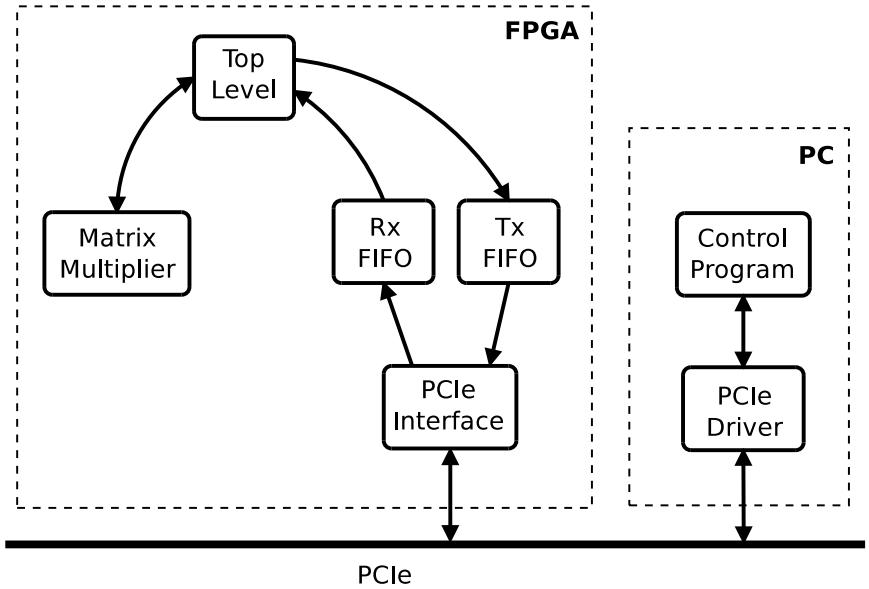
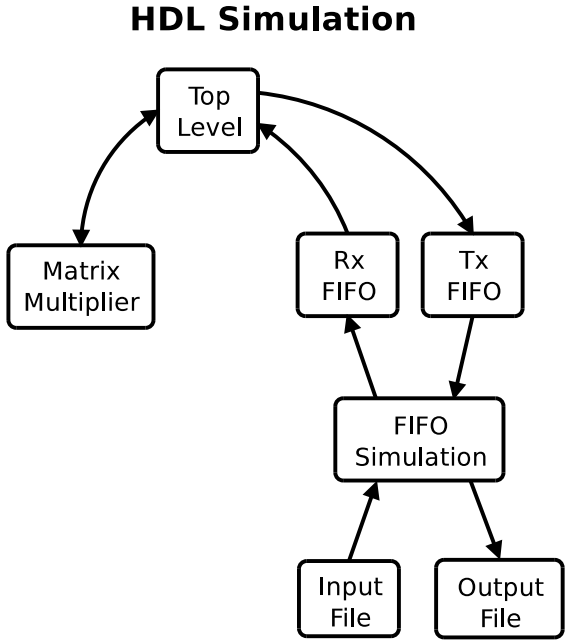
- Matrix multiplier and top level change frequently.
- PCIe bus code rarely changes.
- Idea: Simulate everything after the FIFO interface.




- Frequently changed code can be tested in minutes.

# Problem: Errors Running on FPGA

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Introduction
Simulation Architecture
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Buffer Underruns
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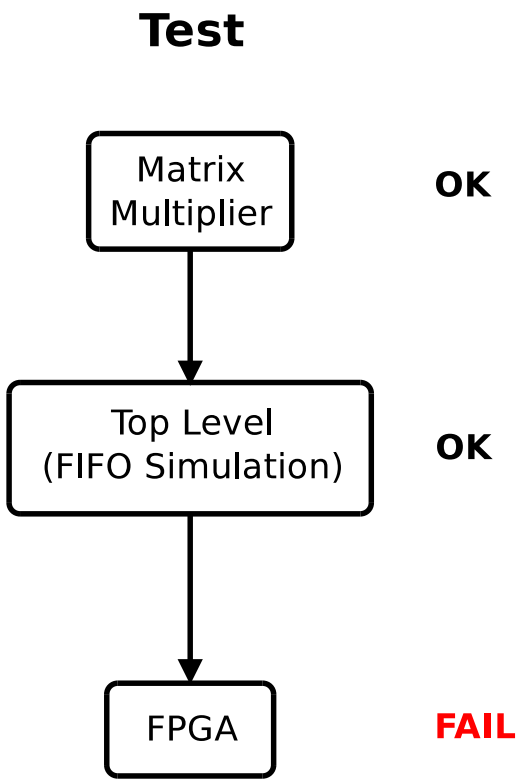



- Sporadic errors when running on FPGA.
- Is the FIFO Simulation not recreating some scenario?

# Diagnosis: Probe Matrix Multiplication in Hardware



- Incorrect results.

$$\begin{bmatrix} 0.025 & 59.50 & 12.0 & 0.0 \\ 1.5 & 32.7 & 12.0 & 0 \\ 0.025 & 89.50 & 12.0 & 0 \\ 0.0 & 23.001 & 0.001 & 1.01 \end{bmatrix} \begin{bmatrix} 0.01 \\ 1.50 \\ 460.0 \\ 60 \end{bmatrix} = \begin{bmatrix} 1929192 \\ 8929282 \\ 8273994 \\ 1234458 \end{bmatrix}$$

- Change test program to use an identity matrix.

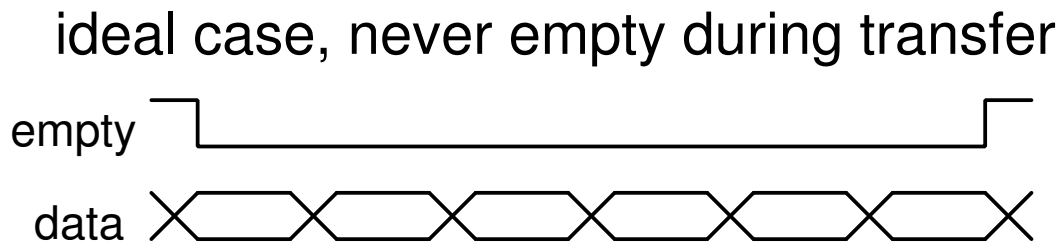
$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 7378292 \\ 9288282 \end{bmatrix}$$

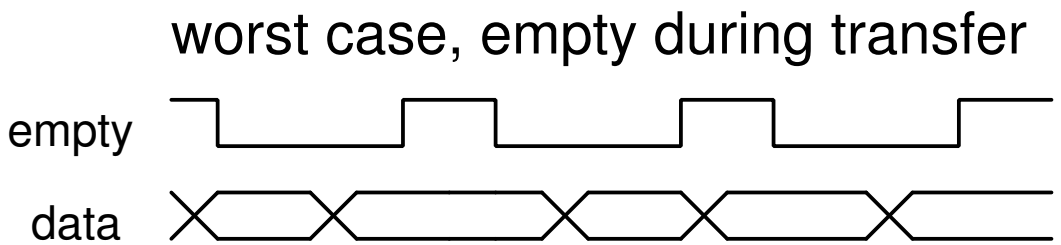
- Partial transfer of input vector? Buffer underrun?

# Update: Include Underrun in FIFO Simulation



- First, add underrun condition to FIFO Simulation.
- Should reproduce error from FPGA.
- Previously, the FIFO Simulation produced the ideal case.



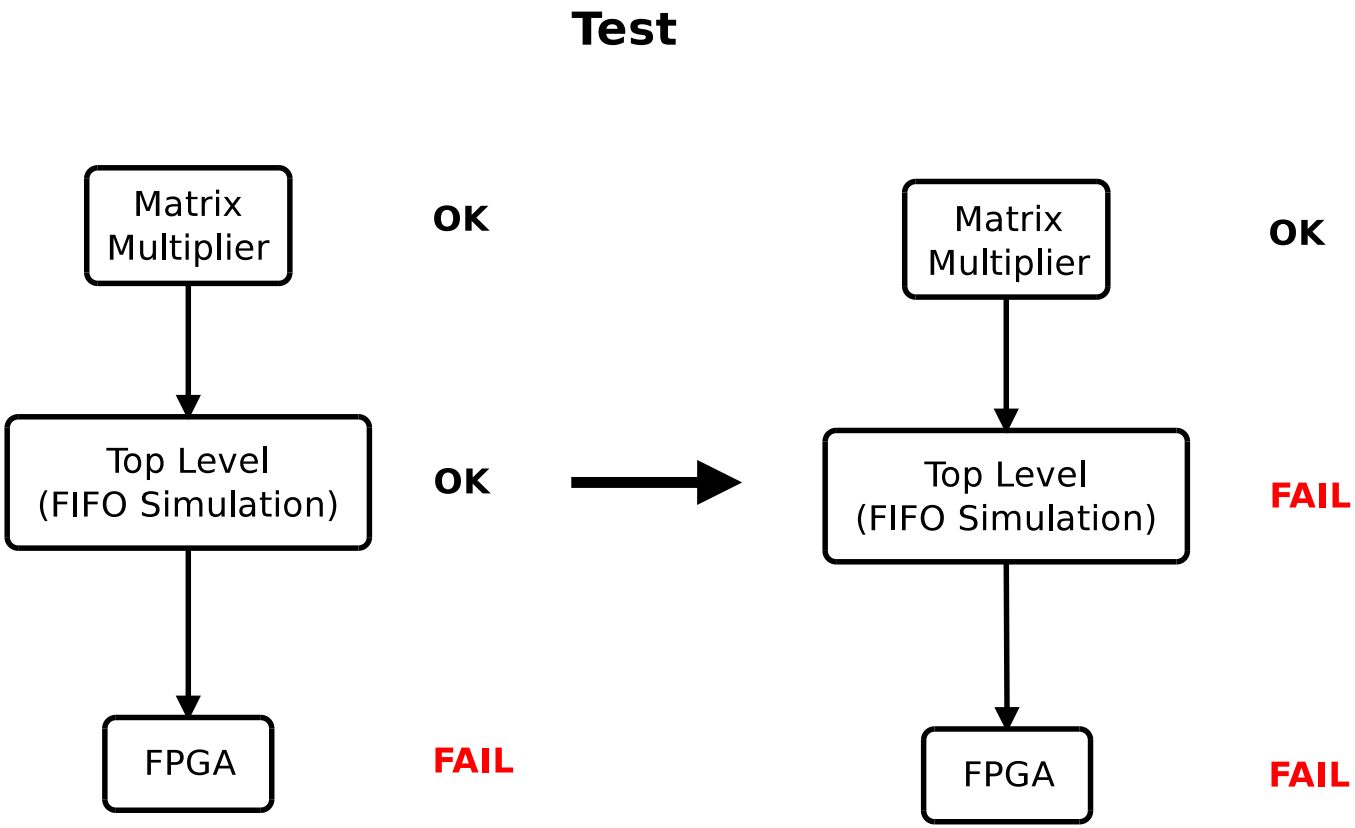




- Now the FIFO Simulation produces the worst case.

# Update: FPGA Error Reproduced in FIFO Simulation



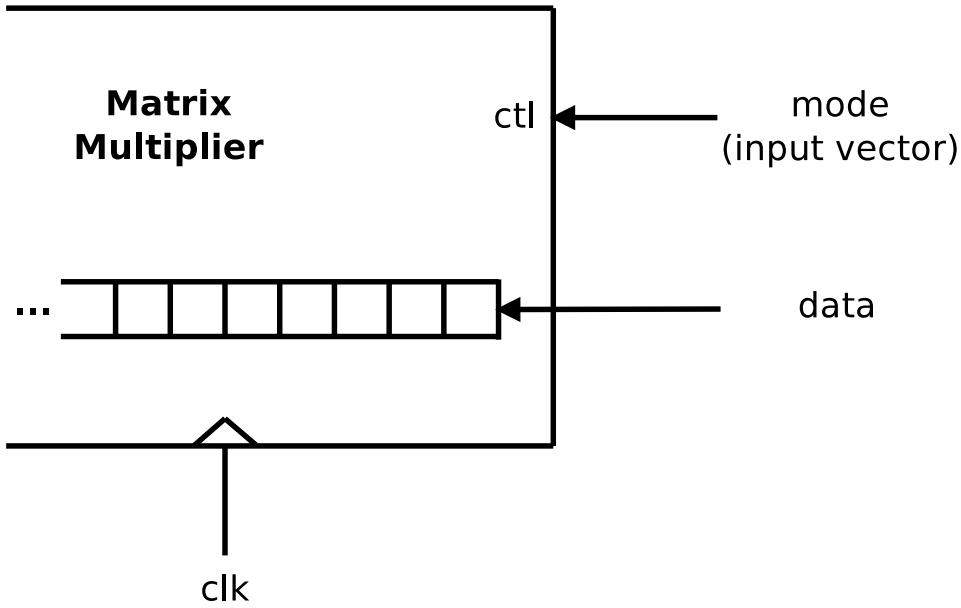
- Re-run FIFO Simulation tests.
- Error in FPGA reproduced in FIFO Simulation.



# Problem: Buffer Underruns



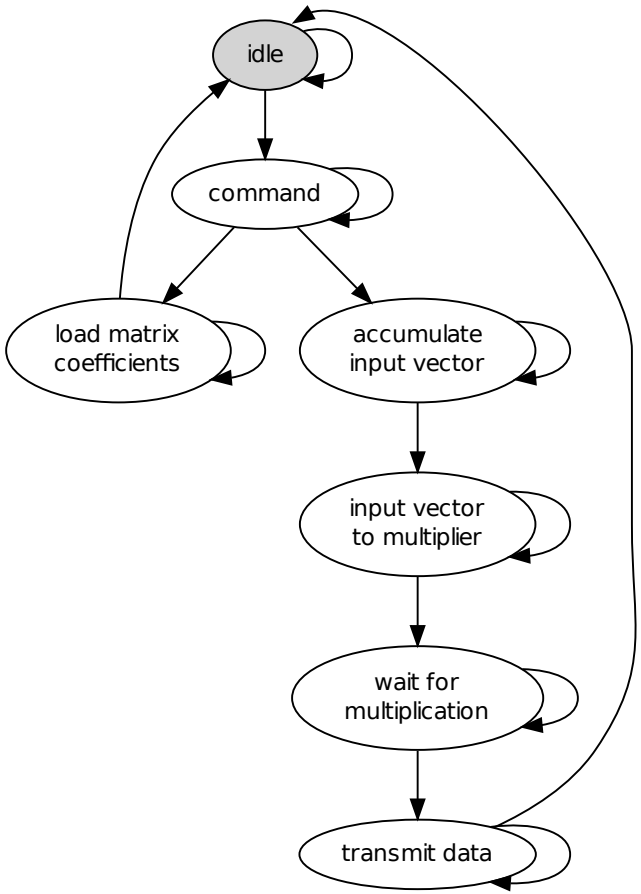
- Why are buffer underruns breaking the top level?
- Input vector is transferred directly from the FIFO in to the data input.
- Matrix multiplier reads a new value on each clock edge.
- **Operation cannot be paused.**



# Solution: Accumulate Input Vector



- Accumulate input vector in top level before transfer to matrix multiplier.



# Success: Architecture Operating Correctly

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Introduction
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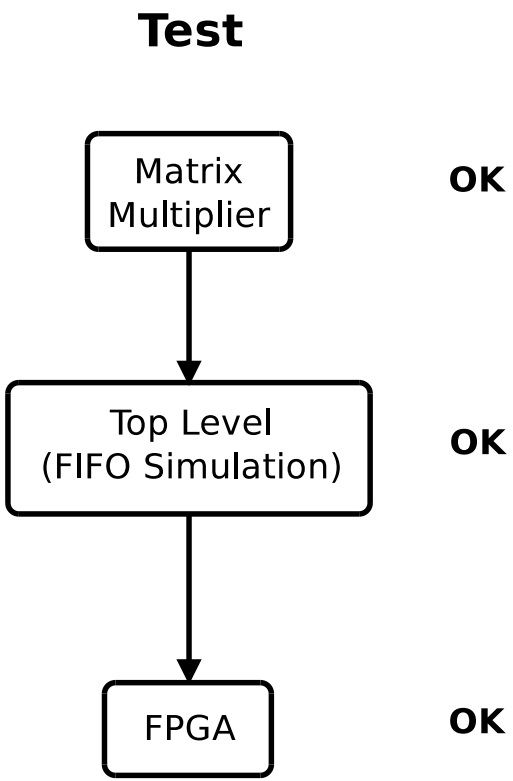

Questions?

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