National Semiconductor

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74F381
4-Bit Arithmetic Logic Unit

General Description

The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional select input codes force the function outputs LOW or HIGH. Carry propagate and generate outputs are provided for use with the 'F182 carry lookahead generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

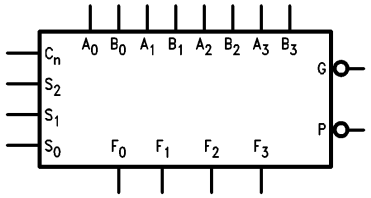
Features

- Low input loading minimizes drive requirements
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- Carry generate and propagate outputs for use with carry lookahead generator

Commercial	Package Number	Package Description
74F381PC	N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
74F381SC (Note 1)	M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F381SJ (Note 1)	M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Logic Symbols



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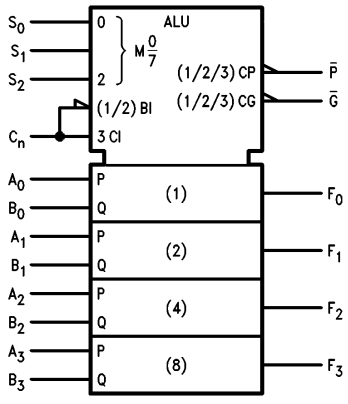
IEEE/IEC



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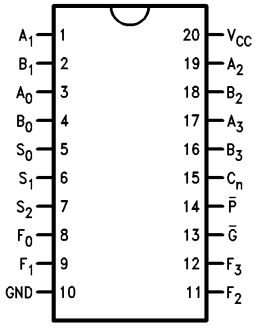
Connection Diagram

Pin Assignment for DIP and SOIC



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RRD-B30M105/Printed in U. S. A.

Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	A Operand Inputs	1.0/3.0	20 μA/ −1.8 mA
B_0-B_3	B Operand Inputs	1.0/3.0	20 μA/ −1.8 mA
S_0-S_2	Function Select Inputs	1.0/1.0	20 μA/ −0.6 mA
C_n	Carry Input	1.0/4.0	20 μA/ −2.4 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	−1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	−1 mA/20 mA
F_0-F_3	Function Outputs	50/33.3	−1 mA/20 mA

Functional Description

Signals applied to the Select inputs S_0-S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package.

The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in *Figure 1*. Note that an 'F382 ALU is used for the most significant package. Typical delays for *Figure 1* are given in *Figure 2*.

Function Select Table

Select			Operation
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level
L = LOW Voltage Level

FIGURE 2. 16-Bit Delay Tabulation

Path Segment	Toward F	Output $C_n + 4$, OVR
A_i or B_i to $\overline{P}$	7.2 ns	7.2 ns
$\overline{P}_i$ to $C_n + 4$ ('F182)	6.2 ns	6.2 ns
C_n to F	8.1 ns	—
C_n or $C_n + 4$, OVR	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

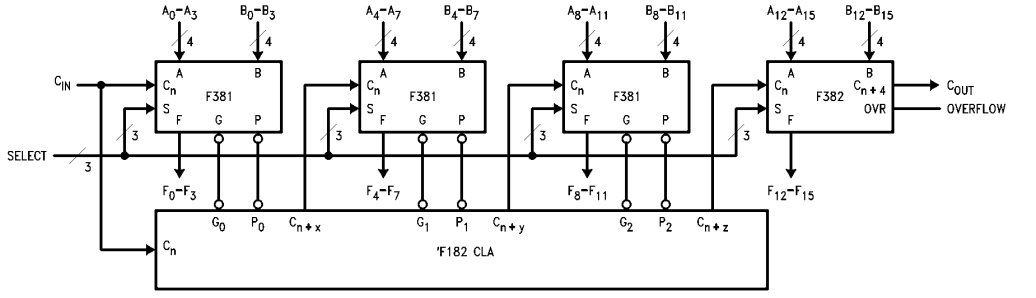

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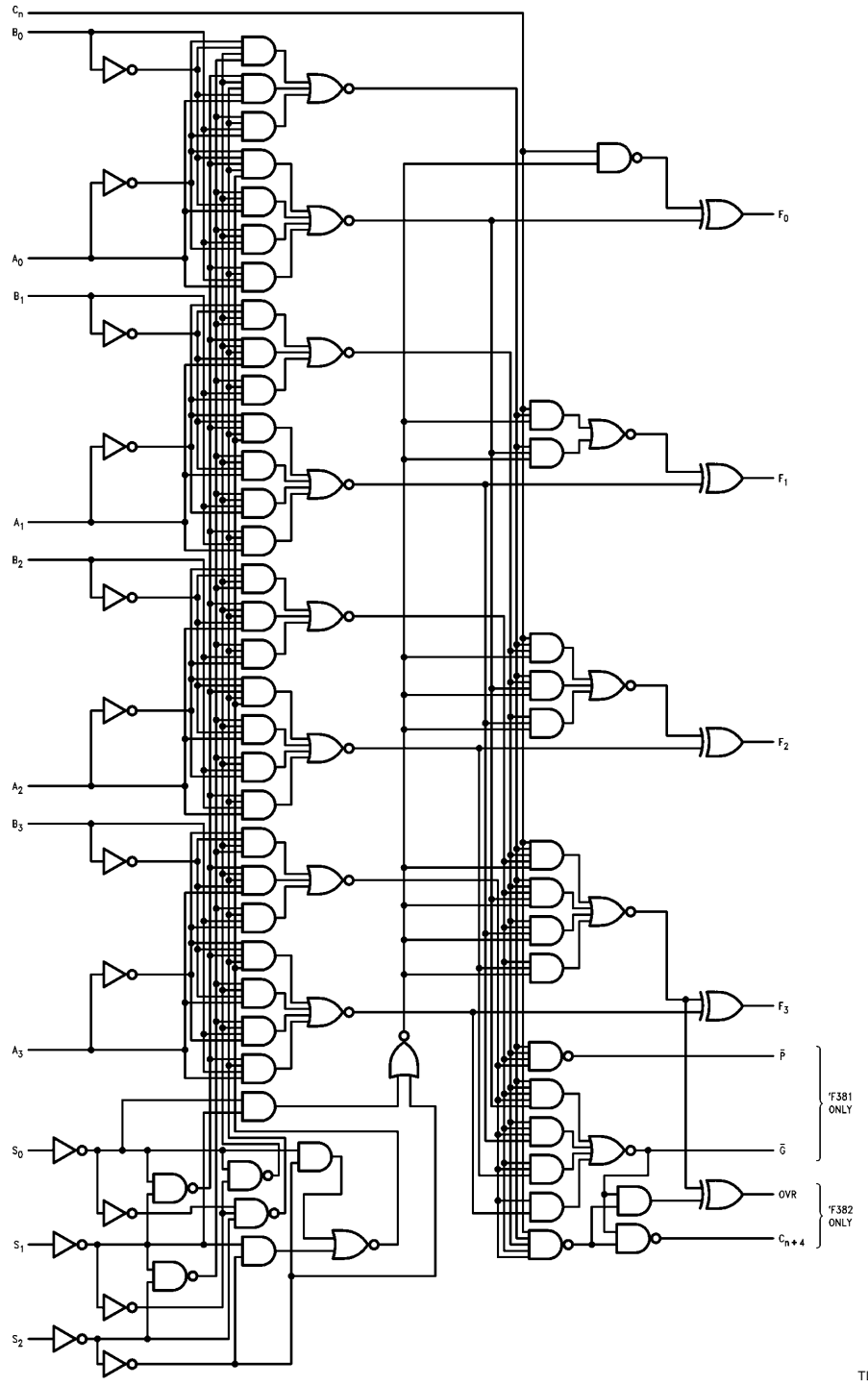
FIGURE 1. 16-Bit Lookahead Carry ALU Expansion

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Table

	Inputs						Outputs					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	L	L	L	X	X	X	L	L	L	L	L	L
B Minus A	H	L	L	L	L	L	H	H	H	H	H	L
				L	L	H	L	H	H	H	L	L
				L	H	L	L	L	L	L	H	H
				L	H	H	H	H	H	H	H	L
				H	L	L	L	L	L	L	H	L
				H	L	H	H	H	H	H	L	L
				H	H	L	H	L	L	L	H	H
				H	H	H	L	L	L	L	H	L
A Minus B	L	H	L	L	L	L	H	H	H	H	H	L
				L	L	H	L	L	L	L	H	H
				L	H	L	L	H	H	H	L	L
				L	H	H	H	H	H	H	H	L
				H	L	L	L	L	L	L	H	L
				H	L	H	H	L	L	L	H	H
				H	H	L	H	H	H	H	L	L
				H	H	H	L	L	L	L	H	L
A Plus B	H	H	L	L	L	L	L	L	L	L	H	H
				L	L	H	H	H	H	H	H	L
				L	H	L	H	H	H	H	H	L
				L	H	H	L	H	H	H	L	L
				H	L	L	H	L	L	L	H	H
				H	L	H	L	L	L	L	H	L
				H	H	L	L	L	L	L	H	L
				H	H	H	H	H	H	H	L	L
A ⊕ B	L	L	H	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	L
				X	H	H	L	L	L	L	L	L
A + B	H	L	H	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	H
				X	H	H	H	H	H	H	H	L
AB	L	H	H	X	L	L	L	L	L	L	L	L
				X	L	H	L	L	L	L	H	H
				X	H	L	L	L	L	L	L	L
				X	H	H	H	H	H	H	H	L
PRESET	H	H	H	X	L	L	H	H	H	H	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	H
				X	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

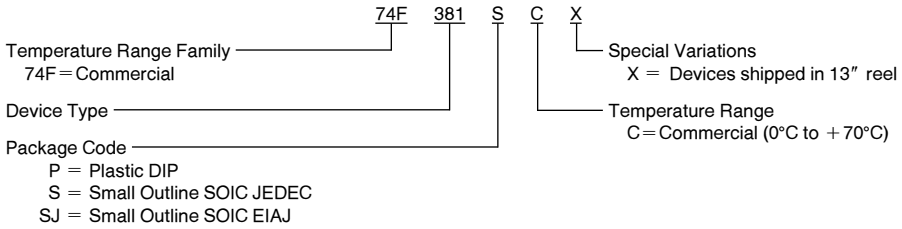
Symbol	Parameter		74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA		V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (S_n)
					−1.8	mA	Max	V_{IN} = 0.5V (A_n, B_n)
					−2.4	mA	Max	V_{IN} = 0.5V (C_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			59	89	mA	Max	

AC Electrical Characteristics

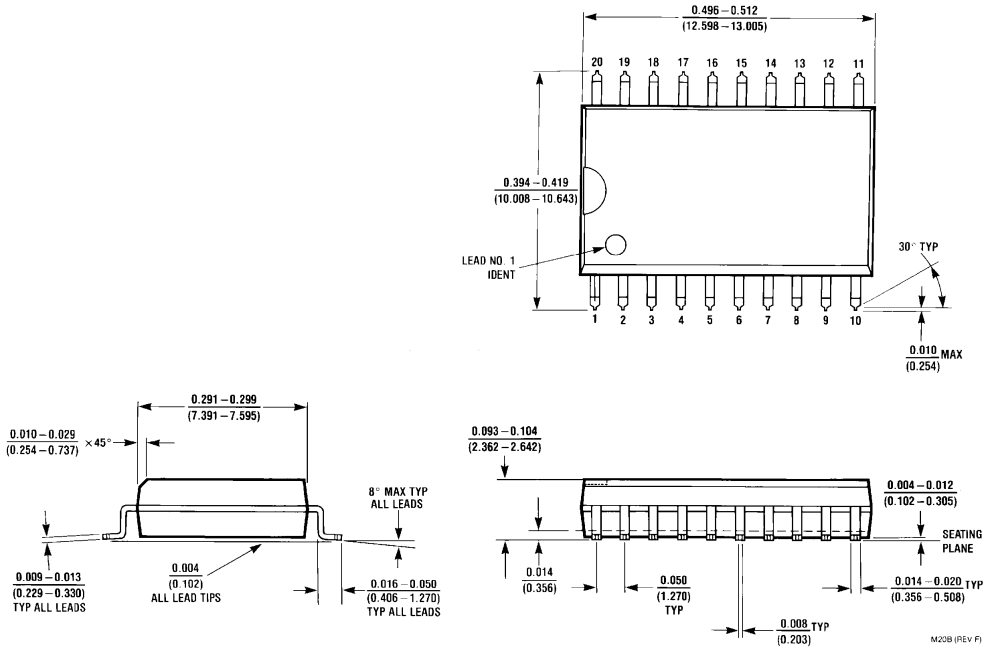
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74F $T_A, V_{CC} =$ Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	8.1	12.0	2.5	13.0	ns
t_{PHL}	C_n to F_i	2.5	5.7	8.0	2.5	9.0	
t_{PLH}	Propagation Delay	4.0	10.4	15.0	4.0	16.0	ns
t_{PHL}	Any A or B to Any F	3.5	8.2	11.0	3.5	12.0	
t_{PLH}	Propagation Delay	4.5	8.3	20.5	4.5	21.5	ns
t_{PHL}	S_i to F_i	4.0	8.2	15.0	4.0	16.0	
t_{PLH}	Propagation Delay	3.5	6.4	10.0	3.5	11.0	ns
t_{PHL}	A_i or B_i to $\overline{G}$	3.5	6.8	10.0	3.0	11.0	
t_{PLH}	Propagation Delay	2.5	7.2	10.5	2.5	11.5	ns
t_{PHL}	A_i or B_i to $\overline{P}$	3.5	6.5	9.5	3.5	10.5	
t_{PLH}	Propagation Delay	4.0	7.8	12.0	4.0	13.0	ns
t_{PHL}	S_i to $\overline{G}$ or $\overline{P}$	4.5	10.2	13.5	4.5	14.5	

Ordering Information

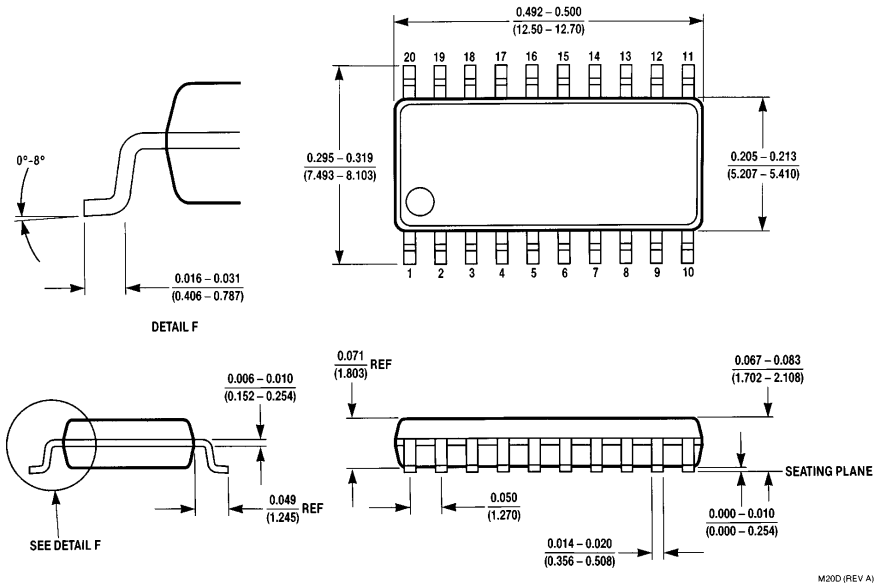
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

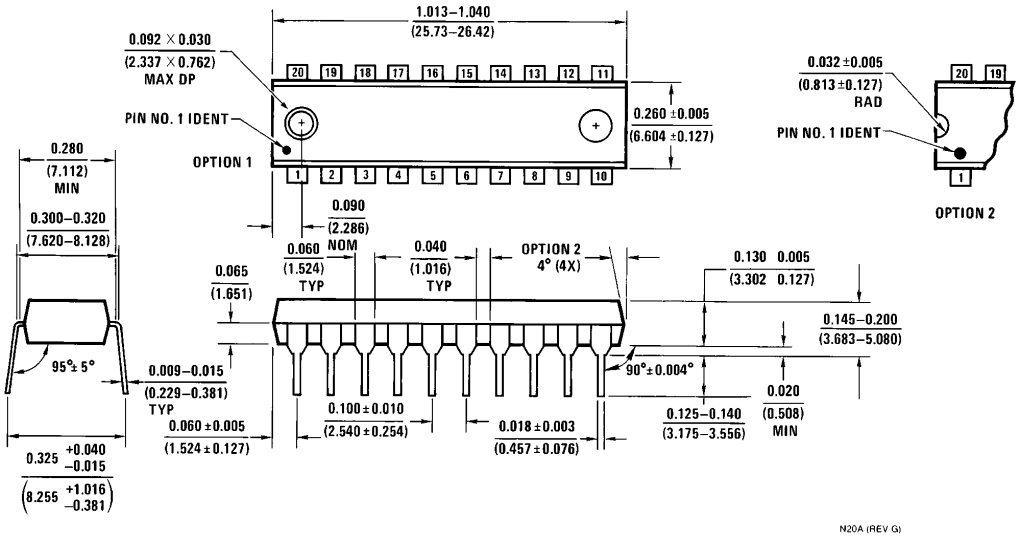


20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B



20-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D

Physical Dimensions inches (millimeters) (Continued)



20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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