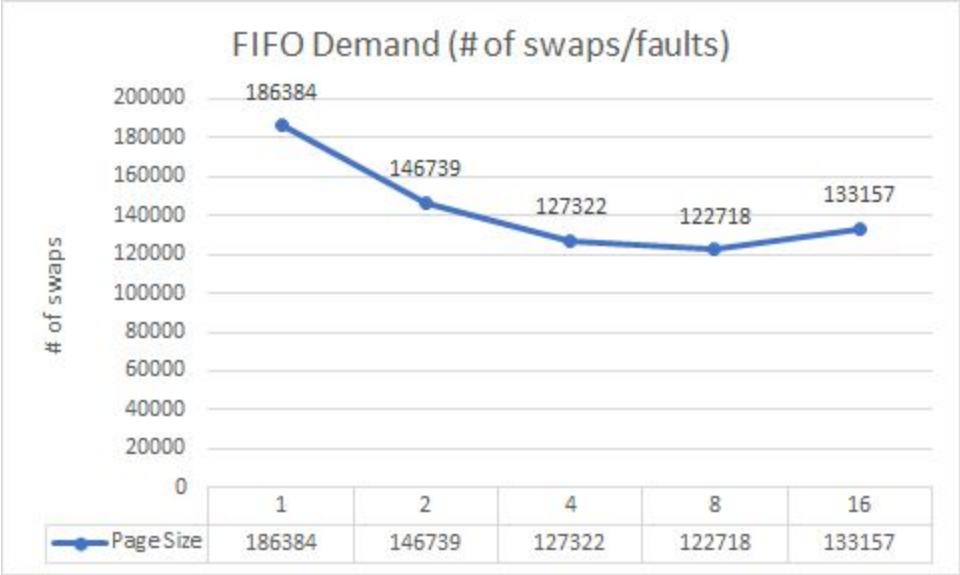
Analysis and Experimentation

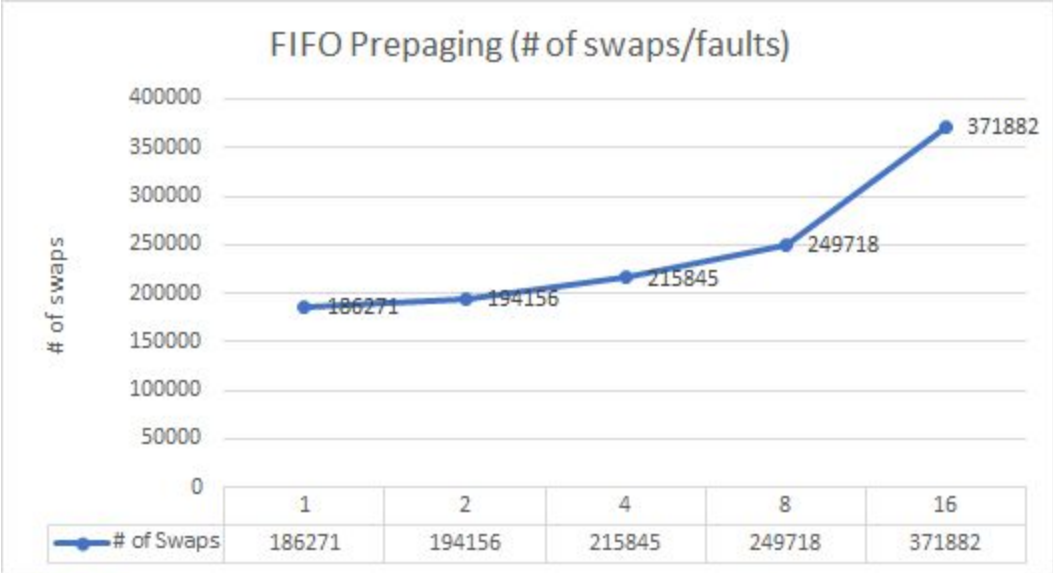
We found that for each algorithm, increasing the page size decreased the number of swaps until the size of 16 where it either slightly increased the number of swaps for demand paging. In the case of prepaging we found that page size of one is the lowest amount of page swaps. For FIFO the number of swaps increased significantly as the page size increased. However for LRU and clock as the page size goes from one to two the amount of page swaps required essentially doubles, and for each successive page size increase the number of page swaps seems to decrease towards a limit. Overall what was most apparent is the ptrace example, prepaging increases the amount of page swaps required versus demand paging. This is in fact what we did not expect as prepaging is intended to reduce the number of page faults by preventing future page faults. What we concluded is that the ptrace example is ordered in a way that results in an increase from prepaging to represent the potential cons of prepaging, because when we tested smaller custom examples on the same algorithms we found the expected results of prepaging versus demand paging.

The clock algorithm performs better in demand paging than any of the other algorithm even at higher page sizes. However it performs the worst at higher page sizes for prepaging. LRU is the worst performing for demand and second worst at prepaging. Where FIFO is second worst for demand and best for prepaging. FIFO has the unique advantage of of having an increasing curve for page size for prepaging. Where the other algorithms increase drastically after page size one and very slowly decrease. This means at smaller page sizes FIFO outperforms the other greatly for prepaging. We expected LRU to be more intensive then clock as they operate similarly except there is more overhead involved with LRU.

FIFO Demand (# of swaps/faults)
1 - 186384
2 - 146739
4 - 127322
8 - 122718
16 - 133157

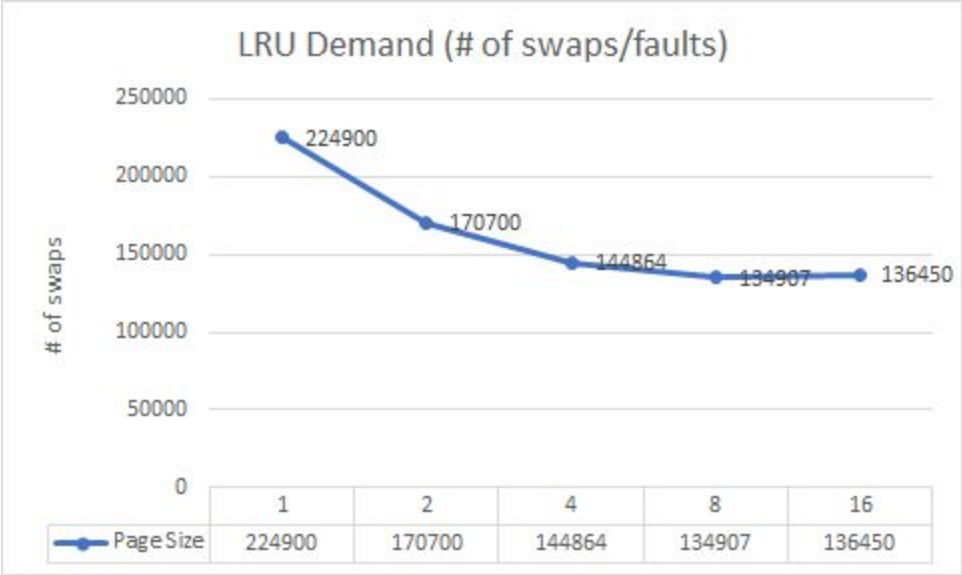



FIFO Prepaging (# of swaps/faults)
1 - 186271
2 - 194156
4 - 215845
8 - 249718
16 - 371882

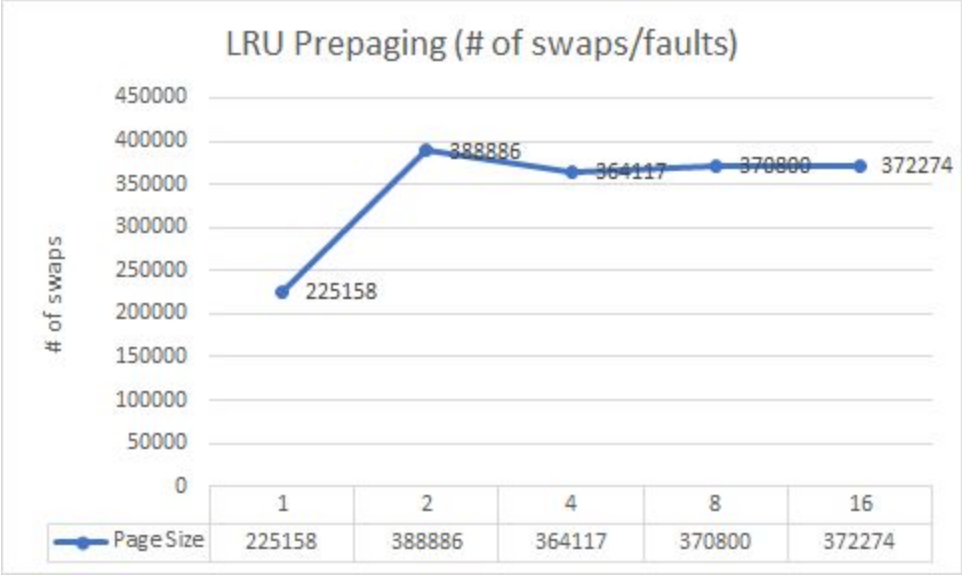



LRU Demand (# of swaps/faults)
1 - 224900

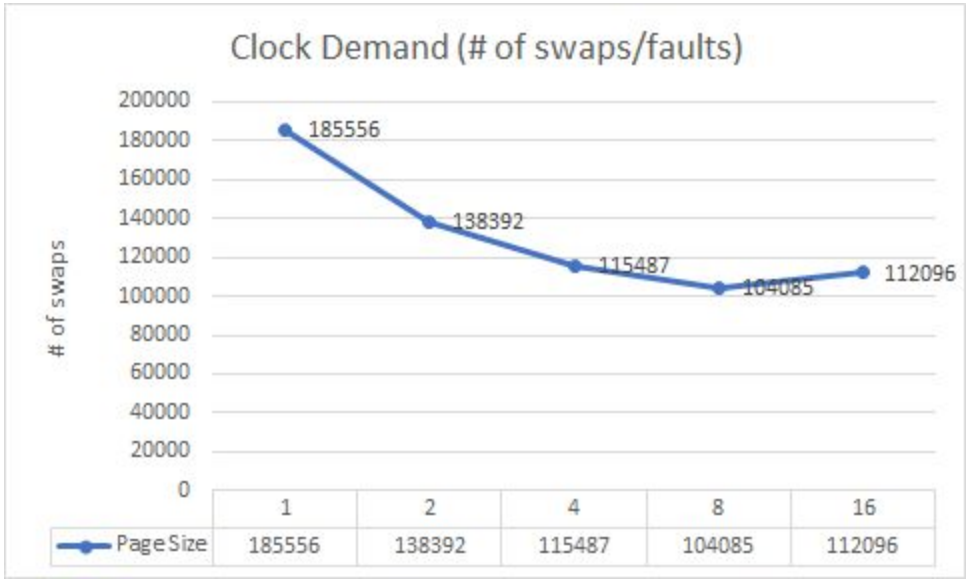
2 - 170700
4 - 144864
8 - 134907
16 - 136450




LRU Prepaging (# of swaps/faults)
1 - 225158
2 - 388886
4 - 364117
8 - 370800
16 - 372274



Clock Demand (# of swaps/faults)
1 - 185556
2 - 138392
4 - 115487
8 - 104085
16 - 112096




Clock Prepaging (# of swaps/faults)
1 - 185354
2 - 416650
4 - 383511
8 - 380246
16 - 376358