Final Project #2: Combinational Fault Testing

Objective: Project #2 will provide students with a practical exercise in fault testing combinational circuits. Students will be randomly assigned two **black box** circuits, for which they will develop minimum test sets to detect the presence of physical faults. If faults do exist, further testing will be conducted to pinpoint the exact location of the fault within the combinational circuit. A presentation will be delivered by each student, outlining the methodology and derivation used to detect the presence of circuit faults. **This is an individual project assignment.**

i) Background:

Lecture 18: Testing has been posted on Canvas. It will provide you with the necessary background and methodologies required to test digital circuits and detect physical faults. In this project we will be using stuck-at-fault testing to detect possible stuck-at-faults or bridge faults

ii) Requirements:

Two combinational circuits will be randomly assigned to you in the form of .vho files. An email has been sent to you with two links corresponding to your two assigned circuits. These two circuits may or may not contain physical faults which have been manually injected into the system. Your assigned circuit diagram, labelled as circuit1-4, may be viewed in the Appendix of this document. Note that these diagrams represent the expected fabricated circuit without the presence of physical faults.

For each assigned combinational circuit:

1) Derive the minimum test set required to detect the presence of physical faults in the circuit.

2) Based on the minimum test set, determine if a fault exists in the circuit. In this case, you must create a testbench for the circuit, insert your vho as the Device-Under-Test (DUT), and apply the minimum test set as stimulus to determine whether a fault exists. Compare the **actual** circuit output to your **expected** output.

3) If a fault exists, conduct further testing to determine the exact location of the fault in the circuit. Consider direct and indirect testing of wires. Create another testbench which clearly outlines your verification methodology and reasoning. Provide your fault diagnosis i.e where the fault resides in the circuit based on your testing methods.

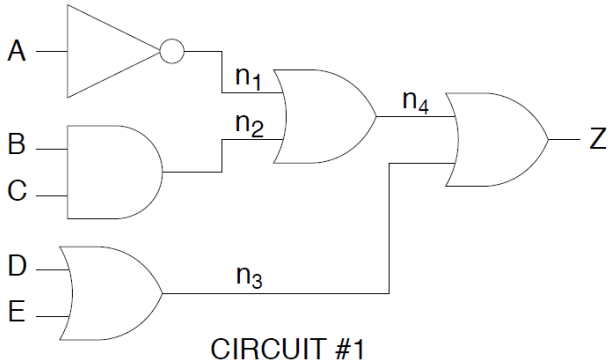
iii) Deliverables:

Create an audio recorded presentation consisting of two parts: Part 1 describes your testing and methodology used to determine the faults in the first assigned circuit, and part2 for the second circuit. Explain in detail the procedures conducted in steps 1 through 3 above, your reasoning, and fault location. Ensure you clearly outline and label the fault on your corresponding circuit figure. If your presentation is too large to upload to canvas, upload your presentation to the cloud and provide the link in your submission as a “presentation.txt” file, included in your project zip.

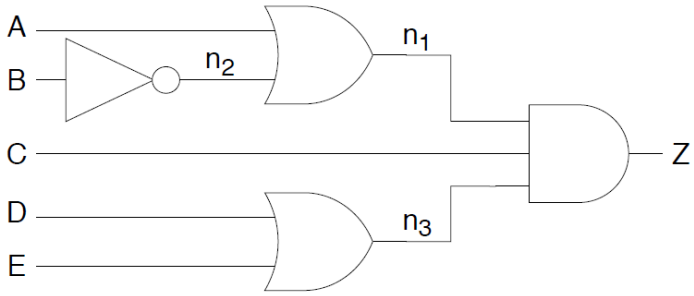
Ensure you include all files required to mimic your results, including testbenches and vhos. Clearly outline and label the fault on the corresponding circuit figure found in the Appendix.

Submit your presentation and vhdl project(s) in one zip. Ensure your circuit figures are included clearly labelling and indicating the faults in your circuit. Uploaded your project to Canvas by the specified due date on the semester schedule: **August 15th, 2020 by 11:59pm**

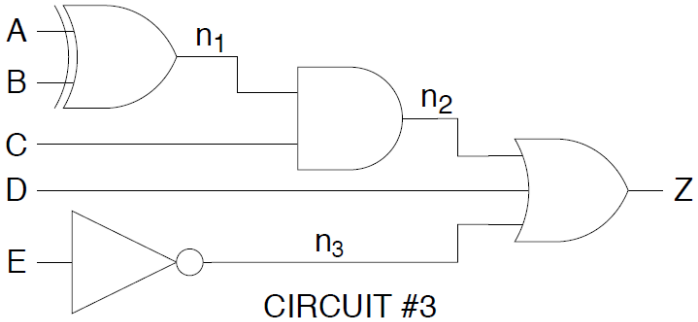
Appendix



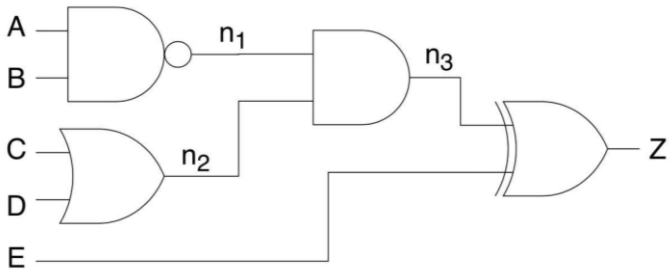
CIRCUIT #1



CIRCUIT #2



CIRCUIT #3



CIRCUIT #4