GD54/74LS164

8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTER

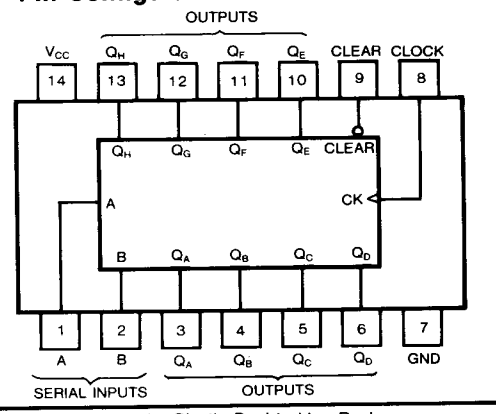
Feature

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

Description

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip flop to the low level at the next clock pulse. A high level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered clocking occurs or the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

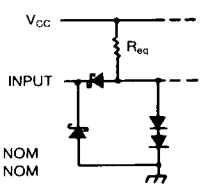
Function Table

INPUTS				OUTPUTS	
CLEAR	CLOCK	A	B	Q_A	$Q_B \cdots Q_H$
L	X	X	X	L	L ··· L
H	L	X	X	Q_{AO}	$Q_{BO} \cdots Q_{HO}$
H	↑	H	H	H	$Q_{Gn} \cdots Q_{Gn}$
H	↑	L	X	L	$Q_{An} \cdots Q_{Gn}$
H	↑	X	L	L	$Q_{An} \cdots Q_{Gn}$

H=high level (steady state), L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low-to-high-level
Q_{AO}, Q_{BO}, Q_{HO}=the level of Q_A, Q_B or Q_H respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn}=the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

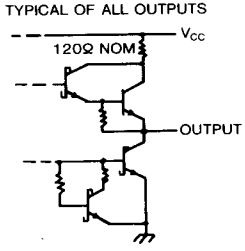
Schematics of Inputs and Outputs

EQUIVALENT OF EACH INPUT

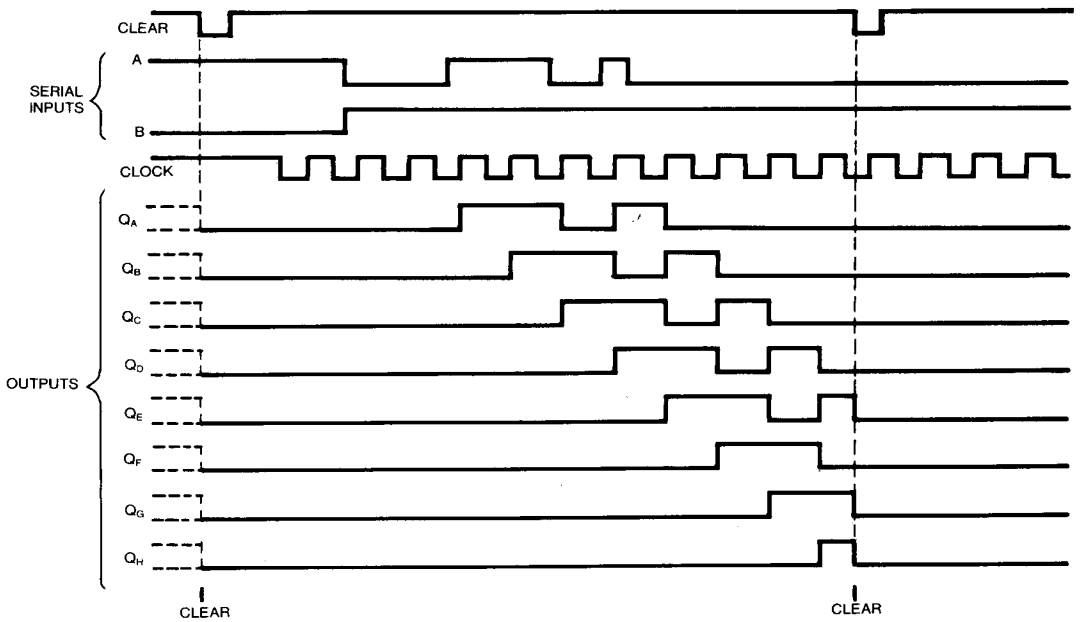


CLEAR, CLOCK: 17KΩ NOM
SERIAL: 25KΩ NOM

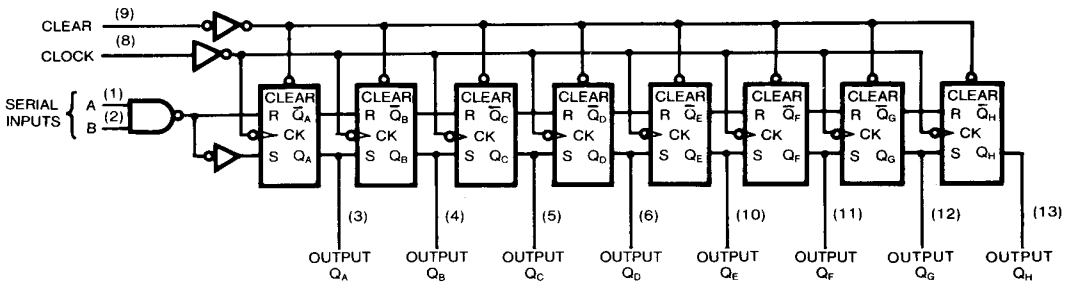
TYPICAL OF ALL OUTPUTS



Typical Clear, Shift, and Clear Sequences



Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_w	Width of clock or clear input pulse		20			ns
t_{su}	Data set up time		15			ns
t_h	Data hold time		5			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min	V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max	V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	mA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)				16	27	mA

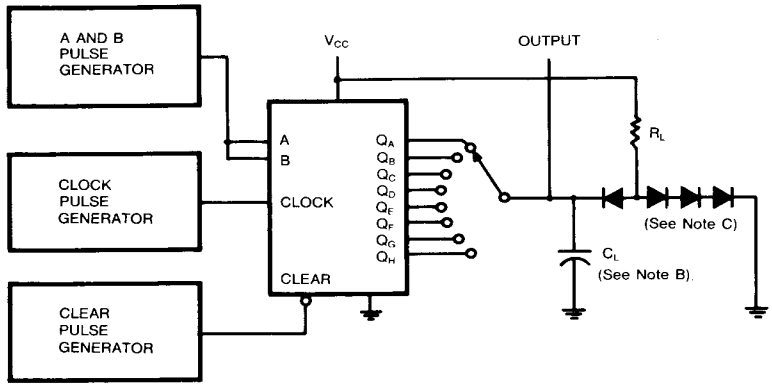
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: I_{CC} is measured with outputs open, serial inputs grouned, the clock input at 2.4V, and a momentary ground, then 4.5V applied.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

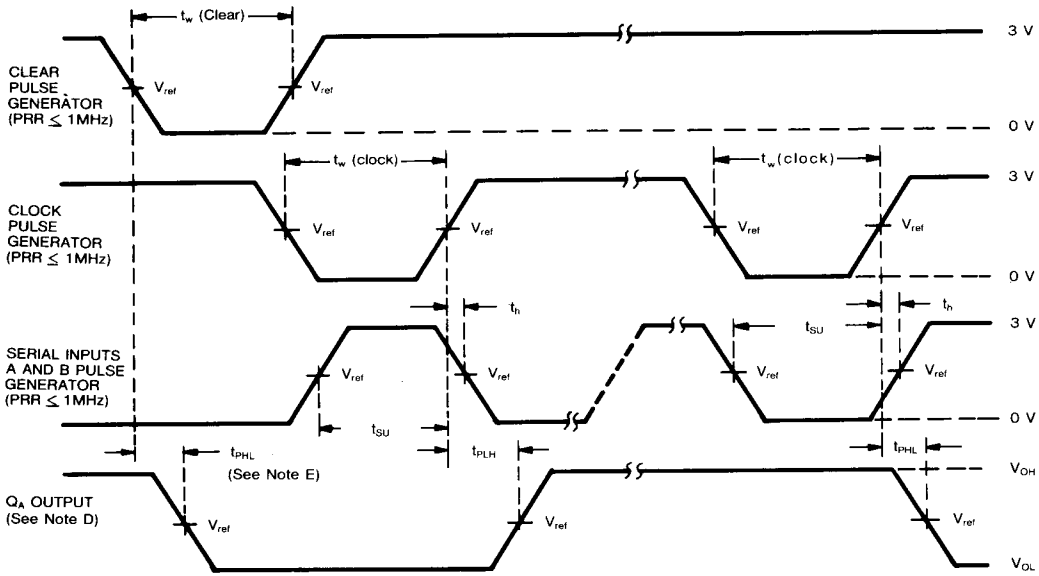
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	$C_L=15pF$, $R_L=2k\Omega$ See Figure 1		24	36	ns
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

#For load circuit and voltage waveforms, see page 3-11.

Parameter Measurement Information



TEST CIRCUIT



VOLTAGE WAVEFORMS

Note A: The pulse generators have the following characteristics: duty cycle ≤50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.
Note B: C_L includes probe and jig capacitance.
Note C: All diodes are 1N3064 or 1N916
Note D: Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
Note E: Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
Note F: $V_{ref} = 1.3V$

Figure 1 Switching Times