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Revision History

Revision Number	Description	Revision Date
001	- Initial Release	October 2021
002	- Removed IBECC registers from Chapter 3	January 2022
003	- Updated Section 3.2, “Processor Memory Controller (MCHBAR) Registers” in Chapter 3 — Added Section 3.2.4 (offset 0x7900) to Section 3.2.41 (offset 0x7B54)	April 2022

§ §

1 Introduction

This is Volume 2 of 12th Generation Intel® Core™ Processors Datasheet. Volume 2 provides register information for the processor.

Refer to document #655258 for the Datasheet, Volume 1 of 2

The processor contains one or more PCI devices within a single physical component. The configuration registers for these devices are mapped as devices residing on the PCI Bus assigned for the processor socket. This document describes these configuration space registers or device-specific control and status registers only.

Table 1. Updated Terminology

Existing	Updated Terminology
TDP	Processor Base Power
cTDP Down Power	Minimum Assured Power
cTDP Down Frequency	Minimum Assured Frequency
cTDP Up	Maximum Assured Power
cTDP Up Frequency	Maximum Assured Frequency
P1 Freq	Processor Base Frequency
Small Core	E-core
Big Core	P-core

2 Processor Configuration Register Definitions and Address Ranges

This section describes the processor configuration register, I/O, memory address ranges and Model Specific Registers (MSRs). The chapter provides register terminology. PCI Devices and Functions are described.

2.1 Register Terminology

Table below lists the register-related terminology and access attributes that are used in this document. Register Attribute Modifiers table provides the attribute modifiers.

Table 2-1. Register Attributes and Terminology

Item	Description
RO	**Read Only:** These bits can only be read by software, writes have no effect. The value of the bits is determined by the hardware only.
RW	**Read / Write:** These bits can be read and written by software.
RW1C	**Read / Write 1 to Clear:** These bits can be read and cleared by software. Writing a '1' to a bit will clear it, while writing a '0' to a bit has no effect. Hardware sets these bits.
RW0C	**Read / Write 0 to Clear:** These bits can be read and cleared by software. Writing a '0' to a bit will clear it, while writing a '1' to a bit has no effect. Hardware sets these bits.
RW1S	**Read / Write 1 to Set:** These bits can be read and set by software. Writing a '1' to a bit will set it, while writing a '0' to a bit has no effect. Hardware clears these bits.
RsvdP	**Reserved and Preserved:** These bits are reserved for future RW implementations and their value should not be modified by software. When writing to these bits, software should preserve the value read. When SW updates a register that has RsvdP fields, it should read the register value first so that the appropriate merge between the RsvdP and updated fields will occur.
RsvdZ	**Reserved and Zero:** These bits are reserved for future RW1C implementations. Software should use 0 for writes.
WO	**Write Only:** These bits can only be written by software, reads return zero.
RC	**Read Clear:** These bits can only be read by software, but a read causes the bits to be cleared. Hardware sets these bits.
RSW1C	**Read Set / Write 1 to Clear:** These bits can be read and cleared by software. Reading a bit will set the bit to '1'. Writing a '1' to a bit will clear it, while writing a '0' to a bit has no effect.
RCW	**Read Clear / Write:** These bits can be read and written by software, but a read causes the bits to be cleared.

Table 2-2. Register Attribute Modifiers

Attribute Modifier	Applicable Attribute	Description
S	RO (w/ -V)	**Sticky:** These bits are only re-initialized to their default value by a “Power Good Reset” (Cold Reset).
	RW	
	RW1C	
	RW1S	

Table 2-2. Register Attribute Modifiers (Continued)

Attribute Modifier	Applicable Attribute	Description
-K	RW	**Key**: These bits control the ability to write other bits (identified with a 'Lock' modifier)
-L	RW	**Lock**: Hardware can make these bits "Read Only" using a separate configuration bit or other logic.
	WO	
-O	RW	**Once**: After reset, these bits can only be written by software once, after which they become "Read Only".
	WO	
-FW	RO	**Firmware Write**: The value of these bits can be updated by processor hardware mechanisms that may be firmware dependent.
-V	RO	**Variant**: The value of these bits can be updated by hardware.

2.2 PCI Devices and Functions

The processor contains multiple PCI devices. The configuration registers for these devices are mapped as devices residing on PCI Bus 0.

- Device 0: Host Bridge / DRAM Controller / LLC Controller 0 – Logically this device appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other processor specific registers.
- Device 1: Host-PCI Express* Bridge (PCIe Gen5) – Logically this device appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0, and is compliant with the *PCI-to-PCI Bridge Architecture Specification, Revision 1.2*. Device 1 is a multi-function device consisting of two functions (0 and 1). Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers.
- Device 2: Processor Graphics – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 2 contains the configuration registers for 3D, 2D, and display functions. In addition, Device 2 is located in two separate physical locations – Processor Graphics (GT) and Display Engine.
- Device 4: Dynamic Tuning Technology (DTT) - Logically, this device appears as a PCI device residing on PCI Bus 0. Device 4 contains the configuration registers for the DPPM device.
- Device 6: Host-PCI Express* Bridge (Gen4) – Logically this device appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0, and is compliant with the *PCI-to-PCI Bridge Architecture Specification, Revision 1.2*. Device 6 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration.
- Device 8: Gauss Newton Algorithm Device (GNA) – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 8 contains the configuration registers for the Gauss Newton Algorithm Device.
- Device 9: Intel® Trace Hub. Logically, this device appears as a PCI device residing on PCI Bus 0. Device 9 contains the configuration registers for the Trace Hub device. Trace Hub documentation can be found at https://software.intel.com/sites/default/files/managed/f3/47/intel-trace-hub-developers-manual-v2.pdf
- Device 10: Crash Log & Telemetry Device – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 10 contains the configuration registers for the Crash Log Device.

- Device 14: Intel® Volume Management Device. Logically, this device appears as a PCI device residing on PCI Bus 0. Device 14 contains the configuration registers for the Volume Management Device.

Table 2-3. Processor PCI Devices and Functions

Description	Device	Function
HOST and DRAM Controller	0	0
PCI Express* Controller Gen5 (x16 PCIe)	1	0
PCI Express* Controller Gen5 (x8 PCIe)	1	1
PCI Express* Controller Gen4 (x4 PCIe)	6	0
Processor Graphics	2	0
Dynamic Tuning Technology	4	0
Gauss Newton Algorithm Device	8	0
Trace Hub	9	0
Crash Log & Telemetry	10	0
Volume Management Device	14	0

From a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the processor and the PCH appear to be on PCI Bus 0.

2.3 System Address Map

The processor supports 512 GB (39 bits) of addressable memory space and 64 KB+3 of addressable I/O space.

This section focuses on how the memory space is partitioned and how the separate memory regions are used. I/O address space has simpler mapping and is explained towards the end of this chapter.

DRAM capacity is limited by the number of address pins available. There is no hardware lock to prevent more memory from being inserted than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to PCI Express*, DMI, or to the Processor Graphics device (Processor Graphics). The processor does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS. The remapbase/remaplimit registers remap logical accesses bound for addresses above 4GB onto physical addresses that fall within DRAM.

The Address Map includes a number of programmable ranges that are not configured using standard PCI BAR configuration:

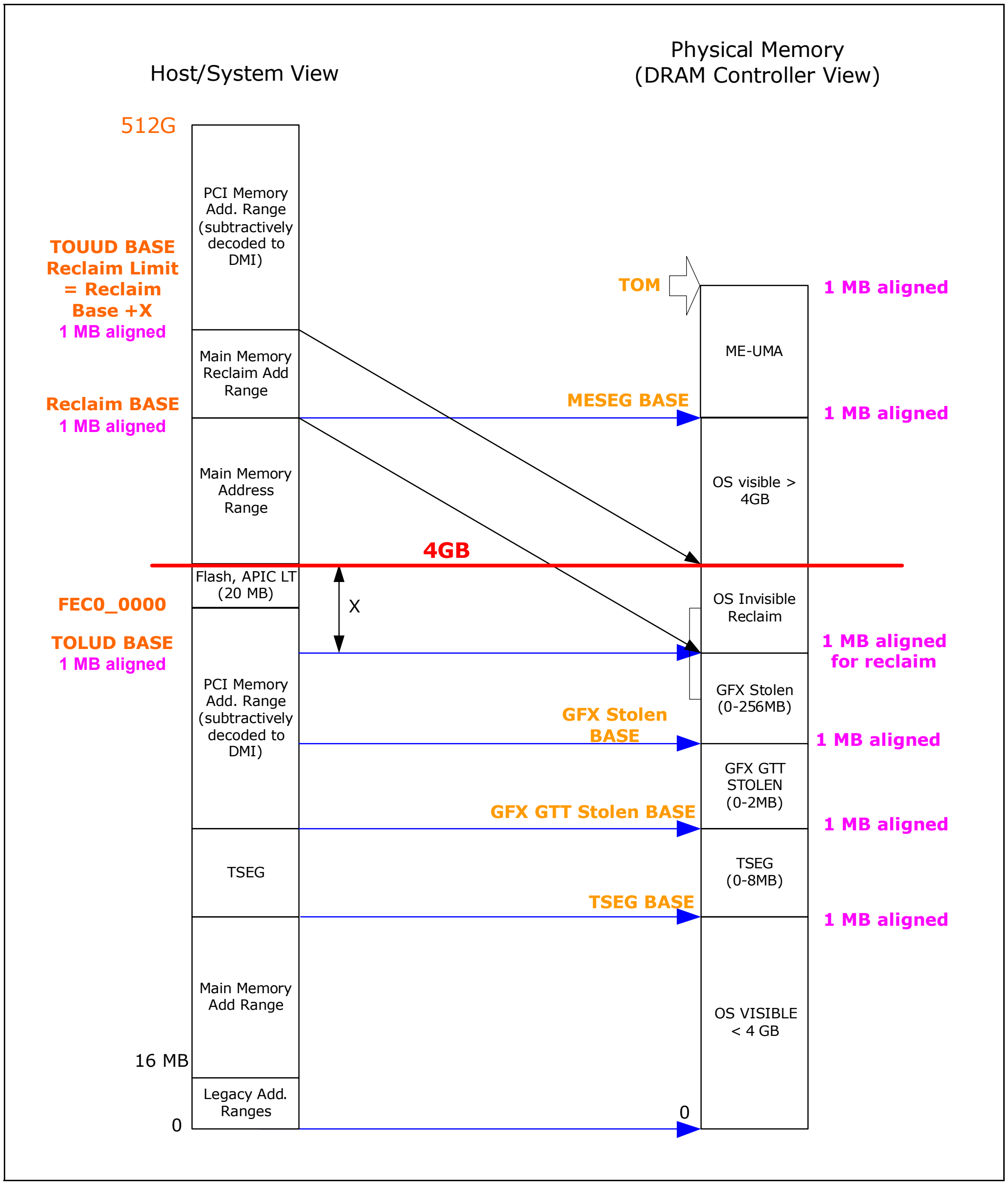
- Device 0:
  - PXPEPBAR – Memory mapped range for PCIe egress port registers. (4 KB window).
  - MCHBAR – Host Memory Mapped Configuration (memory subsystem and power management registers). (128 KB window)
  - DMIBAR – This window is used to access registers associated with the processor/PCH Serial Interconnect (DMI) register memory range. (4 KB window).

  - VTDPVC0BAR - Memory mapped range for VT-d configuration
  - GFXVTBAR - Memory mapped range for VT configuration of the processor graphics device (4KB window).
  - REGBAR - Memory mapped range for System Agent registers (16MB window).
  - GGC.GMS – Graphics Mode Select. Main memory that is pre-allocated to support the Processor Graphics device in VGA (non-linear) and Native (linear) modes. (0 – 512 MB options).
  - GGC.GGMS – GTT Graphics Memory Size. Main memory that is pre-allocated to support the Processor Graphics Translation Table. (0 – 2 MB options).
- For all other PCI devices within the processor that expose PCI configuration space, the behavior is according to PCI specification.

The rules for the above programmable ranges are:

1. For security reasons, the processor positively decodes (FFE0_0000h to FFFF_FFFFh) to DMI. This ensures the boot vector and BIOS execute off the PCH.
2. ALL of these ranges should be unique and NON-OVERLAPPING. It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
3. In the case of overlapping ranges with memory, the memory decode will be given priority. This is an Intel® Trusted Execution Technology (Intel® TXT) requirement. It is necessary to get Intel TXT protection checks, avoiding potential attacks.
4. There are NO Hardware Interlocks to prevent problems in the case of overlapping memory ranges.
5. Accesses to overlapped ranges may produce indeterminate results.
6. Peer-to-peer write cycles are allowed below the Top of Low Usable memory (register TOLUD) for DMI Interface to PCI Express VGA range writes. Peer-to-peer cycles to the Processor Graphics VGA range are not supported.

Figure 2-1. System Address Range Example


Host/System View
Physical Memory
(DRAM Controller View)
512G
PCI Memory Add. Range (subtractively decoded to DMI)
TOUUD BASE
Reclaim Limit = Reclaim Base +X
1 MB aligned
TOM
1 MB aligned
ME-UMA
Main Memory Reclaim Add Range
Reclaim BASE
1 MB aligned
MESEG BASE
1 MB aligned
Main Memory Address Range
OS visible > 4GB
4GB
Flash, APIC LT (20 MB)
X
OS Invisible Reclaim
FEC0_0000
TOLUD BASE
1 MB aligned
1 MB aligned for reclaim
GFX Stolen (0-256MB)
PCI Memory Add. Range (subtractively decoded to DMI)
GFX Stolen BASE
1 MB aligned
GFX GTT STOLEN (0-2MB)
GFX GTT Stolen BASE
1 MB aligned
TSEG
TSEG (0-8MB)
TSEG BASE
1 MB aligned
Main Memory Add Range
OS VISIBLE < 4 GB
16 MB
Legacy Add. Ranges
0
0

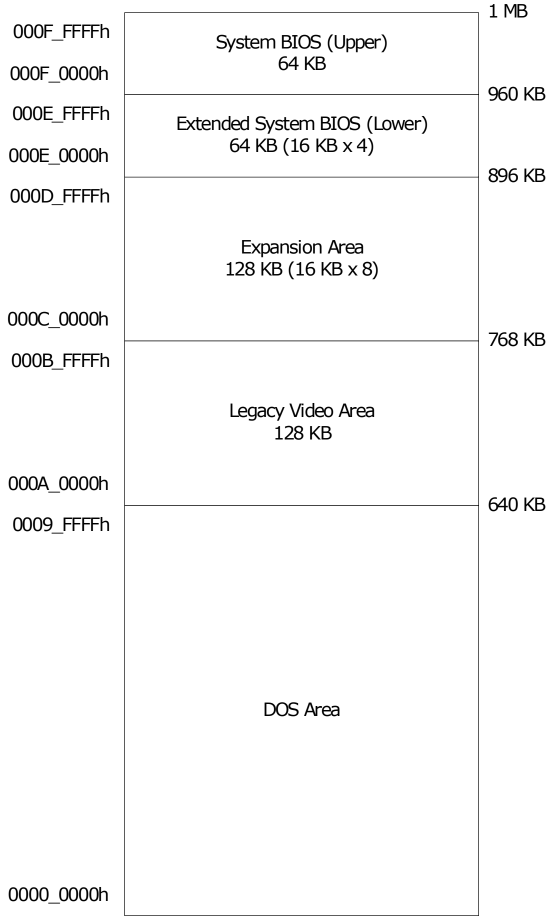
2.4 DOS Legacy Address Range

The memory address range from 0 to 1 MB is known as Legacy Address. This area is divided into the following address regions:

- 0 – 640 KB - DOS Area
- 640 – 768 KB - Legacy Video Buffer Area
- 768 – 896 KB in 16 KB sections (total of 8 sections) – Expansion Area
- 896 – 960 KB in 16 KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB – 1 MB Memory, System BIOS Area

The area between 768 KB – 1 MB is also collectively referred to as PAM (Programmable Address Memory). All accesses to the DOS and PAM ranges from any device are sent to DRAM. However, access to the legacy video buffer area is treated differently.

Figure 2-2. DOS Legacy Address Range



000F_FFFFh
000F_0000h
000E_FFFFh
000E_0000h
000D_FFFFh
000C_0000h
000B_FFFFh
000A_0000h
0009_FFFFh
0000_0000h
System BIOS (Upper)
64 KB
Extended System BIOS (Lower)
64 KB (16 KB x 4)
Expansion Area
128 KB (16 KB x 8)
Legacy Video Area
128 KB
DOS Area
1 MB
960 KB
896 KB
768 KB
640 KB

2.4.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory.

2.4.2 Legacy Video Area (A_0000h – B_FFFFh)

The same address region is used for both Legacy Video Area.

- Legacy Video Area: The legacy 128 KB VGA memory range, frame buffer, at 000A_0000h – 000B_FFFFh, can be mapped to Processor Graphics (Device 2), to PCI Express (Device 1, 6), and/or to the DMI Interface.
- Monochrome Adapter (MDA) Range: Legacy support for monochrome display adapter

Note: The legacy video area is not available for SMM use.

2.4.2.1 Legacy Video Area

The legacy 128 KB VGA memory range, frame buffer at 000A_0000h – 000B_FFFFh, can be mapped to Processor Graphics (Device 2), to PCI Express (Device 1, 6), and/or to the DMI Interface.

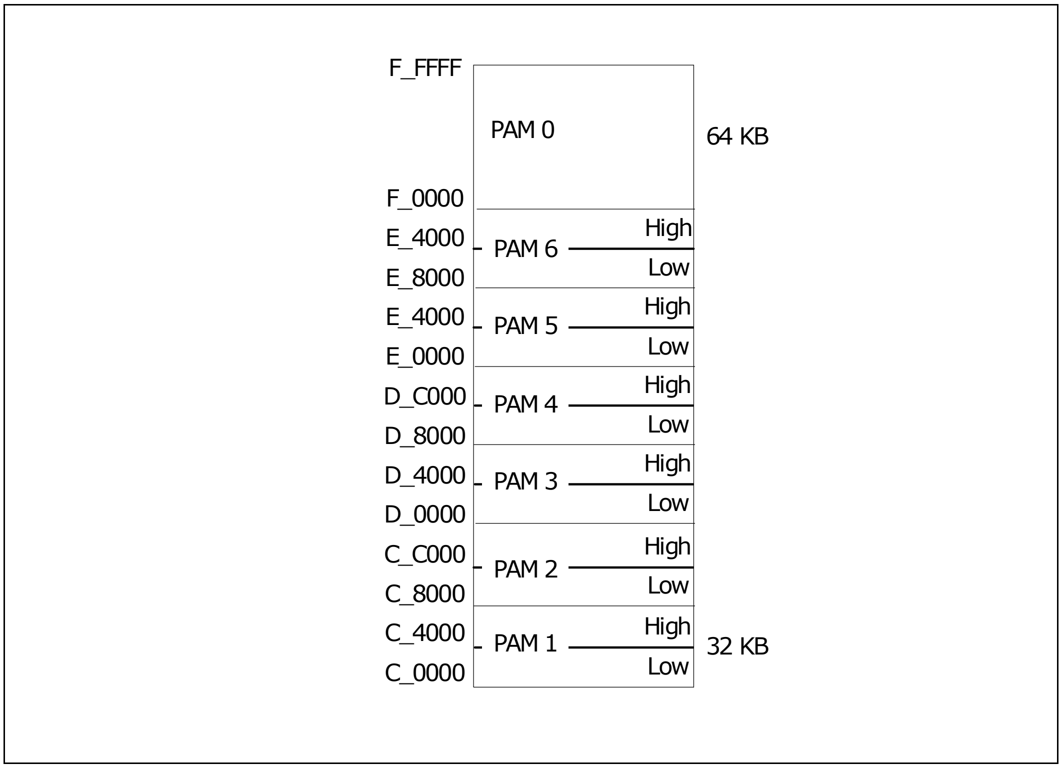
2.4.2.2 Monochrome Adapter (MDA) Range

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. The monochrome adapter may be mapped to Processor Graphics (Device 2), to PCI Express (Device 1, 6), and/or to the DMI Interface.

2.4.3 Programmable Attribute Map (PAM) (C_0000h – F_FFFFh)

PAM is a legacy BIOS ROM area in MMIO. It is overlaid with DRAM and used as a faster ROM storage area. It has a fixed base address (000C_0000h) and fixed size of 256 KB. The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area. Each section has Read enable and Write enable attributes.

Figure 2-3. PAM Region Space


F_FFFF
PAM 0
64 KB
F_0000
E_4000
PAM 6
High
Low
E_8000
E_4000
PAM 5
High
Low
E_0000
D_C000
PAM 4
High
Low
D_8000
D_4000
PAM 3
High
Low
D_0000
C_C000
PAM 2
High
Low
C_8000
C_4000
PAM 1
High
Low
32 KB
C_0000

The PAM registers are mapped in Device 0 configuration space.

- ISA Expansion Area (C_0000h – D_FFFFh)
- Extended System BIOS Area (E_0000h – E_FFFFh)
- System BIOS Area (F_0000h – F_FFFFh)

The processor decodes the Core request, then routes to the appropriate destination (DRAM or DMI).

Snooped accesses from devices to this region are snooped on processor Caches.

Graphics translated requests to this region are not allowed. If such a mapping error occurs, the request will be routed to C_0000h. Writes will have the byte enables de-asserted.

2.5 Lower Main Memory Address Range (1 MB – TOLUD)

This address range extends from 1 MB to the top of Low Usable physical memory that is permitted to be accessible by the processor (as programmed in the TOLUD register). The processor will route all addresses within this range to the DRAM unless it falls into the optional TSEG, optional ISA Hole or optional Processor Graphics stolen memory.

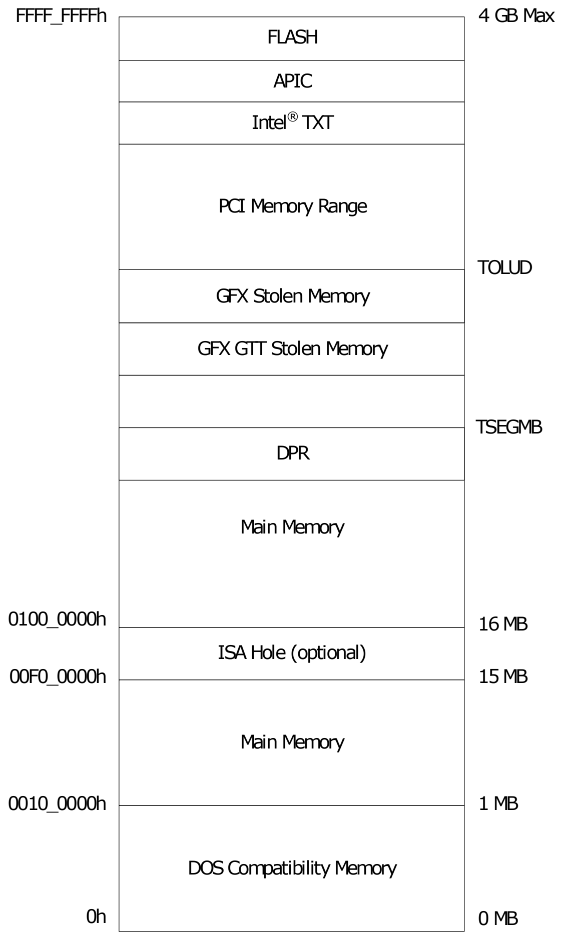
This address range is divided into two sub-ranges:

- 1 MB to TSEGMB

- TSEGMB to TOULUD

TSEGMB indicates the TSEG Memory Base address.

Figure 2-4. Main Memory Address Range


FFFF_FFFFh
4 GB Max
FLASH
APIC
Intel® TXT
PCI Memory Range
TOLUD
GFX Stolen Memory
GFX GTT Stolen Memory
TSEGMB
DPR
Main Memory
0100_0000h
16 MB
ISA Hole (optional)
00F0_0000h
15 MB
Main Memory
0010_0000h
1 MB
DOS Compatibility Memory
0h
0 MB

2.5.1 ISA Hole (15 MB –16 MB)

The ISA Hole (starting at address F0_0000h) is enabled in the Legacy Access Control Register in Device 0 configuration space. If no hole is created, the processor will route the request to DRAM. If a hole is created, the processor will route the request to DMI.

Graphics translated requests to the range will always route to DRAM.

2.5.2 1 MB to TSEGMB

Processor access to this range will be directed to memory with the exception of the ISA Hole (when enabled).

2.5.3 TSEG

For processor initiated transactions, the processor relies on correct programming of SMM Range Registers (SMRR) to enforce TSEG protection.

TSEG is below Processor Graphics stolen memory, which is at the Top of Low Usable physical memory (TOLUD). BIOS will calculate and program the TSEG BASE in Device 0 (TSEGMB), used to protect this region from DMA access. Calculation is:

TSEGMB = TOLUD – DSM SIZE – GSM SIZE – TSEG SIZE

SMM-mode processor accesses to TSEG always access the physical DRAM.

When the extended SMRAM space is enabled, processor accesses without SMM attribute or without write-back attribute to the TSEG range are handled as invalid accesses.

Non-processor originated accesses such as PCI Express, DMI or processor graphics to enabled SMM space are handled as invalid cycle type with reads and writes to location C_0000h and byte enables turned off for writes.

2.5.4 Protected Memory Range (PMR) - (Programmable)

For robust and secure launch of the MVMM, the MVMM code and private data need to be loaded to a memory region protected from bus master accesses. Support for protected memory region is required for DMA-remapping hardware implementations on platforms supporting Intel TXT, and is optional for non-Intel TXT platforms. Since the protected memory region needs to be enabled before the MVMM is launched, hardware should support enabling of the protected memory region independently from enabling the DMA-remapping hardware.

As part of the secure launch process, the SINIT-AC module verifies the protected memory regions are properly configured and enabled. Once launched, the MVMM can setup the initial DMA-remapping structures in protected memory (to ensure they are protected while being setup) before enabling the DMA-remapping hardware units.

To optimally support platform configurations supporting varying amounts of main memory, the protected memory region is defined as two non-overlapping regions:

- **Protected Low-memory Region**: This is defined as the protected memory region below 4 GB to hold the MVMM code/private data, and the initial DMA-remapping structures that control DMA to host physical addresses below 4 GB. DMA-remapping hardware implementations on platforms supporting Intel TXT are required to support protected low-memory region 5.
- **Protected High-memory Region**: This is defined as a variable sized protected memory region above 4 GB, enough to hold the initial DMA-remapping structures for managing DMA accesses to addresses above 4 GB. DMA-remapping hardware implementations on platforms supporting Intel TXT are required to support protected high-memory region 6, if the platform supports main memory above 4 GB.

Once the protected low/high memory region registers are configured, bus master protection to these regions is enabled through the Protected Memory Enable register. For platforms with multiple DMA-remapping hardware units, each of the DMA-remapping hardware units should be configured with the same protected memory regions and enabled.

2.5.5 DRAM Protected Range (DPR)

This protection range only applies to DMA accesses and GMADR translations. It serves a purpose of providing a memory range that is only accessible to processor streams. The range just below TSEGMB is protected from DMA accesses.

The DPR range works independently of any other range, including the PMRC checks in Intel VT-d. It occurs post any Intel VT-d translation. Therefore, incoming cycles are checked against this range after the Intel VT-d translation and faulted if they hit this protected range, even if they passed the Intel VT-d translation.

The system will set up:

- 0 to (TSEG_BASE – DPR size – 1) for DMA traffic
- TSEG_BASE to (TSEG_BASE – DPR size) as no DMA.

After some time, software could request more space for not allowing DMA. It will get some more pages and make sure there are no DMA cycles to the new region. DPR size is changed to the new value. When it does this, there should not be any DMA cycles going to DRAM to the new region.

All upstream cycles from 0 to (TSEG_BASE – 1 – DPR size), and not in the legacy holes (VGA), are decoded to DRAM.

2.5.6 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within the system memory address range (< TOLUD) are created for SMM-mode, legacy VGA graphics compatibility, and GFX GTT stolen memory. **It is the responsibility of BIOS to properly initialize these regions**.

2.6 PCI Memory Address Range (TOLUD – 4 GB)

Top of Low Usable DRAM (TOLUD) – TOLUD is restricted to 4 GB memory (1MB granularity), but the System Agent may support up to a much higher capacity, which is limited by DRAM.

This address range from the top of low usable DRAM (TOLUD) to 4 GB is normally mapped to the DMI Interface.

Device 0 exceptions are:

1. Addresses decoded to the egress port registers (PXPEPBAR)
2. Addresses decoded to the memory mapped range for Host Memory Mapped Configuration Space registers (MCHBAR)
3. Addresses decoded to the registers associated with the PCH Serial Interconnect (DMI) register memory range. (DMIBAR)

For each PCI Express* port, there are two exceptions to this rule:

4. Addresses decoded to the PCI Express Memory Window defined by the MBASE, MLIMIT registers are mapped to PCI Express.
5. Addresses decoded to the PCI Express prefetchable Memory Window defined by the PMBASE, PMLIMIT registers are mapped to PCI Express.

In Processor Graphics configurations, there are exceptions to this rule:

6. Addresses decode to the Processor Graphics translation window (GMADR)
7. Addresses decode to the Processor Graphics translation table or Processor Graphics registers. (GTTMMADR)

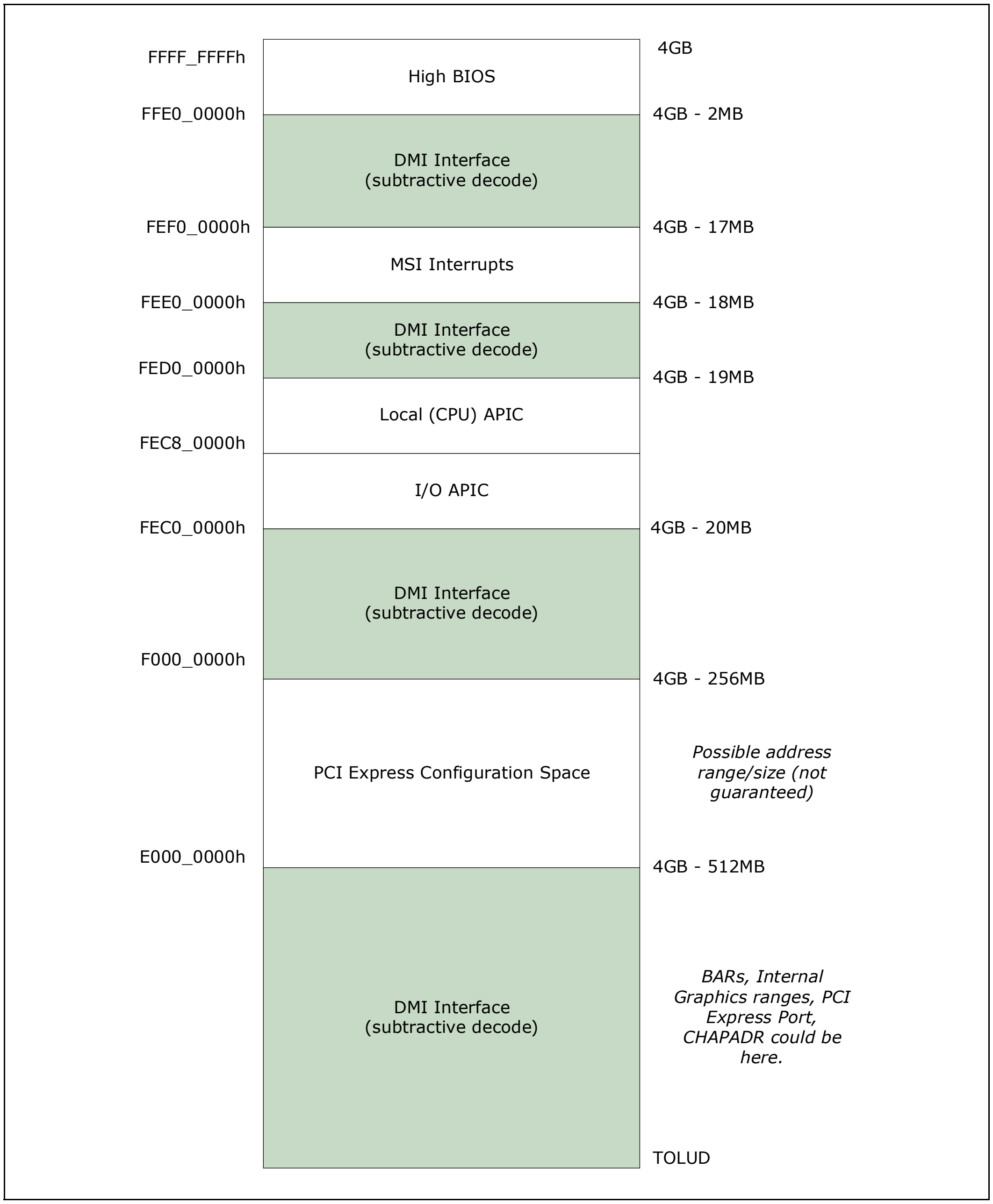
In an Intel VT enable configuration, there are exceptions to this rule:

8. Addresses decoded to the memory mapped window to Graphics Intel VT remap engine registers (GFXVTBAR)
9. Addresses decoded to the memory mapped window to PEG/DMI VC0 Intel VT remap engine registers (VTDPVC0BAR)
10. TCm accesses (to Intel ME stolen memory) from PCH do not go through Intel VT remap engines.

Some of the MMIO Bars may be mapped to this range or to the range above TOUUD.

There are sub-ranges within the PCI memory address range defined as APIC Configuration Space, MSI Interrupt Space, and High BIOS address range. The exceptions listed above for Processor Graphics and the PCI Express ports ***should NOT overlap with these ranges***.

Figure 2-5. PCI Memory Address Range


FFFF_FFFFh
4GB
High BIOS
FFE0_0000h
4GB - 2MB
DMI Interface
(subtractive decode)
FEF0_0000h
4GB - 17MB
MSI Interrupts
FEE0_0000h
4GB - 18MB
DMI Interface
(subtractive decode)
FED0_0000h
4GB - 19MB
Local (CPU) APIC
FEC8_0000h
I/O APIC
FEC0_0000h
4GB - 20MB
DMI Interface
(subtractive decode)
F000_0000h
4GB - 256MB
PCI Express Configuration Space
Possible address range/size (not guaranteed)
E000_0000h
4GB - 512MB
DMI Interface
(subtractive decode)
BARs, Internal Graphics ranges, PCI Express Port, CHAPADR could be here.
TOLUD

2.6.1 APIC Configuration Space (FEC0_0000h – FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the PCH portion of the chipset, but may also exist as stand-alone components like PXH.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

The processor optionally supports additional I/O APICs behind the PCI Express* “Graphics” port. When enabled using the APIC_BASE and APIC_LIMIT registers (mapped PCI Express* Configuration space offset 240h and 244h), the PCI Express* port(s) will positively decode a subset of the APIC configuration space.

Memory requests to this range would then be forwarded to the PCI Express* port. This mode is intended for the entry Workstation/Server SKU of the PCH, and would be disabled in typical Desktop systems. When disabled, any access within the entire APIC Configuration space (FEC0_0000h to FECF_FFFFh) is forwarded to DMI.

2.6.2 HSEG (FEDA_0000h – FEDB_FFFFh)

This decode range is not supported on this processor platform.

2.6.3 MSI Interrupt Memory Space (FEE0_0000h – FEEF_FFFFh)

Any PCI Express* or DMI device may issue a Memory Write to 0FEEx_xxxxh. This Memory Write cycle does not go to DRAM. The system agent will forward this Memory Write along with the data to the processor as an Interrupt Message Transaction.

2.6.4 High BIOS Area

For security reasons, the processor will positively decode this range to DMI. This positive decode ensures any overlapping ranges will be ignored. This ensures that the boot vector and BIOS execute off the PCH.

The top 2 MB (FFE0_0000h – FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS.

The processor begins execution from the High BIOS after reset. This region is positively decoded to DMI. The actual address space required for the BIOS is less than 2 MB. However, the minimum processor MTRR range for this region is 2 MB; thus, the full 2 MB should be considered.

2.7 Upper Main Memory Address Space (4 GB to TOUUD)

The maximum main memory size supported is 64 GB total DRAM memory.

A hole between TOLUD and 4 GB occurs when main memory size approaches 4 GB or larger. As a result, TOM and TOUUD registers and REMAPBASE/REMAPLIMIT registers become relevant.

The remap configuration registers exist to remap lost main memory space. The greater than 32-bit remap handling will be handled similar to other MCHs.

Upstream read and write accesses above 39-bit addressing will be treated as invalid cycles by PEG and DMI.

2.7.1 Top of Memory (TOM)

The “Top of Memory” (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO above TOM).

The TOM was used to allocate the Intel Management Engine (Intel ME) stolen memory. The Intel ME stolen size register reflects the total amount of physical memory stolen by the Intel ME. The Intel ME stolen memory is located at the top of physical memory. The Intel ME stolen memory base is calculated by subtracting the amount of memory stolen by the Intel ME from TOM.

2.7.2 Top of Upper Usable DRAM (TOUUD)

The Top of Upper Usable DRAM (TOUUD) register reflects the total amount of addressable DRAM. If remap is disabled, TOUUD will reflect TOM minus Intel ME stolen size. If remap is enabled, then it will reflect the remap limit. When there is more than 4 GB of DRAM and reclaim is enabled, the reclaim base will be the same as TOM minus Intel ME stolen memory size to the nearest 1 MB alignment.

2.7.3 Top of Low Usable DRAM (TOLUD)

TOLUD register is restricted to 4 GB memory (A[31:20]), but the processor can support up to 64 GB, limited by DRAM pins. For physical memory greater than 4 GB, the TOUUD register helps identify the address range between the 4 GB boundary and the top of physical memory. This identifies memory that can be directly accessed (including remap address calculation) that is useful for memory access indication and early path indication. TOLUD can be 1 MB aligned.

2.7.4 TSEG_BASE

The “TSEG_BASE” register reflects the total amount of low addressable DRAM, below TOLUD. BIOS will calculate memory size and program this register; thus, the system agent has knowledge of where (TOLUD) – (Gfx stolen) – (Gfx GTT stolen) – (TSEG) is located. I/O blocks use this minus DPR for upstream DRAM decode.

2.7.5 Memory Re-claim Background

The following are examples of Memory Mapped IO devices that are typically located below 4 GB:

- High BIOS
- TSEG
- GFX stolen
- GTT stolen
- XAPIC
- Local APIC
- MSI Interrupts
- Mbase/Mlimit
- Pmbase/PMlimit
- Memory Mapped IO space that supports only 32B addressing

The processor provides the capability to re-claim the physical memory overlapped by the Memory Mapped IO logical address space. The MCH re-maps physical memory from the Top of Low Memory (TOLUD) boundary up to the 4 GB boundary to an equivalent sized logical address range located just below the Intel ME stolen memory.

2.7.6 Indirect Accesses to MCHBAR Registers

Similar to prior chipsets, MCHBAR registers can be indirectly accessed using:

- Direct MCHBAR access decode:
  - Cycle to memory from processor
  - Hits MCHBAR base, AND
  - MCHBAR is enabled, AND
  - Within MMIO space (above and below 4 GB)
- GTTMMADR (10000h – 13FFFh) range -> MCHBAR decode:
  - Cycle to memory from processor, AND
  - Device 2 (Processor Graphics) is enabled, AND
  - Memory accesses for device 2 is enabled, AND
  - Targets GFX MMIO Function 0, AND
  - MCHBAR is enabled or cycle is a read. If MCHBAR is disabled, only read access is allowed.
- MCHTMBAR -> MCHBAR (Thermal Monitor)
  - Cycle to memory from processor, AND
  - Targets MCHTMBAR base
- IOBAR -> GTTMMADR -> MCHBAR.
  - Follows IOBAR rules. See GTTMMADR information above as well.

2.7.7 Memory Remapping

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the REMAPBASE register. The top of the re-map window is defined by the value in the REMAPLIMIT register. An address that falls within this window is re-mapped to the physical memory starting at the address defined by the TOLUD register. The TOLUD register should be 1 MB aligned.

2.7.8 Hardware Remap Algorithm

The following pseudo-code defines the algorithm used to calculate the DRAM address to be used for a logical address above the top of physical memory made available using re-claiming.

```
IF (ADDRESS_IN[38:20] >= REMAP_BASE[35:20]) AND
(ADDRESS_IN[38:20] <= REMAP_LIMIT[35:20]) THEN
    ADDRESS_OUT[38:20] = (ADDRESS_IN[38:20] - REMAP_BASE[35:20]) +
0000000b & TOLUD[31:20]
    ADDRESS_OUT[19:0] = ADDRESS_IN[19:0]
```

2.8 PCI Express* Configuration Address Space

PCIEXBAR is located in Device 0 configuration space. The processor detects memory accesses targeting PCIEXBAR. BIOS should assign this address range such that it will not conflict with any other address ranges.

2.9 Graphics Memory Address Ranges

The integrated memory controller can be programmed to direct memory accesses to the Processor Graphics when addresses are within any of the ranges specified using registers in MCH Device 2 configuration space.

- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated using the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table and graphics control registers. This is part of the GTTMMADR register.

These ranges can reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges. They should reside above the top of memory (TOLUD) and below 4 GB so they do not take any physical DRAM memory space.

Alternatively, these ranges can reside above 4 GB, similar to other BARs that are larger than 32 bits in size.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

2.9.1 IOBAR Mapped Access to Device 2 MMIO Space

Device 2, Processor Graphics, contains an IOBAR register. If Device 2 is enabled, Processor Graphics registers or the GTT table can be accessed using this IOBAR. The IOBAR is composed of an index register and a data register.

MMIO_Index: MMIO_INDEX is a 32-bit register. A 32-bit (all bytes enabled) I/O write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An I/O Read returns the current value of this register. I/O read/write accesses less than 32 bits in size (all bytes enabled) will not target this register.

MMIO_Data: MMIO_DATA is a 32-bit register. A 32-bit (all bytes enabled) I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register. I/O read/write accesses less than 32 bits in size (all bytes enabled) will not target this register.

The result of accesses through IOBAR can be:

- Accesses directed to the GTT table. (that is, route to DRAM)
- Accesses to Processor Graphics registers with the device.
- Accesses to Processor Graphics display registers now located within the PCH. (that is, route to DMI).

Note: GTT table space writes (GTTADR) are supported through this mapping mechanism.

This mechanism to access Processor Graphics MMIO registers should NOT be used to access VGA I/O registers that are mapped through the MMIO space. VGA registers should be accessed directly through the dedicated VGA I/O ports.

2.9.2 Trusted Graphics Ranges

Trusted graphics ranges are NOT supported.

2.10 System Management Mode (SMM)

The Core handles all SMM mode transaction routing. The processor does not allow I/O devices access to the CSEG/TSEG/HSEG ranges.

DMI Interface and PCI Express* masters are Not allowed to access the SMM space.

Table 2-4. SMM Regions

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
TSEG (T)	(TOLUD – STOLEN – TSEG) to TOLUD – STOLEN	(TOLUD – STOLEN – TSEG) to TOLUD – STOLEN

2.11 SMM and VGA Access Through GTT TLB

Accesses through GTT TLB address translation SMM DRAM space are not allowed. Writes will be routed to memory address 000C_0000h with byte enables de-asserted and reads will be routed to Memory address 000C_0000h. If a GTT TLB translated address hits VGA space, an error is recorded.

PCI Express* and DMI Interface originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface write accesses through the GMADR range will not be snooped. Only PCI Express and DMI assesses to GMADR linear range (defined using fence registers) are supported. PCI Express and DMI Interface tileY and tileX writes to GMADR are not supported. If, when translated, the resulting physical address is to enable SMM DRAM space, the request will be remapped to address 000C_0000h with de-asserted byte enables.

PCI Express and DMI Interface read accesses to the GMADR range are not supported. Therefore, there are no address translation concerns. PCI Express and DMI Interface reads to GMADR will be remapped to address 000C_0000h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure fetch is not in SMM (actually, anything above base of TSEG or 640 KB - 1 MB). Thus, the fetches will be invalid and go to address 000C_0000h. This is not specific to PCI Express or DMI; it also applies to processor or Processor Graphics engines.

2.12 Intel® Management Engine (Intel® ME) Stolen Memory Accesses

There are two ways to validly access Intel ME stolen memory:

- PCH accesses mapped to VCm will be decoded to ensure only Intel ME stolen memory is targeted. These VCm accesses will route non-snooped directly to DRAM. This is the means by which the Intel ME (located within the PCH) is able to access the Intel ME stolen range.
- The display engine is allowed to access Intel ME stolen memory as part of Intel® KVM technology flows. Specifically, display-initiated HHP reads (for displaying a Intel KVM technology frame) and display initiated LP non-snoop writes (for display writing an Intel KVM technology captured frame) to Intel ME stolen memory are allowed.

2.13 I/O Address Space

The system agent generates either DMI Interface or PCI Express* bus cycles for all processor I/O accesses that it does not claim. The Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA) are used to generate PCI configuration space access.

The processor allows 64K+3 bytes to be addressed within the I/O space. The upper 3 locations can be accessed only during I/O address wrap-around.

A set of I/O accesses are consumed by the Processor Graphics device if it is enabled. The mechanisms for Processor Graphics I/O decode and the associated control is explained in following sub-sections.

The I/O accesses are forwarded normally to the DMI Interface bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to PCH or PCI Express are posted. The PCI Express devices have a register that can disable the routing of I/O cycles to the PCI Express device.

The processor responds to I/O cycles initiated on PCI Express or DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the transaction will complete with an UR completion status.

I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as one transaction. The reads will be split into two separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries will be split into two transactions by the processor.

2.13.1 PCI Express* I/O Address Mapping

The processor can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled using the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in Device 1 Functions 0, 1, 2 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the device assumes that the lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to a 4 KB boundary and produces a size granularity of 4 KB.

The processor positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

```
I/O_Base_Address ≤ processor I/O Cycle Address ≤ I/O_Limit_Address
```

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The processor also forwards accesses to the Legacy VGA I/O ranges according to the settings in the PEG configuration registers BCTRL (VGA Enable) and PCICMD (IOAE), unless a second adapter (monochrome) is present on the DMI Interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set to 1, the processor will decode legacy monochrome I/O ranges and forward them to the DMI Interface. The I/O ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh.

The PEG I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI-Express.

The PCICMD register can disable the routing of I/O cycles to PCI Express.

2.14 Direct Media Interface (DMI) Interface Decode Rules

Note: DMI does not apply to P Processors.

All “SNOOP semantic” PCI Express* transactions are kept coherent with processor caches.

All “Snoop not required semantic” cycles reference the main DRAM address range. PCI Express non-snoop initiated cycles are not snooped.

The processor accepts accesses from the DMI Interface to the following address ranges:

- All snoop memory read and write accesses to Main DRAM including PAM region (except stolen memory ranges, TSEG, A0000h – BFFFFh space)
- Write accesses to enabled VGA range, MBASE/MLIMIT, and PMBASE/PMLIMIT will be routed as peer cycles to the PCI Express interface.
- Write accesses above the top of usable DRAM and below 4 GB (not decoding to PCI Express or GMADR space) will be treated as master aborts.
- Read accesses above the top of usable DRAM and below 4 GB (not decoding to PCI Express) will be treated as unsupported requests.
- Reads and accesses above the TOUUD will be treated as unsupported requests on VC0.

DMI Interface memory read accesses that fall between TOLUD and 4 GB are considered invalid and will master abort. These invalid read accesses will be reassigned to address 000C_0000h and dispatch to DRAM. Reads will return unsupported request completion. Writes targeting PCI Express space will be treated as peer-to-peer cycles.

There is a known usage model for peer writes from DMI to PEG. A video capture card can be plugged into the PCH PCI bus. The video capture card can send video capture data (writes) directly into the frame buffer on an external graphics card (writes to the PEG port). As a result, peer writes from DMI to PEG should be supported.

I/O cycles and configuration cycles are not supported in the upstream direction. The result will be an unsupported request completion status.

2.14.1 DMI Accesses to the Processor that Cross Device Boundaries

The processor does not support transactions that cross device boundaries. This should not occur because PCI Express transactions are not allowed to cross a 4 KB boundary.

For reads, the processor will provide separate completion status for each naturally-aligned 64-byte block or, if chaining is enabled, each 128-byte block. If the starting address of a transaction hits a valid address, the portion of a request that hits that target device (PCI Express or DRAM) will complete normally.

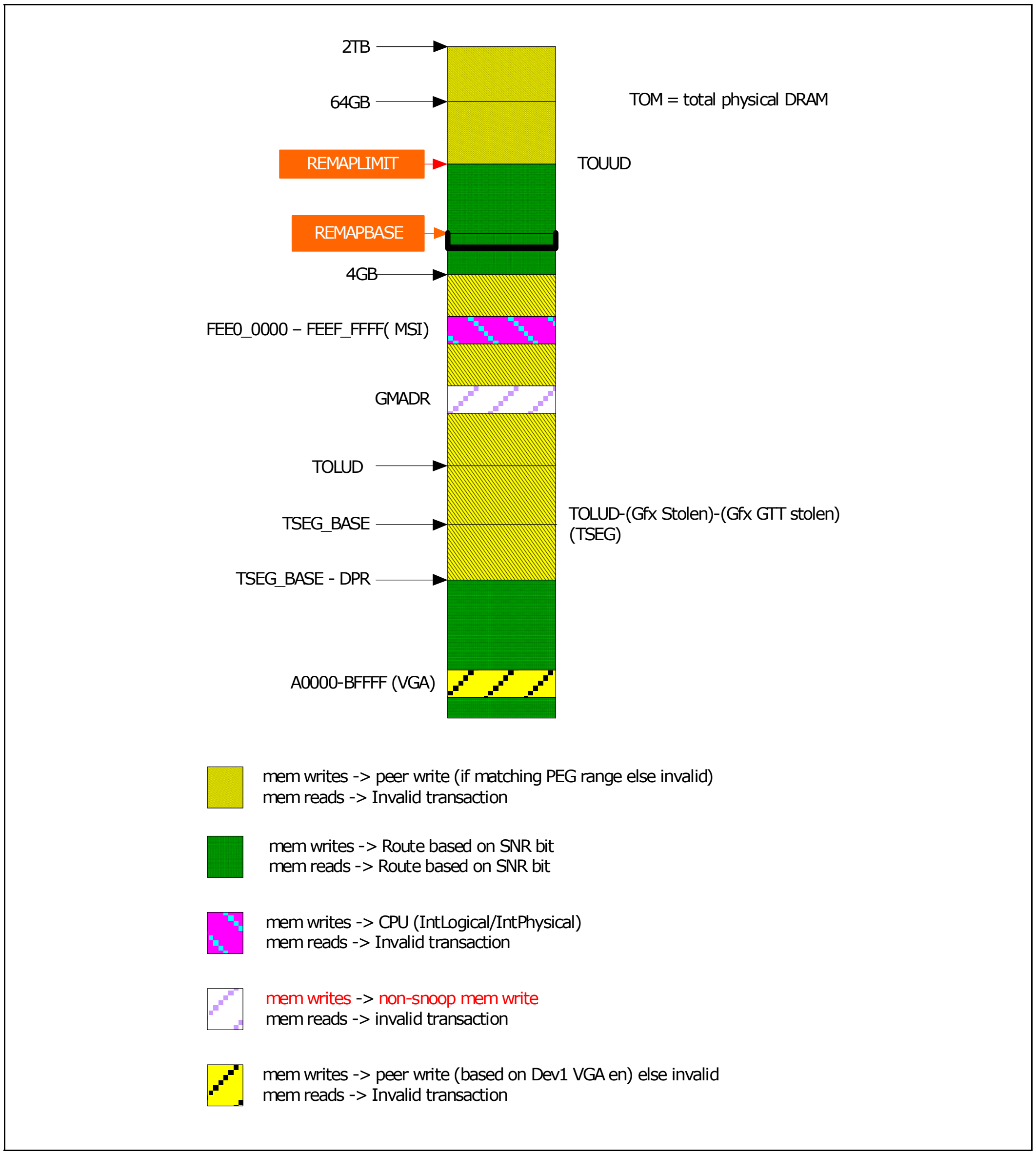
If the starting transaction address hits an invalid address, the entire transaction will be remapped to address 000C_0000h and dispatched to DRAM. A single unsupported request completion will result.

2.14.2 Traffic Class (TC) / Virtual Channel (VC) Mapping Details

- VC0 (enabled by default)
  - Snoop port and Non-snoop Asynchronous transactions are supported.

  - Internal Graphics GMADR writes can occur. These writes will NOT be snooped regardless of the snoop not required (SNR) bit.
  - Processor Graphics GMADR reads (unsupported).
  - Peer writes can occur. The SNR bit is ignored.
  - MSI can occur. These will route and be sent to the cores as Intlogical/ IntPhysical interrupts regardless of the SNR bit.
  - VLW messages can occur. These will route and be sent to the cores as VLW messages regardless of the SNR bit.
  - MCTP messages can occur. These are routed in a peer fashion.
- VC1 (Optionally enabled)
  - Supports non-snoop transactions only. (Used for isochronous traffic). The PCI Express* Egress port (PXPEPBAR) should also be programmed appropriately.
  - The snoop not required (SNR) bit should be set. Any transaction with the SNR bit not set will be treated as an unsupported request.
  - MSI and peer transactions are treated as unsupported requests.
  - No “pacer” arbitration or TWRR arbitration will occur. Never remaps to different port. (PCH takes care of Egress port remapping). The PCH meters TCm Intel ME accesses and Intel® High Definition Audio (Intel® HD Audio) TC1 access bandwidth.
  - Processor Graphics GMADR writes and GMADR reads are not supported.
- VCm accesses
  - VCm access only map to Intel ME stolen DRAM. These transactions carry the direct physical DRAM address (no redirection or remapping of any kind will occur). This is how the PCH Intel ME accesses its dedicated DRAM stolen space.
  - DMI block will decode these transactions to ensure only Intel ME stolen memory is targeted, and abort otherwise.
  - VCm transactions will only route non-snoop.
  - VCm transactions will not go through VTd remap tables.
  - The remapbase/remaplimit registers to not apply to VCm transactions.

Figure 2-6. Example: DMI Upstream VC0 Memory Map


2TB
64GB
TOM = total physical DRAM
REMAPLIMIT
TOUUD
REMAPBASE
4GB
FEE0_0000 – FEEF_FFFF(MSI)
GMADR
TOLUD
TSEG_BASE
TOLUD-(Gfx Stolen)-(Gfx GTT stolen)
(TSEG)
TSEG_BASE - DPR
A0000-BFFFF (VGA)
mem writes -> peer write (if matching PEG range else invalid)
mem reads -> Invalid transaction
mem writes -> Route based on SNR bit
mem reads -> Route based on SNR bit
mem writes -> CPU (IntLogical/IntPhysical)
mem reads -> Invalid transaction
mem writes -> non-snoop mem write
mem reads -> invalid transaction
mem writes -> peer write (based on Dev1 VGA en) else invalid
mem reads -> Invalid transaction

2.15 PCI Express* Interface Decode Rules

All “SNOOP semantic” PCI Express* transactions are kept coherent with processor caches. All “Snoop not required semantic” cycles should reference the direct DRAM address range. PCI Express non-snoop initiated cycles are not snooped. If a “Snoop not required semantic” cycle is outside of the address range mapped to system memory, then it will proceed as follows:

- Reads: Sent to DRAM address 000C_0000h (non-snooped) and will return “unsuccessful completion”.
- Writes: Sent to DRAM address 000C_0000h (non-snooped) with byte enables all disabled Peer writes from PEG to DMI are not supported.

If PEG bus master enable is not set, all reads and writes are treated as unsupported requests.

2.15.1 TC/VC Mapping Details

- VC0 (enabled by default)
    - — Snoop port and Non-snoop Asynchronous transactions are supported.
    - — Processor Graphics GMADR writes can occur. Unlike FSB chipsets, these will NOT be snooped regardless of the snoop not required (SNR) bit.
    - — Processor Graphics GMADR reads (unsupported).
    - — Peer writes are only supported between PEG ports. PEG to DMI peer write accesses are NOT supported.
    - — MSI can occur. These will route to the cores (IntLogical/IntPhysical) regardless of the SNR bit.
- VC1 is not supported.
- VCm is not supported.

2.16 Legacy VGA and I/O Range Decode Rules

The legacy 128 KB VGA memory range 000A_0000h – 000B_FFFFh can be mapped to Processor Graphics (Device 2), PCI Express (Device 1 Functions), and/or to the DMI interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the processor always decodes internally mapped devices first. Internal to the processor, decode precedence is always given to Processor Graphics. The processor always positively decodes internally mapped devices, namely the Processor Graphics. Subsequent decoding of regions mapped to either PCI Express port or the DMI Interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

For the remainder of this section, PCI Express can refer to either the device 1 port functions.

VGA range accesses will always be mapped as UC type memory.

Accesses to the VGA memory range are directed to Processor Graphics depend on the configuration. The configuration is specified by:

- Processor Graphics controller in Device 2 is enabled (DEVEN.D2EN bit 4)

- Processor Graphics VGA in Device 0 Function 0 is enabled through register GGC bit 1.
- Processor Graphics's memory accesses (PCICMD2 04h – 05h, MAE bit 1) in Device 2 configuration space are enabled.
- VGA compatibility memory accesses (VGA Miscellaneous Output register – MSR Register, bit 1) are enabled.
- Software sets the proper value for VGA Memory Map Mode register (VGA GR06 Register, bits 3:2). See the following table for translations.

Table 2-5. Processor Graphics Frame Buffer Accesses

Memory Access GR06(3:2)	A0000h - AFFFFh	B0000h - B7FFFh MDA	B8000h - BFFFFh
00	Processor Graphics	Processor Graphics	Processor Graphics
01	Processor Graphics	PCI Express bridge or DMI interface	PCI Express bridge or DMI interface
10	PCI Express bridge or DMI interface	Processor Graphics	PCI Express bridge or DMI interface
11	PCI Express bridge or DMI interface	PCI Express bridge or DMI interface	Processor Graphics

Note: Additional qualification within Processor Graphics comprehends internal MDA support. The VGA and MDA enabling bits detailed below control segments not mapped to Processor Graphics.

VGA I/O range is defined as addresses where A[15:0] are in the ranges 03B0h to 03BBh, and 03C0h to 03DFh. VGA I/O accesses are directed to Processor Graphics depends on the following configuration:

- Processor Graphics controller in Device 2 is enabled through register DEVEN.D2EN bit 4.
- Processor Graphics VGA in Device 0 Function 0 is enabled through register GGC bit 1.
- Processor Graphics's I/O accesses (PCICMD2 04 – 05h, IOAE bit 0) in Device 2 are enabled.
- VGA I/O decodes for Processor Graphics uses 16 address bits (15:0) there is no aliasing. This is different when compared to a bridge device (Device 1) that used only 10 address bits (A 9:0) for VGA I/O decode.
- VGA I/O input/output address select (VGA Miscellaneous Output register - MSR Register, bit 0) is used to select mapping of I/O access as defined in the following table.

Table 2-6. Processor Graphics VGA I/O Mapping

I/O Access MSRb0	3CX	3DX	3B0h – 3BBh	3BCh – 3BFh
0	Processor Graphics	PCI Express bridge or DMI interface	Processor Graphics	PCI Express bridge or DMI interface
1	Processor Graphics	Processor Graphics	PCI Express bridge or DMI interface	PCI Express bridge or DMI interface

Note: Additional qualification within Processor Graphics comprehends internal MDA support. The VGA and MDA enabling bits detailed below control ranges not mapped to Processor Graphics.

For regions mapped outside of the Processor Graphics (or if Processor Graphics is disabled), the legacy VGA memory range A0000h – BFFFFh are mapped to the DMI Interface or PCI Express depending on the programming of the VGA Enable bit in the BCTRL configuration register in the PEG configuration space, and the MDAPxx bits in the Legacy Access Control (LAC) register in Device 0 configuration space. The same register controls mapping VGA I/O address ranges. The VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – A[15:10] are not decoded). The function and interaction of these two bits is described below:

VGA Enable: Controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. When this bit is set, the following processor accesses will be forwarded to the PCI Express:

- Memory accesses in the range 0A0000h to 0BFFFFh
- I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (including ISA address aliases – A[15:10] are not decoded)

When this bit is set to a “1”:

- Forwarding of these accesses issued by the processor is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers.
- Forwarding of these accesses is also independent of the settings of the ISA Enable settings if this bit is “1”.
- Accesses to I/O address range x3BCh – x3BFh are forwarded to the DMI Interface.

When this bit is set to a “0”:

- Accesses to I/O address range x3BCh – x3BFh are treated like any other I/O accesses; the cycles are forwarded to PCI Express if the address is within IOBASE and IOLIMIT and ISA enable bit is not set. Otherwise, these accesses are forwarded to the DMI interface.
- VGA compatible memory and I/O range accesses are not forwarded to PCI Express but rather they are mapped to the DMI Interface, unless they are mapped to PCI Express using I/O and memory range registers defined above (IOBASE, IOLIMIT)

The following table shows the behavior for all combinations of MDA and VGA.

Table 2-7. VGA and MDA IO Transaction Mapping

VGA_en	MDAP	Range	Destination	Exceptions / Notes
0	0	VGA, MDA	DMI interface	
0	1	Illegal		Undefined behavior results
1	0	VGA	PCI Express	
1	1	VGA	PCI Express	
1	1	MDA	DMI interface	x3BCh – x3BEh will also go to DMI interface

The same registers control mapping of VGA I/O address ranges. The VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – A[15:10] are not decoded). The function and interaction of these two bits is described below.

MDA Present (MDAP): This bit works with the VGA Enable bit in the BCTRL register of Device 1 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set when the VGA Enable bit is not set. If the VGA enable bit is set, accesses to I/O address range x3BCh – x3BFh are forwarded to the DMI Interface. If the VGA enable bit is not set, accesses to I/O address range x3BCh – x3BFh are treated just like any other I/O accesses; that is, the cycles are forwarded to PCI Express if the address is within IOBASE and IOLIMIT and the ISA enable bit is not set; otherwise, the accesses are forwarded to the DMI Interface. MDA resources are defined as the following:

Table 2-8. MDA Resources

Range Type	Address
Memory	0B0000h – 0B7FFFh
I/O	3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh (Including ISA address aliases, A[15:10] are not used in decode)

Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI interface even if the reference includes I/O locations not listed above.

For I/O reads that are split into multiple DWord accesses, this decode applies to each DWord independently. For example, a read to x3B3h and x3B4h (quadword read to x3B0h with BE#=E7h) will result in a DWord read from PEG at 3B0h (BE#=Eh), and a DWord read from DMI at 3B4h (BE=7h). Since the processor will not issue I/O writes crossing the DWord boundary, this case does not exist for writes.

Summary of decode priority:

- Processor Graphics VGA, if enabled, gets:
    - 03C0h – 03CFh: always
    - 03B0h – 03BBh: if MSR[0]=0 (MSR is I/O register 03C2h)
    - 03D0h – 03DFh: if MSR[0]=1

Note: 03BCh – 03BFh never decodes to Processor Graphics; 3BCh – 3BEh are parallel port I/Os, and 3BFh is only used by true MDA devices.

- Else, if MDA Present (if VGA on PEG is enabled), DMI gets:
    - x3B4,5,8,9,A,F (any access with any of these bytes enabled, regardless of the other BEs)
- Else, if VGA on PEG is enabled, PEG gets:
    - x3B0h – x3BBh
    - x3C0h – x3CFh
    - x3D0h – x3DFh
- Else, if ISA Enable=1, DMI gets:
    - upper 768 bytes of each 1K block
- Else, IOBASE/IOLIMIT apply.

2.17 I/O Mapped Registers

The processor contains two registers that reside in the processor I/O address space - the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3 Host Bridge and DRAM Controller (D0:F0)

This chapter documents the Host Bridge and DRAM Controller.

Table 3-1. Summary of Host Bridge and DRAM Controller (D0:F0)

Host Bridge/DRAM Registers (D0:F0)
Processor Memory Controller (MCHBAR) Registers
Power Management (MCHBAR) Registers
Host Controller (MCHBAR) Registers
Direct Media Interface BAR (DMIBAR) Registers
PCI Express Egress Port BAR (PXPEPBAR) Registers
VTDPVC0BAR Registers
Graphics VT BAR (GFXVTBAR) Registers
GTTMMADR (MCHBAR) Registers

3.1 Host Bridge/DRAM Registers (D0:F0)

Host Bridge/DRAM Controller. This chapter documents the registers in: Bus 0, Device 0, Function 0.

3.1.1 Summary of Registers

Table 3-2. Summary of Bus: 0, Device: 0, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	1	Revision Identification (RID_0_0_0_PCI)	00h
40h	8	PCI Express Egress Port Base Address (PXPEPBAR_0_0_0_PCI)	0000000000000000h
48h	8	MCHBAR Base Address Register (MCHBAR_0_0_0_PCI)	0000000000000000h
50h	2	Graphics Control (GGC_0_0_0_PCI)	0500h
54h	4	Device Enable (DEVEN_0_0_0_PCI)	0003D4DFh
58h	4	Protected Audio Video Path Control (PAVPC_0_0_0_PCI)	00000001h
5Ch	4	DMA Protected Range (DPR_0_0_0_PCI)	00000000h
60h	8	PCIEXBAR Base Address Register (PCIEXBAR_0_0_0_PCI)	0000000000000000h
68h	8	DMIBAR Base Address Register (DMIBAR_0_0_0_PCI)	0000000000000000h
80h	1	Programmable Attribute Map 0 (PAM0_0_0_0_PCI)	00h
81h	1	Programmable Attribute Map 1 (PAM1_0_0_0_PCI)	00h
82h	1	Programmable Attribute Map 2 (PAM2_0_0_0_PCI)	00h
83h	1	Programmable Attribute Map 3 (PAM3_0_0_0_PCI)	00h
84h	1	Programmable Attribute Map 4 (PAM4_0_0_0_PCI)	00h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
85h	1	Programmable Attribute Map 5 (PAM5_0_0_0_PCI)	00h
86h	1	Programmable Attribute Map 6 (PAM6_0_0_0_PCI)	00h
87h	1	Legacy Access Control (LAC_0_0_0_PCI)	10h
A0h	8	Top of Memory (TOM_0_0_0_PCI)	0000007FFFF00000h
A8h	8	Top of Upper Usable DRAM (TOUUD_0_0_0_PCI)	0000000000000000h
B0h	4	Base Data of Stolen Memory (BDSM_0_0_0_PCI)	00000000h
B4h	4	Base of GTT Stolen Memory (BGSM_0_0_0_PCI)	00100000h
B8h	4	TSEG Memory Base (TSEGMB_0_0_0_PCI)	00000000h
BCh	4	Top of Low Usable DRAM (TOLUD_0_0_0_PCI)	00100000h
C8h	2	Error Status (ERRSTS_0_0_0_PCI)	0000h
CAh	2	Error Command (ERRCMD_0_0_0_PCI)	0000h
CCh	2	SMI DMI Special Cycle (SMICMD_0_0_0_PCI)	0000h
CEh	2	SMI DMI Special Cycle (SCICMD_0_0_0_PCI)	0000h
DCh	4	Scratchpad Data (SKPD_0_0_0_PCI)	00000000h
E4h	4	Capabilities A (CAPID0_A_0_0_0_PCI)	00000000h
E8h	4	Capabilities B (CAPID0_B_0_0_0_PCI)	00000000h
ECh	4	Capabilities C (CAPID0_C_0_0_0_PCI)	00000000h
F0h	4	Capabilities E (CAPID0_E_0_0_0_PCI)	00000000h

3.1.2 Revision Identification (RID_0_0_0_PCI) — Offset 8h

This register contains the revision number of Device #0.

These bits are read only and writes to this register have no effect.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Revision ID MSB (RID_MSB):** Four upper bits of the Revision ID
3:0	0h RO	**Revision ID (RID):** Four lower bits of the Revision ID

3.1.3 PCI Express Egress Port Base Address (PXPEPBAR_0_0_0_PCI) — Offset 40h

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the EGRESS port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0].

All the bits in this register are locked in Intel TXT mode.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 40h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:12	00000000h RW	**PXPEPBAR:** This field corresponds to bits 41 to 12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the PCI Express Egress Port MMIO register set. All the bits in this register are locked in Intel TXT mode.
11:1	0h RO	**Reserved**
0	0h RW	**PXPEPBAR Enable (PXPEPBAREN):** 0: PXPEPBAR is disabled and does not claim any memory 1: PXPEPBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel TXT.

3.1.4 MCHBAR Base Address Register (MCHBAR_0_0_0_PCI) — Offset 48h

This is the base address for the Host Memory Mapped Configuration space.

There is no physical memory within this 128KB window that can be addressed.

The 128KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, the Host MMIO Memory Mapped Configuration space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset48h, bit 0].

All the bits in this register are locked in Intel TXT mode.

The register space contains memory control, initialization, timing, buffer strength registers, clocking registers and power and thermal management registers.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 48h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:17	0000000h RW	**MCHBAR:** This field corresponds to bits 41 to 17 of the base address Host Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 128KB block of contiguous memory address space. This register ensures that a naturally aligned 128KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the Host Memory Mapped register set. All the bits in this register are locked in Intel TXT mode.
16:1	0h RO	**Reserved**
0	0h RW	**MCHBAREN:** 0: MCHBAR is disabled and does not claim any memory 1: MCHBAR memory mapped accesses are claimed and decoded appropriately This register is locked in Intel TXT mode.

3.1.5 Graphics Control (GGC_0_0_0_PCI) — Offset 50h

All the bits in this register are Intel TXT lockable.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 50h	0500h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	05h RW/L	**GMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. This register is also Intel TXT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. **Locked by:** GGC_0_0_0_PCI.GGCLCK

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW/L	**GGMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. **Locked by:** GGC_0_0_0_PCI.GGCLCK
5:3	0h RO	**Reserved**
2	0h RW/L	**VAMEN:** Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 038000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h. **Locked by:** GGC_0_0_0_PCI.GGCLCK
1	0h RW/L	**IVD:** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO) BIOS Requirement: If a value of 1 is written, GGC[VAMEN] (ie. bit 2 in this register) should be also written to '1 so the sub-class field changes to 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory. **Locked by:** GGC_0_0_0_PCI.GGCLCK
0	0h RW/L	**GGCLCK:** When set to 1b, this bit will lock all bits in this register. **Locked by:** GGC_0_0_0_PCI.GGCLCK

3.1.6 Device Enable (DEVEN_0_0_0_PCI) — Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + 54h	0003D4DFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/L	**D6F1EN:** 0: Bus 0 Device 6 Function 1 is disabled and not visible. 1: Bus 0 Device 6 Function 1 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 1 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG61D
17	1h RW/L	**D10EN:** 0: Bus 0 Device 10 is disabled and not visible. 1: Bus 0 Device 10 is enabled and visible. This bit will be set to 0b and remain 0b if Device 10 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.DEV10_DISABLED
16	1h RW/L	**D6F2EN:** 0: Bus 0 Device 6 Function 2 is disabled and not visible. 1: Bus 0 Device 6 Function 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 2 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG62D
15	1h RW/L	**D8EN:** 0: Bus 0 Device 8 is disabled and not visible. 1: Bus 0 Device 8 is enabled and visible. This bit will be set to 0b and remain 0b if Device 8 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.GMM_DIS
14	1h RW/L	**D14F0EN:** VMD Enable - 0: Bus 0 Device 14 Function 0 is disabled and hidden. 1: Bus 0 Device 14 Function 0 is enabled and visible. **Locked by:** CAPID0_B_0_0_0_PCI.VMD_DIS
13	0h RW/L	**D6F0EN:** 0: Bus 0 Device 6 Function 0 is disabled and not visible. 1: Bus 0 Device 6 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 0 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG60D
12	1h RW/L	**D9EN:** 0: Bus 0 Device 9 is disabled and not visible. 1: Bus 0 Device 9 is enabled and visible. This bit will be set to 0b and remain 0b if Device 9 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.NPK_DIS
11	0h RO	**Reserved**
10	1h RW/L	**D5EN:** 0: Bus 0 Device 5 is disabled and not visible. 1: Bus 0 Device 5 is enabled and visible. This bit will be set to 0b and remain 0b if Device 5 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.IMGU_DIS
9:8	0h RO	**Reserved**
7	1h RW/L	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.CDD

Bit Range	Default & Access	Field Name (ID): Description
6	1h RW/L	**D3F7EN:** NVMe - Device 3 function 7 enable 0: Bus 0 Device 3 function 7 is disabled and hidden 1: Bus 0 Device 3 function 7 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F7D
5	0h RW/L	**D3F0EN:** NVMe - Device 3 function 0 enable 0: Bus 0 Device 3 function 0 is disabled and hidden 1: Bus 0 Device 3 function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled. Locked with CAPID0_A_0_0_0_PCI[31].NVME_F0D **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F0D
4	1h RW/L	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.IGD
3	1h RW/L	**D1F0EN:** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if PEG10 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG10D
2	1h RW/L	**D1F1EN:** 0: Bus 0 Device 1 Function 1 is disabled and hidden. 1: Bus 0 Device 1 Function 1 is enabled and visible. **Locked by:** CAPID0_A_0_0_0_PCI.PEG11D
1	1h RW/L	**D1F2EN:** 0: Bus 0 Device 1 Function 2 is disabled and hidden. 1: Bus 0 Device 1 Function 2 is enabled and visible. **Locked by:** CAPID0_A_0_0_0_PCI.PEG12D
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

3.1.7 Protected Audio Video Path Control (PAVPC_0_0_0_PCI) — Offset 58h

All the bits in this register are locked by Intel TXT. When locked the R/W bits are RO.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + 58h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**PCMBASE:** Sizes supported: 1M, 2M, 4M and 8M. Base value programmed (from Top of Stolen Memory) itself defines the size of the WOPCM. Separate WOPCM size programming is redundant information and not required. Default 1M size programming. 4M recommended. This register is locked (becomes read-only) when PAVPE = 1b. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
19:7	0h RO	**Reserved**
6	0h RW/L	**ASMFEN:** ASMF method enabled 0b Disabled (default). 1b Enabled. This register is locked when PAVPLCK is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
5	0h RO	**Reserved**
4	0h RW/L	**OVTATTACK:** Override of Unsolicited Connection State Attack and Terminate. 0: Disable Override. Attack Terminate allowed. 1: Enable Override. Attack Terminate disallowed. This register bit is locked when PAVPE is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
3	0h RW/L	**HVYMODSEL:** This bit is applicable only for PAVP2 operation mode or for PAVP3 mode only if the per-App memory configuration is disabled. 0: Lite Mode (Non-Serpent mode) 1: Serpent Mode For PAVP3 mode, this one type boot time programming has been replaced by per-App programming (through the Media Crypto Copy command). Note that PAVP2 or PAVP3 mode selection is done by programming bit 8 of the MFX_MODE - Video Mode register. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
2	0h RW/L	**PAVP Lock (PAVPLCK):** This bit locks all writable contents in this register when set (including itself). Only a hardware reset can unlock the register again. This lock bit needs to be set only if PAVP is enabled (bit 1 of this register is asserted). **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
1	0h RW/L	**PAVPE:** 0: PAVP functionality is disabled. 1: PAVP functionality is enabled. This register is locked when PAVPLCK is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/L	**PCME:** This field enables Protected Content Memory within Graphics Stolen Memory. This memory is the same as the WOPCM area, whose size is defined by bit 5 of this register. This register is locked when PAVPLOCK is set. A value of 0 in this field indicates that Protected Content Memory is disabled, and cannot be programmed in this manner when PAVP is enabled. A value of 1 in this field indicates that Protected Content Memory is enabled, and is the only programming option available when PAVP is enabled. For non-PAVP3 Mode, even for Lite mode configuration, this bit should be programmed to 1 and HVYMODESEL = 0). This bit should always be programmed to 1 if bits 1 and 2 (PAVPE and PAVP lock bits) are both set. With per-application Memory configuration support, the range check for the WOPCM memory area should always happen when this bit is set, regardless of Lite mode, Serpent mode, PAVP2 or PAVP3 mode programming. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK

3.1.8 DMA Protected Range (DPR_0_0_0_PCI) — Offset 5Ch

DMA protected range register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + 5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/V/L	**TOPOFDPR:** Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.
19:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RW/L	**DPRSIZE:** This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255 MB. The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1. Note: If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or ME stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation or Intel TXT NoDMA lookup. Therefore incoming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are ORed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all the above checks must pass before a cycle is allowed to DRAM. **Locked by:** DPR_0_0_0_PCI.LOCK
3	0h RO	**Reserved**
2	0h RW/L	**EPM:** This field controls DMA accesses to the DMA Protected Range (DPR) region. 0: DPR is disabled 1: DPR is enabled. All DMA requests accessing DPR region are blocked. HW reports the status of DPR enable/disable through the PRS field in this register. When this bit change, one must have to wait till the status (PRS) has updated before changing it again. **Locked by:** DPR_0_0_0_PCI.LOCK
1	0h RW/V/L	**PRS:** This field indicates the status of DPR. 0: DPR protection disabled 1: DPR protection enabled
0	0h RW/L	**LOCK:** All bits which may be updated by SW in this register are locked down when this bit is set. **Locked by:** DPR_0_0_0_PCI.LOCK

3.1.9 PCIEXBAR Base Address Register (PCIEXBAR_0_0_0_PCI) — Offset 60h

Defines the PCIEXBAR base address.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 60h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:31	000h RW	**PCIEXBAR:** This field corresponds to bits 41 to 32 of the base address for PCI Express enhanced configuration space including bus segments. BIOS will program this register resulting in a base address for a contiguous memory address space. The size of the range is defined by bits [3:1] of this register. This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within the 39-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address +Segment Number*256MB+ Bus Number * 1MB + Device Number * 32KB + Function Number * 4KB This address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
30	0h RW/V	**ADMSK1024:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
29	0h RW/V	**ADMSK512:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
28	0h RW/V	**ADMSK256:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
27	0h RW/V	**ADMSK128:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
26	0h RW/V	**ADMSK64:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
25:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RW	**LENGTH:** This field describes the length of this region. 000: 256MB (buses 0-255). Bits 38:28 are decoded in the PCI Express Base Address Field. 001: 128MB (buses 0-127). Bits 38:27 are decoded in the PCI Express Base Address Field. 010: 64MB (buses 0-63). Bits 38:26 are decoded in the PCI Express Base Address Field. 011: 512MB (buses 0-512). Bits 38:29 are decoded in the PCI Express Base Address Field. 100: 1024MB (buses 0-1024). Bits 38:30 are decoded in the PCI Express Base Address Field. 101: 2048MB (buses 0-2048). Bits 38:31 are decoded in the PCI Express Base Address Field. 110: 4096MB (buses 0-4096). Bits 38:32 are decoded in the PCI Express Base Address Field. 111:Rreserved.
0	0h RW	**PCIEXBAREN:** PCIEX BAR Enable

3.1.10 DMIBAR Base Address Register (DMIBAR_0_0_0_PCI) — Offset 68h

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the Host Bridge. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Dev 0, offset 68h, bit 0] All the bits in this register are locked in Intel TXT mode.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 68h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:12	00000000h RW	**DMIBAR:** This field corresponds to bits 41 to 12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the DMI register set. All the Bits in this register are locked in Intel TXT mode.
11:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**DMIBAREN:** 0: DMIBAR is disabled and does not claim any memory 1: DMIBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel TXT.

3.1.11 Programmable Attribute Map 0 (PAM0_0_0_0_PCI) — Offset 80h

This register controls the read, write and shadowing attributes of the BIOS range from F_0000h to F_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 80h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0F_0000h to 0F_FFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**LOCK:** If this bit is set, all of the PAM* registers are locked (cannot be written) **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.12 Programmable Attribute Map 1 (PAM1_0_0_0_PCI) — Offset 81h

This register controls the read, write and shadowing attributes of the BIOS range from C_0000h to C_7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 81h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C_4000h to 0C_7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.13 Programmable Attribute Map 2 (PAM2_0_0_0_PCI) — Offset 82h

This register controls the read, write and shadowing attributes of the BIOS range from C_8000h to C_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 82h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0CC000h to 0CFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.14 Programmable Attribute Map 3 (PAM3_0_0_0_PCI) — Offset 83h

This register controls the read, write and shadowing attributes of the BIOS range from D0000h to D7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 83h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.15 Programmable Attribute Map 4 (PAM4_0_0_0_PCI) — Offset 84h

This register controls the read, write and shadowing attributes of the BIOS range from D8000h to DFFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 84h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.16 Programmable Attribute Map 5 (PAM5_0_0_0_PCI) — Offset 85h

This register controls the read, write and shadowing attributes of the BIOS range from E_0000h to E_7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 85h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.17 Programmable Attribute Map 6 (PAM6_0_0_0_PCI) — Offset 86h

This register controls the read, write and shadowing attributes of the BIOS range from E_8000h to E_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 86h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0EC000h to 0EFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E8000h to 0EBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.18 Legacy Access Control (LAC_0_0_0_PCI) — Offset 87h

This 8-bit register controls steering of MDA cycles and a fixed DRAM hole from 15-16MB.

There can only be at most one MDA device in the system.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 87h	10h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HEN:** This field enables a memory hole in DRAM space. The DRAM that lies behind this space is not remapped. 0: No memory hole. 1: Memory hole from 15MB to 16MB. This bit is Intel TXT lockable.
6:5	0h RO	**Reserved**
4	1h RW	**MDAPCIE:** This bit works with the VGA Enable bits in the BCTRL register of Non PEG devices to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should be set to 1 by default. It is assumed that these devices will not need to support legacy MDA graphics. However this single bit is added just to support this rare case of using MDA over these devices. The behavior of this bit field is identical to bits [3:0]
3	0h RW	**MDAP60:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 2 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 2 VGA Enable bit is not set. If device 1 function 2 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 2 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 2. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 2. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 2. MDA references are not claimed by device 1 function 2. VGA and MDA memory cycles can only be routed across PEG12 when MAE (PCICMD12[1]) is set. VGA and MDA I/O cycles can only be routed across PEG12 if IOAE (PCICMD12[0]) is set.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MDAP12:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 2 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 2 VGA Enable bit is not set. If device 1 function 2 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 2 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 2. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 2. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 2. MDA references are not claimed by device 1 function 2. VGA and MDA memory cycles can only be routed across PEG12 when MAE (PCICMD12[1]) is set. VGA and MDA I/O cycles can only be routed across PEG12 if IOAE (PCICMD12[0]) is set.
1	0h RW	**MDAP11:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 1 VGA Enable bit is not set. If device 1 function 1 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 1 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 1. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 1. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 1. MDA references are not claimed by device 1 function 1. VGA and MDA memory cycles can only be routed across PEG11 when MAE (PCICMD11[1]) is set. VGA and MDA I/O cycles can only be routed across PEG11 if IOAE (PCICMD11[0]) is set.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**MDAP10:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 0 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 0 VGA Enable bit is not set. If device 1 function 0 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 0 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 0. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 0. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 0. MDA references are not claimed by device 1 function 0. VGA and MDA memory cycles can only be routed across PEG10 when MAE (PCICMD10[1]) is set. VGA and MDA I/O cycles can only be routed across PEG10 if IOAE (PCICMD10[0]) is set.

3.1.19 Top of Memory (TOM_0_0_0_PCI) — Offset A0h

This Register contains the size of physical memory.

BIOS determines the memory size reported to the OS using this Register.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + A0h	0000007FFFF00000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	07FFFFh RW/L	**TOM:** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address bits 41:20 (1MB granularity). Bits 19:0 are assumed to be 0. All the bits in this register are locked in Intel TXT mode. **Locked by:** TOM_0_0_0_PCI.LOCK

Bit Range	Default & Access	Field Name (ID): Description
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TOM_0_0_0_PCI.LOCK

3.1.20 Top of Upper Usable DRAM (TOUUD_0_0_0_PCI) — Offset A8h

This 64 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.

BIOS Restriction: Minimum value for TOUUD is 4GB.

These bits are Intel TXT lockable.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW/L	**TOUUD:** This register contains bits 41 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. All the bits in this register are locked in Intel TXT mode. **Locked by:** TOUUD_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TOUUD_0_0_0_PCI.LOCK

3.1.21 Base Data of Stolen Memory (BDSM_0_0_0_PCI) — Offset B0h

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset BC bits 31:20).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**BDSM:** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20). **Locked by:** BDSM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** BDSM_0_0_0_PCI.LOCK

3.1.22 Base of GTT Stolen Memory (BGSM_0_0_0_PCI) — Offset B4h

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + B4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	001h RW/L	**BGSM:** This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20). **Locked by:** BGSM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** BGSM_0_0_0_PCI.LOCK

3.1.23 TSEG Memory Base (TSEGMB_0_0_0_PCI) — Offset B8h

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20).

NOTE: BIOS must program TSEGMB to a 8MB naturally aligned boundary.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**TSEGMB:** This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20). BIOS must program the value of TSEGMB to be the same as BGSM when TSEG is disabled. **Locked by:** TSEGMB_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TSEGMB_0_0_0_PCI.LOCK

3.1.24 Top of Low Usable DRAM (TOLUD_0_0_0_PCI) — Offset BCh

This 32 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics memory and Graphics Stolen Memory are within the DRAM space defined. From the top, the Host optionally claims 1 to 64MBs of DRAM for internal graphics if enabled, 1or 2MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example:

C1DRB3 is set to 4GB

TSEG is enabled and TSEG size is set to 1MB

Internal Graphics is enabled, and Graphics Mode Select is set to 32MB

GTT Graphics Stolen Memory Size set to 2MB

BIOS knows the OS requires 1G of PCI space.

BIOS also knows the range from 0_FEC0_0000h to 0_FFFF_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC and Intel TXT.

According to the above equation, TOLUD is originally calculated to: 4GB = 1_0000_0000h

The system memory requirements are: 4GB (max addressable space) - 1GB PCI space) - 35MB (lost memory) = 3GB - 35MB (minimum granularity) = 0_ECB0_0000h

Since 0_ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.

These bits are Intel TXT lockable.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + BCh	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	001h RW/L	**TOLUD:** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by TSEG size to determine base of TSEG. All the Bits in this register are locked in Intel TXT mode. This register must be 1MB aligned when reclaim is enabled. **Locked by:** TOLUD_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TOLUD_0_0_0_PCI.LOCK

3.1.25 Error Status (ERRSTS_0_0_0_PCI) — Offset C8h

Please refer to doc #655741 for details.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + C8h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

3.1.26 Error Command (ERRCMD_0_0_0_PCI) — Offset CAh

This register controls the Host Bridge responses to various system errors. Since the Host Bridge does not have an SERRB signal, SERR messages are passed from the CPU to the PCH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + CAh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**MC0 DDR5 CRC Error (MC1_DDR5_CRC):** 1: The Host Bridge generates an SERR message over DMI when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
10	0h RW	**MC0 DDR5 CRC Error (MC0_DDR5_CRC):** 1: The Host Bridge generates an SERR message over DMI when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
9	0h RW	**Data Uncorrectable Error (MC1_DMERR):** 1: The Host Bridge generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
8	0h RW	**Data Single Bit Correctable Error (MC1_DSERR):** 1: The Host Bridge generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0: Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.
7	0h RO	**IBECC Uncorrectable Error (IBECC_UC):** This bit is **deprecated** and kept for backwards compatibility. IBECC error messages are logged in the MCA bank.
6	0h RO	**IBECC Correctable Error (IBECC_COR):** This bit is **deprecated** and kept for backwards compatibility. IBECC error messages are logged in the MCA bank.
5	0h RW	**SERR on FMHC Unsupported Request Event (FMUR):** SERR on FMHC unsupported request event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports an unsupported request event. 0: Reporting of this condition via SERR messaging is disabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**SERR on FMHC CA Event (FMCA):** SERR on FMHC CA event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SERR messaging is disabled.
3	0h RW	**SERR on FMI Asynchronous Notification (FMIAN):** SERR on FMI Asynchronous Notification error event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SERR messaging is disabled.
2	0h RW	**SERR on FMHC Thermal Event (FMITHERMERR):** SERR on FMHC thermal event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SERR messaging is disabled.
1	0h RW	**Data Uncorrectable Error (MC0_DMERR):** 1: The Host Bridge generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	0h RW	**Data Single Bit Correctable Error (MC0_DSERR):** 1: The Host Bridge generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0: Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.

3.1.27 SMI DMI Special Cycle (SMICMD_0_0_0_PCI) — Offset CCh

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + CCh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**MC1 DDR5 CRC Error (MC1_DDR5_CRC):** 1: The Host generates an SMI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**MC0 DDR5 CRC Error (MC0_DDR5_CRC):** 1: The Host generates an SMI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
9	0h RW	**SMI on Multiple Bit Error (MC1_DMESMI):** 1: The Host generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
8	0h RW	**Single Bit Error (MC1_DSESMI):** 1: The Host generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.
7	0h RO	**IBECC Uncorrectable Error (IBECC_UC):** This bit is **deprecated** and kept for backwards compatibility. IBECC error messages are logged in the MCA bank.
6	0h RO	**IBECC Correctable Error (IBECC_COR):** This bit is **deprecated** and kept for backwards compatibility. IBECC error messages are logged in the MCA bank.
5	0h RW	**SMI on FMHC Unsupported Request Event (FMUR):** 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports an unsupported request event. 0: Reporting of this condition via SMI messaging is disabled.
4	0h RW	**SMI on FMHC CA Event (FMCA):** SMI on FMHC CA event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SMI messaging is disabled.
3	0h RW	**SMI on FMI Asynchronous Notification (FMIAN):** SMI on FMI Asynchronous Notification error event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SMI messaging is disabled.
2	0h RW	**SMI on FMHC Thermal Event (FMITHERMERR):** SMI on FMHC thermal event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SMI messaging is disabled.
1	0h RW	**SMI on Multiple Bit Error (MC0_DMESMI):** 1: The Host generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	0h RW	**Single Bit Error (MC0_DSESMI):** 1: The Host generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.

3.1.28 SMI DMI Special Cycle (SCICMD_0_0_0_PCI) — Offset CEh

This register enables various errors to generate an SCI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + CEh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**MC1 DDR5 CRC Error (MC1_DDR5_CRC):** 1: The Host generates an SCI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
10	0h RW	**MC0 DDR5 CRC Error (MC0_DDR5_CRC):** 1: The Host generates an SCI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
9	0h RW	**SCI on Multiple Bit Error (MC1_DMESCI):** 1: The Host generates an SCI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting ECC this bit must be disabled.
8	0h RW	**SCI on Single Bit Error (MC1_DSESCI):** 1: The Host generates an SCI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SCI messaging is disabled. For systems that do not support ECC this bit must be disabled.
7	0h RO	**IBECC Uncorrectable Error (IBECC_UC):** This bit is **deprecated** and kept for backwards compatibility. IBECC error messages are logged in the MCA bank.
6	0h RO	**IBECC Correctable Error (IBECC_COR):** This bit is **deprecated** and kept for backwards compatibility. IBECC error messages are logged in the MCA bank.
5	0h RW	**SMI on FMHC Unsupported Request Event (FMUR):** SCI on FMHC unsupported request event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports an unsupported request event. 0: Reporting of this condition via SCI messaging is disabled.
4	0h RW	**FMCA:** SCI on FMHC CA event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SCI messaging is disabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**SCI on FMI Asynchronous Notification (FMIAN):** SCI on FMI Asynchronous Notification error event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SCI messaging is disabled.
2	0h RW	**FMITHERMERR:** SCI on FMHC thermal event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SCI messaging is disabled.
1	0h RW	**SCI on Multiple Bit Error (MC0_DMESCI):** 1: The Host generates an SCI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	0h RW	**SCI on Single Bit Error (MC0_DSESCI):** 1: The Host generates an SCI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SCI messaging is disabled. For systems that do not support ECC this bit must be disabled.

3.1.29 Scratchpad Data (SKPD_0_0_0_PCI) — Offset DCh

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SKPD:** 1 DWORD of data storage.

3.1.30 Capabilities A (CAPID0_A_0_0_0_PCI) — Offset E4h

Processor capability enumeration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**NVME Device 3 Function 0 Disable (NVME_F0D):** 0: Device 3 Function 0 and associated memory spaces are accessible. 1: Device 3 Function 0 (NVMe F0) and associated memory space are disabled by hardwiring the D3F0EN field, bit 5 of the SoC Device Enable register
30	0h RW/L	**PCIe Device 1 Function 2 Disable (PEG12D):** 0: Device 1 Function 2 and associated memory spaces are accessible. 1: Device 1 Function 2 and associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
29	0h RW/L	**PCIe Device 1 Function 1 Disable (PEG11D):** 0: Device 1 Function 1 and associated memory spaces are accessible. 1: Device 1 Function 1 and associated memory and IO spaces are disabled by hardwiring the D1F1EN field, bit 2 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
28	0h RW/L	**PCIe Device 1 Function 0 Disable (PEG10D):** 0: Device 1 Function 0 and associated memory spaces are accessible. 1: Device 1 Function 0 and associated memory and IO spaces are disabled by hardwiring the D1F0EN field, bit 3 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
27	0h RW/L	**PCIe Link Width Up-config Disable (PELWUD):** 0: Link width upconfig is supported. The Processor advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The Processor does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	0h RW/L	**DMI Width (DW):** 0: DMI x4 1: DMI x2
25	0h RW/L	**DRAM ECC Disable (ECCDIS):** 0: ECC is supported 1: ECC is not supported
24	0h RW/L	**Force DRAM ECC Enable (FDEE):** 0: DRAM ECC optional via software. 1: DRAM ECC enabled. MCHBAR C0MISCCTL bit [0] and C1MISCCTL bit [0] are forced to 1 and Read-Only. Note that FDEE and ECCDIS must not both be set to 1.
23	0h RW/L	**VT-d Disable (VTDD):** 0: VT-d is supported 1: VT-d is not supported
22	0h RW/L	**DMI GEN2 Disable (DMIG2DIS):** 0: Capable of running DMI in Gen 2 mode 1: Not capable of running DMI in Gen 2 mode

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**Reserved**
20:19	0h RW/L	**DRAM Maximum Size per Channel (DDRSZ):** This field defines the maximum allowed memory size per channel. • 0: Unlimited (64GB per channel) • 1: Maximum 8GB per channel • 2: Maximum 4GB per channel • 3: Maximum 2GB per channel
18	0h RW/L	**PCIe Controller Device 6 Function 0 Disabled (PEG60D):** PCIe Controller Device 6 Function 0 is disabled 0: Device 6 Function 0 is supported 1: Device 6 Function 0 is not supported
17	0h RW/L	**DRAM 1N Timing Disable (D1NM):** 0: Part is capable of supporting 1n mode timings on the DDR interface. 1: Part is not capable of supporting 1n mode. Only supported timings are 2n or greater.
16	0h RO	**Reserved**
15	0h RW/L	**DTT Device Disable (CDD):** 0: DTT Device enabled. 1: DTT Device disabled.
14	0h RW/L	**2 DIMMs Per Channel Enable (DDPCD):** Allows Dual Channel operation but only supports 1 DIMM per channel. 0: 2 DIMMs per channel enabled 1: 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero. (MCHBAR offset 260h, bits 22-23 for channel 0 and MCHBAR offset 660h, bits 22-23 for channel 1)
13	0h RW/L	**X2APIC Enable (X2APIC_EN):** Extended Interrupt Mode. 0b: Hardware does not support Extended APIC mode. 1b: Hardware supports Extended APIC mode.
12	0h RW/L	**Dual Memory Channel Support (PDCD):** 0: Capable of Dual Channel 1: Not Capable of Dual Channel - only single channel capable.
11	0h RW/L	**Internal Graphics Disable (IGD):** 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RW/L	**DID0 Override Enable (DID0OE):** 0: Disable ability to override DID0 - For production 1: Enable ability to override DID - For debug and samples only

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Reserved**
8	0h RW/L	**2 Level Memory Support (2LM_SUPPORTED):** 0: 2 Level Memory (2LM) is not supported. Only 1LM is supported. 1: 2 Level Memory (2LM) is supported
7:4	0h RW/L	**Compatibility Revision ID (CRID):** Compatibility Revision ID
3	0h RW/L	**Memory Overclocking (DDR_OVERCLOCK):** Memory Overclocking is enabled. When supported, memory can be trained at higher than default maximum frequencies. 0: Memory Overclocking is not supported 1: Memory Overclocking is supported
2	0h RO	**Reserved**
1	0h RW/L	**NVME F7D (NVME_F7D):** 0: Device 3 Function 7 and associated memory spaces are accessible. 1: Device 3 Function 7 (NVMe F7) and associated memory space are disabled by hardwiring the D3F7EN field, bit 6 of the SoC Device Enable register
0	0h RO	**Reserved**

3.1.31 Capabilities B (CAPID0_B_0_0_0_PCI) — Offset E8h

Processor capability enumeration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Image Processing Unit (IPU) Disable (IPU_DIS):** 0: Device 5 associated memory spaces are accessible. 1: Device 5 associated memory and IO spaces are disabled.
30	0h RW/L	**Trace Hub Disable (TRACE_HUB_DIS):** 0: Trace Hub associated memory spaces are accessible. 1: Trace Hub associated memory and IO spaces are disabled.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RW/L	**Overclocking Enabled (OC_ENABLED):** 0: Overclocking is Disabled 1: Overclocking is Enabled If overclocking is enabled, MSR FLEX_RATIO.OC_BINS contains how many bits of over-clocking are supported. The encoding is as follows: 0: Overclocking is Disabled 1-6: Turbo ratio limits can be incremented by this amount 7: Unlimited If overclocking is disabled, FLEX_RATIO.OC_BINS is meaningless.
28	0h RW/L	**SMT Capability (SMT):** This setting indicates whether the processor is SMT (HyperThreading) capable.
27:25	0h RW/L	**Cache Size (CACHESZ):** This setting indicates the supporting cache sizes.
24	0h RW/L	**SVM Disable (SVM_DISABLE):** 0: SVM enabled 1: SVM disabled
23:21	0h RW/L	**Memory 100MHz Reference Clock (PLL_REF100_CFG):** DDR Maximum Frequency Capability with 100MHz memory reference clock (ref_clk). 0: 100 MHz memory reference clock is not supported 1-6: Reserved 7: Unlimited
20	0h RW/L	**PCIe Gen 3 Disable (PEGG3_DIS):** 0: Capable of running any of the Gen 3-compliant PCIe controllers in Gen 3 mode (Devices 0/1/x, 0/6/x) 1: Not capable of running any of the PCIe controllers in Gen 3 mode
19	0h RW/L	**Processor Package Type (PKGTYP):** This setting indicates the CPU Package Type.
18:17	0h RO	**Reserved**
16	0h RW/L	**PCIe x16 Disable (PEGX16D):** 0: Capable of x16 PCIe Port 1: Not Capable of x16 PCIe port, instead PCIe limited to x8 and below. Causes PCIe port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down (unless in use by the other PEG port or the embedded Display Port), and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down.)
15	0h RW/L	**DMI Gen 3 Disable (DMIG3DIS):** DMI Gen 3 Disable
14:12	0h RW/L	**2 Level Memory Technology Support (LTECH):** 0: 1LM 1: EDRAM0 3: EDRAM0+1 4: 2LM Other values are reserved.
11	0h RW/L	**HDCP Disable (HDCPD):** 0: Capable of HDCP 1: HDCP Disabled
10	0h RW/L	**Device 10 Disable (DEV10_DISABLED):** Indicates if Device 10 (Crash Log/Telemetry) is disabled. 0: Device 10 capability is present 1: Device 10 is disabled and locked from further enabling

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Reserved**
8	0h RW/L	**GNA (GMM) Disable (GNA_DIS):** 0: Device 8 associated memory spaces are accessible. 1: Device 8 associated memory and IO spaces are disabled by hardwiring the D8EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
7	0h RW/L	**DDD:** 0: Debug mode 1: Production mode
6:4	0h RO	**Reserved**
3	0h RW/L	**S/H OPI Enable (SH_OPI_EN):** Specifies if OPI or DMI are enabled for S/H models. 0: DMI is enabled 1: OPI is enabled
2	0h RW/L	**VMD Disable (VMD_DIS):** Indicates if VMD is disabled.
1	0h RW/L	**Global Single PCIe Lane (DPEGFX1):** This bit has no effect on Device 1 unless Device 1 is configured for at least two ports via PEG0CFGSEL strap. 0: All PCIe port widths do not depend on their respective BCTRL[VGAEN]. 1: Each PCIe port width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.
0	0h RW/L	**Single PCIe Lane (SPEGFX1):** This bit has no effect on Device 1 unless Device 1 is configured for a single port via PEG0CFGSEL strap. 0: Device 1 Function 0 width does not depend on its BCTRL[VGAEN]. 1: Device 1 Function 0 width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1.

3.1.32 Capabilities C (CAPID0_C_0_0_0_PCI) — Offset ECh

Processor capability enumeration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PEG62D:** 0: Device 6 Function 2 and associated memory spaces are accessible. 1: Device 6 Function 2 and associated memory space are disabled.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/L	**PCIe Controller Device 6 Function 1 Disabled (PEG61D):** PCIe Controller Device 6 Function 1 is disabled 0: Device 6 Function 1 is supported 1: Device 6 Function 1 is not supported
29	0h RW/L	**PCIe Gen 5 Disable (PEGG5_DIS):** This field will be strap selectable/modifiable to enable PCH Pairing capabilities. 0: Capable of running any of the Gen 5-compliant PCIe controllers in Gen 5 mode (Devices 0/1/x) 1: Not capable of running any of the PEG controllers in Gen 5 mode
28	0h RW/L	**PCIe Gen 4 Disable (PEGG4_DIS):** PCIe Gen 4 Disabled. This field will be strap selectable/modifiable to enable PCH Pairing capabilities. 0: Capable of running any of the Gen 4-compliant PCIe controllers in Gen 4 mode (Devices 0/1/x, 0/6/x) 1: Not capable of running any of the PEG controllers in Gen 4 mode
27:23	00h RW/L	**Maximum DDR4 Frequency (MAX_DATA_RATE_DDR4):** DDR4 Maximum Frequency Capability in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited 1-31: multiples of 266MHz
22	0h RW/L	**DDR4 Support (DDR4_EN):** 0: DDR4 is not supported 1: DDR4 is supported
21:17	00h RW/L	**Maximum LPDDR4 Frequency (MAX_DATA_RATE_LPDDR4):** LPDDR4 Maximum Frequency Capability in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited 1-31: multiples of 266MHz
16	0h RW/L	**LPDDR4 Support (LPDDR4_EN):** 0: LPDDR4 memory is not supported 1: LPDDR4 memory is supported
15	0h RO	**Reserved**
14	0h RW/L	**Dynamic Memory Frequency Change Disable (QCLK_GV_DIS):** 0: Dynamic Memory Frequency Change is enabled 1: Dynamic Memory Frequency Change is disabled
13:10	0h RO	**Reserved**
9	0h RW/L	**SGX Disabled (SGX_DIS):** Software Guard Extension (Intel® SGX) Disabled: Indicates that Intel® SGX is not available on this processor
8:7	0h RW/L	**BCLKOCRANGE:** BCLK (Base clock) Overclocking maximum frequency. • 0: BCLK overclocking is disabled • 1: BCLK maximum frequency is 115MHz • 2: BCLK maximum frequency is 130MHz • 3: Unlimited BCLK maximum frequency

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/L	**Internal Display Disabled (IDD):** Specifies whether the Internal Display is Disabled. 0: Internal Display is enabled. 1: Internal Display is disabled.
5	0h RW/L	**DISPLAY PIPE3 (DISPLAY_PIPE3):** 0: 3rd Display is disabled 1: 3rd Display is enabled
4:0	0h RO	**Reserved**

3.1.33 Capabilities E (CAPID0_E_0_0_0_PCI) — Offset F0h

Processor capability enumeration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/L	**Crash Log Device 10 Disable (CRASHLOG_DIS):** 0: Device 10 associated memory spaces are accessible. 1: Device 10 associated memory and IO spaces are disabled by hardwiring the D10EN field, bit 17 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
23:13	000h RW/L	**VDDQ_TX Maximum VID (VDDQ_VOLTAGE_MAX):** VDDQ_TX Maximum VID value.
12	0h RW/L	**IBECC Disable (IBECC_DIS):** 0: IBECC enabled. 1: IBECC disabled.
11:7	00h RW/L	**Maximum DDR5 Frequency (MAX_DATA_RATE_DDR5):** DDR5 Maximum Frequency Capability in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited 1-31: multiples of 266MHz
6	0h RW/L	**DDR5 Support (DDR5_EN):** 0: DDR5 memory is not supported 1: DDR5 memory is supported
5:1	00h RW/L	**Maximum LPDDR5 Frequency (MAX_DATA_RATE_LPDDR5):** LPDDR5 Maximum Frequency Capability in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited 1-31: multiples of 266MHz

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**LPDDR5 Support (LPDDR5_EN):** 0: LPDDR5 memory is not supported 1: LPDDR5 memory is supported

3.2 Processor Memory Controller (MCHBAR) Registers

This chapter documents the Memory Controller MCHBAR registers.

Base address of these registers are defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

The processor has 2 memory controllers. Each memory controller has 2 channels. Each channel can drive up to 2 sub channels depending on the memory type:

- LPDDR4x\LPDDR5:
  - 2 Memory controllers
  - 2 Channels per memory controller (total 4)
  - 2 sub channels per channel (total 8)
- DDR4:
  - 2 Memory controllers
  - 1 Channel per memory controller (total 2)
  - No sub channels
- DDR5:
  - 2 Memory controllers
  - 2 Channels per memory controller (total 4)
  - No sub channels

The MCHBAR exposes 3 sets of memory controller registers per controller for channel 0, channel 1 as well as broadcast.

- Memory Controller 0 (MC0)
  - Channel 0 offset range: E000h-E7FFh
  - Channel 1 offset range: E800h-EFFFh
  - Broadcast offset range: F000h-F7FFh
  - Shared registers: D800h-DFFFh
- Memory Controller 1 (MC1)
  - Channel 0 offset range: 1E000h-1E7FFh
  - Channel 1 offset range: 1E800h-1EFFFh
  - Broadcast offset range: 1F000h-1F7FFh
  - Shared registers: 1D800h-1DFFFh

Memory Controller Broadcast register behavior is to write to all channels of the same memory controller and read from channel 0.

Note: For brevity, only Channel 0 and the shared registers of MC0 are documented:

- MC0 Channel 1: MC0 Channel 0 + 0800h
- MC0 Broadcast: MC0 Channel 0 + 1000h
- MC1 Channel 0: MC0 Channel 0 + 10000h
- MC1 Channel 1: MC0 Channel 0 + 10800h

- MC1 Broadcast: MC0 Channel 0 + 11000h
- MC1 Shared: MC0 Shared + 10000h

3.2.1 Summary of Registers

Table 3-3. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5400h	8	GFX VT Range Base Address Register (GFXVTBAR_0_0_0_MCHBAR_NCU)	0000000000000000h
5410h	8	VT DMI PEG VC0 Range Base Address Register (VTDPVC0BAR_0_0_0_MCHBAR_NCU)	0000000000000000h
7900h	4	IMR0 BASE (IMR0BASE_0_0_0_MCHBAR_IMPH)	00000000h
7904h	4	IMR0 MASK (IMR0MASK_0_0_0_MCHBAR_IMPH)	00000000h
7920h	4	IMR1 BASE (IMR1BASE_0_0_0_MCHBAR_IMPH)	00000000h
7924h	4	IMR1 MASK (IMR1MASK_0_0_0_MCHBAR_IMPH)	00000000h
7940h	4	IMR2 BASE (IMR2BASE_0_0_0_MCHBAR_IMPH)	00000000h
7944h	4	IMR2 MASK (IMR2MASK_0_0_0_MCHBAR_IMPH)	00000000h
7960h	4	IMR3 BASE (IMR3BASE_0_0_0_MCHBAR_IMPH)	00000000h
7964h	4	IMR3 MASK (IMR3MASK_0_0_0_MCHBAR_IMPH)	00000000h
7980h	4	IMR4 BASE (IMR4BASE_0_0_0_MCHBAR_IMPH)	00000000h
7984h	4	IMR4 MASK (IMR4MASK_0_0_0_MCHBAR_IMPH)	00000000h
79A0h	4	IMR5 BASE (IMR5BASE_0_0_0_MCHBAR_IMPH)	00000000h
79A4h	4	IMR5 MASK (IMR5MASK_0_0_0_MCHBAR_IMPH)	00000000h
79C0h	4	IMR6 BASE (IMR6BASE_0_0_0_MCHBAR_IMPH)	00000000h
79C4h	4	IMR6 MASK (IMR6MASK_0_0_0_MCHBAR_IMPH)	00000000h
79E0h	4	IMR7 BASE (IMR7BASE_0_0_0_MCHBAR_IMPH)	00000000h
79E4h	4	IMR7 MASK (IMR7MASK_0_0_0_MCHBAR_IMPH)	00000000h
7A00h	4	IMR8 BASE (IMR8BASE_0_0_0_MCHBAR_IMPH)	00000000h
7A04h	4	IMR8 MASK (IMR8MASK_0_0_0_MCHBAR_IMPH)	00000000h
7A20h	4	IMR9 BASE (IMR9BASE_0_0_0_MCHBAR_IMPH)	00000000h
7A24h	4	IMR9 MASK (IMR9MASK_0_0_0_MCHBAR_IMPH)	00000000h
7A40h	4	IMR10 BASE (IMR10BASE_0_0_0_MCHBAR_IMPH)	00000000h
7A44h	4	IMR10 MASK (IMR10MASK_0_0_0_MCHBAR_IMPH)	00000000h
7A60h	4	IMR11 BASE (IMR11BASE_0_0_0_MCHBAR_IMPH)	00000000h
7A64h	4	IMR11 MASK (IMR11MASK_0_0_0_MCHBAR_IMPH)	00000000h
7A80h	4	IMR12 BASE (IMR12BASE_0_0_0_MCHBAR_IMPH)	00000000h
7A84h	4	IMR12 MASK (IMR12MASK_0_0_0_MCHBAR_IMPH)	00000000h
7AA0h	4	IMR13 BASE (IMR13BASE_0_0_0_MCHBAR_IMPH)	00000000h
7AA4h	4	IMR13 MASK (IMR13MASK_0_0_0_MCHBAR_IMPH)	00000000h
7AC0h	4	IMR14 BASE (IMR14BASE_0_0_0_MCHBAR_IMPH)	00000000h
7AC4h	4	IMR14 MASK (IMR14MASK_0_0_0_MCHBAR_IMPH)	00000000h
7AF0h	4	IMR15 BASE (IMR15BASE_0_0_0_MCHBAR_IMPH)	00000000h
7AF4h	4	IMR15 MASK (IMR15MASK_0_0_0_MCHBAR_IMPH)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7B10h	4	IMR16 BASE (IMR16BASE_0_0_0_MCHBAR_IMPH)	00000000h
7B14h	4	IMR16 MASK (IMR16MASK_0_0_0_MCHBAR_IMPH)	00000000h
7B30h	4	IMR17 BASE (IMR17BASE_0_0_0_MCHBAR_IMPH)	00000000h
7B34h	4	IMR17 MASK (IMR17MASK_0_0_0_MCHBAR_IMPH)	00000000h
7B50h	4	IMR18 BASE (IMR18BASE_0_0_0_MCHBAR_IMPH)	00000000h
7B54h	4	IMR18 MASK (IMR18MASK_0_0_0_MCHBAR_IMPH)	00000000h
D800h	4	Inter-Channel Decode Parameters (MAD_INTER_CHANNEL_0_0_0_MCHBAR)	00000000h
D804h	4	Intra-Channel 0 Decode Parameters (MAD_INTRA_CH0_0_0_0_MCHBAR)	00000000h
D808h	4	Intra-Channel 1 Decode Parameters (MAD_INTRA_CH1_0_0_0_MCHBAR)	00000000h
D80Ch	4	Channel 0 DIMM Characteristics (MAD_DIMM_CH0_0_0_0_MCHBAR)	10001800h
D810h	4	Channel 1 DIMM Characteristics (MAD_DIMM_CH1_0_0_0_MCHBAR)	10001800h
D824h	4	Channel Hash (CHANNEL_HASH_0_0_0_MCHBAR)	03000000h
D828h	4	Channel Enhanced Hash (CHANNEL_EHASH_0_0_0_MCHBAR)	00000000h
D83Ch	4	Memory Request Counters Configuration (PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR)	00010820h
D840h	8	Memory Request Global Counter (PWM_TOTAL_REQCOUNT_0_0_0_MCHBAR)	0000000000000000h
D848h	8	Memory Request Counter 0 (PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0])	0000000000000000h
D858h	8	RdCAS Counter (PWM_RDCAS_COUNT_0_0_0_MCHBAR)	0000000000000000h
D860h	4	Self Refresh Mode Control (PM_SREF_CONFIG_0_0_0_MCHBAR)	00000200h
D888h	8	Address Compare for ECC Error Inject (ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR)	0000000000000000h
D890h	8	Remap Base (REMAPBASE_0_0_0_MCHBAR)	0000007FFFF00000h
D898h	8	Remap Limit (REMAPLIMIT_0_0_0_MCHBAR)	0000000000000000h
D8A0h	8	WrCAS Counter (PWM_WRCAS_COUNT_0_0_0_MCHBAR)	0000000000000000h
D8A8h	8	Command Counter (PWM_COMMAND_COUNT_0_0_0_MCHBAR)	0000000000000000h
D958h	8	Address Mask for ECC Error Inject (ECC_INJ_ADDR_MASK_0_0_0_MCHBAR)	00000001FFFFFFFFh
D9B8h	4	MAD MC HASH 0 0 0 MCHBAR (MAD_MC_HASH_0_0_0_MCHBAR)	00000006h
D9C0h	4	PMON GLOBAL CONTROL 0 0 0 MCHBAR (PMON_GLOBAL_CONTROL_0_0_0_MCHBAR)	00000000h
D9C4h	4	PMON UNIT CONTROL 0 0 0 MCHBAR (PMON_UNIT_CONTROL_0_0_0_MCHBAR)	00000000h
D9D0h	4	PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0])	00000000h
D9E8h	8	PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[0])	0000000000000000h
DA10h	4	OS Telemetry Control (OS_TELEMETRY_CONTROL_0_0_0_MCHBAR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E000h	8	PRE Command Timing (TC_PRE_0_0_0_MCHBAR)	104070180040C008h
E008h	4	ACT Command Timing (TC_ACT_0_0_0_MCHBAR)	18020810h
E00Ch	4	RD to RD Timings (TC_RDRD_0_0_0_MCHBAR)	04040484h
E010h	4	RD to WR Timings (TC_RDWR_0_0_0_MCHBAR)	04040404h
E014h	4	WR to RD Timings (TC_WRRD_0_0_0_MCHBAR)	08100804h
E018h	4	WR to WR Timings (TC_WRWR_0_0_0_MCHBAR)	04040404h
E020h	8	Roundtrip Latency (SC_ROUNDTRIP_LATENCY_0_0_0_MCHBAR)	1919191919191919h
E048h	4	ECC Error Log 0 (ECCERRLOG0_0_0_0_MCHBAR)	00000000h
E04Ch	4	ECC Error Log 0 (ECCERRLOG1_0_0_0_MCHBAR)	00000000h
E050h	8	Power Down Timing (TC_PWRDN_0_0_0_MCHBAR)	0804100400810204h
E070h	8	ODT Command Timing (TC_ODT_0_0_0_MCHBAR)	0000000006050000h
E080h	4	ODT Matrix (SC_ODT_MATRIX_0_0_0_MCHBAR)	00000000h
E088h	8	Scheduler Configuration (SC_GS_CFG_0_0_0_MCHBAR)	0100000000000020h
E0B8h	4	DDRIO Power Mode Timing (SPID_LOW_POWER_CTL_0_0_0_MCHBAR)	08104426h
E104h	4	TR RRDVALID ctrl 0 0 0 MCHBAR (TR_RRDVALID_CTRL_0_0_0_MCHBAR)	00000000h
E108h	8	TR RRDVALID data 0 0 0 MCHBAR (TR_RRDVALID_DATA_0_0_0_MCHBAR)	0000000000000000h
E40Ch	4	TC REFm 0 0 0 MCHBAR (TC_REFM_0_0_0_MCHBAR)	0000003Ch
E424h	4	MR4 Rank Temperature (MR4_RANK_TEMPERATURE_0_0_0_MCHBAR)	03030303h
E428h	4	DDR4 Temperature (DDR4_MPR_RANK_TEMPERATURE_0_0_0_MCHBAR)	01010101h
E438h	4	Refresh Parameters (TC_RFP_0_0_0_MCHBAR)	2356980Fh
E43Ch	4	Refresh Timing Parameters (TC_RFTP_0_0_0_MCHBAR)	02D01004h
E440h	4	Self-Refresh Timing Parameters (TC_SRFTP_0_0_0_MCHBAR)	00000200h
E444h	4	Refresh Stagger Control (MC_REFRESH_STAGGER_0_0_0_MCHBAR)	00000000h
E448h	8	ZQCAL Control (TC_ZQCAL_0_0_0_MCHBAR)	0000032000010000h
E454h	4	Memory Controller Initial State (MC_INIT_STATE_0_0_0_MCHBAR)	0000000Fh
E460h	4	DIMM Idle Energy (PM_DIMM_IDLE_ENERGY_0_0_0_MCHBAR)	00000000h
E464h	4	DIMM Power-Down Energy (PM_DIMM_PD_ENERGY_0_0_0_MCHBAR)	00000000h
E468h	4	DIMM ACT Energy (PM_DIMM_ACT_ENERGY_0_0_0_MCHBAR)	00000000h
E46Ch	4	DIMM RD Energy (PM_DIMM_RD_ENERGY_0_0_0_MCHBAR)	00000000h
E470h	4	DIMM WR Energy (PM_DIMM_WR_ENERGY_0_0_0_MCHBAR)	00000000h
E478h	4	WR Delay (SC_WR_DELAY_0_0_0_MCHBAR)	00000003h
E488h	4	Per Bank Refresh (SC_PBR_0_0_0_MCHBAR)	0000F011h
E494h	4	Miscellaneous Timing Constrains (TC_LPDDR4_MISC_0_0_0_MCHBAR)	04081056h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E4C0h	8	Self-Refresh Exit Timing Parameters (TC_SREXITTP_0_0_0_MCHBAR)	0200000000000000h
E4E8h	4	Built in Self Test (WDB_MBIST_0_0_0_MCHBAR[0])	00000000h
E4F8h	4	RDB Built in Self Test (RDB_MBIST_0_0_0_MCHBAR)	00000000h
E4FCh	4	ECC Inject Count (ECC_INJECT_COUNT_0_0_0_MCHBAR)	FFFFFFFFh
E5FCh	4	Miscellaneous Control Register (MCMNTS_SPARE_0_0_0_MCHBAR)	00000000h

3.2.2 GFX VT Range Base Address Register (GFXVTBAR_0_0_0_MCHBAR_NCU) — Offset 5400h

This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VT configuration space is disabled and must be enabled by writing a 1 to GFX-VTBAREN.

All the bits in this register are locked in LT mode.

BIOS programs this register after which the register cannot be altered.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5400h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:12	00000000h RW	**GFX VT Base Address (GFXVTBAR):** This field corresponds to bits 41 to 12 of the base address GFX-VT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 4TB of addressable memory space. System Software uses this base address to program the GFX-VT register set. All the Bits in this register are locked in LT mode.
11:1	0h RO	**Reserved**
0	0h RW/L	**GFX VT BAR Enable (GFXVTBAREN):** 0: GFX-VTBAR is disabled and does not claim any memory 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.VTDD

3.2.3 VT DMI PEG VC0 Range Base Address Register (VTDPVC0BAR_0_0_0_MCHBAR_NCU) — Offset 5410h

This is the base address for the DMI/PEG VC0 configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the DMI/PEG VC0 configuration space is disabled and must be enabled by writing a 1 to VC0BAREN.

All the bits in this register are locked in LT mode.

BIOS programs this register after which the register cannot be altered.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5410h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:12	00000000h RW	**VT VC0 Base Address (VTVC0BAR):** This field corresponds to bits 41 to 12 of the base address DMI/PEG VC0 configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 4TB of addressable memory space. System Software uses this base address to program the DMI/PEG VC0 register set. All the Bits in this register are locked in LT mode.
11:1	0h RO	**Reserved**
0	0h RW/L	**VT VC0 BAR Enable (VTVC0BAREN):** 0: VC0BAR is disabled and does not claim any memory 1: VC0BAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.VTDD

3.2.4 IMR0 BASE (IMR0BASE_0_0_0_MCHBAR_IMPH) — Offset 7900h

Specifies bits 41:10 of the start address of IMR0 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR0_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7900h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR0 BASE (IMR0_BASE):** IMR0_BASE - Specifies bits 41:10 of the start address of IMR0 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR0_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.5 IMR0 MASK (IMR0MASK_0_0_0_MCHBAR_IMPH) — Offset 7904h

IMR0MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR0BASE, IMR0RAC, and IMR0WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR0RAC and IMR0WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7904h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR0 MASK (IMR0_MASK):** IMR0_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR0BASE[31:0] value. A match indicates that the incoming address falls within the IMR0 region.

3.2.6 IMR1 BASE (IMR1BASE_0_0_0_MCHBAR_IMPH) — Offset 7920h

Specifies bits 41:10 of the start address of IMR1 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR1_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR1 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7920h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR1 BASE (IMR1_BASE):** IMR1_BASE - Specifies bits 41:10 of the start address of IMR1 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR1_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.7 IMR1 MASK (IMR1MASK_0_0_0_MCHBAR_IMPH) — Offset 7924h

IMR1MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR1BASE, IMR1RAC, and IMR1WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR1RAC and IMR1WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7924h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR1 MASK (IMR1_MASK):** IMR1_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR1BASE[31:0] value. A match indicates that the incoming address falls within the IMR1 region.

3.2.8 IMR2 BASE (IMR2BASE_0_0_0_MCHBAR_IMPH) — Offset 7940h

Specifies bits 41:10 of the start address of IMR2 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR2_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR2 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7940h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR2 BASE (IMR2_BASE):** IMR2_BASE - Specifies bits 41:10 of the start address of IMR2 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR2_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.9 IMR2 MASK (IMR2MASK_0_0_0_MCHBAR_IMPH) — Offset 7944h

IMR2MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR2BASE, IMR2RAC, and IMR2WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR2RAC and IMR2WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7944h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR2 MASK (IMR2_MASK):** IMR2_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR2BASE[31:0] value. A match indicates that the incoming address falls within the IMR2 region.

3.2.10 IMR3 BASE (IMR3BASE_0_0_0_MCHBAR_IMPH) — Offset 7960h

Specifies bits 41:10 of the start address of IMR3 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR3_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR3 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7960h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR3 BASE (IMR3_BASE):** IMR3_BASE - Specifies bits 41:10 of the start address of IMR3 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR3_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.11 IMR3 MASK (IMR3MASK_0_0_0_MCHBAR_IMPH) — Offset 7964h

IMR3MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR3BASE, IMR3RAC, and IMR3WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR3RAC and IMR3WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7964h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR3 MASK (IMR3_MASK):** IMR3_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR3BASE[31:0] value. A match indicates that the incoming address falls within the IMR3 region.

3.2.12 IMR4 BASE (IMR4BASE_0_0_0_MCHBAR_IMPH) — Offset 7980h

Specifies bits 41:10 of the start address of IMR4 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR4_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR4 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7980h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR4 BASE (IMR4_BASE):** IMR4_BASE - Specifies bits 41:10 of the start address of IMR4 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR4_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.13 IMR4 MASK (IMR4MASK_0_0_0_MCHBAR_IMPH) — Offset 7984h

IMR4MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR4BASE, IMR4RAC, and IMR4WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR4RAC and IMR4WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7984h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR4 MASK (IMR4_MASK):** IMR4_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR4BASE[31:0] value. A match indicates that the incoming address falls within the IMR4 region.

3.2.14 IMR5 BASE (IMR5BASE_0_0_0_MCHBAR_IMPH) — Offset 79A0h

Specifies bits 41:10 of the start address of IMR5 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR5_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR5 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 79A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR5 BASE (IMR5_BASE):** IMR5_BASE - Specifies bits 41:10 of the start address of IMR5 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR5_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.15 IMR5 MASK (IMR5MASK_0_0_0_MCHBAR_IMPH) — Offset 79A4h

IMR5MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR5BASE, IMR5RAC, and IMR5WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR5RAC and IMR5WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 79A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR5 MASK (IMR5_MASK):** IMR5_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR5BASE[31:0] value. A match indicates that the incoming address falls within the IMR5 region.

3.2.16 IMR6 BASE (IMR6BASE_0_0_0_MCHBAR_IMPH) — Offset 79C0h

Specifies bits 41:10 of the start address of IMR6 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR6_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR6 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 79C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR6 BASE (IMR6_BASE):** IMR6_BASE - Specifies bits 41:10 of the start address of IMR6 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR6_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.17 IMR6 MASK (IMR6MASK_0_0_0_MCHBAR_IMPH) — Offset 79C4h

IMR6MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR6BASE, IMR6RAC, and IMR6WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR6RAC and IMR6WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 79C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR6 MASK (IMR6_MASK):** IMR6_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR6BASE[31:0] value. A match indicates that the incoming address falls within the IMR6 region.

3.2.18 IMR7 BASE (IMR7BASE_0_0_0_MCHBAR_IMPH) — Offset 79E0h

Specifies bits 41:10 of the start address of IMR7 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR7_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR7 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 79E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR7 BASE (IMR7_BASE):** IMR7_BASE - Specifies bits 41:10 of the start address of IMR7 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR7_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.19 IMR7 MASK (IMR7MASK_0_0_0_MCHBAR_IMPH) — Offset 79E4h

IMR7MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR7BASE, IMR7RAC, and IMR7WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR7RAC and IMR7WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 79E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR7 MASK (IMR7_MASK):** IMR7_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR7BASE[31:0] value. A match indicates that the incoming address falls within the IMR7 region.

3.2.20 IMR8 BASE (IMR8BASE_0_0_0_MCHBAR_IMPH) — Offset 7A00h

Specifies bits 41:10 of the start address of IMR8 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR8_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR8 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR8 BASE (IMR8_BASE):** IMR8_BASE - Specifies bits 41:10 of the start address of IMR8 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR8_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.21 IMR8 MASK (IMR8MASK_0_0_0_MCHBAR_IMPH) — Offset 7A04h

IMR8MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR8BASE, IMR8RAC, and IMR8WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR8RAC and IMR8WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR8 MASK (IMR8_MASK):** IMR8_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR8BASE[31:0] value. A match indicates that the incoming address falls within the IMR8 region.

3.2.22 IMR9 BASE (IMR9BASE_0_0_0_MCHBAR_IMPH) — Offset 7A20h

Specifies bits 41:10 of the start address of IMR9 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR9_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR9 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR9 BASE (IMR9_BASE):** IMR9_BASE - Specifies bits 41:10 of the start address of IMR9 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR9_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.23 IMR9 MASK (IMR9MASK_0_0_0_MCHBAR_IMPH) — Offset 7A24h

IMR9MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR9BASE, IMR9RAC, and IMR9WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR9RAC and IMR9WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR9 MASK (IMR9_MASK):** IMR9_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR9BASE[31:0] value. A match indicates that the incoming address falls within the IMR9 region.

3.2.24 IMR10 BASE (IMR10BASE_0_0_0_MCHBAR_IMPH) — Offset 7A40h

Specifies bits 41:10 of the start address of IMR10 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR10_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR10 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR10 BASE (IMR10_BASE):** IMR10_BASE - Specifies bits 41:10 of the start address of IMR10 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR10_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.25 IMR10 MASK (IMR10MASK_0_0_0_MCHBAR_IMPH) — Offset 7A44h

IMR10MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR10BASE, IMR10RAC, and IMR10WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR10RAC and IMR10WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR10 MASK (IMR10_MASK):** IMR10_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR10BASE[31:0] value. A match indicates that the incoming address falls within the IMR10 region.

3.2.26 IMR11 BASE (IMR11BASE_0_0_0_MCHBAR_IMPH) — Offset 7A60h

Specifies bits 41:10 of the start address of IMR11 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR11_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR11 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR11 BASE (IMR11_BASE):** IMR11_BASE - Specifies bits 41:10 of the start address of IMR11 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR11_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.27 IMR11 MASK (IMR11MASK_0_0_0_MCHBAR_IMPH) — Offset 7A64h

IMR11MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR11BASE, IMR11RAC, and IMR11WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR11RAC and IMR11WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR11 MASK (IMR11_MASK):** IMR11_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR11BASE[31:0] value. A match indicates that the incoming address falls within the IMR11 region.

3.2.28 IMR12 BASE (IMR12BASE_0_0_0_MCHBAR_IMPH) — Offset 7A80h

Specifies bits 41:10 of the start address of IMR12 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR12_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR12 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR12 BASE (IMR12_BASE):** IMR12_BASE - Specifies bits 41:10 of the start address of IMR12 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR12_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.29 IMR12 MASK (IMR12MASK_0_0_0_MCHBAR_IMPH) — Offset 7A84h

IMR12MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR12BASE, IMR12RAC, and IMR12WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR12RAC and IMR12WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7A84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR12 MASK (IMR12_MASK):** IMR12_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR12BASE[31:0] value. A match indicates that the incoming address falls within the IMR12 region.

3.2.30 IMR13 BASE (IMR13BASE_0_0_0_MCHBAR_IMPH) — Offset 7AA0h

Specifies bits 41:10 of the start address of IMR13 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR13_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR13 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7AA0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR13 BASE (IMR13_BASE):** IMR13_BASE - Specifies bits 41:10 of the start address of IMR13 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR13_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.31 IMR13 MASK (IMR13MASK_0_0_0_MCHBAR_IMPH) — Offset 7AA4h

IMR13MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR13BASE, IMR13RAC, and IMR13WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR13RAC and IMR13WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7AA4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR13 MASK (IMR13_MASK):** IMR13_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR13BASE[31:0] value. A match indicates that the incoming address falls within the IMR13 region.

3.2.32 IMR14 BASE (IMR14BASE_0_0_0_MCHBAR_IMPH) — Offset 7AC0h

Specifies bits 41:10 of the start address of IMR14 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR14_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR14 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7AC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR14 BASE (IMR14_BASE):** IMR14_BASE - Specifies bits 41:10 of the start address of IMR14 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR14_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.33 IMR14 MASK (IMR14MASK_0_0_0_MCHBAR_IMPH) — Offset 7AC4h

IMR14MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR14BASE, IMR14RAC, and IMR14WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR14RAC and IMR14WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7AC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR14 MASK (IMR14_MASK):** IMR14_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR14BASE[31:0] value. A match indicates that the incoming address falls within the IMR14 region.

3.2.34 IMR15 BASE (IMR15BASE_0_0_0_MCHBAR_IMPH) — Offset 7AF0h

Specifies bits 41:10 of the start address of IMR15 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR15_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR15 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7AF0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR15 BASE (IMR15_BASE):** IMR15_BASE - Specifies bits 41:10 of the start address of IMR15 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR15_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.35 IMR15 MASK (IMR15MASK_0_0_0_MCHBAR_IMPH) — Offset 7AF4h

IMR15MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR15BASE, IMR15RAC, and IMR15WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR15RAC and IMR15WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7AF4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR15 MASK (IMR15_MASK):** IMR15_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR15BASE[31:0] value. A match indicates that the incoming address falls within the IMR15 region.

3.2.36 IMR16 BASE (IMR16BASE_0_0_0_MCHBAR_IMPH) — Offset 7B10h

Specifies bits 41:10 of the start address of IMR16 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR16_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR16 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7B10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR16 BASE (IMR16_BASE):** IMR16_BASE - Specifies bits 41:10 of the start address of IMR16 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR16_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.37 IMR16 MASK (IMR16MASK_0_0_0_MCHBAR_IMPH) — Offset 7B14h

IMR16MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR16BASE, IMR16RAC, and IMR16WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR16RAC and IMR16WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7B14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR16 MASK (IMR16_MASK):** IMR16_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR16BASE[31:0] value. A match indicates that the incoming address falls within the IMR16 region.

3.2.38 IMR17 BASE (IMR17BASE_0_0_0_MCHBAR_IMPH) — Offset 7B30h

Specifies bits 41:10 of the start address of IMR17 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR17_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR17 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7B30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000 h RW	**IMR17 BASE (IMR17_BASE):** IMR17_BASE - Specifies bits 41:10 of the start address of IMR17 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR17_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.39 IMR17 MASK (IMR17MASK_0_0_0_MCHBAR_IMPH) — Offset 7B34h

IMR17MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR17BASE, IMR17RAC, and IMR17WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR17RAC and IMR17WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7B34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000 h RW	**IMR17 MASK (IMR17_MASK):** IMR17_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR17BASE[31:0] value. A match indicates that the incoming address falls within the IMR17 region.

3.2.40 IMR18 BASE (IMR18BASE_0_0_0_MCHBAR_IMPH) — Offset 7B50h

Specifies bits 41:10 of the start address of IMR18 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR18_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR18 defined region.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7B50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR18 BASE (IMR18_BASE):** IMR18_BASE - Specifies bits 41:10 of the start address of IMR18 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR18_MASK[31:0] applied to bits 41:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

3.2.41 IMR18 MASK (IMR18MASK_0_0_0_MCHBAR_IMPH) — Offset 7B54h

IMR18MASK_0_0_0_MCHBAR_IMPH: This register, along with IMR18BASE, IMR18RAC, and IMR18WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the IOP, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR18RAC and IMR18WAC registers

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7B54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR18 MASK (IMR18_MASK):** IMR18_MASK - These bits are ANDed with bits 41:10 of the incoming address to determine if the combined result matches the IMR18BASE[31:0] value. A match indicates that the incoming address falls within the IMR18 region.

3.2.42 Inter-Channel Decode Parameters (MAD_INTER_CHANNEL_0_0_0_MCHBAR) — Offset D800h

This register holds parameters used by the channel decode stage.

It defines virtual channel L mapping, as well as channel S size.

Also defined is the DDR type installed in the system (what DDR/LPDDR type is used).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D800h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Half Cacheline Mode (HALFCACHELINEMODE):** In this mode, the memory controller operates at 32B data chunkss.
30:29	0h RO	**Reserved**
28:27	0h RW	**Channel Width (CH_WIDTH):** This field defines the width of DRAM Channel 00b: x16 01b: x32 10b: x64 11b: Reserved
26:20	0h RO	**Reserved**
19:12	00h RW	**Channel S Size (CH_S_SIZE):** Channel S size in multiples of 0.5GB. Supported range is 0GB - 64GB.
11:5	0h RO	**Reserved**
4	0h RW	**Channel L Mapping (CH_L_MAP):** Channel L mapping to physical channel. 0b: Channel 0 1b: Channel 1
3	0h RO	**Reserved**
2:0	0h RW	**DDR Type (DDR_TYPE):** Defines the DDR type: 0: DDR4 1: DDR5 2: LPDDR5 3: LPDDR4 4-7: Reserved

3.2.43 Intra-Channel 0 Decode Parameters (MAD_INTRA_CH0_0_0_0_MCHBAR) — Offset D804h

This register holds parameters used by the DRAM decode stage.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D804h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**CRC Mode Enable (CRC):** 0b: Disabled 1b: Enabled
13:12	0h RW	**ECC Channel Configuration (ECC):** 0: No ECC active in the channel. 1: ECC is active in IO, ECC logic is not active. 2: ECC is disabled in IO, but ECC logic is enabled. 3: ECC active in both IO and ECC logic. Notes: • This field must be programmed identically for all populated channels. • In a system with ECC this field must be programmed to 1 during training and then 3 before transitioning from training mode to Normal mode.
11:9	0h RO	**Reserved**
8	0h RW	**Enhanced Interleaving Mode (EIM):** 0b: Disabled 1b: Enabled
7:1	0h RO	**Reserved**
0	0h RW	**DIMM L Mapping (DIMM_L_MAP):** Virtual DIMM L mapping to physical DIMM 0b: DIMM0 1b: DIMM1

3.2.44 Intra-Channel 1 Decode Parameters (MAD_INTRA_CH1_0_0_0_MCHBAR) — Offset D808h

This register holds parameters used by the DRAM decode stage.

Note: Bit definitions are the same as MAD_INTRA_CH0_0_0_0_MCHBAR, offset D804h.

3.2.45 Channel 0 DIMM Characteristics (MAD_DIMM_CH0_0_0_0_MCHBAR) — Offset D80Ch

This register defines the channel DIMM characteristics - number of DIMMs, number of ranks, size and type.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D80Ch	10001800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Decoder Extended Bank Hashing (DECODER_EBH):** Enable address decoder Extended bank hashing. Bit 0: Enable XaB Bit 1: Enable XbB
29:28	1h RW	**BG0 Bit Options (BG0_BIT_OPTIONS):** depending on value, BG[0] will be replaced with C[5] or C[6]. **DDR5:** 0: CAS[5] = zoneaddr[8], BG[0] = zoneaddr[6] 1: CAS[5] = zoneaddr[6], BG[0] = zoneaddr[8] 2: CAS[6] = zoneaddr[6], BG[0] = zoneaddr[9] 3: Reserved **DDR4:** 0: CAS[5] = zoneaddr[9], BG[0] = zoneaddr[6] 1: CAS[5] = zoneaddr[6], BG[0] = zoneaddr[9] 2: CAS[6] = zoneaddr[6], BG[0] = zoneaddr[10] 3: Reserved for LPDDR5 BGMode only- 1: Swap BG[1]/CAS[6] else: keep original BG[1]/CAS[6] 3: Reserved
27:26	0h RW	**DIMM S Number of Ranks (DSNOR):** DIMM S number of ranks 0b: 1 Rank 1b: 2 Ranks
25:24	0h RW	**DIMM S Width (DSW):** Width of DDR chips 0: X8 chips 1: X16 chips 2: X32 chips 3: Reserved
23	0h RO	**Reserved**
22:16	00h RW	**DIMM S Size (DIMM_S_SIZE):** Size of DIMM S in 0.5GB multiples.
15:13	0h RO	**Reserved**
12	1h RW	**DDR5 DIMM L capacity 8Gb (DDR5_DL_8GB):** 0: DDR5 DIMM L capacity is more than 8Gb 1: DDR5 DIMM L capacity is 8Gb
11	1h RW	**DDR5 DIMM S capacity 8Gb (DDR5_DS_8GB):** 0: DDR5 DIMM S capacity is more than 8Gb 1: DDR5 DIMM S capacity is 8Gb

Bit Range	Default & Access	Field Name (ID): Description
10:9	0h RW	**DIMM L Number of Ranks (DLNOR):** 0: 1 Rank 1: 2 Ranks In ERM (enhanced rank mode): 2: 3 ranks 3: 4 ranks
8:7	0h RW	**DIMM L Width (DLW):** DIMM L width of DDR chips 0: X8 chips 1: X16 chips 2: X32 chips 3: Reserved
6:0	00h RW	**DIMM L Size (DIMM_L_SIZE):** Size of DIMM L in 0.5GB multiples

3.2.46 Channel 1 DIMM Characteristics (MAD_DIMM_CH1_0_0_0_MCHBAR) — Offset D810h

This register defines the channel DIMM characteristics - number of DIMMs, number of ranks, size and type.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D810h	10001800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Decoder Extended Bank Hashing (DECODER_EBH):** Enable address decoder Extended bank hashing. Bit 0: Enable XaB Bit 1: Enable XbB
29:28	1h RW	**BG0 Bit Options (BG0_BIT_OPTIONS):** depending on value, BG[0] will be replaced with C[5] or C[6]. **DDR5:** 0: CAS[5] = zoneaddr[8], BG[0] = zoneaddr[6] 1: CAS[5] = zoneaddr[6], BG[0] = zoneaddr[8] 2: CAS[6] = zoneaddr[6], BG[0] = zoneaddr[9] 3: Reserved **DDR4:** 0: CAS[5] = zoneaddr[9], BG[0] = zoneaddr[6] 1: CAS[5] = zoneaddr[6], BG[0] = zoneaddr[9] 2: CAS[6] = zoneaddr[6], BG[0] = zoneaddr[10] 3: Reserved
27:26	0h RW	**DIMM S Number of Ranks (DSNOR):** DIMM S number of ranks 0b: 1 Rank 1b: 2 Ranks

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**DIMM S Width (DSW):** Width of DDR chips 0: X8 chips 1: X16 chips 2: X32 chips 3: Reserved
23	0h RO	**Reserved**
22:16	00h RW	**DIMM S Size (DIMM_S_SIZE):** Size of DIMM S in 0.5GB multiples.
15:13	0h RO	**Reserved**
12	1h RW	**DDR5 DIMM L capacity 8Gb (DDR5_DL_8GB):** 0: DDR5 DIMM L capacity is more than 8Gb 1: DDR5 DIMM L capacity is 8Gb
11	1h RW	**DDR5 DIMM S capacity 8Gb (DDR5_DS_8GB):** 0: DDR5 DIMM S capacity is more than 8Gb 1: DDR5 DIMM S capacity is 8Gb
10:9	0h RW	**DIMM L Number of Ranks (DLNOR):** 0: 1 Rank 1: 2 Ranks In ERM (enhanced rank mode): 2: 3 ranks 3: 4 ranks
8:7	0h RW	**DIMM L Width (DLW):** DIMM L width of DDR chips 0: X8 chips 1: X16 chips 2: X32 chips 3: Reserved
6:0	00h RW	**DIMM L Size (DIMM_L_SIZE):** Size of DIMM L in 0.5GB multiples

3.2.47 Channel Hash (CHANNEL_HASH_0_0_0_MCHBAR) — Offset D824h

This register defines the MC channel selection function.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D824h	03000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Hash Mode (HASH_MODE):** Encoding: 0: Use address bit-6 for channel selection. 1: Use the channel hash function as defined in the other fields of this register.
27	0h RO	**Reserved**
26:24	3h RW	**Hash LSB Mask Bit (HASH_LSB_MASK_BIT):** This field specifies the MC Channel interleave bit. The following encoding is used: 0: Addr[6] 1: Addr[7] 2: Addr[8] 3: Addr[9] 4: Addr[10] 5: Addr[11] 6: Addr[12] 7: Addr[13] For example, setting this field to 2 will interleave the channels at a 4 cacheline granularity. BIOS should set this field same as the lowest selected bit in the Mask field of this register. Note that if the Mask field does not include the corresponding interleave bit, it will still be included in the XOR function by the MC decoding logic.
23:20	0h RO	**Reserved**
19:6	0000h RW	**Hash Mask (HASH_MASK):** The 14-bit mask corresponds to memory request Addr[19:6]. Setting a mask bit to 1 will include that particular address bit in the channel XOR function. For example, if the mask is set to 0C04h, then Channel = Addr[17] Addr[16] Addr[8]
5:0	0h RO	**Reserved**

3.2.48 Channel Enhanced Hash (CHANNEL_EHASH_0_0_0_MCHBAR) — Offset D828h

This register defines the MC Enhanced channel selection function.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D828h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Sub Channels EHASH Mode (EHASH_MODE):** Encoding address bit for sub channel selection (LPDDR): 0: Use address bit-6 for sub channel selection. 1: Use the channel Ehash function as defined in the other fields of this register This mode Should be only used when ther eare 2 Sub-channels per channel (LPDDR)
27	0h RO	**Reserved**
26:24	0h RW	**Enhanced Hash LSB Mask Bit (EHASH_LSB_MASK_BIT):** This specifies the MC Enhanced Channel interleave bit. The following encoding is used: • 000b: Addr[6] • 001b: Addr[7] • 010b: Addr[8] • 011b: Addr[9] • 100b: Addr[10] • 101b: Addr[11] • 110b: Addr[12] • 111b: Addr[13] For example, setting this field to 10b will interleave the sub channels at a 4 cache line granularity. BIOS should set this field same as the lowest selected bit in the Mask field of this register. Note that if the Mask field does not include the corresponding interleave bit, it will still be included in the XOR function by the MC decoding logic. The addresses above refer to channel addresses. When both channels are populated with sub-channels, addresses in this field that are higher than the HASH_LSB_MASK_BIT (defined in CHANNEL_HASH register) are one bit higher in physical address. Examples: • HASH_LSB_MASK_BIT = 0x2: physical Addr[8] • EHASH_LSB_MASK_BIT = 0x2: channel address[8], physical address [9]
23:20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19:6	0000h RW	**Enhanced Hash Mask (EHASH_MASK):** The 14 bit mask corresponds to memory request Addr[19:6]. Setting a mask bit to 1 will include that particular address bit in the channel XOR function. For example, if the mask is set to 14'h0C04, then Channel = Addr[17] Addr[16] Addr[8] The addresses above refer to channel addresses. When both channels are populated with sub-channels, addresses in this field that are higher than the HASH_LSB_MASK_BIT (defined in CHANNEL_HASH register) are one bit higher in physical address. Examples: • HASH_LSB_MASK_BIT = 0x2: physical Addr[8] • EHASH_LSB_MASK_BIT=0x2: channel address[8], physical address [9]
5:0	0h RO	**Reserved**

3.2.49 Memory Request Counters Configuration (PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR) — Offset D83Ch

Configuration register for PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1:0] counters.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D83Ch	00010820h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:15	02h RW	**Memory Source ID3 (CMI_SOURCE_ID3):** Holds 1 of 2 CMI Source IDs that will increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1] counter. When a new memory request enters memory controller that has a Source ID matching either CMI_Source_ID2 or CMI_Source_ID3 the counter will be incremented by 1. The default is the CMI Source ID of IOP (IO Port).
14:10	02h RW	**Memory Source ID2 (CMI_SOURCE_ID2):** Holds 1 of 2 CMI Source IDs that will increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1] counter. When a new memory request enters memory controller that has a Source ID matching either CMI_Source_ID2 or CMI_Source_ID3 the counter will be incremented by 1. The default is the CMI Source ID of IOP (IO Port).

Bit Range	Default & Access	Field Name (ID): Description
9:5	01h RW	**Memory Source ID1 (CMI_SOURCE_ID1):** Holds 1 of 2 CMI Source IDs that increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0] counter. When a new memory request enters the memory controller that has a Source ID matching either CMI_Source_ID0 or CMI_Source_ID1 the counter is incremented by 1. The default is the CMI Source ID of IDP1 (IDI Port 1).
4:0	00h RW	**Memory Source ID0 (CMI_SOURCE_ID0):** Holds 1 of 2 CMI Source IDs that increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0] counter. When a new memory request enters MC that has a Source ID matching either CMI_Source_ID0 or CMI_Source_ID1 the counter will be incremented by 1. The default is the Memory Source ID of IDP0 (IDI Port 0).

3.2.50 Memory Request Global Counter (PWM_TOTAL_REQCOUNT_0_0_0_MCHBAR) — Offset D840h

Counts every 64B memory read and write request entering the Memory Controller to DRAM (sum of all channels).

Each write request counts as a new request incrementing this counter.

However, same-cache-line write requests (both full and partial) are combined to a single 64-byte data transfer to DRAM.

Therefore multiplying the number of requests by 64-bytes will lead to inaccurate memory bandwidth.

The inaccuracy is proportional to the number of same-cache-line writes.

If a SOC has multiple MCs instantiated, all instances of this counter will need to be added together to get total memory request bandwidth.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D840h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RW/V	**Request Count (COUNT):** Count of the total number of 64B CMI read and write requests entering this MC.

3.2.51 Memory Request Counter 0 (PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0]) — Offset D848h

Counts every 64B memory read and write request entering the Memory Controller to DRAM (sum of all channels) from up to two programmable CMI Source IDs, contained in PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR register. Each write request counts as a new request incrementing this counter. However, same-cache-line write requests (both full and partial) are combined to a single 64-byte data transfer to DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate memory bandwidth. The inaccuracy is proportional to the number of same-cache-line writes. If a SOC has multiple MCs instantiated all instances of this counter will need to be added together to get the sum of the requests from the programmable sources.

Note: There are 2 instances of this register. The offset between instances is 8.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D848h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**Request Count (COUNT):** Counts the 64B memory read and write requests entering this memory controller from up to two programmable memory Source IDs, contained in PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR register.

3.2.52 RdCAS Counter (PWM_RDCAS_COUNT_0_0_0_MCHBAR) — Offset D858h

Counts every read (RdCAS) issued by the Memory Controller to DRAM (sum of all channels). All requests result in 64-byte data transfers from DRAM. Use for accurate memory bandwidth calculations.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D858h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**RdCAS Count (COUNT):** Number of accesses

3.2.53 Self Refresh Mode Control (PM_SREF_CONFIG_0_0_0_MCHBAR) — Offset D860h

Defines if and when DDR can go into Self Refresh

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D860h	00000200h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0200h RW/V	**Idle Timer (IDLE_TIMER):** This value is used when the SREF_enable field is set. It defines the number of cycles that there should not be any transaction in order to enter self-refresh. Supported range is 512 to 64K-1

3.2.54 Address Compare for ECC Error Inject (ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR) — Offset D888h

Error injection is issued when ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR[32:0] == ADDR[38:6] and ECC_INJ_ADDR_MASK_0_0_0_MCHBAR[32:0]

For Memory Controller 1 (MC1) - Please refer to doc #655741 for details.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D888h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:33	0h RO	**Reserved**
32:0	000000000h RW	**ADDRESS:** Inject error when ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR[32:0] == ADDR[38:6] and ECC_INJ_ADDR_MASK_0_0_0_MCHBAR[31:0]

3.2.55 Remap Base (REMAPBASE_0_0_0_MCHBAR) — Offset D890h

The value in this register defines the lower boundary of the Remap window.

The Remap window is inclusive of this address.

In the decoder A[19:0] of the Remap Base Address are assumed to be 0's.

Thus the bottom of the defined memory range will be aligned to a 1MB boundary.

When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled.

These bits are Intel TXT lockable.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D890h	0000007FFFF00000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
38:20	7FFFFh RW	**Remap Base Address (REMAPBASE):** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder Address[19:0] of the Remap Base Address are assumed to be 0's. Thus the bottom of the defined memory range will be aligned to a 1MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled. These bits are Intel TXT lockable.
19:0	0h RO	**Reserved**

3.2.56 Remap Limit (REMAPLIMIT_0_0_0_MCHBAR) — Offset D898h

The value in this register defines the upper boundary of the Remap window.

The Remap window is inclusive of this address.

In the decoder Address[19:0] of the Remap Limit Address are assumed to be F's.

Thus the top of the defined range will be one byte less than a 1MB boundary.

When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled.

These Bits are Intel TXT lockable.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D898h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	00000h RW	**Remap Limit (REMAPLMT):** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder Address[19:0] of the Remap Limit Address are assumed to be F's. Thus the top of the defined range will be one byte less than a 1MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. These Bits are Intel TXT lockable.
19:0	0h RO	**Reserved**

3.2.57 WrCAS Counter (PWM_WRCAS_COUNT_0_0_0_MCHBAR) — Offset D8A0h

Counts every write (WrCAS) issued by the Memory Controller to DRAM (sum of all channels).

All requests result in 64-byte data transfers from DRAM. Use for accurate memory bandwidth calculations.

Note: Bit definitions are the same as PWM_RDCAS_COUNT_0_0_0_MCHBAR, offset D858h.

3.2.58 Command Counter (PWM_COMMAND_COUNT_0_0_0_MCHBAR) — Offset D8A8h

Request counter used by the PCU for estimation of MC & MCIO power consumption and its sources.

There are 3 registers for sources and three registers for MC Operations.

Sources:

- GT
- IA Cores
- IO
- MC Operations:
- RD data
- WR data
- Command

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D8A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**Command Counter (COUNT):** Number of accesses.

3.2.59 Address Mask for ECC Error Inject (ECC_INJ_ADDR_MASK_0_0_0_MCHBAR) — Offset D958h

Error injection is issued when ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR[32:0] = ADDR[38:6] AND ECC_INJ_ADDR_MASK_0_0_0_MCHBAR[32:0].

For Memory Controller 1 (MC1) - Please refer to doc #655741 for details.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D958h	00000001FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:33	0h RO	**Reserved**
32:0	1FFFFFFFFh RW	**ADDRESS:** Inject error when ECC_Inj_Addr_Compare[32:0] = ADDR[38:6] AND ECC_Inj_Addr_Mask[32:0]

3.2.60 MAD MC HASH 0 0 0 MCHBAR (MAD_MC_HASH_0_0_0_MCHBAR) — Offset D9B8h

This register holds parameters used by the CMI slice selection. transforming from HPA (Host Physical Address)-->CCA (CMI compresed address)

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9B8h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**Stacked Mode (STACKED_MODE):** Working in stacked mode, this MC handles the high address bits and will decrement Zone1_start/2 from the recived address
12:4	000h RW	**Zone1 start (ZONE1_START):** Address in GB of the non-interleaved portion of non-symmetric memory. i.e. in case slice 0 has 32 GB and slice 1 has 8 G, then start of non-symmetric memory is 16GB so Zone1_start=0x10. if the memory is symmetric, Zone1_start is set to memory size (i.e. for total capacity of 64GB Zone1_start=0x40)

Bit Range	Default & Access	Field Name (ID): Description
3:1	3h RW	**Hash LSB (HASH_LSB):** LSB used in MCI hashing between the two MCs. the Hash bit should be removed from the address in order to get a conseutive address in the MC space. Encoding: 000 - address bit 6 001 - address bit 7 ... 111 - address bit 13
0	0h RW	**Hash enabled (HASH_ENABLED):** Hasing in Zone0 between the two MC is enabled

3.2.61 PMON GLOBAL CONTROL 0 0 0 MCHBAR (PMON_GLOBAL_CONTROL_0_0_0_MCHBAR) — Offset D9C0h

Configuration register for chasis PMON. no central Pmon unit implemented so this register is also a part of MC.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW/V	**Global reset ctrs (GLOBAL_RESET_CTRS):** when set to 1, the counter registers of all units will be reseted to 0. This bit is self clearing.
1	0h RW/V	**Global reset ctrl (GLOBAL_RESET_CTRL):** when set to 1, the counter control registers of all pmons will be reseted to 0. This bit is self clearing.
0	0h RW	**global freeze (GLOBAL_FREEZE):** Freeze. if set to 1, the counters in all units will stop counting and keep their value.

3.2.62 PMON UNIT CONTROL 0 0 0 MCHBAR (PMON_UNIT_CONTROL_0_0_0_MCHBAR) — Offset D9C4h

Configuration register for PMON Unit (holds several coutners)

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RW/V	**reset ctrs (RESET_CTRS):** when set to 1, the counter registers will be reseted to 0. This bit is self clearing.
8	0h RW/V	**reset ctrl (RESET_CTRL):** when set to 1, the counter control registers will be reseted to 0. This bit is self clearing.
7:1	0h RO	**Reserved**
0	0h RW	**frz reg (FRZ):** Freeze. if set to 1, the counters in this unit will stop counting and keep their value.

3.2.63 PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0]) — Offset D9D0h

Configuration register for PMON_COUNTER_DATA

Note: There are 5 instances of this register. The offset between instances is 4.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/V	**edge det (EDGE_DET):** Edge Detect. when set to 1, rather than measuring the event in each cycle it's asserted, the corrosponding counter will increment when a 0 to 1 transition (i.e. rising edge) is detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/V	**rst reg (RST):** Reset when set to 1, the corrosponding coutner will be cleared to 0. this bit is self clearing
16:12	0h RO	**Reserved**
11:8	0h RW/V	**ch mask (CH_MASK):** select which channel or sub channel is counted, or both. In channel events bits [9:8] (lsb) mask the channel, in sub-channel events bits [11:8] mask [ch1-subch1, ch1-subch0, ch0-subch1, ch1-subch0]. To mask out a channel (or sub channel) set the according bit to 0x1. Events that can increment by more than 1 per cycle should set mask to 0x0.
7:0	00h RW/V	**ev sel (EV_SEL):** Event select. Select which of the available events should be recorded in the paired data register. additional bits in the control register may also be required to select from the available events. 0x0 --> disable counter 0x1 --> count local clock ticks

3.2.64 PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[0]) — Offset D9E8h

performance monitor counter

Note: There are 5 instances of this register. The offset between instances is 8.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D9E8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RW/V	**event count (EVENT_COUNT):** number of event occurrences

3.2.65 OS Telemetry Control (OS_TELEMETRY_CONTROL_0_0_0_MCHBAR) — Offset DA10h

This Register enables telemetry the following counters:

- PWM_DDR_SUBCHx_ACT_COUNTER_0_0_0_MCHBAR

- PWM_DDR_SUBCHx_RRDATA_COUNTER_0_0_0_MCHBAR
- PWM_DDR_SUBCHx_WRDATA_COUNTER_0_0_0_MCHBAR

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DA10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Enable OS Telemetry (ENABLEOSTELEMETRY):** Enables OS Telemetry of: • PWM_DDR_SUBCHx_ACT_COUNTER_0_0_0_MCHBAR • PWM_DDR_SUBCHx_RRDATA_COUNTER_0_0_0_MCHBAR • PWM_DDR_SUBCHx_WRDATA_COUNTER_0_0_0_MCHBAR

3.2.66 PRE Command Timing (TC_PRE_0_0_0_MCHBAR) — Offset E000h

DDR timing constraints related to PRE commands

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E000h	104070180040C008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**Reserved**
62:59	2h RW	**Derating Extensions (DERATING_EXT):** Holds LPDDR timing parameters derating tRAS, tRRD, tRP and tRCD in tCK (WCK for LPDDR5) cycles. When LPDDR is hot, this value is added to the appropriate timing parameters. For non LP devices program the field to 0. Supported range is 0-4.
58:51	08h RW	**tRCD Timing Parameter (TRCD):** Holds DDR timing parameter tRCD ACT to CAS (RD or WR) same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 8-59.

Bit Range	Default & Access	Field Name (ID): Description
50:42	01Ch RW	**tRAS Timing Parameter (TRAS):** Holds DDR timing parameter tRAS. ACT to PRE same bank minimum delay in tCK (WCK for LPDDR5) cycles. For DDR/LPDDR Supported range is 28-136
41:32	018h RW	**tWRPRE Timing Parameter (TWRPRE):** Holds DDR timing parameter tWRPRE. WR to PRE same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 18-200.
31:24	0h RO	**Reserved**
23:20	4h RW	**tPPD Timing Parameter (TPPD):** Holds DDR timing parameter tPPD. PRE/PREALL to PRE/PREALL (same rank) minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-7. Note this register is not used in DDR5
19:13	06h RW	**tRDPRE Timing Parameter (TRDPRE):** Holds DDR timing parameter tRDPRE. RD to PRE same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-32.
12:8	00h RW	**tRPab_ext Timing Parameter (TRPAB_EXT):** Holds the value of tRPab-tRPpb for LPDDR in tCK (WCK for LPDDR5) cycles. LPDDR technologies requires a longer time from PREALL to ACT vs. PRE to ACT, the offset between the two should be programmed to this field. When using DDR4 this field should be programmed to 0. For LPDDR4 the following restrictions apply: For single/dual rank sub channels tRP-tRPab_ext > 6. For three/four ranks sub channels tRP-tRPab_ext > 8. Supported range is 0-6.
7:0	08h RW	**tRP Timing Parameter (TRP):** Holds DDR timing parameter tRP (and tRCD). PRE to ACT same bank minimum delay in tCK (WCK for LPDDR5) cycles. ACT to CAS (RD or WR) same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 8-60.

3.2.67 ACT Command Timing (TC_ACT_0_0_0_MCHBAR) — Offset E008h

DDR timing constraints related to ACT commands

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E008h	18020810h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	18h RW	**tREFSBRD Timing (TREFSBRD):** Enforces minimum delay from refsb to ACT. Specified in tCK
23:22	0h RO	**Reserved**
21:15	04h RW	**tRRD Different Group (TRRD_DG):** Holds DDR timing parameter tRRD. ACT to ACT (different bank group in DDR4/DDR5) minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-32.
14:9	04h RW	**tRRD Same Group (TRRD_SG):** Holds DDR timing parameter tRRD/tRRD_L. For LPDDR4/LPDDR5 program tRRD, for DDR4/DDR5 program tRRD_L. ACT to ACT (same bank group in DDR4/DDR5) minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-32.
8:0	010h RW	**tFAW Timing Parameter (TFAW):** Holds DDR timing parameter tFAW (four activates window). In tCK (WCK for LPDDR5) cycles Supported range is 16-88.

3.2.68 RD to RD Timings (TC_RDRD_0_0_0_MCHBAR) — Offset E00Ch

DDR timing constraints related to timing between read and read transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E00Ch	04040484h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RW	**tRDRD Different DIMM (TRDRD_DD):** Minimum delay from RD to RD to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.

Bit Range	Default & Access	Field Name (ID): Description
23:16	04h RW	**tRDRD Different Rank (TRDRD_DR):** Minimum delay from RD to RD to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
15	0h RO	**Reserved**
14:8	04h RW	**tRDRD Different Group (TRDRD_DG):** LPDDR4/LPDDR5: Minimum delay from RD to RD to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to RD to different bank groups in tCK cycles. Supported range is 4-54.
7	1h RW	**Allow 2 Cycle B2B LPDDR (ALLOW_2CYC_B2B_LPDDR):** LPDDR4/LPDDR5: in MPR mode reads work on BL16. In Gear4 this means 2 DCLKs apart reads. Clearing this bit will prevent LPDDR from schedule a read 2 DCLKs after another read.
6:0	04h RW	**tRDRD Same Group (TRDRD_SG):** LPDDR4/LPDDR5: Minimum delay from RD to RD to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to RD to the same bank group in tCK cycles. Supported range is 4-54.

3.2.69 RD to WR Timings (TC_RDWR_0_0_0_MCHBAR) — Offset E010h

DDR timing constraints related to timing between read and write transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E010h	04040404h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RW	**tRDWR Different DIMM (TRDWR_DD):** Minimum delay from RD to WR to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
23:16	04h RW	**tRDWR Different Rank (TRDWR_DR):** Minimum delay from RD to WR to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
15:8	04h RW	**tRDWR Different Group (TRDWR_DG):** LPDDR4/LPDDR5: Minimum delay from RD to WR to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to WR to different bank groups in tCK cycles. Supported range is 4-54.

Bit Range	Default & Access	Field Name (ID): Description
7:0	04h RW	**tRDWR Same Group (TRDWR_SG):** LPDDR4/LPDDR5: Minimum delay from RD to WR to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to WR to the same bank group in tCK cycles. Supported range is 4-54.

3.2.70 WR to RD Timings (TC_WRRD_0_0_0_MCHBAR) — Offset E014h

DDR timing constraints related to timing between write and read transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E014h	08100804h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:25	04h RW	**tWRRD Different DIMM (TWRRD_DD):** Minimum delay from WR to RD to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
24:18	04h RW	**tWRRD Different Rank (TWRRD_DR):** Minimum delay from WR to RD to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
17:9	004h RW	**tWRRD Different Group (TWRRD_DG):** LPDDR4/LPDDR5: Minimum delay from WR to RD to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to RD to different bank groups in tCK cycles. Supported range is 4-65.
8:0	004h RW	**tWRRD Same Group (TWRRD_SG):** LPDDR4/LPDDR5: Minimum delay from WR to RD to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to RD to the same bank group in tCK cycles. Supported range is 4-145.

3.2.71 WR to WR Timings (TC_WRWR_0_0_0_MCHBAR) — Offset E018h

DDR timing constraints related to timing between write and write transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E018h	04040404h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RW	**tWRWR Different DIMM (TWRWR_DD):** Minimum delay from WR to WR to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
23	0h RO	**Reserved**
22:16	04h RW	**tWRWR Different Rank (TWRWR_DR):** Minimum delay from WR to WR to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
15	0h RO	**Reserved**
14:8	04h RW	**tWRWR Different Group (TWRWR_DG):** LPDDR4/LPDDR5: Minimum delay from WR to WR to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to WR to different bank groups in tCK cycles. Supported range is 4-54.
7	0h RO	**Reserved**
6:0	04h RW	**tWRWR Same Group (TWRWR_SG):** LPDDR4/LPDDR5: Minimum delay from WR to WR to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to WR to the same bank group in tCK cycles. Supported range is 4-54.

3.2.72 Roundtrip Latency (SC_ROUNDTRIP_LATENCY_0_0_0_MCHBAR) — Offset E020h

Read Round-trip latency per rank

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E020h	1919191919191919h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	19h RW	**Rank 7 Latency (RANK_7_LATENCY):** Latency from read command to rank 7 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 1 rank 3 (which is indicated by rank = 3 BG[1]=1) Supported range is 19-120.
55:48	19h RW	**Rank 6 Latency (RANK_6_LATENCY):** Latency from read command to rank 6 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 1 rank 2 (which is indicated by rank = 2 BG[1]=1) Supported range is 19-120.
47:40	19h RW	**Rank 5 Latency (RANK_5_LATENCY):** Latency from read command to rank 5 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 0 rank 3 (which is indicated by rank = 1 BG[1]=1) Supported range is 19-120.
39:32	19h RW	**Rank 5 Latency (RANK_4_LATENCY):** Latency from read command to rank 4 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 0 rank 2 (which is indicated by rank = 0 BG[1]=1) Supported range is 19-120.
31:24	19h RW	**Rank 3 Latency (RANK_3_LATENCY):** Latency from read command to rank 3 until first data chunk return to MC in QCLK cycles Supported range is 19-120.
23:16	19h RW	**Rank 2 Latency (RANK_2_LATENCY):** Latency from read command to rank 2 until first data chunk return to MC in QCLK cycles Supported range is 19-120.
15:8	19h RW	**Rank 1 Latency (RANK_1_LATENCY):** Latency from read command to rank 1 until first data chunk return to MC in QCLK cycles Supported range is 19-120.
7:0	19h RW	**Rank 0 Latency (RANK_0_LATENCY):** Latency from read command to rank 0 until first data chunk return to MC in QCLK cycles Supported range is 19-120.

3.2.73 ECC Error Log 0 (ECCERRLOG0_0_0_0_MCHBAR) — Offset E048h

This register logs ECC error information. Read only register/s, please refer to doc #655741 for details.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO/V/P	**Error Bank (ERRBANK):** This field holds the Bank Address of the read transaction that had the ECC error.
28:27	0h RO/V/P	**Error Rank (ERRRANK):** This field holds the Rank ID of the read transaction that had the ECC error. If ddr_1dpc_split_ranks_on_sub-channel feature is enabled then rank 1 is actually logged as rank 3.
26:24	0h RO/V/P	**Error Chunk (ERRCHUNK):** Holds the chunk number of the error stored in the register.
23:16	00h RO/V/P	**Error Syndrome (ERRSYND):** This field contains the error syndrome. A value of 0xFF indicates that the error is due to poisoning.
15:4	0h RO	**Reserved**
3	0h RO/1C/V/P	**Multi-Bit Error Overflow (MERR_OVERFLOW):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.
2	0h RO/1C/V/P	**Multi-Bit Error Status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.
1	0h RO/1C/V/P	**Correctable Single-Bit Error Overflow (CERR_OVERFLOW):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/1C/V/P	**Single Bit Error Status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.

3.2.74 ECC Error Log 0 (ECCERRLOG1_0_0_0_MCHBAR) — Offset E04Ch

This register logs ECC error information. Read only register/s, please refer to doc #655741 for details.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E04Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO/V/P	**Error Bank Group (ERRBANKGROUP):** This field holds the DRAM bank group address of the read transaction that had the ECC error.
28:18	000h RO/V/P	**Error Column (ERRCOL):** This field holds the DRAM column address of the read transaction that had the ECC error.
17:0	00000h RO/V/P	**Error Row (ERRROW):** This field holds the DRAM row (page) address of the read transaction that had the ECC error.

3.2.75 Power Down Timing (TC_PWRDN_0_0_0_MCHBAR) — Offset E050h

DDR timing constraints related to power down

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E050h	0804100400810204h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:59	01h RW	**tPRPDEN Timing Parameter (TPRPDEN):** This this register covers Any CMD --> PDE timing in tCK (WCK for LPDDR5) Note this register must be programmed to a minimum of 4 in Gear2 and a minimum of 2 in Gear1 Note for LP4 and LP5, program as follows. LPDDR4: tCMDPDE + 2 LPDDR5: tCMDPDE + 4
58:54	0h RO	**Reserved**
53:48	04h RW	**tCSL Timing Parameter (TCSL):** Chip Select low pulse width on power down exit (specified in DCLKs) :this is a fixed spec value (and in LPDDR5 this value is in resolution of tCK or multiples of 4WCK) and the value programmed in the register is in MC DCLKs / WCK Note: it should also be noted that tCSL covers for both tCSL and tCSCAL in LPDDR5.
47:42	04h RW	**tCSH Timing Parameter (TCSH):** Chip Select high pulse width on power down exit (specified in DCLKs): this is a fixed spec value (and LPDDR5 this value is in resolution of tCK or multiples of 4WCK) .The Final value programmed in the register is in MC DCLKs/WCK
41:32	004h RW	**tWRPDEN Timing Parameter (TWRPDEN):** Holds DDR timing parameter tWRPDEN. WR to power down minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-204.
31:29	0h RO	**Reserved**
28:21	04h RW	**tRDPDEN Timing Parameter (TRDPDEN):** Holds DDR timing parameter for tRDPDEN. RD to power down minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-100. Notes: • Because CKE power down is asynchrnous CKE may drop on the negative edge of the clock, an increase of +1 is needed for LPDDR4. • An additional increase of +1 is needed in the formula for LPDDR4
20:14	04h RW	**tXP Timing Parameter (TXPDLL):** Holds DDR timing parameter tXP. Power up to RD/WR minimum delay in tCK (WCK for LPDDR5) cycles. Applicable for DDR4 in case of exit from PPD when DRAM is configured to slow-exit mode. Supported range is 4-63.
13:7	04h RW	**tXP Timing Parameter (TXP):** Holds DDR timing parameter tXP. Power up to any command minimum delay in tCK /WCK cycles. Supported range is 4-24.

Bit Range	Default & Access	Field Name (ID): Description
6:0	04h RW	**tCKE Timing Parameter (TCKE):** Holds DDR timing parameter tCKE. Power down to power up (and vice versa) minimum delay in tCK (WCK for LPDDR5) cycles. Note that for LPDDR4 this value is also used for tCKCKEL and tCKELCMD. Supported range is 4-24.

3.2.76 ODT Command Timing (TC_ODT_0_0_0_MCHBAR) — Offset E070h

ODT timing related parameters

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E070h	0000000006050000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved**
31:24	06h RW	**tCWL Timing Parameter (TCWL):** Holds DDR timing parameter tCWL (sometimes referred to as tWCL). Write command to data delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-64 (maximum is for 1N mode) For LPDDR4 the minimum supported value is 4. For DDR4 the minimum supported value is 5.
23	0h RO	**Reserved**
22:16	05h RW	**tCL Timing Parameter (TCL):** Holds DDR timing parameter tCL. Read command to data delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-72.
15:0	0h RO	**Reserved**

3.2.77 ODT Matrix (SC_ODT_MATRIX_0_0_0_MCHBAR) — Offset E080h

ODT matrix (enabled using SC_GS_CFG_0_0_0_MCHBAR.enable_odt_matrix

Note: In DDR5 this matrix should only be used for non target ODT (target ODT should not be specified in this register)

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Write Rank 3 (WRITE_RANK_3):** Indicate which ranks should terminate when writing to rank 3 (bits 3:0 correspond to ODT pins 3:0.) Note: In DDR5 this register should only be used for non target ODT (target ODT should not be specified in this register)
27:24	0h RW	**Write Rank 2 (WRITE_RANK_2):** Indicate which ranks should terminate when writing to rank 2 (bits 3:0 correspond to ODT pins 3:0). Note: In DDR5 this register should only be used for non target ODT (target ODT should not be specified in this register)
23:20	0h RW	**Write Rank 1 (WRITE_RANK_1):** Indicate which ranks should terminate when writing to rank 1 (bits 3:0 correspond to ODT pins 3:0). Note: In DDR5 this register should only be used for non target ODT (target ODT should not be specified in this register)
19:16	0h RW	**Write Rank 0 (WRITE_RANK_0):** Indicate which ranks should terminate when writing to rank 0 (bits 3:0 correspond to ODT pins 3:0), Note: In DDR5 this register should only be used for non target ODT
15:12	0h RW	**Read Rank 3 (READ_RANK_3):** Indicate which ranks should terminate when reading from rank 3 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.
11:8	0h RW	**Read Rank 2 (READ_RANK_2):** Indicate which ranks should terminate when reading from rank 2 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.
7:4	0h RW	**Read Rank 1 (READ_RANK_1):** Indicate which ranks should terminate when reading from rank 1 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.
3:0	0h RW	**Read Rank 0 (READ_RANK_0):** Indicate which ranks should terminate when reading from rank 0 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.

3.2.78 Scheduler Configuration (SC_GS_CFG_0_0_0_MCHBAR) — Offset E088h

this register is used for Scheduler configuration

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E088h	0100000000000020h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60:56	01h RW	**tCPDED Timing Parameter (TCPDED):** Holds DDR timing parameter tCPDED. Power down to command bus tri-state delay in tCK cycles (for DDR4 only) Supported range is 0-7 in 1N mode.
55	0h RO	**Reserved**
54	0h RW	**WCK Differential Low In Idle (WCKDIFFLOWINIDLE):** PHY holds WCK to a differential value instead of turning it off. This register is a shadow copy of the DDRPHY register and should match the factory default value of the DDRPHY register.
53:50	0h RO	**Reserved**
49	0h RW	**Enable Write Zero (WRITE0_ENABLE):** enable write0 for power saving. This bit should only be set in normal mode
48:34	0h RO	**Reserved**
33:32	0h RW	**1 DIMM Per Channel Split Ranks on Sub-channel (DDR_1DPC_SPLIT_RANKS_ON_SUBCH):** Performance optimization for 1 DIMM Per Channel (1DPC) with dual rank. To be used only with Intel Memory reference Code as there are couple of low level configurations to enable it. For DDR5: the only legal configuration is 0x1 or 0x2. This register can never be set to 0 for DDR5
31	0h RW	**Gear2 Mode (GEAR2):** Indicate that MC is working in Gear-2 (Qclk is half the data transfer clock of the DRAM)
30	0h RW	**No Gear2 Param Divide (NO_GEAR2_PARAM_DIVIDE):** Don't do RU[param/2] for DRAM timing parameters when in gear-2, treat the value given in them in DCLKs instead of tCK clocks. For extending the existing ranges (mainly for Overclocking).
29:28	0h RW	**x8 Device (X8_DEVICE):** DIMM is made out of X8 devices LSB is for DIMM 0, MSB is for DIMM 1. For DDR5 1DPC, configure this option the same for both sub channels.
27:17	0h RO	**Reserved**
16	0h RW	**No Gear4 Parameter Divide (NO_GEAR4_PARAM_DIVIDE):** Don't do RU[param/4] for DRAM timing paramters when in Gear4, divide only by 2 (RU[param/2]). This enables a wider parameter range.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Gear4 Mode (GEAR4):** Indicate that MC is working in Gear4 (Qclk is quarter the data transfer clock of the DRAM)
14:12	0h RO	**Reserved**
11:8	0h RW	**Address Mirror (ADDRESS_MIRROR):** DIMM routing causes address mirroring For DDR4: bit 0: DIMM 0 (rank 1 bus is mirrored) bit 1: DIMM 1 (rank 3 bus is mirrored) For DDR5 bit 0: Rank0 on Dimm0 is mirrored bit 1: Rank1 on Dimm0 is mirrored bit 2: Rank0 on Dimm1 is mirrored (Rank 2) bit 3: Rank1 on Dimm1 is mirrored (Rank 3) For LPDDR4 bit 0: Sub channel 0 ranks 0 and 2 CA bus is mirrored. bit 1: Sub channel 1 ranks 0 and 2 CA bus is mirrored. bit 2: Sub channel 0 ranks 1 and 3 CA bus is mirrored. bit 3: Sub channel 1 ranks 1 and 3 CA bus is mirrored.
7:5	1h RW	**N to 1 Ratio (N_TO_1_RATIO):** When using N:1 command stretch mode, every how many B2B valid command cycles a bubble is required Supported range is 1 to 7
4:3	0h RW	**CMD Stretch (CMD_STRETCH):** Command stretch mode: 00b: 1N 01b: 2N 10b: 3N 11b: N:1 Notice that in Gear2 MC uses only the low phase of Dclk for commands, effectively doing a 2N by default. setting 2N in Gear2 will result in 4N at DDR interface
2:0	0h RO	**Reserved**

3.2.79 DDRIO Power Mode Timing (SPID_LOW_POWER_CTL_0_0_0_MCHBAR) — Offset E0B8h

This register holds DDRIO timing constraints regarding power modes latencies.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E0B8h	08104426h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Self-refresh Enable (SELFREFRESH_ENABLE):** allow sending DDRIO self refresh mode indication
30	0h RW	**Power Down Enable (POWERDOWN_ENABLE):** allow sending DDRIO CKE power down mode indication
29	0h RW	**Idle Enable (IDLE_ENABLE):** allow sending DDRIO idle mode indication. Note: LPMODE-1 is not supported in MC
28	0h RW	**CKE Valid Enable (CKEVALID_ENABLE):** Allow deasserting cke_valid when not toggling CKE pins
27:24	8h RW	**CKE Valid Length (CKEVALID_LENGTH):** cke_valid pulse length in DCLK cycles
23:20	1h RW	**Self-refresh Length (SELFREFRESH_LENGTH):** Minimum time allowed in self refresh mode Units is MC DCLKs (which means gearing is not handled in hardware)
19:14	01h RW	**Self-refresh Latency (SELFREFRESH_LATENCY):** Exit latency from self refresh mode till command can be sent in 8xtCK cycles Need to program to a value of 1 as self refresh latency is hidden behind tXSR. This register should never be programmed to 0
13:10	1h RW	**Powerdown Length (POWERDOWN_LENGTH):** Minimum time allowed in CKE power down mode. Units is MC DCLKs (which means gearing is not handled in hardware)
9:5	01h RW	**Powerdown Latency (POWERDOWN_LATENCY):** Exit latency from CKE power down mode till command can be sent in 1xtCK cycles This register should never be programmed to 0
4:1	3h RW	**Idle Length (IDLE_LENGTH):** Minimum time allowed in idle mode
0	0h RW	**Raise CKE After Exit Latency (RAISE_CKE_AFTER_EXIT_LATENCY):** Delay raising of CKE on exit from powerdown and selfrefresh power modes until required latency has passed. If this bit is clear then CKE exit (and tXP) happens in parallel of waking up the PHY, otherwise they happen back to back.

3.2.80 TR RRDVALID ctrl 0 0 0 MCHBAR (TR_RRDVALID_CTRL_0_0_0_MCHBAR) — Offset E104h

This register holds the rrd_valid feature bits

1 trigger signal

1 overflow indication

In 1DPC rank0 of subCh0 and rank3 of subCh1 is used than Trigger signal should be sent to rank0 and rank3 instead of rank and rank1

ERM is not supported

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/V	**Rank 7 overflow (RANK_7_OVERFLOW):** Rank 7 overflow indication
22	0h RW	**Rank 7 wr en (RANK_7_WR_EN):** Rank 7 fix enable
21	0h RW/V	**Rank 7 trigger (RANK_7_TRIGGER):** Rank 7 trigger
20	0h RW/V	**Rank 6 overflow (RANK_6_OVERFLOW):** Rank 6 overflow indication
19	0h RW	**Rank 6 wr en (RANK_6_WR_EN):** Rank 6 fix enable
18	0h RW/V	**Rank 6 trigger (RANK_6_TRIGGER):** Rank 6 trigger
17	0h RW/V	**Rank 5 overflow (RANK_5_OVERFLOW):** Rank 5 overflow indication
16	0h RW	**Rank 5 wr en (RANK_5_WR_EN):** Rank 5 fix enable
15	0h RW/V	**Rank 5 trigger (RANK_5_TRIGGER):** Rank 5 trigger
14	0h RW/V	**Rank 4 overflow (RANK_4_OVERFLOW):** Rank 4 overflow indication
13	0h RW	**Rank 4 wr en (RANK_4_WR_EN):** Rank 4 fix enable
12	0h RW/V	**Rank 4 trigger (RANK_4_TRIGGER):** Rank 4 trigger
11	0h RW/V	**Rank 3 overflow (RANK_3_OVERFLOW):** Rank 3 overflow indication
10	0h RW	**Rank 3 wr en (RANK_3_WR_EN):** Rank 3 fix enable
9	0h RW/V	**Rank 3 trigger (RANK_3_TRIGGER):** Rank 2 trigger
8	0h RW/V	**Rank 2 overflow (RANK_2_OVERFLOW):** Rank 2 overflow indication

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Rank 2 wr en (RANK_2_WR_EN):** Rank 2 fix enable
6	0h RW/V	**Rank 2 trigger (RANK_2_TRIGGER):** Rank 2 trigger
5	0h RW/V	**Rank 1 overflow (RANK_1_OVERFLOW):** Rank 1 overflow indication
4	0h RW	**Rank 1 wr en (RANK_1_WR_EN):** Rank 1 fix enable
3	0h RW/V	**Rank 1 trigger (RANK_1_TRIGGER):** Rank 1 trigger
2	0h RW/V	**Rank 0 overflow (RANK_0_OVERFLOW):** Rank 0 overflow indication
1	0h RW	**Rank 0 wr en (RANK_0_WR_EN):** Rank 0 fix enable
0	0h RW/V	**Rank 0 trigger (RANK_0_TRIGGER):** Rank 0 trigger

3.2.81 TR RRDVALID data 0 0 0 MCHBAR (TR_RRDVALID_DATA_0_0_0_MCHBAR) — Offset E108h

This register holds the rrd_Valid feature counter sign and value bits

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E108h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:57	00h RW/V	**Rank 7 value (RANK_7_VALUE):** Rank 7 value
56	0h RW/V	**Rank 6 sign (RANK_7_SIGN):** Rank 7 sign bit
55:49	00h RW/V	**Rank 6 value (RANK_6_VALUE):** Rank 6 value
48	0h RW/V	**Rank 6 sign (RANK_6_SIGN):** Rank 6 sign bit
47:41	00h RW/V	**Rank 5 value (RANK_5_VALUE):** Rank 5 value
40	0h RW/V	**Rank 5 sign (RANK_5_SIGN):** Rank 5 sign bit
39:33	00h RW/V	**Rank 4 value (RANK_4_VALUE):** Rank 4 value

Bit Range	Default & Access	Field Name (ID): Description
32	0h RW/V	**Rank 4 sign (RANK_4_SIGN):** Rank 4 sign bit
31:25	00h RW/V	**Rank 3 value (RANK_3_VALUE):** Rank 3 value
24	0h RW/V	**Rank 3 sign (RANK_3_SIGN):** Rank 3 sign bit
23:17	00h RW/V	**Rank 2 value (RANK_2_VALUE):** Rank 2 value
16	0h RW/V	**Rank 2 sign (RANK_2_SIGN):** Rank 2 sign bit
15:9	00h RW/V	**Rank 1 value (RANK_1_VALUE):** Rank 1 value
8	0h RW/V	**Rank 1 sign (RANK_1_SIGN):** Rank 1 sign bit
7:1	00h RW/V	**Rank 0 value (RANK_0_VALUE):** Rank 0 value
0	0h RW/V	**Rank 0 sign (RANK_0_SIGN):** Rank 0 sign bit

3.2.82 TC REFm 0 0 0 MCHBAR (TC_REFM_0_0_0_MCHBAR) — Offset E40Ch

Per Bank Refresh parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E40Ch	0000003Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10:0	03Ch RW	**tRFM timing parameter (TRFM):** Duration of REFm command. Default is same as tRFCpb.

3.2.83 MR4 Rank Temperature (MR4_RANK_TEMPERATURE_0_0_0_MCHBAR) — Offset E424h

This register holds the latest MR4 read per rank and used to determine the required refresh rate and thermal conditions of the DRAMs.

Noted: if the register DDR5_1DPC_split_ranks_across_subch is set then: rank_0 -- holds rank0 temperature and rank_3 holds rank1 temperature.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E424h	03030303h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	03h RW/V	**Rank 3 (RANK_3):** Rank 3 refresh rate (MRC should program the temperature appropriately as the reset default may not apply to all techs: for example LPDDR5 1x ref rate is 0xa)
23:21	0h RO	**Reserved**
20:16	03h RW/V	**Rank 2 (RANK_2):** Rank 2 refresh rate, (MRC should program the temperature appropriately as the reset default may not apply to all techs: for example LPDDR5 1x ref rate is 0xa)
15:13	0h RO	**Reserved**
12:8	03h RW/V	**Rank 1 (RANK_1):** Rank 1 refresh rate, (MRC should program the temperature appropriately as the reset default may not apply to all techs: for example LPDDR5 1x ref rate is 0xa)
7:5	0h RO	**Reserved**
4:0	03h RW/V	**Rank 0 (RANK_0):** Rank 0 refresh rate, (MRC should program the temperature appropriately as the reset default may not apply to all techs: for example LPDDR5 1x ref rate is 0xa)

3.2.84 DDR4 Temperature (DDR4_MPR_RANK_TEMPERATURE_0_0_0_MCHBAR) — Offset E428h

This register holds the latest temperature read per rank and used to determine the required refresh rate and thermal conditions of the DRAMs.

Encodings are:

0: Cold (below 45C), single refresh rate required, DRAM may drop refreshes if allowed

1: Normal operating temperature (45C-85C), single refresh rate, DRAM may drop refreshes if double rate refreshes are given

2: Hot (Above 85C), double refresh rate

3: Reserved

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E428h	01010101h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	1h RW/V	**Rank 3 (RANK_3):** Rank 3 refresh rate
23:18	0h RO	**Reserved**
17:16	1h RW/V	**Rank 2 (RANK_2):** Rank 2 refresh rate
15:10	0h RO	**Reserved**
9:8	1h RW/V	**Rank 1 (RANK_1):** Rank 1 refresh rate
7:2	0h RO	**Reserved**
1:0	1h RW/V	**Rank 0 (RANK_0):** Rank 0 refresh rate

3.2.85 Refresh Parameters (TC_RFP_0_0_0_MCHBAR) — Offset E438h

Refresh parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E438h	2356980Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	23h RW	**tREFI x9 (TREFIX9):** Maximum time allowed between refreshes to a rank (in intervals of 1024 DCLK cycles). Should be programmed to 8 * tREFI / 1024 (to allow for possible delays from ZQ or ISOC).

Bit Range	Default & Access	Field Name (ID): Description
23:20	5h RW	**Raise Block Wait (RAISE_BLK_WAIT):** Number of clocks the Main refresh FSM blocks the rank and waits before it progresses to any mantainance operations. Notes this register defined to allow enough time for MC safe logic to indicate to all downstream agents whether it is safe to issue MNT operations. the pipeline latency is 5 clocks in all cases except for LP5 Gear1 where it can be 7 clocks due to longer autosync read/wriite commands. So this register is specified in MC DCLKs and hardware will not change it based on gear.
19:18	1h RW	**Self Refresh Exit - Refresh Debits (SRX_REF_DEBITS):** Number of Refresh debits to be given on Self refresh exit. Set 1 for LPDDR4/DDR4 and 2 for LPDDR5/DDR5.
17	1h RW	**High Priority Referesh on MRS (HPREFONMRS):** Setting this bit will enable MRS refresh at the beginning of MRS flow if the rank reached High Priority refresh WM. Should be set by default, it's intended for System Agent SpeedStep as MC can enter Self refresh while owing refreshes.
16	0h RW	**Enable tREFI Counter While MC Refresh Enable is not Set (COUNTTREFIWHILEREFENOFF):** Setting this bit will enable tREFI counter while MC refresh enable is not set. Sometimes refresh enable bit is cleared in order to block maintenance operetions. This bit will keep tREFI counter on, but won't increase refresh debt, as the MC reset debt when refresh_enable bit not set.
15:12	9h RW	**Refresh Panic Threshold (REFRESH_PANIC_WM):** tREFI count level in which the refresh priority is panic (default is 9). The Maximum value for this field is 9.
11:8	8h RW	**Refresh Priority Threshold (REFRESH_HP_WM):** tREFI count level that turns the refresh priority to high (default is 8)
7:0	0Fh RW	**Rank Idle (OREF_RI):** Rank idle period that defines an opportunity for refresh, in DCLK cycles

3.2.86 Refresh Timing Parameters (TC_RFTP_0_0_0_MCHBAR) — Offset E43Ch

Refresh timing parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E43Ch	02D01004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
30:18	00B4h RW	**tRFC Timing Parameter (TRFC):** Time of refresh: from beginning of refresh until next ACT or refresh is allowed in tCK (WCK for LPDDR5) cycles. Default is 180. Note: MC hardware has a hardcoded delay of 10 pipeline stages for setting CKE to 0 after REFRESH gets issued and MC asserts CKE after tRFC - (tXP + 8), so the minimum value of tRFC must be: (tXP + 8) / Gear + (11 * Gear)
17:0	01004h RW	**tREFI Timing Parameter (TREFI):** Defines the average period between refreshes and the rate that tREFI counter is incremented in tCK (WCK for LPDDR5) cycles. Default is 4100.

3.2.87 Self-Refresh Timing Parameters (TC_SRFTP_0_0_0_MCHBAR) — Offset E440h

Self-refresh timing parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E440h	00000200h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12:0	0200h RW	**tXSDLL Timing Parameter (TXSDLL):** Delay between DDR SR exit and the first command that requires data RD/WR from DDR.

3.2.88 Refresh Stagger Control (MC_REFRESH_STAGGER_0_0_0_MCHBAR) — Offset E444h

Refresh stagger control

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E444h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Trefipulse Stagger Disable (TREFIPULSE_STAGGER_DISABLE):** When set, disables staggering of tREFI debits across ranks
16	0h RW	**Ref Stagger Mode (REF_STAGGER_MODE):** This bit sets the refresh staggering mode: 0: per DIMM refresh stagger 1: per channel refresh stagger
15	0h RW	**Refresh Stagger Enable (REF_STAGGER_EN):** When set this bit enables refresh staggering.
14	0h RW	**Enable Refresh Type Display (EN_REF_TYPE_DISPLAY):** This bit when set displays refresh type on the following address pins (DDR4 BG[0], BA[1:0], DDR5 CA[7:6], LPDDR4 CA_1[2:0], LPDDR5 CA_1[2:0], 00 = Stolen refresh 01 = Opportunistic Refresh 10 = High Priority Refresh 11 = Panic Refresh
13	0h RW	**Disable Stolen Refresh (DISABLE_STOLEN_REFRESH):** This bit when set disables stolen refreshes
12:0	0000h RW	**Refresh Interval (REF_INTERVAL):** Refresh Interval period in DCLKS

3.2.89 ZQCAL Control (TC_ZQCAL_0_0_0_MCHBAR) — Offset E448h

ZQCAL control

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E448h	0000032000010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:45	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
44:32	0320h RW	**tZQCAL Timing Parameter (TZQCAL):** tZQCAL in 2xtCK (2xWCK for LPDDR5) cycles. Used for LPDDR4/5 and DDR5.
31:21	0h RO	**Reserved**
20:10	040h RW	**tZQCS Timing Parameter (TZQCS):** For DDR4 this field tracks tZQCS timing, programmed in units of tCK. For all other DRAM technologies this field tracks tZQLAT timing. In LPDDR5, this field is programmed in units of WCK, otherwise it is programmed in units of tCK.
9:0	0h RO	**Reserved**

3.2.90 Memory Controller Initial State (MC_INIT_STATE_0_0_0_MCHBAR) — Offset E454h

Holds information on available ranks

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E454h	0000000Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	0Fh RW	**Rank Occupancy (RANK_OCCUPANCY):** Indicates which ranks are occupied in the system. Non-enhanced channels (DDR4 and DDR5): • Bit 0: Rank 0 • Bit 1: Rank 1 • Bit 2: Rank 2 • Bit 3: Rank 3 Enhanced channels (LPDDR4 and LPDDR5): • Bit 0: Rank 0 = Sub channel 0 Rank 0 • Bit 1: Rank 1 = Sub channel 0 Rank 1 • Bit 2: Rank 2 = Sub channel 1 Rank 0 • Bit 3: Rank 3 = Sub channel 1 Rank 1 • Bit 4: Sub channel 0 Rank 2 • Bit 5: Sub channel 0 Rank 3 • Bit 6: Sub channel 1 Rank 2 • Bit 7: Sub channel 1 Rank 3 Note: Default on reset is all ranks enabled due to DDRIO requirements, BIOS MRC will write these bits to the proper values after reset based on the actual rank configuration.

3.2.91 DIMM Idle Energy (PM_DIMM_IDLE_ENERGY_0_0_0_MCHBAR) — Offset E460h

This register defines the energy of an idle DIMM with CKE on.

Each 6-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM.

There are 2 6-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E460h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:8	00h RW	**DIMM1 Idle Energy (DIMM1_IDLE_ENERGY):** This register defines the energy consumed by DIMM1 for one clock cycle when the DIMM is idle with CKE on.
7:6	0h RO	**Reserved**
5:0	00h RW	**DIMM0 Idle Energy (DIMM0_IDLE_ENERGY):** This register defines the energy consumed by DIMM0 for one clock cycle when the DIMM is idle with CKE on.

3.2.92 DIMM Power-Down Energy (PM_DIMM_PD_ENERGY_0_0_0_MCHBAR) — Offset E464h

This register defines the energy of an idle DIMM with CKE off.

Each 6-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM.

There are 2 6-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E464h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:8	00h RW	**DIMM1 Power-Down Energy (DIMM1_PD_ENERGY):** This register defines the energy consumed by DIMM1 for one clock cycle when the DIMM is idle with CKE off.
7:6	0h RO	**Reserved**
5:0	00h RW	**DIMM0 Power-Down Energy (DIMM0_PD_ENERGY):** This register defines the energy consumed by DIMM0 for one clock cycle when the DIMM is idle with CKE off.

3.2.93 DIMM ACT Energy (PM_DIMM_ACT_ENERGY_0_0_0_MCHBAR) — Offset E468h

This register defines the combined energy contribution of activate and precharge commands.

Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM.

There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E468h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**DIMM1 ACT Energy (DIMM1_ACT_ENERGY):** This register defines the combined energy contribution of activate and precharge commands.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DIMM0 ACT Energy (DIMM0_ACT_ENERGY):** This register defines the combined energy contribution of activate and precharge commands.

3.2.94 DIMM RD Energy (PM_DIMM_RD_ENERGY_0_0_0_MCHBAR) — Offset E46Ch

This register defines the energy contribution of a read CAS command.

Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM.

There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E46Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**DIMM1 RD Energy (DIMM1_RD_ENERGY):** This register defines the energy contribution of a read CAS command.
7:0	00h RW	**DIMM0 RD Energy (DIMM0_RD_ENERGY):** This register defines the energy contribution of a read CAS command.

3.2.95 DIMM WR Energy (PM_DIMM_WR_ENERGY_0_0_0_MCHBAR) — Offset E470h

This register defines the energy contribution of a write CAS command.

Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM.

There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E470h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**DIMM1 WR Energy (DIMM1_WR_ENERGY):** This register defines the energy contribution of a write CAS command.
7:0	00h RW	**DIMM0 WR Energy (DIMM0_WR_ENERGY):** This register defines the energy contribution of a write CAS command.

3.2.96 WR Delay (SC_WR_DELAY_0_0_0_MCHBAR) — Offset E478h

This register defines the number of cycles decreased/increased from tCWL (TC_ODT_0_0_0_MCHBAR.tCWL) in Dclks.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E478h	00000003h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Add 1Qclk Delay (ADD_1QCLK_DELAY):** In Gear2, MC QCLK is actually 1xClk of the DDR, the regular MC register can only set even number of cycles (working in Dclk == 2 * 1xClk). This bit gives an option to delay the write data by one 1xClk.
11:6	00h RW	**Increased To tCWL (ADD_TCWL):** The number of cycles (DCLK) increased to tCWL. Make sure tCWL + Add_tCWL doesn't overflow.
5:0	03h RW	**Decreased From tCWL (DEC_TCWL):** The number of cycles (DCLK) decreased from tCWL. Configuring this number to be larger than tCWL is forbidden

3.2.97 Per Bank Refresh (SC_PBR_0_0_0_MCHBAR) — Offset E488h

Per Bank Refresh parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E488h	0000F011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:10	03Ch RW	**tRFCpb Timing Parameter (TRFCPB):** Refresh time in tCK (WCK for LPDDR5) for REFpb
9:4	01h RW	**Per Bank Refresh Exit on Idle Count (PBR_EXIT_ON_IDLE_CNT):** Number of tREFI cycles to count before switching PBR off for better clock gating. A value of 0 means no Idle exit.
3	0h RW	**Per Bank Refresh Disable on Hot (PBR_DISABLE_ON_HOT):** Disable PBR when LP4 is at 0.25xtREFI condition
2	0h RO	**Reserved**
1	0h RW	**Per Bank Refresh Out-of-Order Disable (PBR_OOO_DIS):** Disable out of order scheduling of banks for LP4. When using NoPanicPBR, this should be 0, otherwise will initiate PBR when there is high priority bank but might take low priority bank instead.
0	1h RW	**Per Bank Refresh Disable (PBR_DISABLE):** Disable PBR (per bank refresh) for LP4 (DDR4 force PBR off)

3.2.98 Miscellaneous Timing Constrains (TC_LPDDR4_MISC_0_0_0_MCHBAR) — Offset E494h

Miscellaneous timing constrains

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E494h	04081056h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Manual DQS Mode Register Read (MANUAL_DQS_MR_READ):** This bit when set allows software to manually issue a DQS oscillator Mode register read Example: LP4: MR18, MR19 will be read. LP5: MR35, MR36 will be read.
28:22	10h RW	**tMRR Timing Parameter (TMRR):** Time from MRR to MRR or MRR to any other command (specified in DCLKs in LPDDR4, WCK in LPDDR5). LPDDR5: the formula here is: RL + (BL/N_max) + RD (tWCKPST/tCK) + 2. LPDDR4: this needs to be programmed to 16. DDR5: max(14ns, 16 clocks)
21:15	10h RW	**tMRRMRW Timing Parameter (TMRRMRW):** MRR to MRW timing (LPDDR4 specified in DCLKs, LPDDR5 specified in WCK). MRR to MRW command minimum timing: DDR_TIMING_tDQSCK_max: • LPDDR4: RU(tDQSCK(max) / tCK) • LPDDR5: RU(tWCKDQ0(max) / tCK) DDR_TIMING_tBL: • LPDDR4: BL / 2 • LPDDR5: BL / n_max Conversion: • LPDDR4: DDR_TIMING_tCL + DDR_TIMING_tBL + DDR_TIMING_tDQSCK_max + 3; • LPDDR5: DDR_TIMING_tCL + DDR_TIMING_tBL + DDR_TIMING_tDQSCK_max + 2;
14:8	10h RW	**tPREMRR Timing Parameter (TPREMRR):** Enforces safety/timing of any cmd to MRR (specified in tCKs in LP4, WCK in LP5) For LP5: the formula here is: RL + (BL/N_max) + RD (tWCKPST/tCK) + 2 [READ --> MRR] For Other technologies: this needs to be programmed to 16
7:0	56h RW	**tOSCO Timing Parameter (TOSCO):** Delay between DQS_OSC counter stop to MR18/19 read

3.2.99 Self-Refresh Exit Timing Parameters (TC_SREXITTP_0_0_0_MCHBAR) — Offset E4C0h

Self-refresh exit (SRX) timing parameters

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E4C0h	0200000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:58	0h RO	**Reserved**
57:52	20h RW	**tSR Timing Parameter (TSR):** Minimum time in self refresh. LPDDR5 and LPDDR4: it is tSR. DDR4: it is tCKESR DDR5: it is tCSL
51:13	0h RO	**Reserved**
12:0	0000h RW	**tXSR Timing Parameter (TXSR):** Exit self refresh to valid commands delay. in LP4 configure this parameter for tXSR or tXSR abort in terms of tCK (WCK for LPDDR5) cycles if used.

3.2.100 Built in Self Test (WDB_MBIST_0_0_0_MCHBAR[0]) — Offset E4E8h

This register holds the MBIST fields for the WDB and RDB.

Note: There are 2 instances of this register. The offset between instances is 4.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E4E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Run/Busy Bit (RUN_BUSY):** This bit is set during BIST. Hardware clears when done. This bit should keep clocks running in the RF/SRAMs
30:9	0h RO	**Reserved**
8	0h RW	**MBIST Inject Failure (INJECT_FAILURE):** MBIST Failure Injection.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RO/V	**MBIST Completed (COMPLETE):** The MBIST Test has Completed.
0	0h RO/V	**MBIST Passed (PASS):** The MBIST Test has Passed.

3.2.101 RDB Built in Self Test (RDB_MBIST_0_0_0_MCHBAR) — Offset E4F8h

This register holds the MBIST fields for the WDB and RDB.

Note: Bit definitions are the same as WDB_MBIST_0_0_0_MCHBAR[0], offset E4E8h.

3.2.102 ECC Inject Count (ECC_INJECT_COUNT_0_0_0_MCHBAR) — Offset E4FCh

This register defines the count of write chunks (64-bit data packets) until the next ECC error injection in case ECC_inject field in ECC_DEBUG_0_0_0_MCHBAR is 110b or 111b. The count is of chunks in order to allow creating ECC errors on different 64-bit chunks

For Memory Controller 1 (MC1) - Please refer to doc #655741 for details.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E4FCh	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**COUNT:** Chunk count for error inject.

3.2.103 Miscellaneous Control Register (MCMNTS_SPARE_0_0_0_MCHBAR) — Offset E5FCh

Miscellaneous control register.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E5FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**Force x8 Refreshes (FORCEX8REF):** Force accelerated refreshes, eight times the refresh number. Should be mutually exclusive with ForceX2Ref and ForceX4Ref. Constant X8 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause performance degradation. Use with caution.
15:11	0h RO	**Reserved**
10	0h RW	**Disable Low Refresh Rate (DISLOWREFRATE):** Don't allow refresh rate lower than 1X
9	0h RW	**Force x4 Refreshes (FORCEX4REF):** Force accelerated refreshes, four times the refresh number. Should be mutually exclusive with ForceX2Ref and ForceX8Ref. Constant X4 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause performance degradation. Use with caution.
8	0h RW	**Force x2 Refreshes (FORCEX2REF):** Force accelerated refreshes, twice the refresh number. Should be mutually exclusive with ForceX4Ref and ForceX8Ref. Constant x2 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause a performance degradation. Use with caution.
7:0	0h RO	**Reserved**

3.3 Power Management (MCHBAR) Registers

This chapter documents the power management MCHBAR registers.

Base address of these registers are defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.3.1 Summary of Registers

Table 3-4. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5824h	4	BIOS POST Code (BIOS_POST_CODE_0_0_0_MCHBAR_PCU)	00000000h
5828h	8	Cycle Sum of All Active Cores (PKG_IA_C0_ANY_SUM_0_0_0_MCHBAR_PCU)	0000000000000000h
5830h	8	Cycle Sum of Any Active Core (PKG_IA_C0_ANY_0_0_0_MCHBAR_PCU)	0000000000000000h
5838h	8	Cycle Sum of Active Graphics (PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU)	0000000000000000h
5840h	8	Cycle Sum of Overlapping Active GT and Core (PKG_GT_AND_IA_OVERLAP_0_0_0_MCHBAR_PCU)	0000000000000000h
5848h	8	Cycle Sum of Any Active GT Slice (PKG_GT_C0_ANY_SLICE_0_0_0_MCHBAR_PCU)	0000000000000000h
5850h	8	Cycle Sum of All Active GT Slice (PKG_GT_C0_SLICES_SUM_0_0_0_MCHBAR_PCU)	0000000000000000h
5858h	8	Cycle Sum of Any GT Media Engine (PKG_GT_C0_ANY_MEDIA_0_0_0_MCHBAR_PCU)	0000000000000000h
5860h	8	Ratio Sum of Any Active Core (PKG_IA_C0_ANY_RATIO_0_0_0_MCHBAR_PCU)	0000000000000000h
5868h	8	Ratio Sum of Active GT (PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU)	0000000000000000h
5870h	8	Ratio Sum of Active GT Slice (PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU)	0000000000000000h
58E0h	8	DDR Power Limit (DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU)	0000000000000000h
58F0h	4	Package RAPL Performance Status (PACKAGE_RAPL_PERF_STATUS_0_0_0_MCHBAR_PCU)	00000000h
5918h	8	System Agent Performance Status (SA_PERF_STATUS_0_0_0_MCHBAR_PCU)	0000002000000000h
5920h	4	Primary Plane Turbo Policy (PRIP_TURBO_PLCY_0_0_0_MCHBAR_PCU)	00000000h
5924h	4	Secondary Plane Turbo Policy (SECP_TURBO_PLCY_0_0_0_MCHBAR_PCU)	00000010h
5928h	4	Primary Plane Energy Status (PRIP_NRG_STTS_0_0_0_MCHBAR_PCU)	00000000h
592Ch	4	Secondary Plane Energy Status (SECP_NRG_STTS_0_0_0_MCHBAR_PCU)	00000000h
5938h	4	Package Power SKU Unit (PACKAGE_POWER_SKU_UNIT_0_0_0_MCHBAR_PCU)	000A0E03h
593Ch	4	Package Energy Status (PACKAGE_ENERGY_STATUS_0_0_0_MCHBAR_PCU)	00000000h
5948h	4	GT Performance Status (GT_PERF_STATUS_0_0_0_MCHBAR_PCU)	00000000h
5968h	4	Power Plane 0 Efficient Cycles (PP0_EFFICIENT_CYCLES_0_0_0_MCHBAR_PCU)	00000000h
596Ch	4	Power Plane 0 Thread Activity (PP0_THREAD_ACTIVITY_0_0_0_MCHBAR_PCU)	00000000h
597Ch	4	Primary Plane 0 Temperature (PP0_TEMPERATURE_0_0_0_MCHBAR_PCU)	00000000h
5994h	4	RP-State Limits (RP_STATE_LIMITS_0_0_0_MCHBAR_PCU)	000000FFh
5998h	4	RP-State Capability (RP_STATE_CAP_0_0_0_MCHBAR_PCU)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
599Ch	4	Temperature Target (TEMPERATURE_TARGET_0_0_0_MCHBAR_PCU)	00000000h
59A0h	8	Package Power Limit (PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU)	0000000000000000h
59C0h	4	Thermal Status GT (THERM_STATUS_GT_0_0_0_MCHBAR_PCU)	08000000h
59C4h	4	Thermal Interrupt GT (THERM_INTERRUPT_GT_0_0_0_MCHBAR_PCU)	00000000h
59C8h	4	Device Idle Duration Override (DEVICE_IDLE_DURATION_OVERRIDE_0_0_0_MCHBAR_PCU)	00000000h
59F0h	8	Package GT C0 EUs SUM (PKG_GT_C0_EUS_SUM)	0000000000000000h
59F8h	8	Package GT C0 Media Sum (PKG_GT_C0_MEDIA_SUM)	0000000000000000h
5A08h	4	FIVR FFFC EMI Control (FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU)	00000000h
5A0Ch	4	FIVR FFFC RFI Control (FFFC_RFI_CONTROL_0_0_0_MCHBAR_PCU)	00000000h
5A18h	4	FIVR FFFC RFI Control 2 (FFFC_RFI_CONTROL2_0_0_0_MCHBAR_PCU)	00000000h
5DA0h	4	BIOS Mailbox Data (BIOS_MAILBOX_DATA_0_0_0_MCHBAR_PCU)	00000000h
5DA4h	4	BIOS Mailbox Interface (BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR_PCU)	00000000h
5DA8h	4	BIOS Reset Complete (BIOS_RESET_CPL_0_0_0_MCHBAR_PCU)	00000000h
5E00h	4	Memory Controller BIOS Request (MC_BIOS_REQ_0_0_0_MCHBAR_PCU)	00000000h
5E04h	4	Memory Controller BIOS Data (MC_BIOS_DATA_0_0_0_MCHBAR_PCU)	00000000h
5F00h	4	System Agent Power Management Control (SAPMCTL_0_0_0_MCHBAR_PCU)	00002106h
5F3Ch	4	Configurable TDP Nominal (CONFIG_TDP_NOMINAL_0_0_0_MCHBAR_PCU)	00000000h
5F40h	8	Configurable TDP Level 1 (CONFIG_TDP_LEVEL1_0_0_0_MCHBAR_PCU)	0000000000000000h
5F48h	8	Configurable TDP Level 1 (CONFIG_TDP_LEVEL2_0_0_0_MCHBAR_PCU)	0000000000000000h
5F50h	4	Configurable TDP Control (CONFIG_TDP_CONTROL_0_0_0_MCHBAR_PCU)	00000000h
5F54h	4	Turbo Activation Ratio (TURBO_ACTIVATION_RATIO_0_0_0_MCHBAR_PCU)	00000000h
5F58h	4	Overclocking Status (OC_STATUS_0_0_0_MCHBAR_PCU)	00000000h
5F60h	8	Base Clock (BCLK) Frequency (BCLK_FREQ_0_0_0_MCHBAR)	0000000000000000h

3.3.2 BIOS POST Code (BIOS_POST_CODE_0_0_0_MCHBAR_PCU) — Offset 5824h

This register holds 32 writable bits with no functionality behind them.

BIOS writes the current POST code here (port 80).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5824h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**POST Code (POSTCODE):** BIOS will write the current POST code in this field

3.3.3 Cycle Sum of All Active Cores (PKG_IA_C0_ANY_SUM_0_0_0_MCHBAR_PCU) — Offset 5828h

Sum the cycles per number of active cores

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5828h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RO/V	**DATA:** The counter value is incremented as a function of the number of cores that reside in C0 and are active. If N cores are simultaneously in C0, then the number of clock ticks that are incremented is N. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.4 Cycle Sum of Any Active Core (PKG_IA_C0_ANY_0_0_0_MCHBAR_PCU) — Offset 5830h

Sum the cycles of any active cores.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5830h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever one (or more) IA cores are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.5 Cycle Sum of Active Graphics (PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU) — Offset 5838h

Sum the cycles of activity of the GT.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5838h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever GT slices or un-slices are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.6 Cycle Sum of Overlapping Active GT and Core (PKG_GT_AND_IA_OVERLAP_0_0_0_MCHBAR_PCU) — Offset 5840h

Sum the cycles of overlap time between any IA cores and GT.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5840h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever GT slices or un-slices are active and in C0 state and in overlap with one of the IA cores that is active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.7 Cycle Sum of Any Active GT Slice (PKG_GT_C0_ANY_SLICE_0_0_0_MCHBAR_PCU) — Offset 5848h

Sum the cycles of any active GT slice.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5848h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever a GT slice (one of more) is active. Counter rate is the Crystal clock.

3.3.8 Cycle Sum of All Active GT Slice (PKG_GT_C0_SLICES_SUM_0_0_0_MCHBAR_PCU) — Offset 5850h

Sum the cycles of the sum of all active GT slices.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5850h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO	**DATA:** This counter increments by the sum of all active GT slices. Counter rate is the Crystal clock.

3.3.9 Cycle Sum of Any GT Media Engine (PKG_GT_C0_ANY_MEDIA_0_0_0_MCHBAR_PCU) — Offset 5858h

Sum the cycles of any media GT engine.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5858h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO	**DATA:** This counter increments whenever any GT media engine is active. Counter rate is in 24MHz.

3.3.10 Ratio Sum of Any Active Core (PKG_IA_C0_ANY_RATIO_0_0_0_MCHBAR_PCU) — Offset 5860h

new counter, follow exactly the PKG_IA_C0_ANY_0_0_0_MCHBAR_PCU

The only change is +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_IA_C0_ANY_RATIO_0_0_0_MCHBAR_PCU

+IO_WP_CV_P_STATE[IA_RATIO]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5860h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever one or more IA cores are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC)

3.3.11 Ratio Sum of Active GT (PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU) — Offset 5868h

new counter, follow exactly the PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU

The only change is +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU

+ 3 * IO_WP_CV_P_STATE[GT_UNSLICE_RATIO] - IO_WP_CV_GT_CONFIG[UNSLICE_SQUASH_DELTA]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5868h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever GT slices or un-slices are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC)

3.3.12 Ratio Sum of Active GT Slice (PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU) — Offset 5870h

new counter, follow exactly the PKG_GT_C0_ANY_SLICEU

The only change is +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU

+ 3 * IO_WP_CV_P_STATE[GT_SLICE_RATIO] - IO_WP_CV_GT_CONFIG[SLICE_SQUASH_DELTA]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5870h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever any GT slice is active. Counter rate is in Xtal (24/19.2Mhz) clock

3.3.13 DDR Power Limit (DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU) — Offset 58E0h

Allows software to set running average power limits (RAPL) for the DRAM domain and measurement attributes associated with each limit.

The DDR RAPL algorithm uses the minimum of the values from this register and the DDR_RAPL_LIMIT MSR.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 58E0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/L	**LOCKED:** When set, this entire register becomes read-only. This bit will typically be set by BIOS during boot. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
62:48	0h RO	**Reserved**
47	0h RW/L	**Power Limitation #2 Enable (LIMIT2_ENABLE):** Power Limit 2 (PL2) enable bit for DDR domain. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED

Bit Range	Default & Access	Field Name (ID): Description
46:32	0000h RW/L	**Power Limitation #2 (LIMIT2_POWER):** Power Limit 2 (PL2) for DDR domain in Watts. Format is U11.3: Resolution 0.125W, Range 0-2047.875W. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
31:24	0h RO	**Reserved**
23:22	0h RW/L	**Limitation #1 Time Window X (LIMIT1_TIME_WINDOW_X):** Power Limit 1 (PL1) time window X value, for DDR domain. Actual time window for RAPL is: (1/1024 seconds) * (1+(X/4)) * (2Y) **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
21:17	00h RW/L	**Limitation #1 Time Window Y (LIMIT1_TIME_WINDOW_Y):** Power Limit 1 (PL1) time window Y value, for DDR domain. Actual time window for RAPL is: (1/1024 seconds) * (1+(X/4)) * (2Y) **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
16	0h RO	**Reserved**
15	0h RW/L	**Power Limit 1 Enable (LIMIT1_ENABLE):** Power Limit 1 (PL1) enable bit for DDR domain. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
14:0	0000h RW/L	**Power Limit 1 (LIMIT1_POWER):** Power Limit 1 (PL1) for DDR domain in Watts. Format is U11.3: Resolution 0.125W, Range 0-2047.875W. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED

3.3.14 Package RAPL Performance Status (PACKAGE_RAPL_PERF_STATUS_0_0_0_MCHBAR_PCU) — Offset 58F0h

Package RAPL Performance Status Register. This register provides information on the performance impact of the RAPL power limit and indicates the duration for processor went below the requested P-state due to package power constraint.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 58F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**COUNTS:** Counter of the time units within which RAPL was limiting P-states. If limitation occurred anywhere within the time window of 1/1024 seconds, the count will be incremented (limitation on accuracy). This data can serve as a proxy for the potential performance impacts of RAPL on cores performance.

3.3.15 System Agent Performance Status (SA_PERF_STATUS_0_0_0_MCHBAR_PCU) — Offset 5918h

Indicates current various System Agent PLL ratios.

Operating frequency needs to be calculated according to reference clock (BCLK).

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5918h	0000002000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**Reserved**
55:40	0000h RO/V	**System Agent Voltage (SA_VOLTAGE):** This register holds the System Agent voltage. This voltage value is valid only if the System Agent VR is SVID based. The precision is U3.13 (1/8192V resolution).
39:32	20h RO/V	**PSF0 PLL Ratio (PSF0_RATIO):** Reports the PSF0 PLL ratio. The PSF0 frequency is: Ratio * 16.67MHz. The supported ratios are {32, 48, 64} = {533MHz, 800MHz, 1067MHz}.
31:24	00h RO/V	**RING UCLK PLL Ratio (UCLK_RATIO):** RING UCLK RATIO. Reference=100Mhz
23:18	00h RO/V	**IPU PS Ratio (IPU_PS_RATIO):** The frequency is 25MHz * Ratio.
17:12	00h RO/V	**IPU IS Divisor (IPU_IS_DIVISOR):** The frequency is 1600MHz/Divisor.
11	0h RO/V	**On Package Interface (OPI) Link Speed (OPI_LINK_SPEED):** 0: 2Gb/s 1: 4Gb/s
10	0h RO/V	**DDR QCLK Reference (QCLK_REFERENCE):** 0: 133.34Mhz. In frequency calculations use 400.0MHz/3.0. 1: 100.00Mhz
9:2	00h RO/V	**DDR QCLK Ratio (QCLK_RATIO):** Reference determined by the QCLK_REFERENCE field.
1:0	0h RO/V	**Last Display Engine Workpoint Request Served (LAST_DE_WP_REQ_SERVED):** Last display engine workpoint request served by the PCU

3.3.16 Primary Plane Turbo Policy (PRIP_TURBO_PLCY_0_0_0_MCHBAR_PCU) — Offset 5920h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget between the two power planes.

The power plane with the higher policy will get a higher priority.

The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5920h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Priority Level (PRIPTP):** A higher number implies a higher priority.

3.3.17 Secondary Plane Turbo Policy (SECP_TURBO_PLCY_0_0_0_MCHBAR_PCU) — Offset 5924h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget between the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5924h	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:0	10h RW	**Priority Level (SECPTP):** A higher number implies a higher priority.

3.3.18 Primary Plane Energy Status (PRIP_NRG_STTS_0_0_0_MCHBAR_PCU) — Offset 5928h

Reports total energy consumed.

The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Software will read this value and subtract the difference from last value read.

The value of this register is updated every 1mSec.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5928h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** Energy Value

3.3.19 Secondary Plane Energy Status (SECP_NRG_STTS_0_0_0_MCHBAR_PCU) — Offset 592Ch

Reports total energy consumed. The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Software will read this value and subtract the difference from last value read. The value of this register is updated every 1mSec.

Note: Bit definitions are the same as PRIP_NRG_STTS_0_0_0_MCHBAR_PCU, offset 5928h.

3.3.20 Package Power SKU Unit (PACKAGE_POWER_SKU_UNIT_0_0_0_MCHBAR_PCU) — Offset 5938h

Defines units for calculating SKU power and timing parameters.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5938h	000A0E03h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	Ah RO/V	**Time Unit (TIME_UNIT):** Time Units used for power control registers. The actual unit value is calculated by 1 s / Power(2, TIME_UNIT). The default value of Ah corresponds to 976 usec.
15:13	0h RO	**Reserved**
12:8	0Eh RO/V	**Energy Unit (ENERGY_UNIT):** Energy Units used for power control registers. The actual unit value is calculated by 1 J / Power(2, ENERGY_UNIT). The default value of 14 corresponds to Ux.14 number.
7:4	0h RO	**Reserved**
3:0	3h RO/V	**Power Unit (PWR_UNIT):** Power Units used for power control registers. The actual unit value is calculated by 1 W / Power(2, PWR_UNIT). The default value of 0011b corresponds to 1/8 W.

3.3.21 Package Energy Status (PACKAGE_ENERGY_STATUS_0_0_0_MCHBAR_PCU) — Offset 593Ch

Package energy consumed by the entire CPU (including IA, GT and uncore). The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Note: Bit definitions are the same as PRIP_NRG_STTS_0_0_0_MCHBAR_PCU, offset 5928h.

3.3.22 GT Performance Status (GT_PERF_STATUS_0_0_0_MCHBAR_PCU) — Offset 5948h

P-state encoding for the Secondary Power Planes current PLL frequency and the current VID.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5948h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:20	000h RO/V	**Slices Ratio (SLICES_RATIO):** GT Slices frequency, in granularity of 16.666Mhz. When GT is in RC6, or when all slices are disabled, this frequency is ZERO.
19:11	000h RO/V	**Un-slice Ratio (UNSLICE_RATIO):** GT Unslice frequency, in granularity of 16.666Mhz. When GT is in RC6 this frequency is ZERO.
10:8	0h RO	**Reserved**
7:0	00h RO/V/P	**Slices Voltage (SLICES_VOLTAGE):** GT voltage, in VID units according to SVID spec format.

3.3.23 Power Plane 0 Efficient Cycles (PP0_EFFICIENT_CYCLES_0_0_0_MCHBAR_PCU) — Offset 5968h

This register stores a value equal to the product of the number of BCLK cycles in which at least one of the IA cores was active and the efficiency score calculated by the PCU.

The efficiency score is a number between 0 and 1 that indicates the IAs efficiency.

This is a 32 bit accumulation done by P-code to this register out of the PUSH-BUS. Values exceeding 32b will wrap around. This value is used in conjunction with PP0_ANY_THREAD_ACTIVITY to generate statistics for SW.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5968h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** Number of Cycles

3.3.24 Power Plane 0 Thread Activity (PP0_THREAD_ACTIVITY_0_0_0_MCHBAR_PCU) — Offset 596Ch

This register will store a value equal to the product of the number of BCLK cycles and the number of IA threads that are running. This is a 32 bit accumulation done by PCU HW. Values exceeding 32b will wrap around.

This value is used in conjunction with PP0_ANY_THREAD_ACTIVITY to generate statistics for SW.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 596Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** Number of Cycles.

3.3.25 Primary Plane 0 Temperature (PP0_TEMPERATURE_0_0_0_MCHBAR_PCU) — Offset 597Ch

PP0 (IA Cores) temperature in degrees (C).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 597Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**DATA:** Temperature in degrees (C).

3.3.26 RP-State Limits (RP_STATE_LIMITS_0_0_0_MCHBAR_PCU) — Offset 5994h

This register allows software to limit the maximum frequency of the Integrated Graphics Engine (GT) allowed during run-time.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5994h	000000FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	FFh RW	**RP0 State Limit (RPSTT_LIM):** This field indicates the maximum frequency limit for the Integrated Graphics Engine (GT) allowed during run-time.

3.3.27 RP-State Capability (RP_STATE_CAP_0_0_0_MCHBAR_PCU) — Offset 5998h

This register contains the maximum base frequency capability for the Integrated Graphics Engine (GT).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5998h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RO	**RPn Capability (RPN_CAP):** This field indicates the maximum RPN base frequency capability for the Integrated GFX Engine (GT). Values are in units of 50 MHz.
15:8	00h RO	**RP1 Capability (RP1_CAP):** This field indicates the maximum RP1 base frequency capability for the Integrated GFX Engine (GT). Values are in units of 50 MHz.
7:0	00h RO	**RP0 Capability (RP0_CAP):** This field indicates the maximum RP0 base frequency capability for the Integrated GFX Engine (GT). Values are in units of 50 MHz.

3.3.28 Temperature Target (TEMPERATURE_TARGET_0_0_0_MCHBAR_PCU) — Offset 599Ch

Legacy register holding temperature related constants for Platform use.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 599Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCKED:** When set, this entire register becomes read-only. **Locked by:** TEMPERATURE_TARGET.LOCKED
30:24	00h RO/V	**TjMax Tcc Offset (TJ_MAX_TCC_OFFSET):** Temperature offset in degrees (C) from the TjMax. Used for throttling temperature. Will not impact temperature reading. If offset is allowed and set, the throttle will occur and reported at lower then TjMax. **Locked by:** TEMPERATURE_TARGET.LOCKED
23:16	00h RO/V	**Thermal Junction Maximum Temperature (TJMAX):** This field indicates the maximum junction temperature, also referred to as the Throttle Temperature, TCC Activation Temperature or Prochot Temperature. This is the temperature at which the Adaptive Thermal Monitor is activated.
15:8	00h RO/V	**Fan Temperature Offset (FAN_TEMP_TARGET_OFST):** Fan Temperature Target Offset (a.k.a. T-Control) indicates the relative offset from the Thermal Monitor Trip Temperature at which fans should be engaged.
7	0h RO/V	**Tcc Offset Clamping Bit (TCC_OFFSET_CLAMPING_BIT):** When enabled will allow RATL throttling below P1 **Locked by:** TEMPERATURE_TARGET.LOCKED
6:0	00h RO/V	**Tcc Offset Time Window (TCC_OFFSET_TIME_WINDOW):** Describes the RATL averaging time window **Locked by:** TEMPERATURE_TARGET.LOCKED

3.3.29 Package Power Limit (PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU) — Offset 59A0h

The Integrated Graphics driver, CPM driver, BIOS and OS can balance the power budget between the Primary Power Plane (IA) and the Secondary Power Plane (GT) via PRIMARY_PLANE_TURBO_POWER_LIMIT_MSR and SECONDARY_PLANE_TURBO_POWER_LIMIT_MSR.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 59A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/L	**Package Limitation #2 Lock (PKG_PWR_LIM_LOCK):** When set, all settings in this register are locked and are treated as Read Only. This bit will typically set by BIOS during boot time or resume from Sx. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
62:48	0h RO	**Reserved**
47	0h RW/L	**Package Limitation #2 Enable (PKG_PWR_LIM_2_EN):** This bit enables/disables Package Limitation #2 (PL2). 0b: Package Power Limit 2 is Disabled 1b: Package Power Limit 2 is Enabled **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
46:32	0000h RW/L	**Package Power Limitation #2 (PKG_PWR_LIM_2):** This field indicates the power limitation #2. The unit of measurement is defined in MSR PACKAGE_POWER_SKU_UNIT[PWR_UNIT]. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
31:24	0h RO	**Reserved**
23:17	00h RW/L	**Package Limitation #1 Time Window (PKG_PWR_LIM_1_TIME):** Specifies the time window used to calculate average power for PL1 and PL2. The timing interval window is Floating Point number given by 1.x * power(2,y). x = PKG_PWR_LIM_1_TIME[23:22] y = PKG_PWR_LIM_1_TIME[21:17] The unit of measurement is defined in MSR PACKAGE_POWER_SKU_UNIT[TIME_UNIT]. The maximal time window is bounded by MSR PACKAGE_POWER_SKU[PKG_MAX_WIN]. The minimum time window is 1 unit of measurement (as defined above). **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
16	0h RW/L	**Package Clamping limitation #1 (PKG_CLMP_LIM_1):** Allows going below P1. 0b: Power limit throttling is limited between base frequency (P1) and Max turbo frequency (P0). 1b: Power limit throttling is not limited. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
15	0h RW/L	**Package Power Limit 1 Enable (PKG_PWR_LIM_1_EN):** This bit enables/disables Package Power Limit 1. 0b: Package Power Limit 1 is Disabled 1b: Package Power Limit 1 is Enabled **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK

Bit Range	Default & Access	Field Name (ID): Description
14:0	0000h RW/L	**Package Power Limit 1 (PKG_PWR_LIM_1):** This field indicates the power limitation #1. The unit of measurement is defined in PACKAGE_POWER_SKU_UNIT_MSR[PWR_UNIT]. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK

3.3.30 Thermal Status GT (THERM_STATUS_GT_0_0_0_MCHBAR_PCU) — Offset 59C0h

Contains status information about the processors thermal sensor and automatic thermal monitoring facilities.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 59C0h	08000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**VALID:** This bit indicates that the TEMPERATURE field is valid. It is set by PCODE if the temperature is within valid thermal sensor range.
30:27	1h RO	**RESOLUTION:** Supported resolution in degrees C.
26:24	0h RO	**Reserved**
23:16	00h RO/V	**TEMPERATURE:** This is a temperature offset in degrees C below theTJ Max temperature. This number is meaningful only if VALID bit in this register is set.
15	0h RW/0C/V	**Cross Domain Limit Log (CROSS_DOMAIN_LIMIT_LOG):** If set (1), indicates another hardware domain (e.g. processor graphics) has limited energy efficiency optimizations in the processor core domain since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
14	0h RO/V	**Cross Domain Limit Status (CROSS_DOMAIN_LIMIT_STATUS):** RO - If set (1), indicates another hardware domain (e.g. processor graphics) is currently limiting energy efficiency optimizations in the processor core domain.
13	0h RW/0C/V	**Current Limit Log (CURRENT_LIMIT_LOG):** R/WC0 - If set (1), an electrical current limit has been exceeded that has adversely impacted energy efficiency optimizations since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
12	0h RO/V	**Current Limit Status (CURRENT_LIMIT_STATUS):** If set (1), indicates an electrical current limit (e.g. Electrical Design Point/IccMax) is being exceeded and is adversely impacting energy efficiency optimizations.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/0C/V	**Power Limitation Log (POWER_LIMITATION_LOG):** Sticky bit which indicates whether the current P-State is limited by power limitation since the last clearing of this bit or a reset. Software may clear this bit by writing a zero (0). For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level
10	0h RO/V	**Power Limitation Status (POWER_LIMITATION_STATUS):** Indicates whether the current P-State is limited by power limitation. For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level.
9	0h RW/0C/V	**Threshold2 Log (THRESHOLD2_LOG):** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD2_STATUS bit. This bit is set by hardware and cleared by software.
8	0h RO/V	**Threshold2 Status (THRESHOLD2_STATUS):** Indicates that the current temperature is higher than or equal to Threshold 2 temperature.
7	0h RW/0C/V	**Threshold1 Log (THRESHOLD1_LOG):** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD1_STATUS bit. This bit is set by hardware and cleared by software.
6	0h RO/V	**Threshold1 Status (THRESHOLD1_STATUS):** Indicates that the current temperature is higher than or equal to Threshold 1 temperature.
5	0h RW/0C/V	**Out Of Specification Log (OUT_OF_SPEC_LOG):** Sticky log bit indicating that the processor operating out of its thermal specification since the last time this bit was cleared. This bit is set by hardware on a 0 to 1 transition of OUT_OF_SPEC_STATUS.
4	0h RO/V	**Out Of Specification Status (OUT_OF_SPEC_STATUS):** Status bit indicating that the processor is operating out of its thermal specification. Once set, this bit should only clear on a reset.
3	0h RW/0C/V	**PROCHOT# Log (PROCHOT_LOG):** Sticky log bit indicating that xxPROCHOT# has been asserted since the last time this bit was cleared by SW. This bit is set by HW on a 0 to 1 transition of PROCHOT_STATUS.
2	0h RO/V	**PROCHOT# Status (PROCHOT_STATUS):** Status bit indicating that xxPROCHOT# is currently being asserted.
1	0h RW/0C/V	**Thermal Monitor Log (THERMAL_MONITOR_LOG):** Sticky log bit indicating that the core has seen a thermal monitor event since the last time software cleared this bit. This bit is set by hardware on a 0 to 1 transition of THERMAL_MONITOR_STATUS.
0	0h RO/V	**Thermal Monitor Status (THERMAL_MONITOR_STATUS):** Status bit indicating that the Thermal Monitor has tripped and is currently thermally throttling.

3.3.31 Thermal Interrupt GT (THERM_INTERRUPT_GT_0_0_0_MCHBAR_PCU) — Offset 59C4h

Enables and disables the generation of an interrupt on temperature transitions detected with the processors thermal sensors and thermal monitor.

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Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 59C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Power Interrupt Enable (POWER_INT_ENABLE):** When this bit is set, a thermal interrupt will be sent upon throttling due to power limitations.
23	0h RW	**Threshold2 Interrupt Enable (THRESHOLD_2_INT_ENABLE):** Controls the generation of a thermal interrupt whenever the Thermal Threshold 2 Temperature is crossed.
22:16	00h RW	**Threshold2 Relative Temperature (THRESHOLD_2_REL_TEMP):** This value indicates the offset in degrees below TjMax Temperature that should trigger a Thermal Threshold 2 trip.
15	0h RW	**Threshold1 Interrupt Enable (THRESHOLD_1_INT_ENABLE):** Controls the generation of a thermal interrupt whenever the Thermal Threshold 1 Temperature is crossed.
14:8	00h RW	**Threshold1 Relative Temperature (THRESHOLD_1_REL_TEMP):** This value indicates the offset in degrees below TjMax Temperature that should trigger a Thermal Threshold 1 trip.
7:5	0h RO	**Reserved**
4	0h RW	**Out Of Spec Interrupt Enable (OUT_OF_SPEC_INT_ENABLE):** Thermal interrupt enable for the critical temperature condition which is stored in the Critical Temperature Status bit in IA32_THERM_STATUS.
3	0h RO	**Reserved**
2	0h RW	**Bidirectional PROCHOT# Interrupt Enable (PROCHOT_INT_ENABLE):** Bidirectional PROCHOT# assertion interrupt enable. If set, a thermal interrupt is delivered on the rising edge of xxPROCHOT#.
1	0h RW	**Low Temperature Interrupt Enable (LOW_TEMP_INT_ENABLE):** Enables a thermal interrupt to be generated on the transition from a high-temperature to a low-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.
0	0h RW	**High Temperature Interrupt Enable (HIGH_TEMP_INT_ENABLE):** Enables a thermal interrupt to be generated on the transition from a low-temperature to a high-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.

3.3.32 Device Idle Duration Override (DEVICE_IDLE_DURATION_OVERRIDE_0_0_0_MCHBAR_PCU) — Offset 59C8h

MDID override register to be used by OS or software for debug purposes.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 59C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**Force MDID Override (FORCE_MDID_OVERRIDE):** When this bit is set, and bit 1 (the valid bit) is set, the value specified in this field will be used for MDID purposes. If this bit is clear, and bit 1 (the valid bit) is set, this value should be consumed along with the other MDID registers to determine which value is expiring next and reporting that value.
29	0h RW	**Disable MDID Evaluation (DISABLE_MDID_EVALUATION):** Send a value of disabled to the PCH for the MDID field.
28:8	000000h RW	**Next Device Activity (NEXT_DEVICE_ACTIVITY):** These are in 1us increments and can report a maximum value of approximately 2 seconds
7	0h RW	**Interrupt or Memory (IM):** 0: Interrupt. This is a hint for the idle duration time to the next interrupt. 1: Memory. This is a hint for the idle duration time to the next snoop cycle.
6	0h RW	**Opportunistic or Deterministic (OD):** 0: Opportunistic. This is an opportunistic hint as suggested by the sub-system. 1: Deterministic. This is a deterministic hint as suggested by the sub-system.
5:2	0h RO	**Reserved**
1	0h RW	**VALID:** 0: This Idle Duration Override CSR is not valid 1: This Idle Duration Override CSR is valid
0	0h RO	**Reserved**

3.3.33 Package GT C0 EUs SUM (PKG_GT_C0_EUS_SUM) — Offset 59F0h

The counter value is incremented when PKG_GT_C0_ANY_SLICE increments.

Counts in 24Mhz units.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 59F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** Counter value

3.3.34 Package GT C0 Media Sum (PKG_GT_C0_MEDIA_SUM) — Offset 59F8h

The counter value is incremented when PKG_GT_C0_ANY_SLICE increments.

Counts in 24Mhz units.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 59F8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** Counter value.

3.3.35 FIVR FFFC EMI Control (FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU) — Offset 5A08h

FIVR FFFC Control Register

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5A08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA:** Data field.

3.3.36 FIVR FFFC RFI Control (FFFC_RFI_CONTROL_0_0_0_MCHBAR_PCU) — Offset 5A0Ch

Fivr FFFC Control Register

Note: Bit definitions are the same as FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU, offset 5A08h.

3.3.37 FIVR FFFC RFI Control 2 (FFFC_RFI_CONTROL2_0_0_0_MCHBAR_PCU) — Offset 5A18h

Fivr FFFC Control Register

Note: Bit definitions are the same as FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU, offset 5A08h.

3.3.38 BIOS Mailbox Data (BIOS_MAILBOX_DATA_0_0_0_MCHBAR_PCU) — Offset 5DA0h

Data register for the BIOS-to-Firmware mailbox.

This register is used in conjunction with BIOS_MAILBOX_INTERFACE.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5DA0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**DATA:** This field contains the data associated with specific commands.

3.3.39 BIOS Mailbox Interface (BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR_PCU) — Offset 5DA4h

Control and Status register for the BIOS-to-Firmware mailbox.

This register is used in conjunction with BIOS_MAILBOX_DATA.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5DA4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Run/Busy Bit (RUN_BUSY):** SW may write to the two mailbox registers only when RUN_BUSY is cleared (0b). After setting this bit, SW will poll this bit until it is cleared. Firmware will clear RUN_BUSY after updating the mailbox registers with the result and error code.
30:29	0h RO	**Reserved**
28:16	0000h RW/V	**PARAM2:** This field contains additional parameters associated with specific commands. These are documented in the BIOS Writers Guide
15:8	00h RW/V	**PARAM1:** This field contains additional parameters associated with specific commands. These are documented in the BIOS Writers Guide
7:0	00h RW/V	**COMMAND:** On RUN_BUSY assertion this field should contain the SW request command, on RUN_BUSY deassrtion this field will contain the Firmware response code

3.3.40 BIOS Reset Complete (BIOS_RESET_CPL_0_0_0_MCHBAR_PCU) — Offset 5DA8h

This register is used as interface between BIOS and PCU. It is written by BIOS and read by PCU.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5DA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**PCIe Enumeration Done (PCIE_ENUMERATION_DONE):** This will be set after PCIe enumeration is done. This bit will be read by pcode. If it is set, pcode will look at the following register bits: MPVTDTRK_CR_DEVEN_0_0_0_PCI Bit Bit Name 1 D1F2EN 2 D1F1EN 3 D1F0EN If all of these bits are set to a 0x0, this means that there is nothing connected to the PEG devices and the Gen3 PLL can be shut off. Note: Implicit assumption - this bit is asserted prior to (or with) asserting RST_CPL.
0	0h RW/1S	**Reset Complete (RST_CPL):** This bit is set by BIOS to indicate to the CPU Power management function that it has completed to set up all PM relevant configuration and allow CPU Power management function to digest the configuration data and start active PM operation. It is expected that this bit will be set just before BIOS transfer of control to the OS. 0b: Not ready 1b: BIOS PM configuration complete

3.3.41 Memory Controller BIOS Request (MC_BIOS_REQ_0_0_0_MCHBAR_PCU) — Offset 5E00h

This register allows BIOS to request Memory Controller clock frequency.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5E00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RUN/BUSY Bit (RUN_BUSY):** This bit indicates that the BIOS request is pending. BIOS sets this bit together with a command in the lower bits of this register. The PCU may only clear this bit after the BIOS request has completed.
30:27	0h RW	**Request VDDQ TX IccMax (REQ_VDDQ_TX_ICCMAX):** Peak current on VDDQTX rail at this clock frequency and gear configuration. Described in 0.25A resolution. IccMax: 32 * 0.25 = 8A
26:17	000h RW	**Request VDDQ TX Voltage (REQ_VDDQ_TX_VOLTAGE):** Voltage of the VDDQ TX rail at this clock frequency and gear configuration. Described in 5mV resolution.
16:14	0h RO	**Reserved**
13:12	0h RW	**Gear Type (GEAR):** 0h: Gear1 (Default) - DDR bus clock is the same as QCLK 1h: Gear2 - DDR PHY bus clock is double of QCLK 2h: Gear4 - DDR PHY bus clock is quad of QCLK
11:8	0h RW	**Reference Clock Type (MC_PLL_REF):** Request Type: 0h - MC frequency request for 133MHz Qclk granularity. 1h - MC frequency request for 100MHz Qclk granularity. All other values are reserved.
7:0	00h RW	**MC PLL Ratio (MC_PLL_RATIO):** This field holds the memory controller frequency request (QCLK). Each bin is 133/100MHz and not 266/200MHz. This interface replaces the usage of DCLK ratios and Odd Ratio. QCLK frequency is determined by the MC reference clock (MC_FREQ_TYPE) as well as BCLK. Binary Dec DCLK Equation DCLK Freq QCLK Equation QCLK Freq 0000b 0d ----------------------------------- MC PLL - shutdown --- ... 0011b 3d 3 * 66.66 200.00 MHz 3 * 133.33 400.00 MHz 0100b 4d 4 * 66.66 266.66 MHz 4 * 133.33 533.33 MHz 0101b 5d 5 * 66.66 333.33 MHz 5 * 133.33 666.67 MHz 0110b 6d 6 * 66.66 400.00 MHz 6 * 133.33 800.00 MHz 0111b 7d 7 * 66.66 466.66 MHz 7 * 133.33 933.33 MHz 1000b 8d 8 * 66.66 533.33 MHz 8 * 133.33 1066.67 MHz ...

3.3.42 Memory Controller BIOS Data (MC_BIOS_DATA_0_0_0_MCHBAR_PCU) — Offset 5E04h

Memory Controller Frequency information for BIOS, during MRC flow.

Reflects the last frequency requested in MC_BIOS_REQ_0_0_0_MCHBAR_PCU.

In case of Dual MRC for System Agent SpeedStep, the value will change according to the MRC requests.

Post MRC will hold the last MRC request and not the current memory frequency.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5E04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	0h RW	**Request VDDQ TX IccMax (VDDQ_TX_ICCMAX):** Peak current on VDDQTX rail at this clock frequency and gear configuration. Described in 0.25A resolution. IccMax: 32 * 0.25 = 8A
26:17	000h RW	**Request VDDQ TX Voltage (VDDQ_TX_VOLTAGE):** Voltage of the VDDQ TX rail at this clock frequency and gear configuration. Described in 5mV resolution.
16:14	0h RO	**Reserved**
13:12	0h RW/L	**Gear Type (GEAR):** 0h: Gear1 (Default) - DDR bus clock is the same as QCLK 1h: Gear2 - DDR PHY bus clock is double of QCLK 2h: Gear4 - DDR PHY bus clock is quad of QCLK
11:8	0h RW/L	**Reference Clock Type (MC_PLL_REF):** This field holds the memory controller frequency Type. • 0h: MC frequency request for 133MHz Qclk granularity. • 1h: MC frequency request for 100MHz Qclk granularity. All other values are reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**MC PLL Ratio (MC_PLL_RATIO):** This field holds the memory controller frequency (QCLK). Each bin is 133/100MHz and not 266/200MHz. This interface replaces the usage of DCLK ratios and Odd Ratio. QCLK frequency is determined by the MC reference clock (MC_FREQ_TYPE) as well as BCLK. Binary Dec DCLK Equation DCLK Freq QCLK Equation QCLK Freq 0000b 0d ----------------------------------- MC PLL - shutdown --- ... 0011b 3d 3 * 66.66 200.00 MHz 3 * 133.33 400.00 MHz 0100b 4d 4 * 66.66 266.66 MHz 4 * 133.33 533.33 MHz 0101b 5d 5 * 66.66 333.33 MHz 5 * 133.33 666.67 MHz 0110b 6d 6 * 66.66 400.00 MHz 6 * 133.33 800.00 MHz 0111b 7d 7 * 66.66 466.66 MHz 7 * 133.33 933.33 MHz 1000b 8d 8 * 66.66 533.33 MHz 8 * 133.33 1066.67 MHz ... The values above are given in units of 133.33MHz (400/3). A value of zero implies that the memory controller PLL is shut down.

3.3.43 System Agent Power Management Control (SAPMCTL_0_0_0_MCHBAR_PCU) — Offset 5F00h

System Agent Power Management Control.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F00h	00002106h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Force Memory Master DLL When Display Engine is Active (MDLL_ON_DE):** Force memory master DLL on when the Display Engine is active. This includes cases where memory is not accessed. This bit has to be set only if there are issues with the memory DLL wakeup based on the Self Refresh exit indication from Display Engine. 0b: Display Engine wakes up memory DLL using the Self Refresh exit indication only 1b: Force Memory DLL on when the Display Engine is active
14	0h RW	**Force Memory Controller PLL When Display Engine is Active (MPLL_ON_DE):** Force Memory PLLs (MCPLL and GDPLL) on when the Display Engine is active. This includes cases where memory is not accessed. This bit has to be set only if there are issues with the Memory PLL wakeup based on the Self Refresh exit indication from the Display Engine. 0b: Display Engine wakes up Memory PLLs using the Self Refresh exit indication only 1b: Force Memory PLLs on when the Display Engine is active
13	1h RW	**System Agent Clock Gating Memory Controller PLL (SACG_MPLL):** When this bit is set to 1b, FCLK will never be gated when the memory controller PLL is ON. Otherwise, FCLK gating policies are not affected by the locking of the memory controller PLLs.
12	0h RW	**Non-Snoop Wake Self Refresh Exit (NSWAKE_SREXIT):** When this bit is set to 1b, a Non-Snoop wakeup signal from the PCH will cause the PCU to force the memory controller to exit from Self-Refresh. Otherwise, the Non-Snoop indication will not affect the Self Refresh exit policy.
11	0h RW	**System Agent Clock Gating Self Refresh Exit (SACG_SREXIT):** The Display Engine can indicate to the PCU that it wants the Memory Controller to exit self-refresh. When this bit is set to 1b, this request from the Display Engine will cause FCLK to be ungated. Otherwise, this request from the Display Engine has no effect on FCLK gating.
10	0h RW	**Master DLL Shutdown Power State Enable (MDLL_OFF_SEN):** This bit indicates when the Memory Master DLL may be shutdown based on link active power states. 0b: Memory DLL may be shut down in L1 and deeper sleep states. 1b: Memory DLL may be shut down in L0s and deeper sleep states.
9	0h RW	**Memory Controller PLL Shutdown Power State Enable (MPLL_OFF_SEN):** This bit indicates when the Memory PLLs (MCPLL and GDPLL) may be shutdown based on link active power states. 0b: Memory PLLs may be shut down in L1 and deeper sleep states. 1b: Memory PLLs may be shut down in L0s and deeper sleep states.
8	1h RW	**System Agent Clock Gating Power State Enable (SACG_SEN):** This bit indicates when the System Agent clock gating is possible based on link active power states. 0b: System Agent clock gating is allowed in L1 and deeper sleep states. 1b: System Agent clock gating is allowed in L0s and deeper sleep states.
7:3	0h RO	**Reserved**
2	1h RW	**PCIe PLL Shutdown Enable (PPLL_OFF_ENA):** This bit is used to enable shutting down the PCIe/DMI PLL. 0b: PLL shutdown is not allowed 1b: PLL shutdown is allowed
1	1h RW	**Memory Controller PLL Shutdown Enable (MPLL_OFF_ENA):** This bit is used to enable shutting down the Memory Controller PLLs (MCPLL and GDPLL). 0b: PLL shutdown is not allowed 1b: PLL shutdown is allowed

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**System Agent Clock Gating Enable (SACG_ENA):** This bit is used to enable or disable the System Agent Clock Gating (FCLK). 0b: System Agent Clock Gating is Not Allowed 1b: System Agent Clock Gating is Allowed

3.3.44 Configurable TDP Nominal (CONFIG_TDP_NOMINAL_0_0_0_MCHBAR_PCU) — Offset 5F3Ch

This register is used to indicate the Nominal Configurable TDP ratio available for this

specific sku. System BIOS must use this value while building the _PSS table if the feature is enabled.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TDP Ratio (TDP_RATIO):** Nominal TDP level ratio to be used for this specific processor (in units of 100MHz). Note: A value of 0 in this field indicates invalid/undefined TDP point.

3.3.45 Configurable TDP Level 1 (CONFIG_TDP_LEVEL1_0_0_0_MCHBAR_PCU) — Offset 5F40h

Level 1 Configurable TDP settings.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5F40h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**Reserved**
62:48	0000h RO/V	**Minimum Package Power (PKG_MIN_PWR):** Minimum package power setting allowed for this Configurable TDP level. Lower values will be clamped up to this value. Units defined in MSR PACKAGE_POWER_SKU[PWR_UNIT]. Similar to PACKAGE_POWER_SKU[PKG_MIN_PWR].
47	0h RO	**Reserved**
46:32	0000h RO/V	**Maximum Package Power (PKG_MAX_PWR):** Maximum package power setting allowed for this Configurable TDP level. Higher values will be clamped down to this value. Units defined in MSR PACKAGE_POWER_SKU[PWR_UNIT]. Similar to PACKAGE_POWER_SKU[PKG_MAX_PWR].
31:24	0h RO	**Reserved**
23:16	00h RO/V	**TDP Ratio (TDP_RATIO):** TDP ratio for this Configurable TDP Level.
15	0h RO	**Reserved**
14:0	0000h RO/V	**Package TDP (PKG_TDP):** Power Limit (PL1) for this Configurable TDP level. Units defined in MSR PACKAGE_POWER_SKU[PWR_UNIT] Similar to PACKAGE_POWER_SKU[PKG_TDP]

3.3.46 Configurable TDP Level 1 (CONFIG_TDP_LEVEL2_0_0_0_MCHBAR_PCU) — Offset 5F48h

Level 2 Configurable TDP settings.

Note: Bit definitions are the same as CONFIG_TDP_LEVEL1_0_0_0_MCHBAR_PCU, offset 5F40h.

3.3.47 Configurable TDP Control (CONFIG_TDP_CONTROL_0_0_0_MCHBAR_PCU) — Offset 5F50h

Rd/Wr register to allow platform SW to select TDP point and set lock

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Configurable TDP Lock (CONFIG_TDP_LOCK):** Configurable TDP level select lock. 0b: Unlocked. 1b: Locked till next reset. **Locked by:** CONFIG_TDP_CONTROL.CONFIG_TDP_LOCK
30:2	0h RO	**Reserved**
1:0	0h RW/L	**TDP Level (TDP_LEVEL):** Select Configurable TDP level: 0h: Nominal TDP level (default) 1h: Level from CONFIG_TDP_LEVEL_1 2h: Level from CONFIG_TDP_LEVEL_2 3h: Reserved **Locked by:** CONFIG_TDP_CONTROL.CONFIG_TDP_LOCK

3.3.48 Turbo Activation Ratio (TURBO_ACTIVATION_RATIO_0_0_0_MCHBAR_PCU) — Offset 5F54h

Read/write register to allow MSR/MMIO access to ACPI P-state notify (PCS 33).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Turbo Activation Ratio Lock (TURBO_ACTIVATION_RATIO_LOCK):** Locks this register until the next reset. 0b: Unlocked 1b: Locked **Locked by:** TURBO_ACTIVATION_RATIO.TURBO_ACTIVATION_RATIO_LOCK
30:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Maximum Non-Turbo Ratio (MAX_NON_TURBO_RATIO):** CPU will treat any P-state request above this ratio as a request for max turbo 0 is special encoding which disables the feature. **Locked by:** TURBO_ACTIVATION_RATIO.TURBO_ACTIVATION_RATIO_LOCK

3.3.49 Overclocking Status (OC_STATUS_0_0_0_MCHBAR_PCU) — Offset 5F58h

This register exposes the usage of various overclocking features.

Security oriented software can examine which overclocking features have been used and act accordingly.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**Memory Runtime Timing Overclocking Enabled (MC_TIMING_RUNTIME_OC_ENABLED):** Adjusting memory timing values for overclocking is enabled.

3.3.50 Base Clock (BCLK) Frequency (BCLK_FREQ_0_0_0_MCHBAR) — Offset 5F60h

This register reports the BCLK frequency.

It is used by software to calculate various clock frequencies that are derived from BCLK such as Core, Ring, Memory Controller and GT.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5F60h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:32	00000000h RO	**PCIECLK Frequency (PCIECLK_FREQ):** Reported PCIE BCLK Frequency in KHz
31:0	00000000h RO	**BCLK Frequency (BCLK_FREQ):** Reported BCLK Frequency in KHz

3.4 Host Controller (MCHBAR) Registers

This chapter documents the Host Controller MCHBAR registers.

Base address of these registers are defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.4.1 Summary of Registers

Table 3-5. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7090h	4	Type-C Sub-system Device Enable (TCSS_DEVEN_0_0_0_MCHBAR_IMPH)	00003FFFh
7094h	4	Capabilities D (CAPID0_D_0_0_0_MCHBAR)	00000000h
7098h	4	Capabilities F (CAPID0_F_0_0_0_PCI)	00000000h
7110h	8	REGBAR Base Address (REGBAR_0_0_0_MCHBAR_IMPH)	0000000000000000h

3.4.2 Type-C Sub-system Device Enable (TCSS_DEVEN_0_0_0_MCHBAR_IMPH) — Offset 7090h

Allows for enabling/disabling of Type-C PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7090h	00003FFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/L	**Thunderbolt DMA3 Enable (TBT_DMA3_EN):** 0: DMA3 is disabled and hidden. 1: DMA3 is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_TBT_DMA2_DIS
12	1h RW/L	**Thunderbolt DMA2 Enable (TBT_DMA2_EN):** 0: DMA2 is disabled and hidden. 1: DMA2 is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_TBT_DMA2_DIS
11	1h RW/L	**Thunderbolt DMA1 Enable (TBT_DMA1_EN):** 0: DMA1 is disabled and hidden. 1: DMA1 is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_TBT_DMA1_DIS
10	1h RW/L	**Thunderbolt DMA0 Enable (TBT_DMA0_EN):** 0: DMA0 is disabled and hidden. 1: DMA0 is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_TBT_DMA0_DIS
9	1h RW/L	**xDCI Enable (XDCI_EN):** 0: xDCI is disabled and hidden. 1: xDCI is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_XDCI_DIS
8	1h RW/L	**xHCI Enable (XHCI_EN):** 0: xHCI is disabled and hidden. 1: xHCI is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_XHCI_DIS
7	1h RW/L	**PCIe7 Enable (PCIE7_EN):** 0: TypeC PCIE Root Port 7 is disabled 1: TypeC PCIE Root Port 7 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE7_DIS
6	1h RW/L	**PCIe6 Enable (PCIE6_EN):** 0: TypeC PCIE Root Port 6 is disabled 1: TypeC PCIE Root Port 6 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE6_DIS
5	1h RW/L	**PCIe5 Enable (PCIE5_EN):** 0: TypeC PCIE Root Port 5 is disabled 1: TypeC PCIE Root Port 5 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE5_DIS
4	1h RW/L	**PCIe4 Enable (PCIE4_EN):** 0: TypeC PCIE Root Port 4 is disabled 1: TypeC PCIE Root Port 4 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE4_DIS

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW/L	**PCIe3 Enable (PCIE3_EN):** 0: TypeC PCIE Root Port 3 is disabled 1: TypeC PCIE Root Port 3 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE3_DIS
2	1h RW/L	**PCIe2 Enable (PCIE2_EN):** 0: TypeC PCIE Root Port 2 is disabled 1: TypeC PCIE Root Port 2 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE2_DIS
1	1h RW/L	**PCIe1 Enable (PCIE1_EN):** 0: TypeC PCIE Root Port 1 is disabled 1: TypeC PCIE Root Port 1 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE1_DIS
0	1h RW/L	**PCIE0 Enable (PCIE0_EN):** 0: TypeC PCIE Root Port 0 is disabled 1: TypeC PCIE Root Port 0 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE0_DIS

3.4.3 Capabilities D (CAPID0_D_0_0_0_MCHBAR) — Offset 7094h

Processor capability enumeration.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW/L	**DisplayPort Input Port Count (DPIN_PORT_COUNT):** This field indicates the max number of DPin ports.
16	0h RW/L	**TypeC Sub-system IOM Microcontroller Disable (IOM_DIS):** 0: Type C IOM is Enabled 1: Type C IOM is Disabled
15:13	0h RO	**Reserved**
12	0h RW/L	**TypeC Sub-system Thunderbolt DMA2 Disable (TC_TBT_DMA2_DIS):** Indicates if Type-C DMA2 device is disabled.
11	0h RW/L	**TypeC Sub-system Thunderbolt DMA1 Disable (TC_TBT_DMA1_DIS):** Indicates if Type-C DMA1 device is disabled.
10	0h RW/L	**TypeC Sub-system Thunderbolt DMA0 Disable (TC_TBT_DMA0_DIS):** Indicates if Type-C DMA0 device is disabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/L	**TypeC Sub-system USB xDCI Disable (TC_XDCI_DIS):** Indicates if Type-C XDCI device is disabled.
8	0h RW/L	**TypeC Sub-system USB xHCI Disable (TC_XHCI_DIS):** Indicates if Type-C XHCI device is disabled.
7	0h RW/L	**TypeC Sub-system PCIe7 Disable (TC_PCIE7_DIS):** PCIE7 disable.
6	0h RW/L	**TypeC Sub-system PCIe6 Disable (TC_PCIE6_DIS):** PCIE6 disable.
5	0h RW/L	**TypeC Sub-system PCIe5 Disable (TC_PCIE5_DIS):** PCIE5 disable.
4	0h RW/L	**TypeC Sub-system PCIe4 Disable (TC_PCIE4_DIS):** PCIE4 disable.
3	0h RW/L	**TypeC Sub-system PCIe3 Disable (TC_PCIE3_DIS):** PCIE3 disable.
2	0h RW/L	**TypeC Sub-system PCIe2 Disable (TC_PCIE2_DIS):** PCIE2 disable.
1	0h RW/L	**TypeC Sub-system PCIe1 Disable (TC_PCIE1_DIS):** PCIE1 disable.
0	0h RW/L	**TypeC Sub-system PCIe0 Disable (TC_PCIE0_DIS):** PCIE0 root port is disabled.

3.4.4 Capabilities F (CAPID0_F_0_0_0_PCI) — Offset 7098h

Processor capability enumeration.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW/L	**Max Data Rate at Gear1 (MAX_DATA_RATE_AT_GEAR1):** This field controls the max DDR data rate at Gear1 (equal to the QCLK ratio) in 100MHz granularity. 0 means unlimited

3.4.5 REGBAR Base Address (REGBAR_0_0_0_MCHBAR_IMPH) — Offset 7110h

Defines the base address for REGBAR.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 7110h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:24	00000h RW	**REGBAR Base Address (REGFBAR):** This field corresponds to bits 41 to 24 of the base address MMIO space. BIOS will program this register resulting in a base address for a 16MB block of contiguous memory address space.
23:1	0h RO	**Reserved**
0	0h RW	**REGBAR Enable (REGBAREN):** 0: REGBAR is disabled and does not claim any memory 1: REGBAR memory mapped accesses are claimed and decoded appropriately.

3.5 Direct Media Interface BAR (DMIBAR) Registers

This chapter documents the DMIBAR registers. Base address of these registers are defined in the DMIBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.5.1 Summary of Registers

Table 3-6. Summary of DMIBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Identifiers (ID)	00008086h
4h	2	Device Command (CMD)	0006h
6h	2	Primary Status (PSTS)	0090h
8h	4	Revision ID (RID_CC)	060000F0h
Eh	1	Header Type (HTYPE)	00h
1Eh	2	Secondary Status (SSTS)	0000h
2Ch	4	Subsystem Vendor IDs (SVD)	00000000h
34h	1	Capabilities List Pointer (CAPP)	E0h
3Eh	1	Bridge Control (BCTRL)	00h
44h	1	Device Capabilities (DCAP)	01h
48h	2	Device Control (DCTL)	0020h
4Ah	2	Device Status (DSTS)	0010h
4Ch	4	Link Capabilities (LCAP)	01714C10h
50h	2	Link Control (LCTL)	0040h
52h	2	Link Status (LSTS)	1011h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5Ch	2	Root Control (RCTL)	0000h
60h	4	Root Status (RSTS)	00000000h
64h	4	Device Capabilities 2 (DCAP2)	00080837h
68h	2	Device Control 2 (DCTL2)	0000h
6Ah	2	Device Status 2 (DSTS2)	0000h
6Ch	4	Link Capabilities 2 (LCAP2)	0000000Eh
70h	2	Link Control 2 (LCTL2)	0001h
72h	2	Link Status 2 (LSTS2)	0000h
74h	4	Slot Capabilities 2 (SLCAP2)	00000000h
78h	2	Slot Control 2 (SLCTL2)	0000h
7Ah	2	Slot Status 2 (SLSTS2)	0000h
80h	2	Message Signaled Interrupt Identifiers (MID)	9005h
82h	2	Message Signaled Interrupt Message (MC)	0000h
84h	4	Message Signaled Interrupt Message Address (MA)	00000000h
88h	2	Message Signaled Interrupt Message Data (MD)	0000h
90h	2	Subsystem Vendor Capability (SVCAP)	A00Dh
94h	4	Subsystem Vendor IDs (SVID)	00000000h
A0h	2	Power Management Capability (PMCAP)	0001h
A2h	2	PCI Power Management Capabilities (PMC)	C803h
A4h	4	PCI Power Management Control (PMCS)	00000008h
100h	4	Advanced Error Extended (AECH)	00000000h
104h	4	Uncorrectable Error Status (UES)	00000000h
108h	4	Uncorrectable Error Mask (UEM)	00000000h
10Ch	4	Uncorrectable Error Severity (UEV)	00060010h
110h	4	Correctable Error Status (CES)	00000000h
114h	4	Correctable Error Mask (CEM)	00002000h
118h	4	Advanced Error Capabilities And Control (AECC)	00000000h
11Ch	4	Header Log (HL_DW1)	00000000h
120h	4	Header Log (HL_DW2)	00000000h
124h	4	Header Log (HL_DW3)	00000000h
128h	4	Header Log (HL_DW4)	00000000h
12Ch	4	Root Error Command (REC)	00000000h
130h	4	Root Error Status (RES)	00000000h
134h	4	Error Source Identification (ESID)	00000000h
150h	4	PTM Extended Capability Header (PTMECH)	00000000h
284h	4	Port VC Capability Register 1 (PVCCR1)	00000000h
288h	4	Port VC Capability 2 (PVCC2)	00000000h
28Ch	2	Port VC Control (PVCC)	0000h
28Eh	2	Port VC Status (PVCS)	0000h
290h	4	Virtual Channel 0 Resource Capability (V0VCRC)	00000000h
294h	4	Virtual Channel 0 Resource Control (V0CTL)	80000001h

Offset	**Size (Bytes)**	**Register Name (Register Symbol)**	**Default Value**
29Ah	2	Virtual Channel 0 Resource Status (V0STS)	0000h
29Ch	4	Virtual Channel 1 Resource Capability (V1VCRC)	00000000h
2A0h	4	Virtual Channel 1 Resource Control (V1CTL)	00000000h
2A6h	2	Virtual Channel 1 Resource Status (V1STS)	0000h
A30h	4	Secondary PCI Express Extended Capability Header (SPEECH)	00000000h
A34h	4	Link Control 3 (LCTL3)	00000000h
A38h	4	Lane Error Status (LES)	00000000h
A3Ch	4	Lane 0 And Lane 1 Equalization Control (L01EC)	7F7F7F7Fh
A40h	4	Lane 2 And Lane 3 Equalization Control (L23EC)	7F7F7F7Fh
A44h	4	Lane 4 And Lane 5 Equalization Control (L45EC)	7F7F7F7Fh
A48h	4	Lane 6 And Lane 7 Equalization Control (L67EC)	7F7F7F7Fh
A4Ch	4	Lane 8 And Lane 9 Equalization Control (L89EC)	7F7F7F7Fh
A50h	4	Lane 10 And Lane 11 Equalization Control (L1011EC)	7F7F7F7Fh
A54h	4	Lane 12 And Lane 13 Equalization Control (L1213EC)	7F7F7F7Fh
A58h	4	Lane 14 And Lane 15 Equalization Control (L1415EC)	7F7F7F7Fh
A90h	4	Data Link Feature Extended Capability Header (DLFECH)	00000000h
A94h	4	Data Link Feature Capabilities Register (DLFCAP)	00000000h
A98h	4	Data Link Feature Status Register (DLFSTS)	00000000h
A9Ch	4	Physical Layer 16.0 GT/s Extended Capability Header (PL16GECH)	00000000h
AA0h	4	Physical Layer 16.0 GT/s Capability Register (PL16CAP)	00000000h
AA4h	4	Physical Layer 16.0 GT/s Control Register (PL16CTL)	00000000h
AA8h	4	Physical Layer 16.0 GT/s Status Register (PL16S)	00000000h
AACh	4	Physical Layer 16.0 GT/s Local Data Parity Mismatch Status Register (PL16LDPMS)	00000000h
AB0h	4	Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status Register (PL16FRDPMS)	00000000h
AB4h	4	Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status Register (PL16SRDPMS)	00000000h
AB8h	4	Physical Layer 16.0 GT/s Extra Status Register (PL16ES)	00000000h
ABCh	2	Physical Layer 16.0 GT/s Lane 01 Equalization Control Register (PL16L01EC)	FFFFh
ABEh	2	Physical Layer 16.0 GT/s Lane 23 Equalization Control Register (PL16L23EC)	FFFFh
AC0h	2	Physical Layer 16.0 GT/s Lane 45 Equalization Control Register (PL16L45EC)	FFFFh
AC2h	2	Physical Layer 16.0 GT/s Lane 67 Equalization Control Register (PL16L67EC)	FFFFh
AC4h	2	Physical Layer 16.0 GT/s Lane 89 Equalization Control Register (PL16L89EC)	FFFFh
AC6h	2	Physical Layer 16.0 GT/s Lane 1011 Equalization Control Register (PL16L1011EC)	FFFFh
AC8h	2	Physical Layer 16.0 GT/s Lane 1213 Equalization Control Register (PL16L1213EC)	FFFFh
ACAh	2	Physical Layer 16.0 GT/s Lane 1415 Equalization Control Register (PL16L1415EC)	FFFFh
C70h	4	VNN Removal Control (VNNREMCTL)	00000001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C74h	4	VNN Removal Save And Restore Hardware Contexts 1 (VNNRSNRC1)	00000000h
D00h	4	Device ID Override (DIDOVR)	00000000h
EDCh	4	Physical Layer 16.0 GT/s Margining Extended Capability Header (PL16MECH)	00010027h
EE0h	4	Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status (PL16MPCPS)	00000000h
EE4h	4	Physical Layer 16.0 GT/s Lane0 Margin Control and Status Register (PL16L0MCS)	00009C38h
EE8h	4	Physical Layer 16.0 GT/s Lane1 Margin Control and Status Register (PL16L1MCS)	00009C38h
EECh	4	Physical Layer 16.0 GT/s Lane2 Margin Control and Status Register (PL16L2MCS)	00009C38h
EF0h	4	Physical Layer 16.0 GT/s Lane3 Margin Control and Status Register (PL16L3MCS)	00009C38h
EF4h	4	Physical Layer 16.0 GT/s Lane4 Margin Control and Status Register (PL16L4MCS)	00009C38h
EF8h	4	Physical Layer 16.0 GT/s Lane5 Margin Control and Status Register (PL16L5MCS)	00009C38h
EFCh	4	Physical Layer 16.0 GT/s Lane6 Margin Control and Status Register (PL16L6MCS)	00009C38h
F00h	4	Physical Layer 16.0 GT/s Lane7 Margin Control and Status Register (PL16L7MCS)	00009C38h
F04h	4	Physical Layer 16.0 GT/s Lane8 Margin Control and Status Register (PL16L8MCS)	00009C38h
F08h	4	Physical Layer 16.0 GT/s Lane9 Margin Control and Status Register (PL16L9MCS)	00009C38h
F0Ch	4	Physical Layer 16.0 GT/s Lane10 Margin Control and Status Register (PL16L10MCS)	00009C38h
F10h	4	Physical Layer 16.0 GT/s Lane11 Margin Control and Status Register (PL16L11MCS)	00009C38h
F14h	4	Physical Layer 16.0 GT/s Lane12 Margin Control and Status Register (PL16L12MCS)	00009C38h
F18h	4	Physical Layer 16.0 GT/s Lane13 Margin Control and Status Register (PL16L13MCS)	00009C38h
F1Ch	4	Physical Layer 16.0 GT/s Lane14 Margin Control and Status Register (PL16L14MCS)	00009C38h
F20h	4	Physical Layer 16.0 GT/s Lane15 Margin Control and Status Register (PL16L15MCS)	00009C38h

3.5.2 Device Identifiers (ID) — Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Device Identification (DID):** See the Device ID table in the first volume of this document.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel.

3.5.3 Device Command (CMD) — Offset 4h

Device Command

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 4h	0006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	0h RO	**Fast Back to Back Enable (FBE):** This field is reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** This field is reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** This field is reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** This field is reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** This field is reserved per PCI-Express and PCI bridge spec.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	1h RO	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RO	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

3.5.4 Primary Status (PSTS) — Offset 6h

Primary Status

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 6h	0090h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCMD.PERE is not set.
14	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
13	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
12	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
11	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	0h RO	**Primary DEVSEL# Timing Status (PDTS):** This field is reserved per PCI-Express spec
8	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and PCMD.PERE is set.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Primary Fast Back to Back Capable (PFBC):** This field is reserved per PCI-Express spec.
6	0h RO	**Reserved**
5	0h RO	**Primary 66 MHz Capable (PC66):** This field is reserved per PCI-Express spec.
4	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
3	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
2:0	0h RO	**Reserved**

3.5.5 Revision ID (RID_CC) — Offset 8h

Revision ID

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 8h	060000F0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	00h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	00h RO/V	**Programming Interface (PI):** PCI-to-PCI bridge.
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge. The lower nibble, RID[7:0] of this register tracks the Revision ID of the SOC through Set ID Message received from Sideband interface.

3.5.6 Header Type (HTYPE) — Offset Eh

Header Type

Type	Size	Offset	Default
MMIO	8 bit	DMIBAR + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
6:0	00h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.

3.5.7 Secondary Status (SSTS) — Offset 1Eh

Secondary Status

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 1Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
14	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
13	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
12	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.
11	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
10:9	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** This field is reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
7	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** This field is reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
6	0h RO	**Reserved**
5	0h RO	**Secondary 66 MHz Capable (SC66):** This field is reserved per PCI Express spec
4:0	0h RO	**Reserved**

3.5.8 Subsystem Vendor IDs (SVD) — Offset 2Ch

Subsystem Vendor IDs

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/L	**Subsystem ID (SSID):** Values for the Subsystem ID are vendor specific. Subsystem ID values, in conjunction with the Subsystem Vendor ID, form a unique identifier for the PCI product. Subsystem ID and Device ID values are distinct and unrelated to each other, and software should not assume any relationship between them. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
15:0	0000h RW/L	**Subsystem Vendor ID (SVID):** The Subsystem Vendor ID register is used to uniquely identify the addin cardadapter or subsystem where the PCI Express component resides. They provide a mechanism for vendors to distinguish their products from one another even though the assemblies may have the same PCI Express component on them (and, therefore, the same Vendor ID and Device ID). This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL

3.5.9 Capabilities List Pointer (CAPP) — Offset 34h

Capabilities List Pointer

Type	Size	Offset	Default
MMIO	8 bit	DMIBAR + 34h	E0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	E0h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset | Capability | Next Pointer 40h | PCI Express | 80h 80h | Message Signaled Interrupt (MSI) | 90h 90h | Subsystem Vendor | A0h A0h | PCI Power Management | 00h Extended PCIe Capability Linked List Offset | Capability | Next Pointer 100h | Advanced Error Reporting | 000h 140h | Access Control Services | 000h 200h | L1 Sub-states | 000h 220h | Secondary PCI Express Capability | 000h

3.5.10 Bridge Control (BCTRL) — Offset 3Eh

Bridge Control

Type	Size	Offset	Default
MMIO	8 bit	DMIBAR + 3Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
0	0h RO	**Reserved**

3.5.11 Device Capabilities (DCAP) — Offset 44h

Device Capabilities

Type	Size	Offset	Default
MMIO	8 bit	DMIBAR + 44h	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2:0	1h RW/O	**Max Payload Size Supported (MPS):** Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

3.5.12 Device Control (DCTL) — Offset 48h

Device Control

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 48h	0020h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/P	**Aux Power PM Enable (APME):** Must be RW for OS testing. The OS will set this bit to '1' if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	1h RW	**Max Payload Size (MPS):** The root port supports up to 256B max payload. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisorary UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

3.5.13 Device Status (DSTS) — Offset 4Ah

Device Status

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 4Ah	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
4	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
3	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
2	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed TLP
1	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout
0	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

3.5.14 Link Capabilities (LCAP) — Offset 4Ch

Link Capabilities

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 4Ch	01714C10h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	01h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h : : X 0Xh Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
23	0h RO	**Reserved**
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the Root Port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** 0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b: Less than 1 us 001b: 1 us to less than 2 us 010b: 2 us to less than 4 us 011b: 4 us to less than 8 us 100b: 8 us to less than 16 us 101b: 16 us to less than 32 us 110b: 32 us to 64 us 111b: More than 64 us Note: If power management (e.g PLL shutdown) is enabled, BIOS should program this latency to comprehend PLL lock latency.

Bit Range	Default & Access	Field Name (ID): Description
14:12	4h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Support 01 L0s Supported 10 L1 Supported 11 L0s and L1 Supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	01h RO/V	**Maximum Link Width (MLW):** Indicates the maximum link width of the link 0x1: x1 Link Width 0x2: x2 Link Width 0x4: x4 Link Width 0x8: x8 Link Width 0x10: x16 Link Width
3:0	0h RO/V	**Max Link Speed (MLS):** This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This field reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through PCI Express Speed Limit setting or MPC.PCIESD register. This field reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through PCI Express Speed Limit setting or MPC.PCIESD register. Otherwise, this field reports a value of 0011b.

3.5.15 Link Control (LCTL) — Offset 50h

Link Control

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 50h	0040h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets. Default value of this bit is 0b.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved
7	0h RW	**Extended Sync (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	1h RO	**Common Clock Configuration (CCC):** Reserved
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT and LSTS.LTE to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW/L	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state. This register is read only when MPC.SRL field is set This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

3.5.16 Link Status (LSTS) — Offset 52h

Link Status

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 52h	1011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
14	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
13	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.

Bit Range	Default & Access	Field Name (ID): Description
12	1h RO/V	**Slot Clock Configuration (SCC):** In normal mode, Root Port uses the same reference clock as on the platform and does not generate its own clock. Note: When operating in PCI Express mode, the default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
11	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
10	0h RO	**Reserved**
9:4	01h RO/V	**Negotiated Link Width (NLW):** Negotiated link width. 0x1: x1 Link Width 0x2: x2 Link Width 0x4: x4 Link Width 0x8: x8 Link Width 0x10: x16 Link Width The value of this register is undefined if the link has not successfully trained.
3:0	1h RO/V	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.

3.5.17 Root Control (RCTL) — Offset 5Ch

Root Control

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 5Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependant on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependant on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependant on CMD.SEE being set.

3.5.18 Root Status (RSTS) — Offset 60h

Root Status

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requester ID will be updated, and this bit will be cleared. Root Ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requester ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0000h RO/V	**PME Requester ID (RID):** Indicates the PCI requester ID of the last PME requester. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

3.5.19 Device Capabilities 2 (DCAP2) — Offset 64h

Device Capabilities 2

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 64h	00080837h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b: OBFF is not supported. 01b: OBFF is supported using Message signaling only. 10b: OBFF is supported using WAKE# signaling only. 11b: OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system intialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. Note: OBFF is not supported. BIOS should program this field to 00b.
17	0h RW/O	**10-Bit Tag Requester Supported (PX10BTRS):** If this bit is Set, the Function supports 10-Bit Tag Requester capability. Otherwise, the Function does not. This bit must not be Set if the 10-Bit Tag Completer Supported bit is Clear.
16	0h RW/O	**10-Bit Tag Completer Supported (PX10BTCS):** If this bit is Set, the Function supports 10-Bit Tag Completer capability. Otherwise, the Function does not.
15:12	0h RO	**Reserved**
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability.
10	0h RO	**Reserved**
9	0h RW/O	**CAS Completer 128-bit Supported (AC128BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability.
8	0h RW/O	**AtomicOp Completer 64-bit Supported (AC64BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability
7	0h RW/O	**AtomicOp Completer 32-bit Supported (AC32BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability
6	0h RW/O	**Atomic Routing Supported (ARS):** This bit must be set to 1b if the Port supports this optional capability

Bit Range	Default & Access	Field Name (ID): Description
5	1h RO	**ARI Forwarding Supported (AFS):** Applicable only to Switch Downstream Ports and Root Ports - must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this bit 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A & B 0110b Ranges B & C 0111b Ranges A, B & C <-- This is what Root Port supports 1110b Ranges B, C & D 1111b Ranges A, B, C & D All other values are reserved.

3.5.20 Device Control 2 (DCTL2) — Offset 68h

Device Control 2

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 68h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** Optimized Buffer Flush/Fill Enable (OBFFEN): 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12	0h RW/V2	**10-Bit Tag Requester Enable (PX10BTRE):** This bit, in combination with the Extended Tag Field Enable bit in the Device Control register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is Set, the Requester is permitted to use 10-Bit Tags. Software should not change the value of this bit while the Function has outstanding Non-Posted Requests. Otherwise, the result is undefined. Functions that do not implement 10-Bit Tag Requester capability must hardwire this bit to 0b.
11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:8	0h RO	**Reserved**
7	0h RW	**AtomicOp Egress Blocking (AEB):** Applicable and mandatory for Switch Upstream Ports, Switch Downstream Ports, and Root Ports that implement AtomicOp routing capability - otherwise must be hardwired to 0b. When this bit is Set, AtomicOp Requests that target going out this Egress Port must be blocked.
6	0h RW	**AtomicOp Requester Enable (ARE):** Applicable only to Endpoints and Root Ports - must be hardwired to 0b for other Function types. The Function is allowed to initiate AtomicOp Requests only if this bit and the Bus Master Enable bit in the Command register are both Set. This bit is required to be RW if the Endpoint or Root Port is capable of initiating AtomicOp Requests, but otherwise is permitted to be hardwired to 0b. This bit does not serve as a capability bit. This bit is permitted to be RW even if no AtomicOp Requester capabilities are supported by the Endpoint or Root Port.
5	0h RW	**ARI Forwarding Enable (AFE):** When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The Root Port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50us to 100us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

3.5.21 Device Status 2 (DSTS2) — Offset 6Ah

Device Status 2

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 6Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

3.5.22 Link Capabilities 2 (LCAP2) — Offset 6Ch

Link Capabilities 2

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 6Ch	0000000Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/O	**Two Retimers Presence Detect Supported (TRPDS):** When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit must be set to 1b in a Downstream Port when the Supported Link Speeds Vector of the Link Capabilities 2 register indicates support for a Link speed of 16.0 GT/s or higher. It is permitted to be set to 1b regardless of the supported Link speeds, and in Upstream Ports, if the Retimer Presence Detect Supported bit is also set to 1b.
23	0h RW/O	**Retimer Presence Detect Supported (RPDS):** When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit must be set to 1b in a Downstream Port when the Supported Link Speeds Vector of the Link Capabilities 2 register indicates support for a Link speed of 16.0 GT/s or higher. It is permitted to be set to 1b regardless of the supported Link speeds and in Upstream Ports.

Bit Range	Default & Access	Field Name (ID): Description
22:16	00h RW/O	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bits 6:4 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
15:9	00h RW/O	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0GT/s Bits 6:4 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
8	0h RO	**Crosslink Supported (CS):** No support for Crosslink.
7:1	07h RO/V	**Supported Link Speeds Vector (SLSV):** This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported - otherwise, the Link speed is not supported. Bit definitions within this field for PCI Express are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bit 3: 16.0 GT/s Bits 6:3: Reserved.
0	0h RO	**Reserved**

3.5.23 Link Control 2 (LCTL2) — Offset 70h

Link Control 2

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 70h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is operating at 2.5 GT/s, the setting of this field has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Reserved**
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	1h RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by a driver to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

3.5.24 Link Status 2 (LSTS2) — Offset 72h

Link Status 2

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 72h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO/V/P	**Two Retimers Presence Detected (PX2RPD):** When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation. The default value of this bit is 0b. This bit is required for Ports that have the Two Retimers Presence Detect Supported bit of the Link Capabilities 2 register set to 1b. Ports that have the Two Retimers Presence Detect Supported bit set to 0b are permitted to hardwire this bit to 0b.
6	0h RO/V/P	**Retimer Presence Detected (RPD):** When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation. The default value of this bit is 0b. This bit is required for Ports that have the Retimer Presence Detect Supported bit Set. Ports that have the Retimer Presence Detect Supported bit of the Link Capabilities 2 register set to 0b are permitted to hardwire this bit to 0b.
5	0h RW/1C/V/P	**Link Equalization Request (LER):** This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link.
4	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** When set to 1, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
3	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** When set to 1, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
2	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** When set to 1, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
1	0h RO/V/P	**Equalization Complete (EQC):** When set to 1, this bit indicates that the Transmitter Equalization procedure at the 8.0GT/s data rate has completed.
0	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

3.5.25 Slot Capabilities 2 (SLCAP2) — Offset 74h

Slot Capabilities 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

3.5.26 Slot Control 2 (SLCTL2) — Offset 78h

Slot Control 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

3.5.27 Slot Status 2 (SLSTS2) — Offset 7Ah

Slot Status 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

3.5.28 Message Signaled Interrupt Identifiers (MID) — Offset 80h

Message Signaled Interrupt Identifiers

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 80h	9005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

3.5.29 Message Signaled Interrupt Message (MC) — Offset 82h

Message Signaled Interrupt Message

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 82h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
3:1	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

3.5.30 Message Signaled Interrupt Message Address (MA) — Offset 84h

Message Signaled Interrupt Message Address

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	**Reserved**

3.5.31 Message Signaled Interrupt Message Data (MD) — Offset 88h

Message Signaled Interrupt Message Data

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 88h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

3.5.32 Subsystem Vendor Capability (SVCAP) — Offset 90h

Subsystem Vendor Capability

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 90h	A00Dh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

3.5.33 Subsystem Vendor IDs (SVID) — Offset 94h

Subsystem Vendor IDs

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

3.5.34 Power Management Capability (PMCAP) — Offset A0h

Power Management Capability

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + A0h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	01h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

3.5.35 PCI Power Management Capabilities (PMC) — Offset A2h

PCI Power Management Capabilities

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + A2h	C803h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:11	19h RO	**PMES:** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Windows operating systems to enable PME# in devices connected behind this root port.
10	0h RO	**D2S:** The D2 state is not supported.
9	0h RO	**D1S:** The D1 state is not supported.
8:6	0h RO	**AC:** Reports 375mA maximum suspend well current required when in the D3COLD state.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification.

3.5.36 PCI Power Management Control (PMCS) — Offset A4h

PCI Power Management Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A4h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DTA:** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** This field is reserved per PCI Express specification

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**B2/B3 Support (B23S):** This field is reserved per PCI Express specification.
21:16	0h RO	**Reserved**
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Windows operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved**
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RO	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00: D0 state 11: D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

3.5.37 Advanced Error Extended (AECH) — Offset 100h

Advanced Error Extended

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

3.5.38 Uncorrectable Error Status (UES) — Offset 104h

Uncorrectable Error Status

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/1C/V/P	**Poisoned TLP Egress Blocked Status (PTLPEBS):** Indicates that poisoned TLP Egress Blocked error has occurred. Note: This bit can only be set if DPCCAPR.PTLPEBS = '1' and DPCCTLR.PTLPEBE = '1'.
25	0h RO	**Reserved**
24	0h RW/1C/V/P	**AtomicOp Egress Blocked Status (AEBS):** AtomicOp Egress Blocked Status
23:22	0h RO	**Reserved**
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Indicates an ACS Violation is logged.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Status (TE):** Not supported.

3.5.39 Uncorrectable Error Mask (UEM) — Offset 108h

Uncorrectable Error Mask

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Mask (PTLPEBM):** Mask for Poisoned TLP Egress Blocked error.
25	0h RO	**Reserved**
24	0h RW/P	**AtomicOp Egress Blocked Mask (AEBM):** Mask for AtomicOp Egress Blocked
23:22	0h RO	**Reserved**
21	0h RW/P	**ACS Violation Mask (AVM):** Mask for ACS Violation errors.
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Training Error Mask (TE):** Not supported.

3.5.40 Uncorrectable Error Severity (UEV) — Offset 10Ch

Uncorrectable Error Severity

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 10Ch	00060010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Severity (PTLPEBS):** Severity for Poisoned TLP Egress Blocked error.
25	0h RO	**Reserved**
24	0h RW/P	**AtomicOp Egress Blocked Severity (AEBS):** AtomicOp Egress Blocked Severity
23:22	0h RO	**Reserved**
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS Violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Severity (TE):** TE not supported.

3.5.41 Correctable Error Status (CES) — Offset 110h

Correctable Error Status

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

3.5.42 Correctable Error Mask (CEM) — Offset 114h

Correctable Error Mask

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 114h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved**
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	**Reserved**
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

3.5.43 Advanced Error Capabilities And Control (AECC) — Offset 118h

Advanced Error Capabilities And Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**Completion Timeout Prefix/Header Log Capable (CTPHLC):** If set, this bit indicates that port records the prefix/header of Request TLPs that experience a Completion Timeout error. Note: BIOS should program this bit before enable the Completion Timeout mechanism.
11:9	0h RO	**Reserved**
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	00h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

3.5.44 Header Log (HL_DW1) — Offset 11Ch

Header Log

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 11Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st DWORD of TLP (DW1):** Byte0 && Byte1 && Byte2 && Byte3

3.5.45 Header Log (HL_DW2) — Offset 120h

Header Log

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd DWORD of TLP (DW2):** Byte4 && Byte5 && Byte6 && Byte7

3.5.46 Header Log (HL_DW3) — Offset 124h

Header Log

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd DWORD of TLP (DW3):** Byte8 && Byte9 && Byte10 && Byte11

3.5.47 Header Log (HL_DW4) — Offset 128h

Header Log

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th DWORD of TLP (DW4):** Byte12 && Byte13 && Byte14 && Byte15

3.5.48 Root Error Command (REC) — Offset 12Ch

Root Error Command

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 12Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

3.5.49 Root Error Status (RES) — Offset 130h

Root Error Status

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved
26:7	0h RO	**Reserved**
6	0h RW/1C/V/P	**Fatal Error Messages Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

3.5.50 Error Source Identification (ESID) — Offset 134h

Error Source Identification

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requester ID if an internally detected error.
15:0	0000h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error.

3.5.51 PTM Extended Capability Header (PTMECH) — Offset 150h

PTM Extended Capability Header

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

3.5.52 Port VC Capability Register 1 (PVCCR1) — Offset 284h

Port VC Capability Register 1

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 284h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RO	**Function Arbitration Table Entry Size (FARES):** Indicates the size (in bits) of Function Arbitration table entry in the device. Defined encodings are: 00b Size of Function Arbitration table entry is 1 bit 01b Size of Function Arbitration table entry is 2 bits 10b Size of Function Arbitration table entry is 4 bits 11b Size of Function Arbitration table entry is 8 bits
9:8	0h RO	**Reference Clock (RC):** Indicates the reference clock for Virtual Channels that support time-based WRR Function Arbitration. Defined encodings are: 00b 100 ns reference clock 01b 11b Reserved
7	0h RO	**Reserved**
6:4	0h RO	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict priority VC Arbitration. The minimum value of this field is 000b and the maximum value is Extended VC Count.
3	0h RO	**Reserved**
2:0	0h RW/O	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The minimum value of this field is zero (for devices that only support the default VC). The maximum value is seven.

3.5.53 Port VC Capability 2 (PVCC2) — Offset 288h

Port VC Capability 2

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 288h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.
23:8	0h RO	**Reserved**
7:0	00h RO	**VC Arbitration Capability (VCAC):** Indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid for all devices that report a Low Priority Extended VC Count greater than 0. Each bit location within this field corresponds to a VC Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the device can be configured to provide different VC arbitration services. Defined bit positions are: Bit 0 Hardware fixed arbitration scheme, e.g., Round Robin Bit 1 Weighted Round Robin (WRR) arbitration with 32 phases Bit 2 WRR arbitration with 64 phases Bit 3 WRR arbitration with 128 phases Bits 4-7 Reserved

3.5.54 Port VC Control (PVCC) — Offset 28Ch

Port VC Control

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 28Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RW	**VC Arbitration Select (VCAS):** Used by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability register 2. The permissible values of this field are numbers corresponding to one of the asserted bits in the VC Arbitration Capability field. This field cannot be modified when more than one VC in the LPVC group is enabled.
0	0h WO	**Load VC Arbitration Table (LVCAT):** Used by software to update the VC Arbitration Table. This bit is valid when the selected VC Arbitration uses the VC Arbitration Table. Software Sets this bit to request hardware to apply new values programmed into VC Arbitration Table - Clearing this bit has no effect. Software checks the VC Arbitration Table Status bit to confirm that new values stored in the VC Arbitration Table are latched by the VC arbitration logic. This bit always returns 0b when read.

3.5.55 Port VC Status (PVCS) — Offset 28Eh

Port VC Status

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 28Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VC Arbitration Table Status (VCATS):** Indicates the coherency status of the VC Arbitration Table. This bit is valid when the selected VC uses the VC Arbitration Table. This bit is Set by hardware when any entry of the VC Arbitration Table is written by software. This bit is Cleared by hardware when hardware finishes loading values stored in the VC Arbitration Table after software sets the Load VC Arbitration Table bit in the Port VC Control register. Default value of this bit is 0b.

3.5.56 Virtual Channel 0 Resource Capability (V0VCRC) — Offset 290h

Virtual Channel 0 Resource Capability

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 290h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Function Arbitration Table Offset (FATO):** Indicates the location of the Function Arbitration Table associated with the VC resource. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.
23	0h RO	**Reserved**
22:16	00h RW/O	**Maximum Time Slots (MTS):** Indicates the maximum number of time slots (minus 1) that the VC resource is capable of supporting when it is configured for time-based WRR Function Arbitration. For example, a value of 000 0000b in this field indicates the supported maximum number of time slots is 1 and a value of 111 1111b indicates the supported maximum number of time slots is 128. This field is valid only when the Function Arbitration Capability indicates that the VC resource supports time-based WRR Function Arbitration.
15:8	0h RO	**Reserved**
7:0	00h RO	**Function Arbitration Capability (FAC):** Indicates types of Function Arbitration supported by the VC resource. Each bit location within this field corresponds to a Function Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Function Arbitration Select field. Defined bit positions are: Bit 0 Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) Bit 1 Weighted Round Robin (WRR) arbitration with 32 phases Bit 2 WRR arbitration with 64 phases Bit 3 WRR arbitration with 128 phases Bit 4 Time-based WRR with 128 phases Bit 5 WRR arbitration with 256 phases Bits 6-7 Reserved

3.5.57 Virtual Channel 0 Resource Control (V0CTL) — Offset 294h

Virtual Channel 0 Resource Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 294h	80000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** When Set, this bit enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. Default value of this bit is 1b for the first VC resource and 0b for other VC resource(s). Notes: 1. This bit is hardwired to 1b for the default VC (VC0), i.e., writing to this field has no effect for VC0. 2. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Set in both components on a Link. 3. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Cleared in both components on a Link. 4. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 5. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel.
30:27	0h RO	**Reserved**
26:24	0h RO	**Virtual Channel Identifier (ID):** This field assigns a VC ID to the VC resource. This field cannot be modified when the VC is already enabled. Note: For the first VC resource (default VC), this field is a read-only field that must be hardwired to 000b.
23:20	0h RO	**Reserved**
19:17	0h RW	**Function Arbitration Select (FAS):** This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.
16	0h RW	**Load Function Arbitration Table (LFAT):** When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table - clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
9:8	0h RO	**Reserved**
7:1	00h RW/L	**Transaction Class / Virtual Channel Map (TVM):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
0	1h RO	**Transaction Class / Virtual Channel Map TC0 (TVMT0):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.

3.5.58 Virtual Channel 0 Resource Status (V0STS) — Offset 29Ah

Virtual Channel 0 Resource Status

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 29Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO/V	**VC Negotiation Pending (NP):** This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. When this bit is Set by hardware, it indicates that the VC resource is still in the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete. For a nondefault Virtual Channel, software may use this bit when enabling or disabling the VC. For the default VC, this bit indicates the status of the process of Flow Control initialization. Before using a Virtual Channel, software must check whether the VC Negotiation Pending bits for that Virtual Channel are Clear in both components on a Link.
0	0h RO	**Function Arbitration Table Status (FATS):** This bit indicates the coherency status of the Function Arbitration Table associated with the VC resource. This bit is valid only when the Function Arbitration Table is used by the selected Function Arbitration for the VC resource. This bit is Set by hardware when any entry of the Function Arbitration Table is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the Function Arbitration Table after software sets the Load FunctionArbitration Table bit. Default value of this bit is 0b

3.5.59 Virtual Channel 1 Resource Capability (V1VCRC) — Offset 29Ch

Virtual Channel 1 Resource Capability

Note: Bit definitions are the same as V0VCRC, offset 290h.

3.5.60 Virtual Channel 1 Resource Control (V1CTL) — Offset 2A0h

Virtual Channel 1 Resource Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 2A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
30:28	0h RO	**Reserved**
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel Note: BIOS is required to program VCID[3] to 0 when operating at DMI2. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL

Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RO	**Reserved**
19:17	0h RW	**Function Arbitration Select (FAS):** This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.
16	0h RW	**Load Function Arbitration Table (LFAT):** When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table - clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
9:8	0h RO	**Reserved**
7:1	00h RW/L	**Transaction Class / Virtual Channel Map (TVM):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
0	0h RO	**Reserved**

3.5.61 Virtual Channel 1 Resource Status (V1STS) — Offset 2A6h

Virtual Channel 1 Resource Status

Note: Bit definitions are the same as V0STS, offset 29Ah.

3.5.62 Secondary PCI Express Extended Capability Header (SPEECH) — Offset A30h

Secondary PCI Express Extended Capability Header

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

3.5.63 Link Control 3 (LCTL3) — Offset A34h

Link Control 3

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RW	**Enable Lower SKP OS Generation Vector (ELSOSGV):** When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bits 6:4 Rsvd Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved**
1	0h RW/P	**Link Equalization Request Interrupt Enable (LERIE):** When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW/1S/V	**Perform Equalization (PE):** When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization Phase 1.

3.5.64 Lane Error Status (LES) — Offset A38h

Lane Error Status

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V/P	**Lane 15 Error Status (L15ES):** Lane 15 detected a Lane-based error.
14	0h RW/1C/V/P	**Lane 14 Error Status (L14ES):** Lane 14 detected a Lane-based error.
13	0h RW/1C/V/P	**Lane 13 Error Status (L13ES):** Lane 13 detected a Lane-based error.
12	0h RW/1C/V/P	**Lane 12 Error Status (L12ES):** Lane 12 detected a Lane-based error.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C/V/P	**Lane 11 Error Status (L11ES):** Lane 11 detected a Lane-based error.
10	0h RW/1C/V/P	**Lane 10 Error Status (L10ES):** Lane 10 detected a Lane-based error.
9	0h RW/1C/V/P	**Lane 9 Error Status (L9ES):** Lane 9 detected a Lane-based error.
8	0h RW/1C/V/P	**Lane 8 Error Status (L8ES):** Lane 8 detected a Lane-based error.
7	0h RW/1C/V/P	**Lane 7 Error Status (L7ES):** Lane 7 detected a Lane-based error.
6	0h RW/1C/V/P	**Lane 6 Error Status (L6ES):** Lane 6 detected a Lane-based error.
5	0h RW/1C/V/P	**Lane 5 Error Status (L5ES):** Lane 5 detected a Lane-based error.
4	0h RW/1C/V/P	**Lane 4 Error Status (L4ES):** Lane 4 detected a Lane-based error.
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 detected a Lane-based error.

3.5.65 Lane 0 And Lane 1 Equalization Control (L01EC) — Offset A3Ch

Lane 0 And Lane 1 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A3Ch	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.66 Lane 2 And Lane 3 Equalization Control (L23EC) — Offset A40h

Lane 2 And Lane 3 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A40h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset Hint (UPL3TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.67 Lane 4 And Lane 5 Equalization Control (L45EC) — Offset A44h

Lane 4 And Lane 5 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A44h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 5 Receiver Preset Hint (UPL5RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 5 Transmitter Preset (UPL5TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 5 Receiver Preset Hint (DPL5RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 5 Transmitter Preset (DPL5TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 4 Receiver Preset Hint (UPL4RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 4 Transmitter Preset (UPL4TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 4 Receiver Preset Hint (DPL4RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 4 Transmitter Preset (DPL4TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.68 Lane 6 And Lane 7 Equalization Control (L67EC) — Offset A48h

Lane 6 And Lane 7 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A48h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 7 Receiver Preset Hint (UPL7RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
27:24	Fh RW	**Upstream Port Lane 7 Transmitter Preset (UPL7TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 7 Receiver Preset Hint (DPL7RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 7 Transmitter Preset (DPL7TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 6 Receiver Preset Hint (UPL6RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 6 Transmitter Preset (UPL6TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 6 Receiver Preset Hint (DPL6RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 6 Transmitter Preset (DPL6TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.69 Lane 8 And Lane 9 Equalization Control (L89EC) — Offset A4Ch

Lane 8 And Lane 9 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A4Ch	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 9 Receiver Preset Hint (UPL9RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 9 Transmitter Preset (UPL9TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 9 Receiver Preset Hint (DPL9RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 9 Transmitter Preset (DPL9TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 8 Receiver Preset Hint (UPL8RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 8 Transmitter Preset (UPL8TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 8 Receiver Preset Hint (DPL8RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 8 Transmitter Preset (DPL8TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.70 Lane 10 And Lane 11 Equalization Control (L1011EC) — Offset A50h

Lane 10 And Lane 11 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A50h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 11 Receiver Preset Hint (UPL11RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 11 Transmitter Preset (UPL11TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 11 Receiver Preset Hint (DPL11RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 11 Transmitter Preset (DPL11TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 10 Receiver Preset Hint (UPL10RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Upstream Port Lane 10 Transmitter Preset (UPL10TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 10 Receiver Preset Hint (DPL10RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 10 Transmitter Preset (DPL10TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.71 Lane 12 And Lane 13 Equalization Control (L1213EC) — Offset A54h

Lane 12 And Lane 13 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A54h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 13 Receiver Preset Hint (UPL13RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 13 Transmitter Preset (UPL13TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 13 Receiver Preset Hint (DPL13RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 13 Transmitter Preset (DPL13TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 12 Receiver Preset Hint (UPL12RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 12 Transmitter Preset (UPL12TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 12 Receiver Preset Hint (DPL12RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 12 Transmitter Preset (DPL12TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.72 Lane 14 And Lane 15 Equalization Control (L1415EC) — Offset A58h

Lane 14 And Lane 15 Equalization Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A58h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 15 Receiver Preset Hint (UPL15RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
27:24	Fh RW	**Upstream Port Lane 15 Transmitter Preset (UPL15TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 15 Receiver Preset Hint (DPL15RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 15 Transmitter Preset (DPL15TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 14 Receiver Preset Hint (UPL14RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization.. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 14 Transmitter Preset (UPL14TP):** Field contains the Transmit Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 14 Receiver Preset Hint (DPL14RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 14 Transmitter Preset (DPL14TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.73 Data Link Feature Extended Capability Header (DLFECH) — Offset A90h

Data Link Feature Extended Capability Header

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability.

3.5.74 Data Link Feature Capabilities Register (DLFCAP) — Offset A94h

Data Link Feature Capabilities Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Data Link Feature Exchange Enable (DLFEE):** If set, this bit indicates that this Port will enter the DL_Feature negotiation state. Default is 1b.
30:23	0h RO	**Reserved**
22:1	000000h RW/O	**Local Feature Supported (LFS):** These bits indicate that the Downstream Port supports the associated Data Link Feature. For this version of this specification, this field is hardwired to 0.
0	0h RW/O	**Local Scaled Flow Control Supported (LSFCS):** This bit indicates that the Port supports the Scaled Flow Control Feature.

3.5.75 Data Link Feature Status Register (DLFSTS) — Offset A98h

Data Link Feature Status Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Data Link Feature Status Valid (DLFSV):** This bit indicates that the Downstream Port has received a Data Link Feature DLLP after the Link entered L0. When this bit is 1b, bits 23:0 are frozen. Software must clear this bit to re-enable capturing information. This bit is cleared on DL_Down.
30:23	0h RO	**Reserved**
22:1	000000h RO/V	**Remote Feature Supported (RFS):** These bits indicate that the Remote Port supports the corresponding Data Link Feature. These bits capture all information from the Data Link Feature DLLP even when this Port does not support the corresponding feature.
0	0h RO/V	**Remote Scaled Flow Control Supported (RSFCS):** This bit indicates that the Remote Port indicated it supports the Scaled Flow Control Feature

3.5.76 Physical Layer 16.0 GT/s Extended Capability Header (PL16GECH) — Offset A9Ch

Physical Layer 16.0 GT/s Extended Capability Header

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + A9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Physical Layer 16.0 GT/s Capability

3.5.77 Physical Layer 16.0 GT/s Capability Register (PL16CAP) — Offset AA0h

Physical Layer 16.0 GT/s Capability Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

3.5.78 Physical Layer 16.0 GT/s Control Register (PL16CTL) — Offset AA4h

Physical Layer 16.0 GT/s Control Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

3.5.79 Physical Layer 16.0 GT/s Status Register (PL16S) — Offset AA8h

Physical Layer 16.0 GT/s Status Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + AA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW/1C/V/P	**Link Equalization Request 16.0 GT/s (LERG4):** This bit is Set by hardware to request the 16.0 GT/s Link equalization process to be performed on the Link. The default value of this bit is 0b.
3	0h RO/V/P	**Equalization 16.0 GT/s Phase 3 Successful (EQP3SG4):** When set to 1b, this bit indicates that Phase 3 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V/P	**Equalization 16.0 GT/s Phase 2 Successful (EQP2SG4):** When set to 1b, this bit indicates that Phase 2 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.
1	0h RO/V/P	**Equalization 16.0 GT/s Phase 1 Successful (EQP1SG4):** When set to 1b, this bit indicates that Phase 1 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.
0	0h RO/V/P	**Equalization 16.0 GT/s Complete (EQG4):** When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 16.0 GT/s data rate has completed. The default value of this bit is 0b.

3.5.80 Physical Layer 16.0 GT/s Local Data Parity Mismatch Status Register (PL16LDPMS) — Offset AACh

Physical Layer 16.0 GT/s Local Data Parity Mismatch Status Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + AACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**Local Data Parity Mismatch Status (LDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

3.5.81 Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status Register (PL16FRDPMS) — Offset AB0h

Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + AB0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**First Retimer Data Parity Mismatch Status (FRDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

3.5.82 Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status Register (PL16SRDPMS) — Offset AB4h

Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + AB4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**Second Retimer Data Parity Mismatch Status (SRDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

3.5.83 Physical Layer 16.0 GT/s Extra Status Register (PL16ES) — Offset AB8h

Physical Layer 16.0 GT/s Extra Status Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

3.5.84 Physical Layer 16.0 GT/s Lane 01 Equalization Control Register (PL16L01EC) — Offset ABCh

Physical Layer 16.0 GT/s Lane 01 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + ABCh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 1 Transmitter Preset (UP16L1TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 1 Transmitter Preset (DP16L1TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 0 Transmitter Preset (UP16L0TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 0 Transmitter Preset (DP16L0TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.85 Physical Layer 16.0 GT/s Lane 23 Equalization Control Register (PL16L23EC) — Offset ABEh

Physical Layer 16.0 GT/s Lane 23 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + ABEh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 3 Transmitter Preset (UP16L3TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 3 Transmitter Preset (DP16L3TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 2 Transmitter Preset (UP16L2TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 2 Transmitter Preset (DP16L2TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.86 Physical Layer 16.0 GT/s Lane 45 Equalization Control Register (PL16L45EC) — Offset AC0h

Physical Layer 16.0 GT/s Lane 45 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + AC0h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 5 Transmitter Preset (UP16L5TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Downstream Port 16 GT/s Lane 5 Transmitter Preset (DP16L5TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 4 Transmitter Preset (UP16L4TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 4 Transmitter Preset (DP16L4TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.87 Physical Layer 16.0 GT/s Lane 67 Equalization Control Register (PL16L67EC) — Offset AC2h

Physical Layer 16.0 GT/s Lane 67 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + AC2h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 7 Transmitter Preset (UP16L7TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 7 Transmitter Preset (DP16L7TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 6 Transmitter Preset (UP16L6TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 6 Transmitter Preset (DP16L6TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.88 Physical Layer 16.0 GT/s Lane 89 Equalization Control Register (PL16L89EC) — Offset AC4h

Physical Layer 16.0 GT/s Lane 89 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + AC4h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 9 Transmitter Preset (UP16L9TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 9 Transmitter Preset (DP16L9TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 8 Transmitter Preset (UP16L8TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 8 Transmitter Preset (DP16L8TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.89 Physical Layer 16.0 GT/s Lane 1011 Equalization Control Register (PL16L1011EC) — Offset AC6h

Physical Layer 16.0 GT/s Lane 1011 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + AC6h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 11 Transmitter Preset (UP16L11TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 11 Transmitter Preset (DP16L11TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 10 Transmitter Preset (UP16L10TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 10 Transmitter Preset (DP16L10TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.90 Physical Layer 16.0 GT/s Lane 1213 Equalization Control Register (PL16L1213EC) — Offset AC8h

Physical Layer 16.0 GT/s Lane 1213 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + AC8h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 13 Transmitter Preset (UP16L13TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Downstream Port 16 GT/s Lane 13 Transmitter Preset (DP16L13TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 12 Transmitter Preset (UP16L12TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 12 Transmitter Preset (DP16L12TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.91 Physical Layer 16.0 GT/s Lane 1415 Equalization Control Register (PL16L1415EC) — Offset ACAh

Physical Layer 16.0 GT/s Lane 1415 Equalization Control Register

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + ACAh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 15 Transmitter Preset (UP16L15TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 15 Transmitter Preset (DP16L15TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 14 Transmitter Preset (UP16L14TP):** Field contains the Transmit Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 14 Transmitter Preset (DP16L14TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

3.5.92 VNN Removal Control (VNNREMCTL) — Offset C70h

VNN Removal Control

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + C70h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Receiver Eye Margin Error Tracking Mechanism Disable (REMETMD):** When this bit is set MAC will not track Error count during Receiver Equalization (EQ Phase 2 - PDMI, EQ Phase 3 - PCIe). Preset/Coeff evaluation will be based on FOM returned by PHY alone. This bit must be configured before training to GEN3 data rate.
30:9	0h RO	**Reserved**
8	0h RW	**Function Disable VNN Removal (FDVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link is function disable, so that VNN is allow to be remove when platform permitted.
7	0h RW	**Hot Plug VNN Removal Enable (HPVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when clkreq_b deassetion in Detect state, so that VNN is allow to be remove when platform permitted.
6	0h RW	**Detect Not PCIe VNN Removal Enable (DNPVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering Detect Not PCIe when link is unown, so that VNN is allow to be remove when platform permitted.
5	0h RW	**RTD3 VNN Removal Enable (RTD3VNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering L23 due to RTD3, so that VNN is allow to be remove when platform permitted.
4	0h RW	**Link Disable VNN Removal Enable (LDVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering Link Disable, so that VNN is allow to be remove when platform permitted.
3:2	0h RW	**Internal States Propagation Latency For VNN Removal Exit (ISPLFVNNRE):** This register configure internal delay of IP to allow boundary lock to deassert. This counter will start count after contexts propagation is done and early boundary lock is deassert. 00 8 osc clocks 01 16 osc clocks 10 32 osc clocks 11 64 osc clocks Note: For each x4 instance, only the value from Port 1 is used. This is a per controller register

Bit Range	Default & Access	Field Name (ID): Description
1:0	1h RW	**Link Reset Suppression Latency For VNN Removal Exit (LRSLFVNNRE):** This register configure the Link Reset Suppression latency after pmc had deassert restore_b during VNN Removal, and link clock pll had achieved lock. Link reset will be suppress upon IP Inaccessible exit with restore_b assertion, and the counter will start count when restore_b deassert with link clock had achieved lock. After timer expire, link reset will be deassert. 00 4 osc clocks 01 8 osc clocks 10 16 osc clocks 11 32 osc clocks Note: For each x4 instance, only the value from Port 1 is used. This is a per controller register

3.5.93 VNN Removal Save And Restore Hardware Contexts 1 (VNNRSNRC1) — Offset C74h

VNN Removal Save And Restore Hardware Contexts 1

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + C74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Spare 31 State Contexts (VNNS31SC):** Spare Flag for VNN Removal
30	0h RW	**VNN Spare 30 State Contexts (VNNS30SC):** Spare Flag for VNN Removal
29	0h RW	**VNN Spare 29 State Contexts (VNNS29SC):** Spare Flag for VNN Removal
28	0h RW	**VNN Spare 28 State Contexts (VNNS28SC):** Spare Flag for VNN Removal
27	0h RW	**VNN Spare 27 State Contexts (VNNS27SC):** Spare Flag for VNN Removal
26	0h RW	**VNN Spare 26 State Contexts (VNNS26SC):** Spare Flag for VNN Removal
25	0h RW	**VNN Spare 25 State Contexts (VNNS25SC):** Spare Flag for VNN Removal
24	0h RW	**VNN Spare 24 State Contexts (VNNS24SC):** Spare Flag for VNN Removal
23	0h RW	**VNN Spare 23 State Contexts (VNNS23SC):** Spare Flag for VNN Removal
22	0h RW	**VNN Spare 22 State Contexts (VNNS22SC):** Spare Flag for VNN Removal

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**VNN Spare 21 State Contexts (VNNS21SC):** Spare Flag for VNN Removal
20	0h RW	**VNN Spare 20 State Contexts (VNNS20SC):** Present Detect State Flag (PDS) information stored to this flag, so that link will restore back PDS upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
19	0h RW	**VNN Spare 19 State Contexts (VNNS19SC):** Spare Flag for VNN Removal
18	0h RW	**VNN Spare 18 State Contexts (VNNS18SC):** Spare Flag for VNN Removal
17	0h RW	**VNN Spare 17 State Contexts (VNNS17SC):** Spare Flag for VNN Removal
16	0h RW	**VNN Spare 16 State Contexts (VNNS16SC):** Spare Flag for VNN Removal
15	0h RW	**VNN Spare 15 State Contexts (VNNS15SC):** Spare Flag for VNN Removal
14	0h RW	**VNN Spare 14 State Contexts (VNNS14SC):** Spare Flag for VNN Removal
13	0h RW	**VNN Spare 13 State Contexts (VNNS13SC):** Spare Flag for VNN Removal
12	0h RW	**VNN Spare 12 State Contexts (VNNS12SC):** Spare Flag for VNN Removal
11	0h RW	**VNN Spare 11 State Contexts (VNNS11SC):** Spare Flag for VNN Removal
10	0h RW	**VNN Spare 10 State Contexts (VNNS10SC):** Spare Flag for VNN Removal
9	0h RW	**VNN Spare 9 State Contexts (VNNS9SC):** Spare Flag for VNN Removal
8	0h RW	**VNN Spare 8 State Contexts (VNNS8SC):** Spare Flag for VNN Removal
7	0h RW	**VNN Spare 7 State Contexts (VNNS7SC):** Spare Flag for VNN Removal
6	0h RW	**VNN Spare 6 State Contexts (VNNS6SC):** Spare Flag for VNN Removal
5	0h RW	**VNN Spare 5 State Contexts (VNNS5SC):** Link Down indicaton will be reflected here.
4	0h RW	**VNN Spare 4 State Contexts (VNNS4SC):** DL_ACTIVE (LA) information stored to this flag, so that link will restore back LA upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
3	0h RW	**VNN Spare 3 State Contexts (VNNS3SC):** Legacy Present Detect State Flag (PDS) information stored to this flag, so that link will restore back Legacy PDS Flag upon VNN Removal restoration. Based on PCIEALC.PDSP, this information or New PDS Implementation Context[20] will be selected. Writing to this registers have no effect unless restore_b is assert. Legacy Present Detect State Flag (PDS) information stored to this flag, so that link will restore back Legacy PDS Flag upon VNN Removal restoration. Based on PCIEALC.PDSP, this information or New PDS Implementation Context[20] will be selected. Writing to this registers have no effect unless restore_b is assert.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**VNN Detect Not PCIe State Contexts (VNNDNPSC):** When Link entered Detect Not PCIe state, LTSSM will push the link Detect Not PCIe state information to this flag, so that link will restore back to Detect Not PCIe state behavior upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
1	0h RW	**VNN L23 State Contexts (VNNL23SC):** When Link entered L23 state, LTSSM will push the link L23 state information to this flag, so that link will restore back to L23 state behavior (Actual State restore to Detect Quiet PG) upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
0	0h RW	**VNN Link Disable State Contexts (VNNLDSC):** When Link entered Link Disable state, LTSSM will push the link disable state information to this flag, so that link will restore back to disable state behavior (Actual State restore to Detect Quiet PG) upon VNN Removal restoration.

3.5.94 Device ID Override (DIDOVR) — Offset D00h

Device ID Override

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + D00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/L	**Device Identifier 0 Override Enable (DID0OVRE):** When this register is set, the register field DID0OVR will override DID bit [6:0] This register is Read-Only if LPCR.DIDOVR_LOCK field is set **Locked by:** LPCR.DIDOVR_LOCK
23:16	00h RW	**Device Identifier 0 Override (DID0OVR):** These bits will override the current DID bit[6:0] using the lower 7-bit of this register
15:9	0h RO	**Reserved**
8	0h RW/L	**Device Identifier 2 Override Enable (DID2OVRE):** When this register is set, the register field DID0OVR will override DID bit [6:0] This register is Read-Only if LPCR.DIDOVR_LOCK field is set **Locked by:** LPCR.DIDOVR_LOCK
7:0	00h RW	**Device Identifier 2 Override (DID2OVR):** These bits will override the current DID bit[6:0] using the lower 7-bit of this register

3.5.95 Physical Layer 16.0 GT/s Margining Extended Capability Header (PL16MECH) — Offset EDCh

Physical Layer 16.0 GT/s Margining Extended Capability Header

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + EDCh	00010027h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.
19:16	1h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0027h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Physical Layer 16.0 GT/s Margining Capability

3.5.96 Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status (PL16MPCPS) — Offset EE0h

Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + EE0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**Margining Software Ready (MARGINSWRDY):** When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO/V	**Margining Ready (MARGINRDY):** Indicates when the Margining feature is ready to accept margining commands. Behavior is undefined if this bit is Clear and, for any Lane, any of the Receiver Number, Margin Type, Usage Model, or Margin Payload fields are written. If Margining uses Driver Software is Set, Margining Ready must be Set no later than 100 ms after the later of Margining Software Ready becoming Set or the link training to 16.0 GT/s. If Margining uses Driver Software is Clear, Margining Ready must be Set no later than 100 ms after the Link trains to 16.0 GT/s.
15:1	0h RO	**Reserved**
0	0h RW/O	**Margining uses Driver Software (MARGINDRISW):** If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. In this case the value read from Margining Software Ready is undefined

3.5.97 Physical Layer 16.0 GT/s Lane0 Margin Control and Status Register (PL16L0MCS) — Offset EE4h

Physical Layer 16.0 GT/s Lane0 Margin Control and Status Register

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + EE4h	00009C38h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO/V	**Margin Payload Status (MPSTS):** This field is only meaningful, when the Margin Type This field must be reset to the default value if the Port goes to DL_Down status.
23	0h RO	**Reserved**
22	0h RO/V	**Usage Model Status (UMS):** This field must be reset to the default value if the Port goes to DL_Down status.
21:19	0h RO/V	**Margin Type Status (MTS):** This field must be reset to the default value if the Port goes to DL_Down status.
18:16	0h RO/V	**Receiver Number Status (RNS):** This field must be reset to the default value if the Port goes to DL_Down status.
15:8	9Ch RW	**Margin Payload (MP):** This fields value is used in conjunction with the Margin Type field. The default value is 9Ch. This field must be reset to the default value if the Port goes to DL_Down status.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Usage Model (UM):** The default value is 0b. This field must be reset to the default value if the Port goes to DL_Down status.
5:3	7h RW	**Margin Type (MT):** The default value is 111b. This field must be reset to the default value if the Port goes to DL_Down status.
2:0	0h RW	**Receiver Number (RN):** The default value is 000b. This field must be reset to the default value if the Port goes to DL_Down status.

3.5.98 Physical Layer 16.0 GT/s Lane1 Margin Control and Status Register (PL16L1MCS) — Offset EE8h

Physical Layer 16.0 GT/s Lane1 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.99 Physical Layer 16.0 GT/s Lane2 Margin Control and Status Register (PL16L2MCS) — Offset EECh

Physical Layer 16.0 GT/s Lane2 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.100 Physical Layer 16.0 GT/s Lane3 Margin Control and Status Register (PL16L3MCS) — Offset EF0h

Physical Layer 16.0 GT/s Lane3 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.101 Physical Layer 16.0 GT/s Lane4 Margin Control and Status Register (PL16L4MCS) — Offset EF4h

Physical Layer 16.0 GT/s Lane4 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.102 Physical Layer 16.0 GT/s Lane5 Margin Control and Status Register (PL16L5MCS) — Offset EF8h

Physical Layer 16.0 GT/s Lane5 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.103 Physical Layer 16.0 GT/s Lane6 Margin Control and Status Register (PL16L6MCS) — Offset EFCh

Physical Layer 16.0 GT/s Lane6 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.104 Physical Layer 16.0 GT/s Lane7 Margin Control and Status Register (PL16L7MCS) — Offset F00h

Physical Layer 16.0 GT/s Lane7 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.105 Physical Layer 16.0 GT/s Lane8 Margin Control and Status Register (PL16L8MCS) — Offset F04h

Physical Layer 16.0 GT/s Lane8 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.106 Physical Layer 16.0 GT/s Lane9 Margin Control and Status Register (PL16L9MCS) — Offset F08h

Physical Layer 16.0 GT/s Lane9 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.107 Physical Layer 16.0 GT/s Lane10 Margin Control and Status Register (PL16L10MCS) — Offset F0Ch

Physical Layer 16.0 GT/s Lane10 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.108 Physical Layer 16.0 GT/s Lane11 Margin Control and Status Register (PL16L11MCS) — Offset F10h

Physical Layer 16.0 GT/s Lane11 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.109 Physical Layer 16.0 GT/s Lane12 Margin Control and Status Register (PL16L12MCS) — Offset F14h

Physical Layer 16.0 GT/s Lane12 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.110 Physical Layer 16.0 GT/s Lane13 Margin Control and Status Register (PL16L13MCS) — Offset F18h

Physical Layer 16.0 GT/s Lane13 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.111 Physical Layer 16.0 GT/s Lane14 Margin Control and Status Register (PL16L14MCS) — Offset F1Ch

Physical Layer 16.0 GT/s Lane14 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.5.112 Physical Layer 16.0 GT/s Lane15 Margin Control and Status Register (PL16L15MCS) — Offset F20h

Physical Layer 16.0 GT/s Lane15 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

3.6 PCI Express Egress Port BAR (PXPEPBAR) Registers

This chapter documents the PXPEPBAR registers. Base address of these registers are defined in the PXPEPBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.6.1 Summary of Registers

Table 3-7. Summary of PXPEPBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Egress Port Virtual Channel Capabilities (EPVCECH)	04010002h
4h	4	Egress Port VC Capability Register 1 (EPPVCCAP1)	00000001h
8h	4	Egress Port VC Capability Register 2 (EPPVCCAP2)	00000000h
Ch	4	Egress Port VC Control (EPPVCCTL)	00000000h
10h	4	Egress Port Virtual Channel 0 Resource Capability (EPVC0RCAP)	00000001h
14h	4	Egress Port Virtual Channel 0 Resource Control (EPVC0RCTL)	800000FFh
1Ah	2	Egress Port Virtual Channel 0 Resource Status (EPVC0RSTS)	0000h
1Ch	4	Egress Port Virtual Channel 1 Resource Capability (EPVC1RCAP)	00008001h
20h	4	Egress Port Virtual Channel 1 Resource Control (EPVC1RCTL)	01000000h
26h	2	Egress Port Virtual Channel 1 Resource Status (EPVC1RSTS)	0000h
40h	4	Egress Port Capablity Declaration (EPRCLDECH)	00010005h
44h	4	Egress Port Element Declaration Capability (EPESD)	00000501h
50h	4	Egress Port Link Element Declaration 1 (EPLE1D)	01000000h
58h	4	Egress Port Link Another Root Complex Declaration 1 (EPLE1A)	00000000h
5Ch	4	Egress Port Second Link Declaration 1 (EPULE1A)	00000000h
60h	4	Egress Port Link Element Declaration 2 (EPLE2D)	02000002h
68h	4	Egress Port Link Another Root Complex Declaration 2 (EPLE2A)	00000000h
6Ch	4	Egress Port Second Link Declaration 2 (EPULE2A)	00000000h
70h	4	Egress Port Link Element Declaration 3 (EPLE3D)	03000002h
78h	4	Egress Port Link Another Root Complex Declaration 3 (EPLE3A)	00000000h
7Ch	4	Egress Port Second Link Declaration 3 (EPULE3A)	00000000h
80h	4	Egress Port Link Element Declaration 4 (EPLE4D)	04000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
88h	4	Egress Port Link Another Root Complex Declaration 4 (EPLE4A)	00000000h
8Ch	4	Egress Port Second Link Declaration 4 (EPULE4A)	00000000h
90h	4	Egress Port Link Element Declaration 5 (EPLE5D)	05000002h
98h	4	Egress Port Link Another Root Complex Declaration 5 (EPLE5A)	00000000h
9Ch	4	Egress Port Second Link Declaration 5 (EPULE5A)	00000000h
A0h	4	Miscellaneous Port Configuration PXPEPBAR (MPCP)	00000000h

3.6.2 Egress Port Virtual Channel Capabilities (EPVCECH) — Offset 0h

Egress Port Virtual Channel Capabilities

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 0h	04010002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	040h RO	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability). Bits [21:20] are reserved and software must mask them to allow for future uses of these bits
19:16	1h RO	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	0002h RO	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

3.6.3 Egress Port VC Capability Register 1 (EPPVCCAP1) — Offset 4h

Egress Port VC Capability Register 1

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 4h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RO	**Port Arbitration Table Entry Size (PATES):** Indicates that the size of the Port Arbitration table entry is 1 bit.
9:8	0h RO	**Reference Clock (RC):** Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. 00: 100 ns
7	0h RO	**Reserved**
6:4	0h RO	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	0h RO	**Reserved**
2:0	1h RW/L	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. **Locked by:** MPCP.SRL

3.6.4 Egress Port VC Capability Register 2 (EPPVCCAP2) — Offset 8h

Egress Port VC Capability Register 2

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

3.6.5 Egress Port VC Control (EPPVCCTL) — Offset Ch

Egress Port VC Control

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:1	0h RW	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled.
0	0h RO	**Reserved**

3.6.6 Egress Port Virtual Channel 0 Resource Capability (EPVC0RCAP) — Offset 10h

Egress Port Virtual Channel 0 Resource Capability

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 10h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**Port Arbitration Capability (PAC):** Indicates types of Port Arbitration supported by this VC0 resource. The default value of 01h indicates that the only port arbitration capability for VC0 is non-configurable, hardware-fixed arbitration scheme.

3.6.7 Egress Port Virtual Channel 0 Resource Control (EPVC0RCTL) — Offset 14h

Egress Port Virtual Channel 0 Resource Control

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 14h	800000FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**VC0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	0h RO	**Reserved**
26:24	0h RO	**VC0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	0h RO	**Reserved**
19:17	0h RW	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. The value of 0h corresponds to the bit position of the only asserted bit in the Port Arbitration Capability field.
16:8	0h RO	**Reserved**
7:1	7Fh RW	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	1h RO	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

3.6.8 Egress Port Virtual Channel 0 Resource Status (EPVC0RSTS) — Offset 1Ah

Egress Port Virtual Channel 0 Resource Status

Type	Size	Offset	Default
MMIO	16 bit	PXPEPBAR + 1Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO/V	**VC0 Negotiation Pending (VC0NP):** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). For this default VC, this bit indicates the status of the process of Flow Control initialization. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	0h RO	**Reserved**

3.6.9 Egress Port Virtual Channel 1 Resource Capability (EPVC1RCAP) — Offset 1Ch

Egress Port Virtual Channel 1 Resource Capability

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 1Ch	00008001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Port Arbitration Table Offset (PATO):** No VC0 port arbitration is necessary.
23	0h RO	**Reserved**
22:16	00h RO	**Maximum Time Slots (MTS):** No VC0 port arbitration is necessary.
15	1h RO	**Reject Snoop Transactions (RSNPT):** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**Port Arbitration Capability (PAC):** Indicates types of Port Arbitration supported by this VC1 resource. The default value of 01h indicates that the only port arbitration capability for VC1 is a non-configurable, hardware-fixed arbitration scheme.

3.6.10 Egress Port Virtual Channel 1 Resource Control (EPVC1RCTL) — Offset 20h

Egress Port Virtual Channel 1 Resource Control

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 20h	01000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VC1 Enable (VC1E):** This bit will be ignored by the hardware. The bit is R/W for specification compliance, but writing to it will result in no behavior change in the hardware (other than the bit value reflecting the written value). 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions in note below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. Notes 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27	0h RO	**Reserved**
26:24	1h RW	**VC1 ID (VC1ID):** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	0h RO	**Reserved**
19:17	0h RW	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. The default value of 0h corresponds to bit position of the only asserted bit in the Port Arbitration Capability field.
16:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7:1	00h RW	**TC/VC1 Map (TCVC1M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	0h RO	**TC0/VC1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

3.6.11 Egress Port Virtual Channel 1 Resource Status (EPVC1RSTS) — Offset 26h

Egress Port Virtual Channel 1 Resource Status

Type	Size	Offset	Default
MMIO	16 bit	PXPEPBAR + 26h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO/V	**VC1 Negotiation Pending (VC1NP):** The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). For this non-default Virtual Channel, software may use this bit when enabling or disabling the VC. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	0h RO	**Reserved**

3.6.12 Egress Port Capablity Declaration (EPRCLDECH) — Offset 40h

Egress Port Capablity Declaration

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 40h	00010005h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**Pointer to Next Capability (PNC):** This value terminates the PCI Express extended capabilities list associated with this RCRB.
19:16	1h RO	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	0005h RO	**Extended Capability ID (ECID):** Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

3.6.13 Egress Port Element Declaration Capability (EPESD) — Offset 44h

Egress Port Element Declaration Capability

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 44h	00000501h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	00h RW/L	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** MPCP.SRL
15:8	05h RO	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 5 (one each for PEG0, PEG11 PEG12, PEG1 and DMI).
7:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:0	1h RO	**Element Type (ET):** Indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.

3.6.14 Egress Port Link Element Declaration 1 (EPLE1D) — Offset 50h

Egress Port Link Element Declaration 1

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 50h	01000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	01h RO	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	00h RW/L	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** MPCP.SRL
15:2	0h RO	**Reserved**
1	0h RO	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	0h RW/L	**Link Valid (LV):** Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** MPCP.SRL

3.6.15 Egress Port Link Another Root Complex Declaration 1 (EPLE1A) — Offset 58h

Egress Port Link Another Root Complex Declaration 1

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW/L	**Low Link Address (LLA):** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry. **Locked by:** MPCP.SRL
11:0	0h RO	**Reserved**

3.6.16 Egress Port Second Link Declaration 1 (EPULE1A) — Offset 5Ch

Egress Port Second Link Declaration 1

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW/L	**Upper Link Address (ULA):** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry. **Locked by:** MPCP.SRL

3.6.17 Egress Port Link Element Declaration 2 (EPLE2D) — Offset 60h

Egress Port Link Element Declaration 2

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 60h	02000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	02h RO	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG1.0). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	00h RW/L	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** MPCP.SRL
15:2	0h RO	**Reserved**
1	1h RO	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port for PEG0. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	0h RW/L	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** MPCP.SRL

3.6.18 Egress Port Link Another Root Complex Declaration 2 (EPLE2A) — Offset 68h

Egress Port Link Another Root Complex Declaration 2

Note: Bit definitions are the same as EPLE1A, offset 58h.

3.6.19 Egress Port Second Link Declaration 2 (EPULE2A) — Offset 6Ch

Egress Port Second Link Declaration 2

Note: Bit definitions are the same as EPULE1A, offset 5Ch.

3.6.20 Egress Port Link Element Declaration 3 (EPLE3D) — Offset 70h

Egress Port Link Element Declaration 3

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 70h	03000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	03h RO	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG1.1). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	00h RW/L	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** MPCP.SRL
15:2	0h RO	**Reserved**
1	1h RO	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port for PEG1. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	0h RW/L	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** MPCP.SRL

3.6.21 Egress Port Link Another Root Complex Declaration 3 (EPLE3A) — Offset 78h

Egress Port Link Another Root Complex Declaration 3

Note: Bit definitions are the same as EPLE1A, offset 58h.

3.6.22 Egress Port Second Link Declaration 3 (EPULE3A) — Offset 7Ch

Egress Port Second Link Declaration 3

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 7Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW/L	**Upper Link Address (ULA):** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry **Locked by:** MPCP.SRL

3.6.23 Egress Port Link Element Declaration 4 (EPLE4D) — Offset 80h

Egress Port Link Element Declaration 4

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 80h	04000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RO	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG1.2). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	00h RW/L	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** MPCP.SRL
15:2	0h RO	**Reserved**
1	1h RO	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port for PEG1. The link address specifies the configuration address (segment, bus, device, function) of the target root port.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** MPCP.SRL

3.6.24 Egress Port Link Another Root Complex Declaration 4 (EPLE4A) — Offset 88h

Egress Port Link Another Root Complex Declaration 4

Note: Bit definitions are the same as EPLE1A, offset 58h.

3.6.25 Egress Port Second Link Declaration 4 (EPULE4A) — Offset 8Ch

Egress Port Second Link Declaration 4

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW/L	**Upper Link Address (ULA):** Upper Link Address: Memory mapped base address of the RCRB that is the target element (DMI) for this link entry. **Locked by:** MPCP.SRL

3.6.26 Egress Port Link Element Declaration 5 (EPLE5D) — Offset 90h

Egress Port Link Element Declaration 5

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 90h	05000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	05h RO	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (PEG6.0). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	00h RW/L	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** MPCP.SRL
15:2	0h RO	**Reserved**
1	1h RO	**Link Type (LTYP):** Indicates that the link points to configuration space of the integrated device which controls the x16 root port for PEG1. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	0h RW/L	**Link Valid (LV):** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** MPCP.SRL

3.6.27 Egress Port Link Another Root Complex Declaration 5 (EPLE5A) — Offset 98h

Egress Port Link Another Root Complex Declaration 5

Note: Bit definitions are the same as EPLE1A, offset 58h.

3.6.28 Egress Port Second Link Declaration 5 (EPULE5A) — Offset 9Ch

Egress Port Second Link Declaration 5

Note: Bit definitions are the same as EPULE4A, offset 8Ch.

3.6.29 Miscellaneous Port Configuration PXPEPBAR (MPCP) — Offset A0h

Miscellaneous Port Configuration PXPEPBAR

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Secured Register Lock (SRL):** When this bit is set, all the secured registers in PXPEPBAR will be locked and will be Read-Only. Refer to register description
30:0	0h RO	**Reserved**

3.7 VTDPVC0BAR Registers

This chapter documents the VC0PREMAP BAR registers. Base address of these registers are defined in the VTDPVC0BAR_0_0_0_MCHBAR_NCU register which resides in the MCHBAR register collection.

3.7.1 Summary of Registers

Table 3-8. Summary of VTDPVC0BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Version Register (VER_REG_0_0_0_VTDBAR)	00000050h
8h	8	Capability Register (CAP_REG_0_0_0_VTDBAR)	08D2008C40690462h
10h	8	Extended Capability Register (ECAP_REG_0_0_0_VTDBAR)	0000060000F050DAh
18h	4	Global Command Register (GCMD_REG_0_0_0_VTDBAR)	00000000h
1Ch	4	Global Status Register (GSTS_REG_0_0_0_VTDBAR)	00000000h
20h	8	Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR)	0000000000000000h
28h	8	Context Command Register (CCMD_REG_0_0_0_VTDBAR)	0800000000000000h
34h	4	Fault Status Register (FSTS_REG_0_0_0_VTDBAR)	00000000h
38h	4	Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR)	80000000h
3Ch	4	Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR)	00000000h
40h	4	Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR)	00000000h
44h	4	Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR)	00000000h
58h	8	Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR)	0000000000000000h
64h	4	Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR)	00000000h
68h	4	Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6Ch	4	Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR)	00000000h
70h	8	Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR)	0000000000000000h
78h	8	Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR)	0000000000000000h
80h	8	Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR)	0000000000000000h
88h	8	Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR)	0000000000000000h
90h	8	Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR)	0000000000000000h
9Ch	4	Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR)	00000000h
A0h	4	Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR)	80000000h
A4h	4	Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR)	00000000h
A8h	4	Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR)	00000000h
ACh	4	Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR)	00000000h
B8h	8	Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR)	0000000000000000h
C0h	8	Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR)	0000000000000000h
C8h	8	Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR)	0000000000000000h
D0h	8	Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR)	0000000000000000h
DCh	4	Page Request Status Register (PRS_REG_0_0_0_VTDBAR)	00000000h
E0h	4	Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR)	80000000h
E4h	4	Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR)	00000000h
E8h	4	Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR)	00000000h
ECh	4	Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR)	00000000h
100h	8	MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR)	0000000000000000h
108h	8	MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR)	0000000000000000h
120h	8	Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR)	0000000000000000h
128h	8	Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR)	0000000000000000h
130h	8	Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR)	0000000000000000h
138h	8	Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR)	0000000000000000h
140h	8	Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR)	0000000000000000h
148h	8	Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
150h	8	Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR)	0000000000000000h
158h	8	Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR)	0000000000000000h
160h	8	Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR)	0000000000000000h
168h	8	Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR)	0000000000000000h
170h	8	Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR)	0000000000000000h
180h	8	Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR)	0000000000000000h
188h	8	Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR)	0000000000000000h
190h	8	Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR)	0000000000000000h
198h	8	Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR)	0000000000000000h
1A0h	8	Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR)	0000000000000000h
1A8h	8	Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR)	0000000000000000h
1B0h	8	Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR)	0000000000000000h
1B8h	8	Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR)	0000000000000000h
1C0h	8	Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR)	0000000000000000h
1C8h	8	Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR)	0000000000000000h
1D0h	8	Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR)	0000000000000000h
1D8h	8	Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR)	0000000000000000h
1E0h	8	Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR)	0000000000000000h
1E8h	8	Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR)	0000000000000000h
1F0h	8	Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR)	0000000000000000h
1F8h	8	Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR)	0000000000000000h
200h	8	Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR)	0000000000000000h
208h	8	Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR)	0000000000000000h
210h	8	Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR)	0000000000000000h
218h	8	Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR)	0000000000000000h
400h	8	Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
408h	8	Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR)	0000000000000000h
500h	8	Invalidate Address Register (IVA_REG_0_0_0_VTDBAR)	0000000000000000h
508h	8	IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR)	0200000000000000h

3.7.2 Version Register (VER_REG_0_0_0_VTDBAR) — Offset 0h

Register to report the architecture version supported. Backward compatibility for the architecture is maintained with new revision numbers, allowing software to load remapping hardware drivers written for prior architecture versions.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 0h	00000050h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	5h RO/V	**Major Version Number (MAJOR):** Indicates supported architecture version.
3:0	0h RO/V	**Minor Version Number (MINOR):** Indicates supported architecture minor version.

3.7.3 Capability Register (CAP_REG_0_0_0_VTDBAR) — Offset 8h

Register to report general remapping hardware capabilities.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 8h	08D2008C40690462h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
60	0h RO/V	**First Level 5-level Paging (FL5LP):** • 0: Hardware does not support 5-level paging for requests-with-PASID subject to first-level translation. • 1: Hardware supports 5-level paging for requests-with-PASID subject to first-level translation.
59	1h RO/V	**Posted Interrupt Support (PI):** • 0 = Hardware does not support Posting of Interrupts. • 1 = Hardware supports Posting of Interrupts. Hardware implementations reporting this field as Set must also report Interrupt Remapping support (IR field in Extended Capability Register)
58:57	0h RO	**Reserved**
56	0h RO/V	**First Level 1-GByte Page Support (FL1GP):** A value of 1 in this field indicates 1-GByte page size is supported for first-level translation.
55	1h RO/V	**Read Draining (DRD):** • 0 = Hardware does not support draining of DMA read requests. • 1 = Hardware supports draining of DMA read requests.
54	1h RO/V	**Write Draining (DWD):** • 0 = Hardware does not support draining of DMA write requests. • 1 = Hardware supports draining of DMA write requests.
53:48	12h RO/V	**Maximum Address Mask Value (MAMV):** The value in this field indicates the maximum supported value for the Address Mask (AM) field in the Invalidation Address register (IVA_REG) and IOTLB Invalidation Descriptor (iotlb_inv_dsc) used for invalidations of second-level translation. This field is valid only when the PSI field in Capability register is reported as Set.
47:40	00h RO/V	**Number of Fault-Recording Registers (NFR):** Number of fault recording registers is computed as N+1, where N is the value reported in this field. Implementations must support at least one fault recording register (NFR = 0) for each remapping hardware unit in the platform. The maximum number of fault recording registers per remapping hardware unit is 256.
39	1h RO/V	**Page Selective Invalidation (PSI):** • 0 = Hardware supports only domain and global invalidates for IOTLB. • 1 = Hardware supports page selective, domain and global invalidates for IOTLB. Hardware implementations reporting this field as set are recommended to support a Maximum Address Mask Value (MAMV) value of at least 9 (or 18 if supporting 1GB pages with second level translation).
38	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
37:34	3h RO/V	**Second Level Large Page Support (SLLPS):** This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: • 0 = 21-bit offset to page frame (2MB) • 1 = 30-bit offset to page frame (1GB) • 2 = 39-bit offset to page frame (512GB) • 3 = 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.
33:24	040h RO/V	**Fault-Recording Register Offset (FRO):** This field specifies the location to the first fault recording register relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first fault recording register is calculated as X+(16*Y).
23	0h RO	**Reserved**
22	1h RO/V	**Zero Length Read (ZLR):** • 0 = Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. • 1 = Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages. DMA remapping hardware implementations are recommended to report ZLR field as Set.
21:16	29h RO/V	**Maximum Guest Address Width (MGAW):** This field indicates the maximum DMA virtual addressability supported by remapping hardware. The Maximum Guest Address Width (MGAW) is computed as (N+1), where N is the value reported in this field. For example, a hardware implementation supporting 48-bit MGAW reports a value of 47 (101111b) in this field. If the value in this field is X, untranslated and translated DMA requests to addresses above 2(x+1)-1 are always blocked by hardware. Translations requests to address above 2(x+1)-1 from allowed devices return a null Translation Completion Data Entry with R=W=0. Guest addressability for a given DMA request is limited to the minimum of the value reported through this field and the adjusted guest address width of the corresponding page-table structure. (Adjusted guest address widths supported by hardware are reported through the SAGAW field). Implementations are recommended to support MGAW at least equal to the physical addressability (host address width) of the platform.
15:13	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
12:8	04h RO/V	**Supported Adjusted Guest Address Widths (SAGAW):** This 5-bit field indicates the supported adjusted guest address widths (which in turn represents the levels of page-table walks for the 4KB base page size) supported by the hardware implementation. A value of 1 in any of these bits indicates the corresponding adjusted guest address width is supported. The adjusted guest address widths corresponding to various bit positions within this field are: • 0 = 30-bit AGAW (2-level page table) • 1 = 39-bit AGAW (3-level page table) • 2 = 48-bit AGAW (4-level page table) • 3 = 57-bit AGAW (5-level page table) • 4 = Reserved Software must ensure that the adjusted guest address width used to setup the page tables is one of the supported guest address widths reported in this field.
7	0h RO/V	**Caching Mode (CM):** • 0 = Not-present and erroneous entries are not cached in any of the remapping caches. Invalidations are not required for modifications to individual not present or invalid entries. However, any modifications that result in decreasing the effective permissions or partial permission increases require invalidations for them to be effective. • 1 = Not-present and erroneous mappings may be cached in the remapping caches. Any software updates to the remapping structures (including updates to not-present or erroneous entries) require explicit invalidation. Hardware implementations of this architecture must support a value of 0 in this field.
6	1h RO/V	**Protected High-Memory Region (PHMR):** • 0 = Indicates protected high-memory region is not supported. • 1 = Indicates protected high-memory region is supported.
5	1h RO/V	**Protected Low-Memory Region (PLMR):** • 0 = Indicates protected low-memory region is not supported. • 1 = Indicates protected low-memory region is supported.
4	0h RO/V	**Required Write-Buffer Flushing (RWBF):** • 0 = Indicates no write-buffer flushing is needed to ensure changes to memory-resident structures are visible to hardware. • 1 = Indicates software must explicitly flush the write buffers to ensure updates made to memory-resident remapping structures are visible to hardware.
3	0h RO/V	**Advanced Fault Logging (AFL):** • 0: Indicates advanced fault logging is not supported. Only primary fault logging is supported. • 1: Indicates advanced fault logging is supported.
2:0	2h RO/V	**Number of Domains Supported (ND):** • 000b: Hardware supports 4-bit domain-ids with support for up to 16 domains. • 001b: Hardware supports 6-bit domain-ids with support for up to 64 domains. • 010b: Hardware supports 8-bit domain-ids with support for up to 256 domains. • 011b: Hardware supports 10-bit domain-ids with support for up to 1024 domains. • 100b: Hardware supports 12-bit domain-ids with support for up to 4K domains. • 100b: Hardware supports 14-bit domain-ids with support for up to 16K domains. • 110b: Hardware supports 16-bit domain-ids with support for up to 64K domains. • 111b: Reserved.

3.7.4 Extended Capability Register (ECAP_REG_0_0_0_VTDBAR) — Offset 10h

Register to report remapping hardware extended capabilities.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 10h	0000060000F050DAh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:44	0h RO	**Reserved**
43	0h RO/V	**PASID Support Limitation (PSL):** This field is valid only when Process Address Space ID Support (PASID) field (bit 40) is reported as Set. When this field is reported as Set, extendedcontext-entries with PASID Enable (PASIDE) field Set do not support Requests-withoutPASID. Hardware implementations must report a value of 0 in this field. Virtual implementations may report a value of 1 in this field to disallow guest software from using an extended-context-entry for both Virtual Address (VA) and I/O Virtual Address (IOVA) concurrently.
42	1h RO/V	**Page Request Draining Support (PDS):** • 0 = Hardware does not support Page-Request Drain (PD) flag in Inv_wait_dsc. • 1 = Hardware supports Page-Request Drain (PD) flag in Inv_wait_dsc. This field is valid only when Device-TLB support field is reported as Set.
41	1h RO/V	**Device-TLB Invalidation Throttle (DIT):** • 0 = Hardware does not support Device-TLB Invalidation Throttling. • 1 = Hardware supports Device-TLB Invalidation Throttling. This field is valid only when Page Request Support (PRS) field is reported as Set.
40	0h RO/V	**Process Address Space ID Support (PASID):** • 0 = Hardware does not support requests tagged with Process Address Space IDs. • 1 = Hardware supports requests tagged with Process Address Space IDs.
39:35	00h RO/V	**PASID Size Supported (PSS):** This field reports the PASID size supported by the remapping hardware for requests-with-PASID. A value of N in this field indicates hardware supports PASID field of N+1 bits (For example, value of 7 in this field, indicates 8-bit PASIDs are supported). Requests-with-PASID with PASID value beyond the limit specified by this field are treated as error by the remapping hardware. This field is valid only when PASID field is reported as Set.
34	0h RO/V	**Extended Accessed Flag Support (EAFS):** • 0 = Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. • 1 = Hardware supports the extended accessed (EA) bit in first-level paging-structure entries. This field is valid only when PASID field is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RO/V	**No Write Flag Support (NWFS):** • 0 = Hardware ignores the No Write (NW) flag in Device-TLB translationrequests, and behaves as if NW is always 0. • 1 = Hardware supports the No Write (NW) flag in Device-TLB translationrequests. This field is valid only when Device-TLB support (DT) field is reported as Set.
32	0h RO	**Reserved**
31	0h RO/V	**Supervisor Request Support (SRS):** • 0 = H/W does not support requests-with-PASID seeking supervisor privilege. • 1 = H/W supports requests-with-PASID seeking supervisor privilege. The field is valid only when PASID field is reported as Set.
30	0h RO/V	**Execute Request Support (ERS):** • 0 = H/W does not support requests-with-PASID seeking execute permission. • 1 = H/W supports requests-with-PASID seeking execute permission. This field is valid only when PASID field is reported as Set.
29	0h RO/V	**Page Request Support (PRS):** • 0 = Hardware does not support Page Requests. • 1 = Hardware supports Page Requests This field is valid only when Device-TLB (DT) field is reported as Set.
28	0h RO/V	**ECAP Ignore (IGN):** Ignore this field
27	0h RO/V	**Deferred Invalidate Support (DIS):** • 0 = Hardware does not support deferred invalidations of IOTLB and Device-TLB. • 1 = Hardware supports deferred invalidations of IOTLB and Device-TLB. This field is valid only when PASID field is reported as Set.
26	0h RO/V	**Nested Translation Support (NEST):** • 0 = Hardware does not support nested translations. • 1 = Hardware supports nested translations. This field is valid only when PASID field is reported as Set.
25	0h RO/V	**Memory Type Support (MTS):** • 0 = Hardware does not support Memory Type in first-level translation and Extended Memory type in second-level translation. • 1 = Hardware supports Memory Type in first-level translation and Extended Memory type in second-level translation. This field is valid only when PASID and ECS fields are reported as Set. Remapping hardware units with, one or more devices that operate in processor coherency domain, under its scope must report this field as Set.
24	0h RO/V	**Extended Context Support (ECS):** • 0 = Hardware does not support extended-root-entries and extended-context-entries. • 1 = Hardware supports extended-root-entries and extended-context-entries. Implementations reporting PASID or PRS fields as Set, must report this field as Set.

Bit Range	Default & Access	Field Name (ID): Description
23:20	Fh RO/V	**Maximum Handle Mask Value (MHMV):** The value in this field indicates the maximum supported value for the Handle Mask (HM) field in the interrupt entry cache invalidation descriptor (iec_inv_dsc). This field is valid only when the IR field in Extended Capability register is reported as Set.
19:18	0h RO	**Reserved**
17:8	050h RO/V	**IOTLB Register Offset (IRO):** This field specifies the offset to the IOTLB registers relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first IOTLB invalidation register is calculated as X+(16*Y).
7	1h RO/V	**Snoop Control (SC):** • 0 = Hardware does not support 1-setting of the SNP field in the page-table entries. • 1 = Hardware supports the 1-setting of the SNP field in the page-table entries.
6	1h RO/V	**Pass Through (PT):** • 0 = Hardware does not support pass-through translation type in context entries and extended-context-entries. • 1 = Hardware supports pass-through translation type in context entries and extended-context-entries. Pass-through translation is specified through Translation-Type (T) field value of 10b in context-entries, or T field value of 010b in extended-context-entries. Hardware implementations supporting PASID must report a value of 1b in this field.
5	0h RO	**Reserved**
4	1h RO/V	**Extended Interrupt Mode (EIM):** • 0 = On Intel64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). • 1 = On Intel64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode). This field is valid only on Intel64 platforms reporting Interrupt Remapping support (IR field Set).
3	1h RO/V	**Interrupt Remapping support (IR):** • 0 = Hardware does not support interrupt remapping. • 1 = Hardware supports interrupt remapping. Implementations reporting this field as Set must also support Queued Invalidation (QI).
2	0h RO/V	**Device-TLB Support (DT):** • 0 = Hardware does not support device-IOTLBs. • 1 = Hardware supports Device-IOTLBs. Implementations reporting this field as Set must also support Queued Invalidation (QI). Hardware implementations supporting I/O Page Requests (PRS field Set in Extended Capability register) must report a value of 1b in this field.
1	1h RO/V	**Queued Invalidation Support (QI):** • 0 = Hardware does not support queued invalidations. • 1 = Hardware supports queued invalidations.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/V	**Page-Walk Coherency (C):** This field indicates if hardware access to the root, context, extended-context and interrupt-remap tables, and second-level paging structures for requests-without-PASID, are coherent (snooped) or not. • 0 = Indicates hardware accesses to remapping structures are non-coherent. • 1 = Indicates hardware accesses to remapping structures are coherent. Hardware access to advanced fault log, invalidation queue, invalidation semaphore, page-request queue, PASID-table, PASID-state table, and first-level page-tables are always coherent.

3.7.5 Global Command Register (GCMD_REG_0_0_0_VTDBAR) — Offset 18h

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

Register to control r mapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

- 1. Tmp = Read GSTS_REG
- 2. Status = (Tmp & 96FFFFFFh) // Reset the one-shot bits
- 3. Command = (Status | (Y << X))
- 4. Write Command to GCMD_REG
- 5. Wait until GSTS_REG[X] indicates command is serviced.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping: • 0 = Disable DMA remapping. • 1 = Enable DMA remapping. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA read/write requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30	0h WO	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address (RTA_REG) register. Hardware reports the status of the Set Root Table Pointer operation through the RTPS field in the Global Status register. The Set Root Table Pointer operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. .After a Set Root Table Pointer operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries. While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.
29	0h RO	**Set Fault Log (SFL):** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the Set Fault Log operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Enable Advanced Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: • 0 = Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. • 1 = Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.
27	0h RO	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26	0h WO	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. • 0 = Disable queued invalidations. • 1 = Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25	0h WO	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. • 0 = Disable interrupt-remapping hardware. • 1 = Enable interrupt-remapping hardware. Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
24	0h WO	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address (IRTA_REG) register. Hardware reports the status of the Set Interrupt Remap Table Pointer operation through the IRTPS field in the Global Status register. The Set Interrupt Remap Table Pointer operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After a Set Interrupt Remap Table Pointer operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23	0h WO	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Block Compatibility format interrupts. • 1 = Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.
22:0	0h RO	**Reserved**

3.7.6 Global Status Register (GSTS_REG_0_0_0_VTDBAR) — Offset 1Ch

Register to report general remapping hardware status.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Translation Enable Status (TES):** This field indicates the status of DMA-remapping hardware. • 0 = DMA-remapping hardware is not enabled. • 1 = DMA-remapping hardware is enabled
30	0h RO/V	**Root Table Pointer Status (RTPS):** This field indicates the status of the root- table pointer in hardware. This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware completes the Set Root Table Pointer operation using the value provided in the Root-Entry Table Address register.
29	0h RO	**Fault Log Status (FLS):** This field: • Is cleared by hardware when software Sets the SFL field in the Global Command register. • Is Set by hardware when hardware completes the Set Fault Log Pointer operation using the value provided in the Advanced Fault Log register.
28	0h RO	**Advanced Fault Logging Status (AFLS):** This field is valid only for implementations supporting advanced fault logging. It indicates the advanced fault logging status: • 0 = Advanced Fault Logging is not enabled. • 1 = Advanced Fault Logging is enabled.
27	0h RO	**Write Buffer Flush Status (WBFS):** This field is valid only for implementations requiring write buffer flushing. This field indicates the status of the write buffer flush command. It is: • Set by hardware when software sets the WBF field in the Global Command register. • Cleared by hardware when hardware completes the write buffer flushing operation.
26	0h RO/V	**Queued Invalidation Enable Status (QIES):** This field indicates queued invalidation enable status. • 0 = queued invalidation is not enabled. • 1 = queued invalidation is enabled
25	0h RO/V	**Interrupt Remapping Enable Status (IRES):** This field indicates the status of Interrupt-remapping hardware. • 0 = Interrupt-remapping hardware is not enabled. • 1 = Interrupt-remapping hardware is enabled

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO/V	**Interrupt Remapping Pointer Status (IRTPS):** This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is Set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23	0h RO/V	**Compatibility Format Interrupt Status (CFIS):** This field indicates the status of Compatibility format interrupts on Intel64 implementations supporting interrupt-remapping. The value reported in this field is applicable only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Compatibility format interrupts are blocked. • 1 = Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).
22:0	0h RO	**Reserved**

3.7.7 Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR) — Offset 20h

Register providing the base address of root-entry table.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 20h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**
51:12	00000000 00h RW	**Root Table Address (RTA):** This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
11	0h RW/V	**Root Table Type (RTT):** This field specifies the type of root-table referenced by the Root Table Address (RTA) field: • 0 = Root Table. • 1 = Extended Root Table
10:0	0h RO	**Reserved**

3.7.8 Context Command Register (CCMD_REG_0_0_0_VTDBAR) — Offset 28h

Register to manage context cache. The act of writing the uppermost byte of the CCMD_REG with the ICC field Set causes the hardware to perform the context-cache invalidation.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 28h	0800000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate Context Cache (ICC):** Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field is Clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must submit a context-cache invalidation request through this field only when there are no invalidation requests pending at this remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flush before invalidating the context cache.
62:61	0h RW	**Context Invalidation Request Granularity (CIRG):** Software provides the requested invalidation granularity through this field when setting the ICC field: • 00: Reserved. • 01: Global Invalidation request. • 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. • 11: Device-selective invalidation request. The target source-id(s) must be specified through the SID and FM fields, and the domain-id (that was programmed in the context-entry for these device(s)) must be provided in the DID field. Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.

Bit Range	Default & Access	Field Name (ID): Description
60:59	1h RO/V	**Context Actual Invalidation Granularity (CAIG):** Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field). The following are the encodings for this field: • 00: Reserved. • 01: Global Invalidation performed. This could be in response to a global, domain-selective or device-selective invalidation request. • 10: Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or device-selective invalidation request. • 11: Device-selective invalidation performed using the source-id and domain-id specified by software in the SID and FM fields. This can only be in response to a device-selective invalidation request.
58:34	0h RO	**Reserved**
33:32	0h WO	**Function Mask (FM):** Software may use the Function Mask to perform device-selective invalidations on behalf of devices supporting PCI Express Phantom Functions...This field specifies which bits of the function number portion (least significant three bits) of the SID field to mask when performing device-selective invalidations. The following encodings are defined for this field: • 00: No bits in the SID field masked. • 01: Mask most significant bit of function number in the SID field. • 10: Mask two most significant bit of function number in the SID field. • 11: Mask all three bits of function number in the SID field. The context-entries corresponding to all the source-ids specified through the FM and SID fields must have to the domain-id specified in the DID field.
31:16	0000h WO	**Source ID (SID):** Indicates the source-id of the device whose corresponding context-entry needs to be selectively invalidated. This field along with the FM field must be programmed by software for device-selective invalidation requests.
15:0	0000h RW	**Domain ID (DID):** Indicates the id of the domain whose context-entries need to be selectively invalidated. This field must be programmed by software for both domain-selective and device-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware may ignore and not implement bits15:N, where N is the supported domain-id width reported in the Capability register.

3.7.9 Fault Status Register (FSTS_REG_0_0_0_VTDBAR) — Offset 34h

Register indicating the various error status.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO/V	**Fault Record Index (FRI):** This field is valid only when the PPF field is Set. The FRI field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the PPF field was Set by hardware. The value read from this field is undefined when the PPF field is clear.
7	0h RW/1C/V/P	**Page Request Overflow (PRO):** Hardware detected a Page Request Overflow error. Hardware implementations not supporting the Page Request Queue implement this bit as RsvdZ.
6	0h RW/1C/V/P	**Invalidation Time-out Error (ITE):** Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting device Device-IOTLBs implement this bit as RsvdZ.
5	0h RW/1C/V/P	**Invalidation Completion Error (ICE):** Hardware received an unexpected or invalid Device-IOTLB invalidation completion. This could be due to either an invalid ITag or invalid source-id in an invalidation completion response. At this time, a fault event may be generated based on the programming of hte Fault Event Control register. Hardware implementations not supporting Device-IOTLBs implement this bit as RsvdZ.
4	0h RW/1C/V/P	**Invalidation Queue Error (IQE):** Hardware detected an error associated with the invalidation queue. This could be due to either a hardware error while fetching a descriptor from the invalidation queue, or hardware detecting an erroneous or invalid descriptor in the invalidation queue. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting queued invalidations implement this bit as RsvdZ.
3	0h RO/V	**Advanced Pending Fault (APF):** When this field is Clear, hardware sets this field when the first fault record (at index 0) is written to a fault log. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
2	0h RO/V	**Advanced Fault Overflow (AFO):** Hardware sets this field to indicate advanced fault log overflow condition. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO/V/P	**Primary Pending Fault (PPF):** This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this remapping hardware unit. • 0 = No pending faults in any of the fault recording registers. • 1 = One or more fault recording registers has pending faults. The FRI field is updated by hardware whenever the PPF field is set by hardware. Also, depending on the programming of Fault Event Control register, a fault event is generated when hardware sets this field.
0	0h RW/1C/V/P	**Primary Fault Overflow (PFO):** Hardware sets this field to indicate overflow of fault recording registers. Software writing 1 clears this field. When this field is Set, hardware does not record any new faults until software clears this field.

3.7.10 Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR) — Offset 38h

Register specifying the fault event interrupt message control bits.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 38h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0 = No masking of interrupt. When an interrupt condition is detected, hardware issues an interrupt message (using the Fault Event Data and Fault Event Address register values). • 1 = This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition, which is defined as: • When primary fault logging is active, an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. • When advanced fault logging is active, an interrupt condition occurs when hardware records a fault in the first fault record (at index 0) of the current fault log and sets the APF field in the Fault Status register. • Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. • Hardware detected invalid Device-IOTLB invalidation completion, setting the ICE field in the Fault Status register. • Hardware detected Device-IOTLB invalidation completion time-out, setting the ITE field in the Fault Status register. If any of the status fields in the Fault Status register was already Set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set or other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending, or due to software clearing the IM field. • Software servicing all the pending interrupt status fields in the Fault Status register as follows: - When primary fault logging is active, software clearing the Fault (F) field in all the Fault Recording registers with faults, causing the PPF field in Fault Status register to be evaluated as clear. - Software clearing other status fields in the Fault Status register by writing back the value read from the respective fields.
29:0	0h RO	**Reserved**

3.7.11 Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR) — Offset 3Ch

Register specifying the interrupt message data

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data may treat this field as RsvdZ.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

3.7.12 Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR) — Offset 40h

Register specifying the interrupt message address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

3.7.13 Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR) — Offset 44h

Register specifying the interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Extended Interrupt Mode are required to implement this register. Hardware implementations not supporting Extended Interrupt Mode may treat this field as RsvdZ.

3.7.14 Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR) — Offset 58h

Register to specify the base address of the memory-resident fault-log region. This register is treated as RsvdZ for implementations not supporting advanced translation fault logging (AFL field reported as 0 in the Capability register).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 58h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0000000000000h RO	**Fault Log Address (FLA):** This field specifies the base of 4KB aligned fault-log region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Software specifies the base address and size of the fault log region through this register, and programs it in hardware through the SFL field in the Global Command register. When implemented, reads of this field return the value that was last programmed to it.
11:9	0h RO	**Fault Log Size (FLS):** This field specifies the size of the fault log region pointed by the FLA field. The size of the fault log region is 2X * 4KB, where X is the value programmed in this register. When implemented, reads of this field return the value that was last programmed to it.
8:0	0h RO	**Reserved**

3.7.15 Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR) — Offset 64h

Register to enable the DMA-protected memory regions setup through the PLMBASE,..PLMLIMT, PHMBASE, PHMLIMIT registers. This register is always treated as RO for implementations not supporting protected memory regions (PLMR and PHMR fields reported as Clear in the Capability register).

Protected memory regions may be used by software to securely initialize remapping structures in memory. To avoid impact to legacy BIOS usage of memory, software is recommended to not overlap protected memory regions with any reserved memory regions of the platform reported through the Reserved Memory Region Reporting (RMRR) structures.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Protected Memory (EPM):** This field controls DMA accesses to the protected low-memory and protected high-memory regions. • 0 = Protected memory regions are disabled. • 1 = Protected memory regions are enabled.DMA requests accessing protected memory regions are handled as follows: - When DMA remapping is not enabled, all DMA requests accessing protected memory regions are blocked. - When DMA remapping is enabled: • DMA requests processed as pass-through (Translation Type value of 10b in Context-Entry) and accessing the protected memory regions are blocked. • DMA requests with translated address (AT=10b) and accessing the protected memory regions are blocked. • DMA requests that are subject to address remapping, and accessing the protected memory regions may or may not be blocked by hardware. For such requests, software must not depend on hardware protection of the protected memory regions, and instead program the DMA-remapping page-tables to not allow DMA to protected memory regions. Remapping hardware access to the remapping structures are not subject to protected memory region checks. DMA requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register.Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field. After writing to this field software must wait for the operation to be completed and reflected in the PRS status field (bit 0) before changing the value of this field again.
30:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/V	**Protected Region Status (PRS):** This field indicates the status of protected memory region(s): • 0 = Protected memory region(s) disabled. • 1 = Protected memory region(s) enabled.

3.7.16 Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR) — Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled.

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register).

The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant zero bit position with 0 in the value read back from the register. Bits N:0 of this register is decoded by hardware as all 0s...Software must setup the protected low memory region below 4GB.

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Base (PLMB):** This register specifies the base of protected low-memory region in system memory.
19:0	0h RO	**Reserved**

3.7.17 Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR) — Offset 6Ch

Register to set up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register)

The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The Protected low-memory base and limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits 31: (N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Limit (PLML):** This register specifies the last host physical address of the DMA-protected low-memory region in system memory.
19:0	0h RO	**Reserved**

3.7.18 Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR) — Offset 70h

Register to set up the base address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0s

Software may setup the protected high memory region either above or below 4GB

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 70h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW	**Protected High-Memory Base (PHMB):** This register specifies the base of protected (high) memory region in system memory Hardware ignores, and does not implement, bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

3.7.19 Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR) — Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The protected high-memory base & limit registers functions as follows

- Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 78h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW	**Protected High-Memory Limit (PHML):** This register specifies the last host physical address of the DMA-protected high-memory region in system memory Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

3.7.20 Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR) — Offset 80h

Register indicating the invalidation queue head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 80h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO/V	**Queue Head (QH):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware Hardware resets this field to 0 whenever the queued invalidation is disabled (QIES field Clear in the Global Status register).
3:0	0h RO	**Reserved**

3.7.21 Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR) — Offset 88h

Register indicating the invalidation tail head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 88h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW	**Queue Tail (QT):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.
3:0	0h RO	**Reserved**

3.7.22 Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR) — Offset 90h

Register to configure the base address and size of the invalidation queue. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 90h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RW	**Invalidation Queue Base Address (IQA):** This field points to the base of 4KB aligned invalidation request queue. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field return the value that was last programmed to it.
11:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Queue Size (QS):** This field specifies the size of the invalidation request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the invalidation queue is 2^(X + 8).

3.7.23 Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR) — Offset 9Ch

Register to report completion status of invalidation wait descriptor with Interrupt Flag (IF) Set

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Invalidation Wait Descriptor Complete (IWC):** Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field Set. Hardware implementations not supporting queued invalidations implement this field as RsvdZ.

3.7.24 Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR) — Offset A0h

Register specifying the invalidation event interrupt control bits

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + A0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0= No masking of interrupt. When a invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values) • 1= This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • An Invalidation Wait Descriptor with Interrupt Flag (IF) field Set completed, setting the IWC field in the Invalidation Completion Status register • If the IWC field in the Invalidation Completion Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • 0= Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • 1= Software servicing the IWC field in the Invalidation Completion Status register.
29:0	0h RO	**Reserved**

3.7.25 Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR) — Offset A4h

Register specifying the Invalidation Event interrupt message data

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields Hardware implementations supporting only 16-bit interrupt data treat this field as Rsvd.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

3.7.26 Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR) — Offset A8h

Register specifying the Invalidation Event Interrupt message address

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Note: Bit definitions are the same as FEADDR_REG_0_0_0_VTDBAR, offset 40h.

3.7.27 Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR) — Offset ACh

Register specifying the Invalidation Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Queued Invalidations and Extended Interrupt Mode are required to implement this register Hardware implementations not supporting Queued Invalidations or Extended Interrupt Mode may treat this field as RsvdZ.

3.7.28 Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR) — Offset B8h

Register providing the base address of Interrupt remapping table. This register is treated as RsvdZ by implementations reporting Interrupt Remapping (IR) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**
51:12	0000000000h RW/V	**Interrupt Remapping Table Address (IRTA):** This field points to the base of 4KB aligned interrupt remapping table Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field returns value that was last programmed to it.
11	0h RW/V	**Extended Interrupt Mode Enable (EIME):** This field is used by hardware on Intel64 platforms as follows: • 0=xAPIC mode is active. Hardware interprets only low 8-bits of Destination-ID field in the IRTEs. The high 24-bits of the Destination-ID field are treated as reserved • 1= x2APIC mode is active. Hardware interprets all 32-bits of Destination-ID field in the IRTEs This field is implemented as RsvdZ on implementations reporting Extended Interrupt Mode (EIM) field as Clear in Extended Capability register.
10:4	0h RO	**Reserved**
3:0	0h RW/V	**IRTA Size (S):** This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2(X+1), where X is the value programmed in this field.

3.7.29 Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR) — Offset C0h

Register indicating the page request queue head. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO	**Page Queue Head (PQH):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be processed next by software.
3:0	0h RO	**Reserved**

3.7.30 Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR) — Offset C8h

Register indicating the page request queue tail. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO/V	**Page Queue Tail (PQT):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be written next by hardware.
3:0	0h RO	**Reserved**

3.7.31 Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR) — Offset D0h

Register to configure the base address and size of the page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Page Request Queue Base Address (PQA):** This field points to the base of 4KB aligned page request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Software must configure this register before enabling page requests in any extended-context-entries.
11:3	0h RO	**Reserved**
2:0	0h RO	**Page Request Queue Size (PQS):** This field specifies the size of the page request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the page request queue is 2^(X + 8)

3.7.32 Page Request Status Register (PRS_REG_0_0_0_VTDBAR) — Offset DCh

Register to report pending page request in page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V/P	**Pending Page Request (PPR):** Pending Page Request: Indicates pending page requests to be serviced by software in the page request queue. This field is Set by hardware when a streaming page request entry (page_stream_reg_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, is added to the page request queue.

3.7.33 Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR) — Offset E0h

Register specifying the page request event interrupt control bits. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + E0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Interrupt Mask (IM):** Interrupt Mask • 0=No masking of interrupt. When a page request event condition is detected, hardware issues an interrupt message (using the Page Request Event Data and Page Request Event Address register values) • 1=This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Interrupt Pending: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • A streaming page request entry (page_stream_req_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, was added to page request queue, resulting in hardware setting the Pending Page Request (PPR) field in Page Request Status register • If the PPR field in the Page Request Event Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • Software servicing the PPR field in the Page Request Event Status register.
29:0	0h RO	**Reserved**

3.7.34 Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR) — Offset E4h

Register specifying the Page Request Event interrupt message data. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Extended Interrupt Message Data (EIMD):** Extended Interrupt Message Data
15:0	0000h RO	**Interrupt Message Data (IMD):** Interrupt Message Data: Data value in the interrupt request. Software requirements for programming this register are described in VTd Spec

3.7.35 Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR) — Offset E8h

Register specifying the Page Request Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Message Address (MA):** Message Address: When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

3.7.36 Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR) — Offset ECh

Register specifying the Page Request Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Message Upper Address (MUA):** Message Upper Address: This field specifies the upper address (bits.. 63:32) for the page request event interrupt.

3.7.37 MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR) — Offset 100h

Register reporting the Memory Type Range Register Capability. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

When implemented, value reported in this register must match IA32_MTRRCAP Model Specific Register (MSR) value reported by the host IA-32 processor(s).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 100h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:11	0h RO	**Reserved**
10	0h RO	**Write Combining (WC):** • 0 = Write-combining (WC) memory type is not supported. • 1 = Write-combining (WC) memory type is supported.Indicates whether the Write Combining memory type is supported.
9	0h RO	**Reserved**
8	0h RO	**Fixed Range MTRRs Supported (FIX):** • 0 = No fixed range MTRRs are supported • 1 = Fixed range MTRRs (MTRR_FIX64K_00000 through MTRR_FIX4K_0F8000) are supported
7:0	00h RO	**Variable MTRR Count (VCNT):** Indicates number of variable range MTRRs are supported.

3.7.38 MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR) — Offset 108h

Register for enabling/configuring Memory Type Range Registers. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 108h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Reserved**
11	0h RO	**MTRR Enable (E):** • 0 = Disable MTRRs; UC memory type is applied. FE field has no effect. • 1 = Enable MTRRs. FE field can disable the fixed-range MTRRs. Type specified in the default memory type field is used for areas of memory not already mapped by either fixed or variable MTRR
10	0h RO	**Fixed Range MTRR Enable (FE):** • 0 = Disable fixed range MTRRs. • 1 = Enable fixed range MTRRs. When fixed range MTRRs are enabled, they take priority over the variable range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed range MTRRs.
9:8	0h RO	**Reserved**
7:0	00h RO	**Default Memory Type (MEMTYPE):** Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0,1,4, 5 and 6.

3.7.39 Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR) — Offset 120h

Fixed Range MTRR covering the 64K memory space from 0x00000 - 0x7FFFF.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 120h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RO	**R7 IOMMU (R7):** Register Field 7
55:48	00h RO	**R6 IOMMU (R6):** Register Field 6
47:40	00h RO	**R5 IOMMU (R5):** Register Field 5
39:32	00h RO	**R4 IOMMU (R4):** Register Field 4
31:24	00h RO	**R3 IOMMU (R3):** Register Field 3
23:16	00h RO	**R2 IOMMU (R2):** Register Field 2
15:8	00h RO	**R1 IOMMU (R1):** Register Field 1
7:0	00h RO	**R0 IOMMU (R0):** Register Field 0

3.7.40 Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR) — Offset 128h

Fixed Range MTRR covering the 16K memory space from 0x80000 - 0x9FFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.41 Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR) — Offset 130h

Fixed Range MTRR covering the 16K memory space from 0xA0000 - 0xBFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.42 Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR) — Offset 138h

Fixed Range MTRR covering the 4K memory space 0xC0000 - 0xC7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.43 Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR) — Offset 140h

Fixed Range MTRR covering the 4K memory space from 0xC8000 - 0xCFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.44 Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR) — Offset 148h

Fixed Range MTRR covering the 4K memory space from 0xD0000 - 0xD7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.45 Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR) — Offset 150h

Fixed Range MTRR covering the 4K memory space from 0xD80000 - 0xDFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.46 Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR) — Offset 158h

Fixed Range MTRR covering the 4K memory space from 0xE0000 - 0xE7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.47 Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR) — Offset 160h

Fixed Range MTRR covering the 4K memory space from 0xE8000 - 0xEFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.48 Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR) — Offset 168h

Fixed Range MTRR covering the 4K memory space from 0xF0000 - 0xF7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.49 Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR) — Offset 170h

Fixed Range MTRR covering the 4K memory space from 0xF8000 - 0xFFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.7.50 Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR) — Offset 180h

Variable-Range MTRR BASE0

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 180h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 0
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 0

3.7.51 Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR) — Offset 188h

Variable-Range MTRR MASK0

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 188h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 0
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 0 mask
10:0	0h RO	**Reserved**

3.7.52 Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR) — Offset 190h

Variable-Range MTRR BASE1

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 190h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 1
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 1

3.7.53 Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR) — Offset 198h

Variable-Range MTRR MASK1

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 198h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 1
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 1 mask
10:0	0h RO	**Reserved**

3.7.54 Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR) — Offset 1A0h

Variable-Range MTRR BASE2

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 2
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 2

3.7.55 Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR) — Offset 1A8h

Variable-Range MTRR MASK2

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 2
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 2 mask
10:0	0h RO	**Reserved**

3.7.56 Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR) — Offset 1B0h

Variable-Range MTRR BASE3

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1B0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 3
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 3

3.7.57 Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR) — Offset 1B8h

Variable-Range MTRR MASK3

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 3
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 3 mask
10:0	0h RO	**Reserved**

3.7.58 Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR) — Offset 1C0h

Variable-Range MTRR BASE4

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 4
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 4

3.7.59 Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR) — Offset 1C8h

Variable-Range MTRR MASK4

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 4
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 4 mask
10:0	0h RO	**Reserved**

3.7.60 Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR) — Offset 1D0h

Variable-Range MTRR BASE5

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 5
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 5

3.7.61 Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR) — Offset 1D8h

Variable-Range MTRR MASK5

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1D8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 5
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 5 mask
10:0	0h RO	**Reserved**

3.7.62 Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR) — Offset 1E0h

Variable-Range MTRR BASE6

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1E0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 6
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 6

3.7.63 Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR) — Offset 1E8h

Variable-Range MTRR MASK6

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1E8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 6
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 6 mask
10:0	0h RO	**Reserved**

3.7.64 Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR) — Offset 1F0h

Variable-Range MTRR BASE7

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 7
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 7

3.7.65 Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR) — Offset 1F8h

Variable-Range MTRR MASK7

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1F8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 7
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 7 mask
10:0	0h RO	**Reserved**

3.7.66 Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR) — Offset 200h

Variable-Range MTRR BASE8

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 200h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 8
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 8

3.7.67 Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR) — Offset 208h

Variable-Range MTRR MASK8

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 208h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 8
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 8 mask
10:0	0h RO	**Reserved**

3.7.68 Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR) — Offset 210h

Variable-Range MTRR BASE9

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 210h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 9
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 9

3.7.69 Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR) — Offset 218h

Variable-Range MTRR MASK9

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 218h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 9
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 9 mask
10:0	0h RO	**Reserved**

3.7.70 Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR) — Offset 400h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 400h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RO/V/P	**Fault Info (FI):** When the Fault Reason (FR) field indicates one of the address translation fault conditions, bits 63:12 of this field contain the page address in the faulted request. When PASID Present field is 0 (i.e, faulted request is a request without PASID), hardware treat bits 63:N as reserved (0), where N is the maximum guest address width (MGAW) supported. For requests-with PASID (PASID Present field = 1), hardware treats bits 63:N as reserved (0), where N corresponds to the largest AGAW value supported by hardware. When the Fault Reason (FR) field indicates interrupt-remapping fault conditions other than Fault Reason 25h, bits 63:48 of this field indicate the interrupt_index computed for the faulted interrupt request, and bits 47:12 are cleared. When the Fault Reason (FR) field indicates interrupt-remapping fault condition of blocked Compatibility mode interrupt (Fault Reason 25h), the content of this field is undefined. This field is relevant only when the F field is Set.
11:0	0h RO	**Reserved**

3.7.71 Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR) — Offset 408h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 408h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C/V/P	**Fault FRCDH (F):** Hardware sets this field to indicate a fault is logged in this Fault Recording register. The F field is set by hardware after the details of the fault is recorded in other fields When this field is Set, hardware may collapse additional faults from the same source-id (SID) Software writes the value read from this field to Clear it.
62	0h RO/V/P	**Type FRCDH (T):** Type of the faulted request: • 0: Write request or Page (PRS) Request • 1: Read request or AtomicOp request This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
61:60	0h RO/V/P	**Address Type (AT):** This field captures the AT field from the faulted DMA request Hardware implementations not supporting Device-IOTLBs (DI field Clear in Extended Capability register) treat this field as RsvdZ When supported, this field is valid only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
59:40	00000h RO/V/P	**PASID Value (PV):** PASID value in the faulted request. This field is relevant only when the PP field is set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
39:32	00h RO/V/P	**Fault Reason (FR):** Reason for the fault This field is relevant only when the F field is set.
31	0h RO/V/P	**PASID Present (PP):** When set, indicates the faulted request has a PASID tag. The value of the PASID field is reported in the PASID Value (PV) field. This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the non-recoverable address translation fault conditions. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
30	0h RO/V/P	**Execute Permission Requested (EXE):** When set, indicates Execute permission was requested by the faulted read request. This field is relevant only when the PP field and T field are both Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
29	0h RO/V/P	**Privilege Mode Requested (PRIV):** When set, indicates Supervisor privilege was requested by the faulted request. This field is relevant only when the PP field is Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
28:16	0h RO	**Reserved**
15:0	0000h RO/V/P	**Source Identifier (SID):** Requester-id associated with the fault condition This field is relevant only when the F field is set.

3.7.72 Invalidate Address Register (IVA_REG_0_0_0_VTDBAR) — Offset 500h

Register to provide the DMA address whose corresponding IOTLB entry needs to be invalidated through the corresponding IOTLB Invalidate register. This register is a write-only register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 500h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h WO	**IVA Address (ADDR):** Software provides the DMA address that needs to be page-selectively invalidated. To make a page-selective invalidation request to hardware, software must first write the appropriate fields in this register, and then issue the appropriate page-selective invalidate command through the IOTLB_REG. Hardware ignores bits 63:N, where N is the maximum guest address width (MGAW) supported. A value returned on a read of this field is undefined A value returned on a read of this field is undefined
11:7	0h RO	**Reserved**
6	0h WO	**Invalidation Hint (IH):** The field provides hint to hardware about preserving or flushing the non-leaf (page-directory) entries that may be cached in hardware: • 0 = Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware must flush both the cached leaf and non-leaf page-table entries corresponding to the mappings specified by ADDR and AM fields. • 1 = Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware may preserve the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields. A value returned on a read of this field is undefined

Bit Range	Default & Access	Field Name (ID): Description
5:0	00h WO	**Address Mask (AM):** The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation of contiguous mappings for size-aligned regions. For example:..Mask ADDR bits Pages..Value masked invalidated.. 0 None 1.. 1 12 2.. 2 13:12 4.. 3 14:12 8.. 4 15:12 16 When invalidating mappings for super-pages, software must specify the appropriate mask value. For example, when invalidating mapping for a 2MB page, software must specify an address mask value of at least 9...Hardware implementations report the maximum supported mask value through the Capability register.

3.7.73 IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR) — Offset 508h

Register to invalidate IOTLB. The act of writing the upper byte of the IOTLB_REG with IVT field Set causes the hardware to perform the IOTLB invalidation.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 508h	0200000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate IOTLB (IVT):** Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field Hardware clears the IVT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must not submit another invalidation request through this register while the IVT field is Set, nor update the associated Invalidate Address register Software must not submit IOTLB invalidation requests when there is a context-cache invalidation request pending at this remapping hardware unit. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flushing before invalidating the IOTLB.
62	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
61:60	0h RW	**IOTLB Invalidation Request Granularity (IIRG):** When requesting hardware to invalidate the IOTLB (by setting the IVT field), software writes the requested invalidation granularity through this field. The following are the encodings for the field • 00 = Reserved • 01 = Global invalidation request • 10 = Domain-selective invalidation request. The target domain-id must be specified in the DID field • 11 = Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, and the domain-id must be provided in the DID field Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the IVT field. At this time, the granularity at which actual invalidation was performed is reported through the IAIG field
59	0h RO	**Reserved**
58:57	1h RO/V	**IOTLB Actual Invalidation Granularity (IAIG):** Hardware reports the granularity at which an invalidation request was processed through this field when reporting invalidation completion (by clearing the IVT field). The following are the encodings for this field • 00 = Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests • 01 = Global Invalidation performed. This could be in response to a global, domain-selective, or page-selective invalidation request • 10 = Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or a page-selective invalidation request • 11 = Domain-page-selective invalidation performed using the address, mask and hint specified by software in the Invalidate Address register and domain-id specified in DID field. This can be in response to a page-selective invalidation request.
56:50	0h RO	**Reserved**
49	0h RW	**Drain Reads (DR):** This field is ignored by hardware if the DRD field is reported as clear in the Capability register. When the DRD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining any translated DMA read requests • 1 = Hardware must drain DMA read requests.
48	0h RW	**Drain Writes (DW):** This field is ignored by hardware if the DWD field is reported as Clear in the Capability register. When the DWD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining DMA write requests • 1 = Hardware must drain relevant translated DMA write requests.

Bit Range	Default & Access	Field Name (ID): Description
47:32	0000h RW	**Domain ID (DID):** Indicates the ID of the domain whose IOTLB entries need to be selectively invalidated. This field must be programmed by software for domain-selective and page-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware ignores and not implements bits 47:(32+N), where N is the supported domain-id width reported in the Capability register.
31:0	0h RO	**Reserved**

3.8 Graphics VT BAR (GFXVTBAR) Registers

This chapter documents the GFXVTBAR registers. Base address of these registers are defined in the GFXVTBAR_0_0_0_MCHBAR_NCU register which resides in the MCHBAR register collection.

3.8.1 Summary of Registers

Table 3-9. Summary of GFXVTBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Version Register (VER_REG_0_0_0_VTDBAR)	00000040h
8h	8	Capability Register (CAP_REG_0_0_0_VTDBAR)	09C0000C406F0466h
10h	8	Extended Capability Register (ECAP_REG_0_0_0_VTDBAR)	0000079E2FF050DFh
18h	4	Global Command Register (GCMD_REG_0_0_0_VTDBAR)	00000000h
1Ch	4	Global Status Register (GSTS_REG_0_0_0_VTDBAR)	00000000h
20h	8	Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR)	0000000000000000h
28h	8	Context Command Register (CCMD_REG_0_0_0_VTDBAR)	0800000000000000h
34h	4	Fault Status Register (FSTS_REG_0_0_0_VTDBAR)	00000000h
38h	4	Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR)	80000000h
3Ch	4	Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR)	00000000h
40h	4	Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR)	00000000h
44h	4	Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR)	00000000h
58h	8	Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR)	0000000000000000h
64h	4	Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR)	00000000h
68h	4	Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR)	00000000h
6Ch	4	Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR)	00000000h
70h	8	Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR)	0000000000000000h
78h	8	Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80h	8	Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR)	0000000000000000h
88h	8	Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR)	0000000000000000h
90h	8	Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR)	0000000000000000h
9Ch	4	Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR)	00000000h
A0h	4	Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR)	80000000h
A4h	4	Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR)	00000000h
A8h	4	Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR)	00000000h
ACh	4	Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR)	00000000h
B8h	8	Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR)	0000000000000000h
C0h	8	Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR)	0000000000000000h
C8h	8	Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR)	0000000000000000h
D0h	8	Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR)	0000000000000000h
DCh	4	Page Request Status Register (PRS_REG_0_0_0_VTDBAR)	00000000h
E0h	4	Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR)	80000000h
E4h	4	Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR)	00000000h
E8h	4	Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR)	00000000h
ECh	4	Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR)	00000000h
100h	8	MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR)	0000000000000000h
108h	8	MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR)	0000000000000000h
120h	8	Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR)	0000000000000000h
128h	8	Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR)	0000000000000000h
130h	8	Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR)	0000000000000000h
138h	8	Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR)	0000000000000000h
140h	8	Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR)	0000000000000000h
148h	8	Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR)	0000000000000000h
150h	8	Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR)	0000000000000000h
158h	8	Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR)	0000000000000000h
160h	8	Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
168h	8	Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR)	0000000000000000h
170h	8	Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR)	0000000000000000h
180h	8	Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR)	0000000000000000h
188h	8	Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR)	0000000000000000h
190h	8	Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR)	0000000000000000h
198h	8	Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR)	0000000000000000h
1A0h	8	Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR)	0000000000000000h
1A8h	8	Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR)	0000000000000000h
1B0h	8	Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR)	0000000000000000h
1B8h	8	Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR)	0000000000000000h
1C0h	8	Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR)	0000000000000000h
1C8h	8	Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR)	0000000000000000h
1D0h	8	Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR)	0000000000000000h
1D8h	8	Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR)	0000000000000000h
1E0h	8	Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR)	0000000000000000h
1E8h	8	Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR)	0000000000000000h
1F0h	8	Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR)	0000000000000000h
1F8h	8	Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR)	0000000000000000h
200h	8	Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR)	0000000000000000h
208h	8	Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR)	0000000000000000h
210h	8	Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR)	0000000000000000h
218h	8	Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR)	0000000000000000h
400h	8	Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR)	0000000000000000h
408h	8	Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR)	0000000000000000h
500h	8	Invalidate Address Register (IVA_REG_0_0_0_VTDBAR)	0000000000000000h
508h	8	IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR)	0200000000000000h

3.8.2 Version Register (VER_REG_0_0_0_VTDBAR) — Offset 0h

Register to report the architecture version supported. Backward compatibility for the architecture is maintained with new revision numbers, allowing software to load remapping hardware drivers written for prior architecture versions.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 0h	00000040h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	4h RO	**Major Version Number (MAJOR):** Indicates supported architecture version.
3:0	0h RO	**Minor Version Number (MINOR):** Indicates supported architecture minor version.

3.8.3 Capability Register (CAP_REG_0_0_0_VTDBAR) — Offset 8h

Register to report general remapping hardware capabilities.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 8h	09C0000C406F0466h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60	0h RO	**First Level 5-level Paging (FL5LP):** • 0: Hardware does not support 5-level paging for requests-with-PASID subject to first-level translation. • 1: Hardware supports 5-level paging for requests-with-PASID subject to first-level translation.

Bit Range	Default & Access	Field Name (ID): Description
59	1h RO	**Posted Interrupt Support (PI):** • 0 = Hardware does not support Posting of Interrupts. • 1 = Hardware supports Posting of Interrupts. Hardware implementations reporting this field as Set must also report Interrupt Remapping support (IR field in Extended Capability Register)
58:57	0h RO	**Reserved**
56	1h RO	**First Level 1-GByte Page Support (FL1GP):** A value of 1 in this field indicates 1-GByte page size is supported for first-level translation.
55	1h RO	**Read Draining (DRD):** • 0 = Hardware does not support draining of DMA read requests. • 1 = Hardware supports draining of DMA read requests.
54	1h RO	**Write Draining (DWD):** • 0 = Hardware does not support draining of DMA write requests. • 1 = Hardware supports draining of DMA write requests.
53:48	00h RO	**Maximum Address Mask Value (MAMV):** The value in this field indicates the maximum supported value for the Address Mask (AM) field in the Invalidation Address register (IVA_REG) and IOTLB Invalidation Descriptor (iotlb_inv_dsc) used for invalidations of second-level translation. This field is valid only when the PSI field in Capability register is reported as Set.
47:40	00h RO	**Number of Fault-Recording Registers (NFR):** Number of fault recording registers is computed as N+1, where N is the value reported in this field. Implementations must support at least one fault recording register (NFR = 0) for each remapping hardware unit in the platform. The maximum number of fault recording registers per remapping hardware unit is 256.
39	0h RO	**Page Selective Invalidation (PSI):** • 0 = Hardware supports only domain and global invalidates for IOTLB. • 1 = Hardware supports page selective, domain and global invalidates for IOTLB. Hardware implementations reporting this field as set are recommended to support a Maximum Address Mask Value (MAMV) value of at least 9 (or 18 if supporting 1GB pages with second level translation).
38	0h RO	**Reserved**
37:34	3h RO	**Second Level Large Page Support (SLLPS):** This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: • 0 = 21-bit offset to page frame (2MB) • 1 = 30-bit offset to page frame (1GB) • 2 = 39-bit offset to page frame (512GB) • 3 = 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.

Bit Range	Default & Access	Field Name (ID): Description
33:24	040h RO	**Fault-Recording Register Offset (FRO):** This field specifies the location to the first fault recording register relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first fault recording register is calculated as X+(16*Y).
23	0h RO	**Reserved**
22	1h RO	**Zero Length Read (ZLR):** • 0 = Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. • 1 = Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages. DMA remapping hardware implementations are recommended to report ZLR field as Set.
21:16	2Fh RO	**Maximum Guest Address Width (MGAW):** This field indicates the maximum DMA virtual addressability supported by remapping hardware. The Maximum Guest Address Width (MGAW) is computed as (N+1), where N is the value reported in this field. For example, a hardware implementation supporting 48-bit MGAW reports a value of 47 (101111b) in this field. If the value in this field is X, untranslated and translated DMA requests to addresses above 2(x+1)-1 are always blocked by hardware. Translations requests to address above 2(x+1)-1 from allowed devices return a null Translation Completion Data Entry with R=W=0. Guest addressability for a given DMA request is limited to the minimum of the value reported through this field and the adjusted guest address width of the corresponding page-table structure. (Adjusted guest address widths supported by hardware are reported through the SAGAW field). Implementations are recommended to support MGAW at least equal to the physical addressability (host address width) of the platform.
15:13	0h RO	**Reserved**
12:8	04h RO	**Supported Adjusted Guest Address Widths (SAGAW):** This 5-bit field indicates the supported adjusted guest address widths (which in turn represents the levels of page-table walks for the 4KB base page size) supported by the hardware implementation. A value of 1 in any of these bits indicates the corresponding adjusted guest address width is supported. The adjusted guest address widths corresponding to various bit positions within this field are: • 0 = 30-bit AGAW (2-level page table) • 1 = 39-bit AGAW (3-level page table) • 2 = 48-bit AGAW (4-level page table) • 3 = 57-bit AGAW (5-level page table) • 4 = Reserved Software must ensure that the adjusted guest address width used to setup the page tables is one of the supported guest address widths reported in this field.
7	0h RO	**Caching Mode (CM):** • 0 = Not-present and erroneous entries are not cached in any of the remapping caches. Invalidations are not required for modifications to individual not present or invalid entries. However, any modifications that result in decreasing the effective permissions or partial permission increases require invalidations for them to be effective. • 1 = Not-present and erroneous mappings may be cached in the remapping caches. Any software updates to the remapping structures (including updates to not-present or erroneous entries) require explicit invalidation. Hardware implementations of this architecture must support a value of 0 in this field.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO	**Protected High-Memory Region (PHMR):** • 0 = Indicates protected high-memory region is not supported. • 1 = Indicates protected high-memory region is supported.
5	1h RO	**Protected Low-Memory Region (PLMR):** • 0 = Indicates protected low-memory region is not supported. • 1 = Indicates protected low-memory region is supported.
4	0h RO	**Required Write-Buffer Flushing (RWBF):** • 0 = Indicates no write-buffer flushing is needed to ensure changes to memory-resident structures are visible to hardware. • 1 = Indicates software must explicitly flush the write buffers to ensure updates made to memory-resident remapping structures are visible to hardware.
3	0h RO	**Advanced Fault Logging (AFL):** • 0: Indicates advanced fault logging is not supported. Only primary fault logging is supported. • 1: Indicates advanced fault logging is supported.
2:0	6h RO	**Number of Domains Supported (ND):** • 000b: Hardware supports 4-bit domain-ids with support for up to 16 domains. • 001b: Hardware supports 6-bit domain-ids with support for up to 64 domains. • 010b: Hardware supports 8-bit domain-ids with support for up to 256 domains. • 011b: Hardware supports 10-bit domain-ids with support for up to 1024 domains. • 100b: Hardware supports 12-bit domain-ids with support for up to 4K domains. • 100b: Hardware supports 14-bit domain-ids with support for up to 16K domains. • 110b: Hardware supports 16-bit domain-ids with support for up to 64K domains. • 111b: Reserved.

3.8.4 Extended Capability Register (ECAP_REG_0_0_0_VTDBAR) — Offset 10h

Register to report remapping hardware extended capabilities.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 10h	0000079E2FF050DFh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:44	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
43	0h RO	**PASID Support Limitation (PSL):** This field is valid only when Process Address Space ID Support (PASID) field (bit 40) is reported as Set. When this field is reported as Set, extendedcontext-entries with PASID Enable (PASIDE) field Set do not support Requests-withoutPASID. Hardware implementations must report a value of 0 in this field. Virtual implementations may report a value of 1 in this field to disallow guest software from using an extended-context-entry for both Virtual Address (VA) and I/O Virtual Address (IOVA) concurrently.
42	1h RO	**Page Request Draining Support (PDS):** • 0 = Hardware does not support Page-Request Drain (PD) flag in Inv_wait_dsc. • 1 = Hardware supports Page-Request Drain (PD) flag in Inv_wait_dsc. This field is valid only when Device-TLB support field is reported as Set.
41	1h RO	**Device-TLB Invalidation Throttle (DIT):** • 0 = Hardware does not support Device-TLB Invalidation Throttling. • 1 = Hardware supports Device-TLB Invalidation Throttling. This field is valid only when Page Request Support (PRS) field is reported as Set.
40	1h RO	**Process Address Space ID Support (PASID):** • 0 = Hardware does not support requests tagged with Process Address Space IDs. • 1 = Hardware supports requests tagged with Process Address Space IDs.
39:35	13h RO	**PASID Size Supported (PSS):** This field reports the PASID size supported by the remapping hardware for requests-with-PASID. A value of N in this field indicates hardware supports PASID field of N+1 bits (For example, value of 7 in this field, indicates 8-bit PASIDs are supported). Requests-with-PASID with PASID value beyond the limit specified by this field are treated as error by the remapping hardware. This field is valid only when PASID field is reported as Set.
34	1h RO	**Extended Accessed Flag Support (EAFS):** • 0 = Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. • 1 = Hardware supports the extended accessed (EA) bit in first-level paging-structure entries. This field is valid only when PASID field is reported as Set.
33	1h RO	**No Write Flag Support (NWFS):** • 0 = Hardware ignores the No Write (NW) flag in Device-TLB translationrequests, and behaves as if NW is always 0. • 1 = Hardware supports the No Write (NW) flag in Device-TLB translationrequests. This field is valid only when Device-TLB support (DT) field is reported as Set.
32	0h RO	**Reserved**
31	0h RO	**Supervisor Request Support (SRS):** • 0 = H/W does not support requests-with-PASID seeking supervisor privilege. • 1 = H/W supports requests-with-PASID seeking supervisor privilege. The field is valid only when PASID field is reported as Set.
30	0h RO	**Execute Request Support (ERS):** • 0 = H/W does not support requests-with-PASID seeking execute permission. • 1 = H/W supports requests-with-PASID seeking execute permission. This field is valid only when PASID field is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
29	1h RO	**Page Request Support (PRS):** • 0 = Hardware does not support Page Requests. • 1 = Hardware supports Page Requests This field is valid only when Device-TLB (DT) field is reported as Set.
28	0h RO	**IGN:** Ignore this field
27	1h RO	**Deferred Invalidate Support (DIS):** • 0 = Hardware does not support deferred invalidations of IOTLB and Device-TLB. • 1 = Hardware supports deferred invalidations of IOTLB and Device-TLB. This field is valid only when PASID field is reported as Set.
26	1h RO	**Nested Translation Support (NEST):** • 0 = Hardware does not support nested translations. • 1 = Hardware supports nested translations. This field is valid only when PASID field is reported as Set.
25	1h RO	**Memory Type Support (MTS):** • 0 = Hardware does not support Memory Type in first-level translation and Extended Memory type in second-level translation. • 1 = Hardware supports Memory Type in first-level translation and Extended Memory type in second-level translation. This field is valid only when PASID and ECS fields are reported as Set. Remapping hardware units with, one or more devices that operate in processor coherency domain, under its scope must report this field as Set.
24	1h RO	**Extended Context Support (ECS):** • 0 = Hardware does not support extended-root-entries and extended-context-entries. • 1 = Hardware supports extended-root-entries and extended-context-entries. Implementations reporting PASID or PRS fields as Set, must report this field as Set.
23:20	Fh RO	**Maximum Handle Mask Value (MHMV):** The value in this field indicates the maximum supported value for the Handle Mask (HM) field in the interrupt entry cache invalidation descriptor (iec_inv_dsc). This field is valid only when the IR field in Extended Capability register is reported as Set.
19:18	0h RO	**Reserved**
17:8	050h RO	**IOTLB Register Offset (IRO):** This field specifies the offset to the IOTLB registers relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first IOTLB invalidation register is calculated as X+(16*Y).
7	1h RO	**Snoop Control (SC):** • 0 = Hardware does not support 1-setting of the SNP field in the page-table entries. • 1 = Hardware supports the 1-setting of the SNP field in the page-table entries.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO	**Pass Through (PT):** • 0 = Hardware does not support pass-through translation type in context entries and extended-context-entries. • 1 = Hardware supports pass-through translation type in context entries and extended-context-entries. Pass-through translation is specified through Translation-Type (T) field value of 10b in context-entries, or T field value of 010b in extended-context-entries. Hardware implementations supporting PASID must report a value of 1b in this field.
5	0h RO	**Reserved**
4	1h RO	**Extended Interrupt Mode (EIM):** • 0 = On Intel64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). • 1 = On Intel64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode). This field is valid only on Intel64 platforms reporting Interrupt Remapping support (IR field Set).
3	1h RO	**Interrupt Remapping Support (IR):** • 0 = Hardware does not support interrupt remapping. • 1 = Hardware supports interrupt remapping. Implementations reporting this field as Set must also support Queued Invalidation (QI).
2	1h RO	**Device-TLB Support (DT):** • 0 = Hardware does not support device-IOTLBs. • 1 = Hardware supports Device-IOTLBs. Implementations reporting this field as Set must also support Queued Invalidation (QI). Hardware implementations supporting I/O Page Requests (PRS field Set in Extended Capability register) must report a value of 1b in this field.
1	1h RO	**Queued Invalidation Support (QI):** • 0 = Hardware does not support queued invalidations. • 1 = Hardware supports queued invalidations.
0	1h RO	**Page-Walk Coherency (C):** This field indicates if hardware access to the root, context, extended-context and interrupt-remap tables, and second-level paging structures for requests-without-PASID, are coherent (snooped) or not. • 0 = Indicates hardware accesses to remapping structures are non-coherent. • 1 = Indicates hardware accesses to remapping structures are coherent. Hardware access to advanced fault log, invalidation queue, invalidation semaphore, page-request queue, PASID-table, PASID-state table, and first-level page-tables are always coherent.

3.8.5 Global Command Register (GCMD_REG_0_0_0_VTDBAR) — Offset 18h

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

Register to control r mapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

- 1. Tmp = Read GSTS_REG
- 2. Status = (Tmp & 96FFFFFFh) // Reset the one-shot bits
- 3. Command = (Status | (Y << X))
- 4. Write Command to GCMD_REG
- 5. Wait until GSTS_REG[X] indicates command is serviced.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping: • 0 = Disable DMA remapping. • 1 = Enable DMA remapping. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA read/write requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30	0h WO	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address (RTA_REG) register. Hardware reports the status of the Set Root Table Pointer operation through the RTPS field in the Global Status register. The Set Root Table Pointer operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. .After a Set Root Table Pointer operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries. While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Set Fault Log (SFL):** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the Set Fault Log operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.
28	0h RO	**Enable Advanced Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: • 0 = Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. • 1 = Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.
27	0h RO	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26	0h RW	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. • 0 = Disable queued invalidations. • 1 = Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25	0h RW	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. • 0 = Disable interrupt-remapping hardware. • 1 = Enable interrupt-remapping hardware. Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
24	0h WO	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address (IRTA_REG) register. Hardware reports the status of the Set Interrupt Remap Table Pointer operation through the IRTPS field in the Global Status register. The Set Interrupt Remap Table Pointer operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After a Set Interrupt Remap Table Pointer operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23	0h RW	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Block Compatibility format interrupts. • 1 = Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.
22:0	0h RO	**Reserved**

3.8.6 Global Status Register (GSTS_REG_0_0_0_VTDBAR) — Offset 1Ch

Register to report general remapping hardware status.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Translation Enable Status (TES):** This field indicates the status of DMA-remapping hardware. • 0 = DMA-remapping hardware is not enabled. • 1 = DMA-remapping hardware is enabled
30	0h RO/V	**Root Table Pointer Status (RTPS):** This field indicates the status of the root- table pointer in hardware. This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware completes the Set Root Table Pointer operation using the value provided in the Root-Entry Table Address register.
29	0h RO	**Fault Log Status (FLS):** This field: • Is cleared by hardware when software Sets the SFL field in the Global Command register. • Is Set by hardware when hardware completes the Set Fault Log Pointer operation using the value provided in the Advanced Fault Log register.
28	0h RO	**Advanced Fault Logging Status (AFLS):** This field is valid only for implementations supporting advanced fault logging. It indicates the advanced fault logging status: • 0 = Advanced Fault Logging is not enabled. • 1 = Advanced Fault Logging is enabled.
27	0h RO	**Write Buffer Flush Status (WBFS):** This field is valid only for implementations requiring write buffer flushing. This field indicates the status of the write buffer flush command. It is: • Set by hardware when software sets the WBF field in the Global Command register. • Cleared by hardware when hardware completes the write buffer flushing operation.
26	0h RO/V	**Queued Invalidation Enable Status (QIES):** This field indicates queued invalidation enable status. • 0 = queued invalidation is not enabled. • 1 = queued invalidation is enabled
25	0h RO/V	**Interrupt Remapping Enable Status (IRES):** This field indicates the status of Interrupt-remapping hardware. • 0 = Interrupt-remapping hardware is not enabled. • 1 = Interrupt-remapping hardware is enabled

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO/V	**Interrupt Remapping Pointer Status (IRTPS):** This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is Set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23	0h RO/V	**Compatibility Format Interrupt Status (CFIS):** This field indicates the status of Compatibility format interrupts on Intel64 implementations supporting interrupt-remapping. The value reported in this field is applicable only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Compatibility format interrupts are blocked. • 1 = Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).
22:0	0h RO	**Reserved**

3.8.7 Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR) — Offset 20h

Register providing the base address of root-entry table.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 20h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**
51:12	00000000 00h RW	**Root Table Address (RTA):** This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
11	0h RW	**Root Table Type (RTT):** This field specifies the type of root-table referenced by the Root Table Address (RTA) field: • 0 = Root Table. • 1 = Extended Root Table
10:0	0h RO	**Reserved**

3.8.8 Context Command Register (CCMD_REG_0_0_0_VTDBAR) — Offset 28h

Register to manage context cache. The act of writing the uppermost byte of the CCMD_REG with the ICC field Set causes the hardware to perform the context-cache invalidation.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 28h	0800000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate Context Cache (ICC):** Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field is Clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must submit a context-cache invalidation request through this field only when there are no invalidation requests pending at this remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flush before invalidating the context cache.
62:61	0h RW	**Context Invalidation Request Granularity (CIRG):** Software provides the requested invalidation granularity through this field when setting the ICC field: • 00: Reserved. • 01: Global Invalidation request. • 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. • 11: Device-selective invalidation request. The target source-id(s) must be specified through the SID and FM fields, and the domain-id (that was programmed in the context-entry for these device(s)) must be provided in the DID field. Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.

Bit Range	Default & Access	Field Name (ID): Description
60:59	1h RO/V	**Context Actual Invalidation Granularity (CAIG):** Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field). The following are the encodings for this field: • 00: Reserved. • 01: Global Invalidation performed. This could be in response to a global, domain-selective or device-selective invalidation request. • 10: Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or device-selective invalidation request. • 11: Device-selective invalidation performed using the source-id and domain-id specified by software in the SID and FM fields. This can only be in response to a device-selective invalidation request.
58:34	0h RO	**Reserved**
33:32	0h RW	**Function Mask (FM):** Software may use the Function Mask to perform device-selective invalidations on behalf of devices supporting PCI Express Phantom Functions...This field specifies which bits of the function number portion (least significant three bits) of the SID field to mask when performing device-selective invalidations. The following encodings are defined for this field: • 00: No bits in the SID field masked. • 01: Mask most significant bit of function number in the SID field. • 10: Mask two most significant bit of function number in the SID field. • 11: Mask all three bits of function number in the SID field. The context-entries corresponding to all the source-ids specified through the FM and SID fields must have to the domain-id specified in the DID field.
31:16	0000h RW	**SID:** Indicates the source-id of the device whose corresponding context-entry needs to be selectively invalidated. This field along with the FM field must be programmed by software for device-selective invalidation requests.
15:0	0000h RW	**DID:** Indicates the id of the domain whose context-entries need to be selectively invalidated. This field must be programmed by software for both domain-selective and device-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware may ignore and not implement bits15:N, where N is the supported domain-id width reported in the Capability register.

3.8.9 Fault Status Register (FSTS_REG_0_0_0_VTDBAR) — Offset 34h

Register indicating the various error status.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Fault Record Index (FRI):** This field is valid only when the PPF field is Set. The FRI field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the PPF field was Set by hardware. The value read from this field is undefined when the PPF field is clear.
7	0h RW/1C	**Page Request Overflow (PRO):** Hardware detected a Page Request Overflow error. Hardware implementations not supporting the Page Request Queue implement this bit as RsvdZ.
6	0h RW/1C	**Invalidation Time-out Error (ITE):** Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting device Device-IOTLBs implement this bit as RsvdZ.
5	0h RW/1C	**Invalidation Completion Error (ICE):** Hardware received an unexpected or invalid Device-IOTLB invalidation completion. This could be due to either an invalid ITag or invalid source-id in an invalidation completion response. At this time, a fault event may be generated based on the programming of hte Fault Event Control register. Hardware implementations not supporting Device-IOTLBs implement this bit as RsvdZ.
4	0h RW/1C	**Invalidation Queue Error (IQE):** Hardware detected an error associated with the invalidation queue. This could be due to either a hardware error while fetching a descriptor from the invalidation queue, or hardware detecting an erroneous or invalid descriptor in the invalidation queue. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting queued invalidations implement this bit as RsvdZ.
3	0h RO	**Advanced Pending Fault (APF):** When this field is Clear, hardware sets this field when the first fault record (at index 0) is written to a fault log. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
2	0h RO	**Advanced Fault Overflow (AFO):** Hardware sets this field to indicate advanced fault log overflow condition. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO/V	**Primary Pending Fault (PPF):** This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this remapping hardware unit. • 0 = No pending faults in any of the fault recording registers. • 1 = One or more fault recording registers has pending faults. The FRI field is updated by hardware whenever the PPF field is set by hardware. Also, depending on the programming of Fault Event Control register, a fault event is generated when hardware sets this field.
0	0h RW/1C	**Primary Fault Overflow (PFO):** Hardware sets this field to indicate overflow of fault recording registers. Software writing 1 clears this field. When this field is Set, hardware does not record any new faults until software clears this field.

3.8.10 Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR) — Offset 38h

Register specifying the fault event interrupt message control bits.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 38h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0 = No masking of interrupt. When an interrupt condition is detected, hardware issues an interrupt message (using the Fault Event Data and Fault Event Address register values). • 1 = This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition, which is defined as: • When primary fault logging is active, an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. • When advanced fault logging is active, an interrupt condition occurs when hardware records a fault in the first fault record (at index 0) of the current fault log and sets the APF field in the Fault Status register. • Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. • Hardware detected invalid Device-IOTLB invalidation completion, setting the ICE field in the Fault Status register. • Hardware detected Device-IOTLB invalidation completion time-out, setting the ITE field in the Fault Status register. If any of the status fields in the Fault Status register was already Set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set or other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending, or due to software clearing the IM field. • Software servicing all the pending interrupt status fields in the Fault Status register as follows: - When primary fault logging is active, software clearing the Fault (F) field in all the Fault Recording registers with faults, causing the PPF field in Fault Status register to be evaluated as clear. - Software clearing other status fields in the Fault Status register by writing back the value read from the respective fields.
29:0	0h RO	**Reserved**

3.8.11 Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR) — Offset 3Ch

Register specifying the interrupt message data

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data may treat this field as RsvdZ.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

3.8.12 Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR) — Offset 40h

Register specifying the interrupt message address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

3.8.13 Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR) — Offset 44h

Register specifying the interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Extended Interrupt Mode are required to implement this register. Hardware implementations not supporting Extended Interrupt Mode may treat this field as RsvdZ.

3.8.14 Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR) — Offset 58h

Register to specify the base address of the memory-resident fault-log region. This register is treated as RsvdZ for implementations not supporting advanced translation fault logging (AFL field reported as 0 in the Capability register).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 58h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0000000000000h RO	**Fault Log Address (FLA):** This field specifies the base of 4KB aligned fault-log region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Software specifies the base address and size of the fault log region through this register, and programs it in hardware through the SFL field in the Global Command register. When implemented, reads of this field return the value that was last programmed to it.
11:9	0h RO	**Fault Log Size (FLS):** This field specifies the size of the fault log region pointed by the FLA field. The size of the fault log region is 2X * 4KB, where X is the value programmed in this register. When implemented, reads of this field return the value that was last programmed to it.
8:0	0h RO	**Reserved**

3.8.15 Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR) — Offset 64h

Register to enable the DMA-protected memory regions setup through the PLMBASE,..PLMLIMT, PHMBASE, PHMLIMIT registers. This register is always treated as RO for implementations not supporting protected memory regions (PLMR and PHMR fields reported as Clear in the Capability register).

Protected memory regions may be used by software to securely initialize remapping structures in memory. To avoid impact to legacy BIOS usage of memory, software is recommended to not overlap protected memory regions with any reserved memory regions of the platform reported through the Reserved Memory Region Reporting (RMRR) structures.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Protected Memory (EPM):** This field controls DMA accesses to the protected low-memory and protected high-memory regions. • 0 = Protected memory regions are disabled. • 1 = Protected memory regions are enabled.DMA requests accessing protected memory regions are handled as follows: - When DMA remapping is not enabled, all DMA requests accessing protected memory regions are blocked. - When DMA remapping is enabled: • DMA requests processed as pass-through (Translation Type value of 10b in Context-Entry) and accessing the protected memory regions are blocked. • DMA requests with translated address (AT=10b) and accessing the protected memory regions are blocked. • DMA requests that are subject to address remapping, and accessing the protected memory regions may or may not be blocked by hardware. For such requests, software must not depend on hardware protection of the protected memory regions, and instead program the DMA-remapping page-tables to not allow DMA to protected memory regions. Remapping hardware access to the remapping structures are not subject to protected memory region checks. DMA requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register.Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field. After writing to this field software must wait for the operation to be completed and reflected in the PRS status field (bit 0) before changing the value of this field again.
30:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/V	**Protected Region Status (PRS):** This field indicates the status of protected memory region(s): • 0 = Protected memory region(s) disabled. • 1 = Protected memory region(s) enabled.

3.8.16 Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR) — Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled.

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register).

The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant zero bit position with 0 in the value read back from the register. Bits N:0 of this register is decoded by hardware as all 0s...Software must setup the protected low memory region below 4GB.

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Base (PLMB):** This register specifies the base of protected low-memory region in system memory.
19:0	0h RO	**Reserved**

3.8.17 Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR) — Offset 6Ch

Register to set up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register)

The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The Protected low-memory base and limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits 31: (N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Limit (PLML):** This register specifies the last host physical address of the DMA-protected low-memory region in system memory.
19:0	0h RO	**Reserved**

3.8.18 Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR) — Offset 70h

Register to set up the base address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0s

Software may setup the protected high memory region either above or below 4GB

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 70h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	00000h RW	**Protected High-Memory Base (PHMB):** This register specifies the base of protected (high) memory region in system memory Hardware ignores, and does not implement, bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

3.8.19 Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR) — Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The protected high-memory base & limit registers functions as follows

- Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 78h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	00000h RW	**Protected High-Memory Limit (PHML):** This register specifies the last host physical address of the DMA-protected high-memory region in system memory Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

3.8.20 Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR) — Offset 80h

Register indicating the invalidation queue head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 80h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO/V	**Queue Head (QH):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware Hardware resets this field to 0 whenever the queued invalidation is disabled (QIES field Clear in the Global Status register).
3:0	0h RO	**Reserved**

3.8.21 Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR) — Offset 88h

Register indicating the invalidation tail head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 88h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW	**Queue Tail (QT):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.
3:0	0h RO	**Reserved**

3.8.22 Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR) — Offset 90h

Register to configure the base address and size of the invalidation queue. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 90h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RW	**Invalidation Queue Base Address (IQA):** This field points to the base of 4KB aligned invalidation request queue. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field return the value that was last programmed to it.
11:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Queue Size (QS):** This field specifies the size of the invalidation request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the invalidation queue is 2^(X + 8).

3.8.23 Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR) — Offset 9Ch

Register to report completion status of invalidation wait descriptor with Interrupt Flag (IF) Set

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Invalidation Wait Descriptor Complete (IWC):** Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field Set. Hardware implementations not supporting queued invalidations implement this field as RsvdZ.

3.8.24 Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR) — Offset A0h

Register specifying the invalidation event interrupt control bits

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + A0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0= No masking of interrupt. When a invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values) • 1= This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • An Invalidation Wait Descriptor with Interrupt Flag (IF) field Set completed, setting the IWC field in the Invalidation Completion Status register • If the IWC field in the Invalidation Completion Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • 0= Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • 1= Software servicing the IWC field in the Invalidation Completion Status register.
29:0	0h RO	**Reserved**

3.8.25 Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR) — Offset A4h

Register specifying the Invalidation Event interrupt message data

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields Hardware implementations supporting only 16-bit interrupt data treat this field as Rsvd.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

3.8.26 Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR) — Offset A8h

Register specifying the Invalidation Event Interrupt message address

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Note: Bit definitions are the same as FEADDR_REG_0_0_0_VTDBAR, offset 40h.

3.8.27 Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR) — Offset ACh

Register specifying the Invalidation Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Queued Invalidations and Extended Interrupt Mode are required to implement this register Hardware implementations not supporting Queued Invalidations or Extended Interrupt Mode may treat this field as RsvdZ.

3.8.28 Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR) — Offset B8h

Register providing the base address of Interrupt remapping table. This register is treated as RsvdZ by implementations reporting Interrupt Remapping (IR) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RW	**Interrupt Remapping Table Address (IRTA):** This field points to the base of 4KB aligned interrupt remapping table Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field returns value that was last programmed to it.
11	0h RW	**Extended Interrupt Mode Enable (EIME):** This field is used by hardware on Intel64 platforms as follows: • 0=xAPIC mode is active. Hardware interprets only low 8-bits of Destination-ID field in the IRTEs. The high 24-bits of the Destination-ID field are treated as reserved • 1= x2APIC mode is active. Hardware interprets all 32-bits of Destination-ID field in the IRTEs This field is implemented as RsvdZ on implementations reporting Extended Interrupt Mode (EIM) field as Clear in Extended Capability register.
10:4	0h RO	**Reserved**
3:0	0h RW	**S:** This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2(X+1), where X is the value programmed in this field.

3.8.29 Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR) — Offset C0h

Register indicating the page request queue head. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW	**Page Queue Head (PQH):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be processed next by software.
3:0	0h RO	**Reserved**

3.8.30 Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR) — Offset C8h

Register indicating the page request queue tail. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW/V	**Page Queue Tail (PQT):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be written next by hardware.
3:0	0h RO	**Reserved**

3.8.31 Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR) — Offset D0h

Register to configure the base address and size of the page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RW	**Page Request Queue Base Address (PQA):** This field points to the base of 4KB aligned page request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Software must configure this register before enabling page requests in any extended-context-entries.
11:3	0h RO	**Reserved**
2:0	0h RW	**Page Request Queue Size (PQS):** This field specifies the size of the page request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the page request queue is 2^(X + 8)

3.8.32 Page Request Status Register (PRS_REG_0_0_0_VTDBAR) — Offset DCh

Register to report pending page request in page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Pending Page Request (PPR):** Pending Page Request: Indicates pending page requests to be serviced by software in the page request queue. This field is Set by hardware when a streaming page request entry (page_stream_reg_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, is added to the page request queue.

3.8.33 Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR) — Offset E0h

Register specifying the page request event interrupt control bits. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + E0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** Interrupt Mask • 0=No masking of interrupt. When a page request event condition is detected, hardware issues an interrupt message (using the Page Request Event Data and Page Request Event Address register values) • 1=This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Interrupt Pending: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • A streaming page request entry (page_stream_req_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, was added to page request queue, resulting in hardware setting the Pending Page Request (PPR) field in Page Request Status register • If the PPR field in the Page Request Event Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • Software servicing the PPR field in the Page Request Event Status register.
29:0	0h RO	**Reserved**

3.8.34 Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR) — Offset E4h

Register specifying the Page Request Event interrupt message data. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** Extended Interrupt Message Data
15:0	0000h RW	**Interrupt Message Data (IMD):** Interrupt Message Data: Data value in the interrupt request. Software requirements for programming this register are described in VTd Spec

3.8.35 Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR) — Offset E8h

Register specifying the Page Request Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MA):** Message Address: When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

3.8.36 Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR) — Offset ECh

Register specifying the Page Request Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Message Upper Address: This field specifies the upper address (bits.. 63:32) for the page request event interrupt.

3.8.37 MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR) — Offset 100h

Register reporting the Memory Type Range Register Capability. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

When implemented, value reported in this register must match IA32_MTRRCAP Model Specific Register (MSR) value reported by the host IA-32 processor(s).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 100h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:11	0h RO	**Reserved**
10	0h RO	**Write Combining (WC):** • 0 = Write-combining (WC) memory type is not supported. • 1 = Write-combining (WC) memory type is supported.Indicates whether the Write Combining memory type is supported.
9	0h RO	**Reserved**
8	0h RO	**Fixed Range MTRRs Supported (FIX):** • 0 = No fixed range MTRRs are supported • 1 = Fixed range MTRRs (MTRR_FIX64K_00000 through MTRR_FIX4K_0F8000) are supported
7:0	00h RO	**Variable MTRR Count (VCNT):** Indicates number of variable range MTRRs are supported.

3.8.38 MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR) — Offset 108h

Register for enabling/configuring Memory Type Range Registers. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 108h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Reserved**
11	0h RO	**MTRR Enable (E):** • 0 = Disable MTRRs; UC memory type is applied. FE field has no effect. • 1 = Enable MTRRs. FE field can disable the fixed-range MTRRs. Type specified in the default memory type field is used for areas of memory not already mapped by either fixed or variable MTRR
10	0h RO	**Fixed Range MTRR Enable (FE):** • 0 = Disable fixed range MTRRs. • 1 = Enable fixed range MTRRs. When fixed range MTRRs are enabled, they take priority over the variable range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed range MTRRs.
9:8	0h RO	**Reserved**
7:0	00h RO	**Default Memory Type (MEMTYPE):** Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0,1,4, 5 and 6.

3.8.39 Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR) — Offset 120h

Fixed Range MTRR covering the 64K memory space from 0x00000 - 0x7FFFF.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 120h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RO	**R7:** Register Field 7
55:48	00h RO	**R6:** Register Field 6
47:40	00h RO	**R5:** Register Field 5
39:32	00h RO	**R4:** Register Field 4
31:24	00h RO	**R3:** Register Field 3
23:16	00h RO	**R2:** Register Field 2
15:8	00h RO	**R1:** Register Field 1
7:0	00h RO	**R0:** Register Field 0

3.8.40 Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR) — Offset 128h

Fixed Range MTRR covering the 16K memory space from 0x80000 - 0x9FFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.41 Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR) — Offset 130h

Fixed Range MTRR covering the 16K memory space from 0xA0000 - 0xBFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.42 Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR) — Offset 138h

Fixed Range MTRR covering the 4K memory space 0xC0000 - 0xC7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.43 Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR) — Offset 140h

Fixed Range MTRR covering the 4K memory space from 0xC8000 - 0xCFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.44 Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR) — Offset 148h

Fixed Range MTRR covering the 4K memory space from 0xD0000 - 0xD7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.45 Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR) — Offset 150h

Fixed Range MTRR covering the 4K memory space from 0xD80000 - 0xDFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.46 Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR) — Offset 158h

Fixed Range MTRR covering the 4K memory space from 0xE0000 - 0xE7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.47 Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR) — Offset 160h

Fixed Range MTRR covering the 4K memory space from 0xE8000 - 0xEFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.48 Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR) — Offset 168h

Fixed Range MTRR covering the 4K memory space from 0xF0000 - 0xF7FFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.49 Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR) — Offset 170h

Fixed Range MTRR covering the 4K memory space from 0xF8000 - 0xFFFFF.

Note: Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.50 Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR) — Offset 180h

Variable-Range MTRR BASE0

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 180h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 0
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 0

3.8.51 Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR) — Offset 188h

Variable-Range MTRR MASK0

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 188h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 0
11	0h RO	**VALID:** Valid bit for variable range 0 mask
10:0	0h RO	**Reserved**

3.8.52 Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR) — Offset 190h

Variable-Range MTRR BASE1

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 190h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 1
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 1

3.8.53 Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR) — Offset 198h

Variable-Range MTRR MASK1

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 198h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 1
11	0h RO	**VALID:** Valid bit for variable range 1 mask
10:0	0h RO	**Reserved**

3.8.54 Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR) — Offset 1A0h

Variable-Range MTRR BASE2

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 2
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 2

3.8.55 Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR) — Offset 1A8h

Variable-Range MTRR MASK2

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 2
11	0h RO	**VALID:** Valid bit for variable range 2 mask
10:0	0h RO	**Reserved**

3.8.56 Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR) — Offset 1B0h

Variable-Range MTRR BASE3

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1B0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 3
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 3

3.8.57 Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR) — Offset 1B8h

Variable-Range MTRR MASK3

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 3
11	0h RO	**VALID:** Valid bit for variable range 3 mask
10:0	0h RO	**Reserved**

3.8.58 Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR) — Offset 1C0h

Variable-Range MTRR BASE4

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 4
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 4

3.8.59 Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR) — Offset 1C8h

Variable-Range MTRR MASK4

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 4
11	0h RO	**VALID:** Valid bit for variable range 4 mask
10:0	0h RO	**Reserved**

3.8.60 Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR) — Offset 1D0h

Variable-Range MTRR BASE5

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 5
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 5

3.8.61 Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR) — Offset 1D8h

Variable-Range MTRR MASK5

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1D8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 5
11	0h RO	**VALID:** Valid bit for variable range 5 mask
10:0	0h RO	**Reserved**

3.8.62 Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR) — Offset 1E0h

Variable-Range MTRR BASE6

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1E0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 6
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 6

3.8.63 Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR) — Offset 1E8h

Variable-Range MTRR MASK6

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1E8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 6
11	0h RO	**VALID:** Valid bit for variable range 6 mask
10:0	0h RO	**Reserved**

3.8.64 Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR) — Offset 1F0h

Variable-Range MTRR BASE7

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 7
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 7

3.8.65 Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR) — Offset 1F8h

Variable-Range MTRR MASK7

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1F8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 7
11	0h RO	**VALID:** Valid bit for variable range 7 mask
10:0	0h RO	**Reserved**

3.8.66 Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR) — Offset 200h

Variable-Range MTRR BASE8

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 200h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 8
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 8

3.8.67 Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR) — Offset 208h

Variable-Range MTRR MASK8

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 208h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 8
11	0h RO	**VALID:** Valid bit for variable range 8 mask
10:0	0h RO	**Reserved**

3.8.68 Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR) — Offset 210h

Variable-Range MTRR BASE9

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 210h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 9
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 9

3.8.69 Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR) — Offset 218h

Variable-Range MTRR MASK9

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 218h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 9
11	0h RO	**VALID:** Valid bit for variable range 9 mask
10:0	0h RO	**Reserved**

3.8.70 Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR) — Offset 400h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 400h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RO/V	**Fault Info (FI):** When the Fault Reason (FR) field indicates one of the address translation fault conditions, bits 63:12 of this field contains the page address in the faulted request. When PASID Present field is 0 (i.e, faulted request is a request without PASID), hardware treat bits 63:N as reserved (0), where N is the maximum guest address width (MGAW) supported. For requests-withPASID (PASID Present field = 1), hardware treats bits 63:N as reserved (0), where N corresponds to the largest AGAW value supported by hardware. When the Fault Reason (FR) field indicates interrupt-remapping fault conditions other than Fault Reason 25h, bits 63:48 of this field indicate the interrupt_index computed for the faulted interrupt request, and bits 47:12 are cleared. When the Fault Reason (FR) field indicates interrupt-remapping fault condition of blocked Compatibility mode interrupt (Fault Reason 25h), contents of this field is undefined. This field is relevant only when the F field is Set.
11:0	0h RO	**Reserved**

3.8.71 Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR) — Offset 408h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 408h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C	**F:** Hardware sets this field to indicate a fault is logged in this Fault Recording register. The F field is set by hardware after the details of the fault is recorded in other fields When this field is Set, hardware may collapse additional faults from the same source-id (SID) Software writes the value read from this field to Clear it.

Bit Range	Default & Access	Field Name (ID): Description
62	0h RO/V	**T:** Type of the faulted request: • 0=0: Write request or Page (PRS) Request • 1=1: Read request or AtomicOp request This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
61:60	0h RO/V	**Address Type (AT):** This field captures the AT field from the faulted DMA request Hardware implementations not supporting Device-IOTLBs (DI field Clear in Extended Capability register) treat this field as RsvdZ When supported, this field is valid only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
59:40	00000h RO/V	**PASID Value (PV):** PASID value in the faulted request. This field is relevant only when the PP field is set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
39:32	00h RO/V	**Fault Reason (FR):** Reason for the fault This field is relevant only when the F field is set.
31	0h RO/V	**PASID Present (PP):** When set, indicates the faulted request has a PASID tag. The value of the PASID field is reported in the PASID Value (PV) field. This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the non-recoverable address translation fault conditions. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
30	0h RO/V	**Execute Permission Requested (EXE):** When set, indicates Execute permission was requested by the faulted read request. This field is relevant only when the PP field and T field are both Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
29	0h RO/V	**Privilege Mode Requested (PRIV):** When set, indicates Supervisor privilege was requested by the faulted request. This field is relevant only when the PP field is Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
28:16	0h RO	**Reserved**
15:0	0000h RO/V	**Source Identifier (SID):** Requester-id associated with the fault condition This field is relevant only when the F field is set.

3.8.72 Invalidate Address Register (IVA_REG_0_0_0_VTDBAR) — Offset 500h

Register to provide the DMA address whose corresponding IOTLB entry needs to be invalidated through the corresponding IOTLB Invalidate register. This register is a write-only register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 500h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RW	**ADDR:** Software provides the DMA address that needs to be page-selectively invalidated. To make a page-selective invalidation request to hardware, software must first write the appropriate fields in this register, and then issue the appropriate page-selective invalidate command through the IOTLB_REG. Hardware ignores bits 63:N, where N is the maximum guest address width (MGAW) supported. A value returned on a read of this field is undefined A value returned on a read of this field is undefined
11:7	0h RO	**Reserved**
6	0h RW	**Invalidation Hint (IH):** The field provides hint to hardware about preserving or flushing the non-leaf (page-directory) entries that may be cached in hardware: • 0 = Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware must flush both the cached leaf and non-leaf page-table entries corresponding to the mappings specified by ADDR and AM fields. • 1 = Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware may preserve the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields. A value returned on a read of this field is undefined
5:0	00h RW	**Address Mask (AM):** The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation of contiguous mappings for size-aligned regions. For example:..Mask ADDR bits Pages..Value masked invalidated.. 0 None 1.. 1 12 2.. 2 13:12 4.. 3 14:12 8.. 4 15:12 16 When invalidating mappings for super-pages, software must specify the appropriate mask value. For example, when invalidating mapping for a 2MB page, software must specify an address mask value of at least 9...Hardware implementations report the maximum supported mask value through the Capability register.

3.8.73 IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR) — Offset 508h

Register to invalidate IOTLB. The act of writing the upper byte of the IOTLB_REG with IVT field Set causes the hardware to perform the IOTLB invalidation.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 508h	0200000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate IOTLB (IVT):** Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field Hardware clears the IVT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must not submit another invalidation request through this register while the IVT field is Set, nor update the associated Invalidate Address register Software must not submit IOTLB invalidation requests when there is a context-cache invalidation request pending at this remapping hardware unit. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flushing before invalidating the IOTLB.
62	0h RO	**Reserved**
61:60	0h RW	**IOTLB Invalidation Request Granularity (IIRG):** When requesting hardware to invalidate the IOTLB (by setting the IVT field), software writes the requested invalidation granularity through this field. The following are the encodings for the field • 00 = Reserved • 01 = Global invalidation request • 10 = Domain-selective invalidation request. The target domain-id must be specified in the DID field • 11 = Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, and the domain-id must be provided in the DID field Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the IVT field. At this time, the granularity at which actual invalidation was performed is reported through the IAIG field
59	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
58:57	1h RO/V	**IOTLB Actual Invalidation Granularity (IAIG):** Hardware reports the granularity at which an invalidation request was processed through this field when reporting invalidation completion (by clearing the IVT field). The following are the encodings for this field • 00 = Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests • 01 = Global Invalidation performed. This could be in response to a global, domain-selective, or page-selective invalidation request • 10 = Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or a page-selective invalidation request • 11 = Domain-page-selective invalidation performed using the address, mask and hint specified by software in the Invalidate Address register and domain-id specified in DID field. This can be in response to a page-selective invalidation request.
56:50	0h RO	**Reserved**
49	0h RW	**Drain Reads (DR):** This field is ignored by hardware if the DRD field is reported as clear in the Capability register. When the DRD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining any translated DMA read requests • 1 = Hardware must drain DMA read requests.
48	0h RW	**Drain Writes (DW):** This field is ignored by hardware if the DWD field is reported as Clear in the Capability register. When the DWD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining DMA write requests • 1 = Hardware must drain relevant translated DMA write requests.
47:32	0000h RW	**DID:** Indicates the ID of the domain whose IOTLB entries need to be selectively invalidated. This field must be programmed by software for domain-selective and page-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware ignores and not implements bits 47:(32+N), where N is the supported domain-id width reported in the Capability register.
31:0	0h RO	**Reserved**

3.9 GTTMMADR (MCHBAR) Registers

This chapter documents the GTTMMADR MCHBAR registers. Base address of these registers are defined in the GTTMMADR_0_2_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.9.1 Summary of Registers

Table 3-10. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
138148h	4	P-State Limits (P_STATE_LIMITS_0_2_0_GTTMMADR)	000000FFh
138158h	4	Primary Plane Turbo Power Policy (PRIP_TURBO_PLCY_0_2_0_GTTMMADR)	00000000h
13815Ch	4	Secondare Plane Turbo Power Policy (SECP_TURBO_PLCY_0_2_0_GTTMMADR)	00000010h
138180h	8	Cycle Sum of Active Graphics (PKG_GT_C0_ANY_0_2_0_GTTMMADR)	0000000000000000h
138188h	8	Cycle Sum of Overlapping Active GT and Core (PKG_GT_AND_IA_OVERLAP_0_2_0_GTTMMADR)	0000000000000000h
138190h	8	Cycle Sum of Any Active GT Slice (PKG_GT_C0_ANY_SLICE_0_2_0_GTTMMADR)	0000000000000000h
138198h	8	Cycle Sum of All Active GT Slice (PKG_GT_C0_SLICES_SUM_0_2_0_GTTMMADR)	0000000000000000h
1381A0h	8	Cycle Sum of Any Graphics (PKG_GT_C0_ANY_MEDIA_0_2_0_GTTMMADR)	0000000000000000h
1381B4h	4	GT Performance Status (GT_PERF_STATUS_0_2_0_GTTMMADR)	00000000h
1381B8h	4	Thermal Status GT (THERM_STATUS_GT_0_2_0_GTTMMADR)	08000000h
1381BCh	4	GT Thermal Interrupt (THERM_INTERRUPT_GT_0_2_0_GTTMMADR)	00000000h
1381C8h	4	PCU Reference Clock (PCU_REFERENCE_CLOCK_0_2_0_GTTMMADR)	00000000h
145868h	8	Graphics Any Ratio (PKG_GT_C0_ANY_RATIO_0_2_0_GTTMMADR)	0000000000000000h
145870h	8	Cycle Sum of Any Active GT Slice Ratio (PKG_GT_C0_ANY_SLICE_RATIO_0_2_0_GTTMMADR)	0000000000000000h
1459F0h	8	Cycle Sum of Graphics EUs (PKG_GT_C0_EUS_SUM_0_2_0_GTTMMADR)	0000000000000000h
1459F8h	8	Cycle Sum of Any Active Media (PKG_GT_C0_MEDIA_SUM_0_2_0_GTTMMADR)	0000000000000000h

3.9.2 P-State Limits (P_STATE_LIMITS_0_2_0_GTTMMADR) — Offset 138148h

This register allows SW to limit the maximum frequency allowed during run-time.

PCODE will sample this register in slow loop.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 138148h	000000FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCK:** This bit will lock all settings in this register. **Locked by:** P_STATE_LIMITS_0_2_0_GTTMMADR.LOCK
30:16	0h RO	**Reserved**
15:8	00h RW/L	**P-state Minimum (PSTT_MIN):** PG1 ratio (used to be an offset from P1, now absolute to avoid avoid interaction with ConfigTDP). This is clipped to be greater than or equal to Pn (or Pm when LPM is enabled), and less than or equal to P1 (after any adjustments by flex ratio, ConfigTDP, etc). **Locked by:** P_STATE_LIMITS_0_2_0_GTTMMADR.LOCK
7:0	FFh RW/L	**P-state Limit (PSTT_LIM):** This field indicates the maximum IA frequency limit allowed during run-time. **Locked by:** P_STATE_LIMITS_0_2_0_GTTMMADR.LOCK

3.9.3 Primary Plane Turbo Power Policy (PRIP_TURBO_PLCY_0_2_0_GTTMMADR) — Offset 138158h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget betwen the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 138158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**PRIPTP:** Priority Level. A higher number implies a higher priority.

3.9.4 Secondare Plane Turbo Power Policy (SECP_TURBO_PLCY_0_2_0_GTTMMADR) — Offset 13815Ch

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget betwen the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 13815Ch	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	10h RW	**SECPTP:** Priority Level. A higher number implies a higher priority.

3.9.5 Cycle Sum of Active Graphics (PKG_GT_C0_ANY_0_2_0_GTTMMADR) — Offset 138180h

Sum the cycles of active GT

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 138180h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** RO, This counter increments whenever GT slices or un slices are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.9.6 Cycle Sum of Overlapping Active GT and Core (PKG_GT_AND_IA_OVERLAP_0_2_0_GTTMMADR) — Offset 138188h

Sum the cycles of overlap time between any IA cores and GT

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 138188h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever GT slices or un slices are active and in C0 state and in overlap with one of the IA cores that is active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.9.7 Cycle Sum of Any Active GT Slice (PKG_GT_C0_ANY_SLICE_0_2_0_GTTMMADR) — Offset 138190h

Sum the cycles of any active GT slice.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 138190h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** RO, This counter increments whenever any GT slice is active. Counter rate is in Xtal (24/19.2Mhz) clock.

3.9.8 Cycle Sum of All Active GT Slice (PKG_GT_C0_SLICES_SUM_0_2_0_GTTMMADR) — Offset 138198h

Sum the cycles of the sum of active GT slices.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 138198h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO	**DATA:** RO, This counter increments by the sum of active GT slices. Counter rate is in 24MHz.

3.9.9 Cycle Sum of Any Graphics (PKG_GT_C0_ANY_MEDIA_0_2_0_GTTMMADR) — Offset 1381A0h

Sum the cycles of any media GT engine.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 1381A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO	**DATA:** RO, This counter increments whenever any GT media engine is active. Counter rate is in 24MHz.

3.9.10 GT Performance Status (GT_PERF_STATUS_0_2_0_GTTMMADR) — Offset 1381B4h

P-state encoding for the Secondary Power Planes current PLL frequency and the current VID.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 1381B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:20	000h RO/V	**SLICE RATIO (SLICES_RATIO):** GT Slices frequency, in granularity of 16.666Mhz. When GT is in RC6, or when all slices are disabled, this frequency is ZERO.
19:11	000h RO/V	**UNSLICE RATIO (UNSLICE_RATIO):** GT Unslice frequency, in granularity of 16.666Mhz. When GT is in RC6 this frequency is ZERO.
10:8	0h RO	**Reserved**
7:0	00h RO/V/P	**SLICES VOLTAGE (SLICES_VOLTAGE):** GT voltage, in VID units according to SVID spec format.

3.9.11 Thermal Status GT (THERM_STATUS_GT_0_2_0_GTTMMADR) — Offset 1381B8h

Contains status information about the processors thermal sensor and automatic thermal monitoring facilities.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 1381B8h	08000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**VALID:** This bit indicates that the TEMPERATURE field is valid. It is set by PCODE if the temperature is within valid thermal sensor range.
30:27	1h RO	**RESOLUTION:** Supported resolution in degrees C.
26:24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23:16	00h RO/V	**TEMPERATURE:** This is a temperature offset in degrees C below theTJ Max temperature. This number is meaningful only if VALID bit in this register is set.
15	0h RW/0C/V	**Cross Domain limit log (CROSS_DOMAIN_LIMIT_LOG):** R/WC0 - If set (1), indicates another hardware domain (e.g. processor graphics) has limited energy efficiency optimizations in the processor core domain since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
14	0h RO/V	**Cross Domain Limit status (CROSS_DOMAIN_LIMIT_STATUS):** RO - If set (1), indicates another hardware domain (e.g. processor graphics) is currently limiting energy efficiency optimizations in the processor core domain.
13	0h RW/0C/V	**Curent Limit log (CURRENT_LIMIT_LOG):** R/WC0 - If set (1), an electrical current limit has been exceeded that has adversely impacted energy efficiency optimizations since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
12	0h RO/V	**Current Limit status (CURRENT_LIMIT_STATUS):** RO - If set (1), indicates an electrical current limit (e.g. Electrical Design Point/IccMax) is being exceeded and is adversely impacting energy efficiency optimizations.
11	0h RW/0C/V	**Power Limitation log (POWER_LIMITATION_LOG):** R/WC0 - Sticky bit which indicates whether the current P-state is limited by power limitation since the last clearing of this bit or a reset. SW may clear this bit by writing a zero (0). For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level
10	0h RO/V	**Power Limitation status (POWER_LIMITATION_STATUS):** RO - Indicates whether the current P-state is limited by power limitation. For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level.
9	0h RW/0C/V	**THRESHOLD2 log (THRESHOLD2_LOG):** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD2_STATUS bit. This bit is set by HW and cleared by SW.
8	0h RO/V	**THRESHOLD2 status (THRESHOLD2_STATUS):** Indicates that the current temperature is higher than or equal to Threshold 2 temperature.
7	0h RW/0C/V	**THRESHOLD1 log (THRESHOLD1_LOG):** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD1_STATUS bit. This bit is set by HW and cleared by SW.
6	0h RO/V	**THRESHOLD1 status (THRESHOLD1_STATUS):** Indicates that the current temperature is higher than or equal to Threshold 1 temperature.
5	0h RW/0C/V	**Outof Spec log (OUT_OF_SPEC_LOG):** Sticky log bit indicating that the processor operating out of its thermal specification since the last time this bit was cleared. This bit is set by HW on a 0 to 1 transition of OUT_OF_SPEC_STATUS.
4	0h RO/V	**Outof Spec status (OUT_OF_SPEC_STATUS):** Status bit indicating that the processor is operating out of its thermal specification. Once set, this bit should only clear on a reset.
3	0h RW/0C/V	**PROCHOT log (PROCHOT_LOG):** Sticky log bit indicating that xxPROCHOT# has been asserted since the last time this bit was cleared by SW. This bit is set by HW on a 0 to 1 transition of PROCHOT_STATUS.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**PROCHOT status (PROCHOT_STATUS):** Status bit indicating that xxPROCHOT# is currently being asserted.
1	0h RW/0C/V	**Thermal Monitor log (THERMAL_MONITOR_LOG):** Sticky log bit indicating that the core has seen a thermal monitor event since the last time SW cleared this bit. This bit is set by HW on a 0 to 1 transition of THERMAL_MONITOR_STATUS.
0	0h RO/V	**Thermal Monitor Status (THERMAL_MONITOR_STATUS):** Status bit indicating that the Thermal Monitor has tripped and is currently thermally throttling.

3.9.12 GT Thermal Interrupt (THERM_INTERRUPT_GT_0_2_0_GTTMMADR) — Offset 1381BCh

Enables and disables the generation of an interrupt on temperature transitions detected with the processors thermal sensors and thermal monitor.

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Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 1381BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Power Interrupt Enable (POWER_INT_ENABLE):** When this bit is set, a thermal interrupt will be sent upon throttling due to power limitations.
23	0h RW	**Threshold2 Interrupt Enable (THRESHOLD_2_INT_ENABLE):** Controls the generation of a thermal interrupt whenever the Thermal Threshold 2 Temperature is crossed.
22:16	00h RW	**Threshold2 Temperature Level (THRESHOLD_2_REL_TEMP):** This value indicates the offset in degrees below TJ Max Temperature that should trigger a Thermal Threshold 2 trip.
15	0h RW	**Threshold1 Interrupt Enable (THRESHOLD_1_INT_ENABLE):** Controls the generation of a thermal interrupt whenever the Thermal Threshold 1 Temperature is crossed.
14:8	00h RW	**Threshold1 Temperature Level (THRESHOLD_1_REL_TEMP):** This value indicates the offset in degrees below TJ Max Temperature that should trigger a Thermal Threshold 1 trip.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Out of Spec Interrupt Enable (OUT_OF_SPEC_INT_ENABLE):** Thermal interrupt enable for the critical temperature condition which is stored in the Critical Temperature Status bit in IA32_THERM_STATUS.
3	0h RO	**Reserved**
2	0h RW	**PROCHOT Interrupt Enable (PROCHOT_INT_ENABLE):** Bidirectional PROCHOT# assertion interrupt enable. If set, a thermal interrupt is delivered on the rising edge of xxPROCHOT#.
1	0h RW	**Low Temperature Interrupt Enable (LOW_TEMP_INT_ENABLE):** Enables a thermal interrupt to be generated on the transition from a high-temperature to a low-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.
0	0h RW	**High Temperature Interrupt Enable (HIGH_TEMP_INT_ENABLE):** Enables a thermal interrupt to be generated on the transition from a low-temperature to a high-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.

3.9.13 PCU Reference Clock (PCU_REFERENCE_CLOCK_0_2_0_GTTMMADR) — Offset 1381C8h

This register will count BCLK cycles. Values exceeding 32b will wrap around. This value is used for energy and power calculations.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 1381C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Time Value (TIME_VAL):** Number of Cycles

3.9.14 Graphics Any Ratio (PKG_GT_C0_ANY_RATIO_0_2_0_GTTMMADR) — Offset 145868h

new counter, follow exactly the PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU

The only change is that they do +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU

+ 3 * IO_WP_CV_P_STATE[GT_UNSLICE_RATIO] - IO_WP_CV_GT_CONFIG[UNSLICE_SQUASH_DELTA]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 145868h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** RO, This counter increments whenever GT slices or un slices are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC)

3.9.15 Cycle Sum of Any Active GT Slice Ratio (PKG_GT_C0_ANY_SLICE_RATIO_0_2_0_GTTMMADR) — Offset 145870h

new counter, follow exactly the PKG_GT_C0_ANY_SLICEU

The only change is that they do +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU

+ 3 * IO_WP_CV_P_STATE[GT_SLICE_RATIO] - IO_WP_CV_GT_CONFIG[SLICE_SQUASH_DELTA]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 145870h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** RO, This counter increments whenever any GT slice is active. Counter rate is in Xtal (24/19.2Mhz) clock

3.9.16 Cycle Sum of Graphics EUs (PKG_GT_C0_EUS_SUM_0_2_0_GTTMMADR) — Offset 1459F0h

GT EUS MCNT

The counter value is incremented when PKG_GT_C0_ANY_SLICE icrements.

Counts in 24Mhz units.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 1459F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** mmio for software pcode interaface

3.9.17 Cycle Sum of Any Active Media (PKG_GT_C0_MEDIA_SUM_0_2_0_GTTMMADR) — Offset 1459F8h

GT MEDIA MCNT

The counter value is incremented when PKG_GT_C0_ANY_SLICE icrements.

Counts in 24Mhz units.

Note: Bit definitions are the same as PKG_GT_C0_EUS_SUM_0_2_0_GTTMMADR, offset 1459F0h.

4 Processor Graphics (D2:F0)

This chapter documents the Processor Graphics Registers.

Table 4-1. Summary of Processor Graphics (D2:F0)

Processor Graphics Registers (D2:F0)

4.1 Processor Graphics Registers (D2:F0)

Processor Graphics device. This section describes the registers in: Bus 0, Device 2, Function 0.

4.1.1 Summary of Registers

Table 4-2. Summary of Bus: 0, Device: 2, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID2_0_2_0_PCI)	8086h
2h	2	Device ID (DID2_0_2_0_PCI)	9A40h
4h	2	PCI Command (PCICMD_0_2_0_PCI)	0000h
6h	2	PCI Status (PCISTS2_0_2_0_PCI)	0010h
8h	4	Revision Identification and Class Code register (RID2_CC_0_2_0_PCI)	03000000h
Ch	1	Cache Line Size (CLS_0_2_0_PCI)	00h
Dh	1	Master Latency Timer (MLT2_0_2_0_PCI)	00h
Eh	1	Header Type (HDR2_0_2_0_PCI)	00h
Fh	1	Built In Self Test (BIST_0_2_0_PCI)	00h
10h	4	Graphics Translation Table Memory Mapped Range Address (GTTMMADR0_0_2_0_PCI)	00000004h
14h	4	Graphics Translation Table Memory Mapped Range Address (GTTMMADR1_0_2_0_PCI)	00000000h
18h	4	Graphics Memory Range Address (GMADR0_0_2_0_PCI)	0000000Ch
1Ch	4	Graphics Memory Range Address (GMADR1_0_2_0_PCI)	00000000h
20h	4	I/O Base Address (IOBAR_0_2_0_PCI)	00000001h
2Ch	2	Subsystem Vendor Identification (SVID2_0_2_0_PCI)	0000h
2Eh	2	Subsystem Identification (SID2_0_2_0_PCI)	0000h
30h	4	Video BIOS ROM Base Address (ROMADR_0_2_0_PCI)	00000000h
34h	1	Capabilities Pointer (CAPPOINT_0_2_0_PCI)	40h
3Ch	1	Interrupt Line (INTRLINE_0_2_0_PCI)	00h
3Dh	1	Interrupt Pin (INTRPIN_0_2_0_PCI)	01h
3Eh	1	Minimum Grant (MINGNT_0_2_0_PCI)	00h
3Fh	1	Maximum Latency (MAXLAT_0_2_0_PCI)	00h
40h	2	Capability Identifier (CAPID0_0_2_0_PCI)	7009h
42h	2	Capabilities Control (CAPCTRL0_0_2_0_PCI)	010Ch

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
44h	4	Capabilities A (CAPID0_A_0_2_0_PCI)	00000000h
48h	4	Capabilities B (CAPID0_B_0_2_0_PCI)	00000000h
50h	2	PCI Mirror of GMCH Graphics Control (MGGC0_0_2_0_PCI)	0500h
54h	2	Mirror of Device Enable (DEVEN0_0_2_0_PCI)	00BFh
58h	1	Device 2 Control (DEV2CTL_0_2_0_PCI)	00h
60h	4	Multi Size Aperture Control (MSAC_0_2_0_PCI)	00000000h
68h	4	Push Aperture (PUSHAP_0_2_0_PCI)	00000000h
6Ch	1	VTd Status (VTD_STATUS_0_2_0_PCI)	00h
70h	2	PCI Express Capability Header (PCIECAPHDR_0_2_0_PCI)	AC10h
72h	2	PCI Express Capability (PCIECAP_0_2_0_PCI)	0092h
74h	4	Device Capabilities (DEVICECAP_0_2_0_PCI)	10008000h
78h	2	PCI Express Device Control (DEVICECTL_0_2_0_PCI)	0000h
7Ah	2	PCI Express Capability Structure (DEVICESTS_0_2_0_PCI)	0000h
ACh	2	Message Signaled Interrupts Capability ID (MSI_CAPID_0_2_0_PCI)	D005h
AEh	2	Message Control (MC_0_2_0_PCI)	0100h
B0h	4	Message Address (MA_0_2_0_PCI)	00000000h
B4h	2	Message Data (MD_0_2_0_PCI)	0000h
B8h	4	MSI Mask Bits (MSI_MASK_0_2_0_PCI)	00000000h
BCh	4	MSI Pending Bits (MSI_PEND_0_2_0_PCI)	00000000h
C0h	4	Mirror of Base Data of Stolen Memory (BDSM0_0_2_0_PCI)	00000000h
C4h	4	Mirror of Base Data of Stolen Memory (BDSM1_0_2_0_PCI)	00000000h
C8h	4	Graphics VTD Base Address LSB (GFXVTDBAR_LSB_0_2_0_PCI)	00000000h
CCh	4	Graphics VTD Base Address MSB (GFXVTDBAR_MSB_0_2_0_PCI)	00000000h
D0h	2	Power Management Capabilities ID (PMCAPID_0_2_0_PCI)	0001h
D2h	2	Power Management Capabilities (PMCAP_0_2_0_PCI)	0022h
D4h	2	Power Management Control and Status (PMCS_0_2_0_PCI)	0000h
E0h	2	Software SMI (SWSMI_0_2_0_PCI)	0000h
E4h	4	Graphics System Event (GSE_0_2_0_PCI)	00000000h
E8h	2	Software SCI (SWSCI_0_2_0_PCI)	0000h
F0h	4	Device 2 Mirror of Protected Audio Video Path Control (PAVPC0_0_2_0_PCI)	00000000h
F4h	4	Device 2 Mirror of Protected Audio Video Path Control (PAVPC1_0_2_0_PCI)	00000000h
F8h	4	Stepping Revision ID (SRID_0_2_0_PCI)	00000000h
FCh	4	ASL Storage (ASLS_0_2_0_PCI)	00000000h
100h	4	PASID Extended Capability Header (PASID_EXTCAP_0_2_0_PCI)	2001001Bh
104h	2	PASID Capability (PASID_CAP_0_2_0_PCI)	1400h
106h	2	PASID Control (PASID_CTRL_0_2_0_PCI)	0000h
200h	4	ATS Extended Capability Header (ATS_EXTCAP_0_2_0_PCI)	3001000Fh
204h	2	ATS Capability (ATS_CAP_0_2_0_PCI)	0060h
206h	2	ATS Control (ATS_CTRL_0_2_0_PCI)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
300h	4	Page Request Extended Capability Header (PR_EXTCAP_0_2_0_PCI)	00010013h
304h	2	Page Request Control (PR_CTRL_0_2_0_PCI)	0000h
306h	2	Page Request Status (PR_STATUS_0_2_0_PCI)	8100h
308h	4	Outstanding Page Request Capacity (OPRC_0_2_0_PCI)	00008000h
30Ch	4	Outstanding Page Request Allocation (OPRA_0_2_0_PCI)	00000000h
320h	4	SRIOV Extended Capability Header (SRIOV_ECAPHDR_0_2_0_PCI)	00010010h
324h	4	SRIOV Capabilities (SRIOV_CAP_0_2_0_PCI)	00000000h
32Ah	2	SRIOV Status (SRIOV_STS_0_2_0_PCI)	0000h
32Ch	2	SRIOV Initial VFs (SRIOV_INITVFS_0_2_0_PCI)	0007h
32Eh	2	SRIOV Total VFs (SRIOV_TOTVFS_0_2_0_PCI)	0007h
334h	2	First VF Offset (FIRST_VF_OFFSET_0_2_0_PCI)	0001h
336h	2	VF Stride (VF_STRIDE_0_2_0_PCI)	0001h
33Ah	2	VF Device ID (VF_DEVICEID_0_2_0_PCI)	9A40h
33Ch	4	Supported Page Sizes (SUPPORTED_PAGE_SIZES_0_2_0_PCI)	00000553h
340h	4	System Page Sizes (SYSTEM_PAGE_SIZES_0_2_0_PCI)	00000001h
344h	4	VF BAR0 Lower DWORD (VF_BAR0_LDW_0_2_0_PCI)	00000004h
348h	4	VF BAR0 Upper DWORD (VF_BAR0_UDW_0_2_0_PCI)	00000000h
34Ch	4	VF BAR1 LDW (VF_BAR1_LDW_0_2_0_PCI)	0000000Ch
350h	4	VF BAR1 UDW (VF_BAR1_UDW_0_2_0_PCI)	00000000h
35Ch	4	VF Migration State Array Offset (VF_MIGST_OFFSET_0_2_0_PCI)	00000000h

4.1.2 Vendor ID (VID2_0_2_0_PCI) — Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** PCI standard identification for Intel.

4.1.3 Device ID (DID2_0_2_0_PCI) — Offset 2h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 2h	9A40h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:7	134h RO	**Device ID MSB (DID_MSB):** Upper byte of the Device ID.
6:0	40h RO/V	**Device ID LSB (DID_LSB):** Lower byte of the Device ID.

4.1.4 PCI Command (PCICMD_0_2_0_PCI) — Offset 4h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW/V	**Interrupt Disable (INTDIS):** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	0h RO	**Fast Back-To-Back (FB2B):** Not Implemented. Hardwired to 0.
8	0h RO	**SERR Enable (SEN):** Not Implemented. Hardwired to 0.
7	0h RO	**Wait Cycle Control (WCC):** Not Implemented. Hardwired to 0.
6	0h RO	**Parity Error Enable (PER):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	0h RO	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	0h RO	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	0h RW/V	**Bus Master Enable (BME):** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.
1	0h RW/V	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	0h RW/V/L	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is read-only 0 if DEV2CTL[0].IOBARDIS at offset 58h is 1. **Locked by:** DEV2CTL_0_2_0_PCI.IOBARDIS

4.1.5 PCI Status (PCISTS2_0_2_0_PCI) — Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	0h RO	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	0h RO	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	0h RO	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	0h RO	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	0h RO	**Device Select Timing (DEVT):** Hardwired to 00.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.
7	0h RO	**Fast Back-To-Back (FB2B):** Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).
6	0h RO	**User Defined Format (UDF):** Hardwired to 0.
5	0h RO	**66MHz PCI Capable (C66):** Hardwired to 0.
4	1h RO	**Capability List (CLIST):** This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	0h RO/V	**Interrupt Status (INTSTS):** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
2:0	0h RO	**Reserved**

4.1.6 Revision Identification and Class Code register (RID2_CC_0_2_0_PCI) — Offset 8h

This register contains the revision number for Device #2 Functions 0 and contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 8h	03000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	03h RO/V	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 03h, indicating a Display Controller Device.
23:16	00h RO/V	**Sub-Class Code (SUBCC):** When MGGC0[VAMEN] is 0, this value is 00h. When MGGC0[VAMEN] is 1, this value is 80h, indicating other display device.
15:8	00h RO	**Programming Interface (PI):** When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller.When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.
7:0	00h RO	**Revision ID (RID):** Revision ID of the device

4.1.7 Cache Line Size (CLS_0_2_0_PCI) — Offset Ch

PCI standard Cache Line Size register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size Value (CLS):** This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

4.1.8 Master Latency Timer (MLT2_0_2_0_PCI) — Offset Dh

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Master Latency Timer Count Value (MLTCV):** Hardwired to 0s.

4.1.9 Header Type (HDR2_0_2_0_PCI) — Offset Eh

This register contains the Header Type of the IGD.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi Function Status (MFUNC):** Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
6:0	00h RO	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

4.1.10 Built In Self Test (BIST_0_2_0_PCI) — Offset Fh

This register is used for control and status of Built In Self Test (BIST).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST Supported (BISTS):** BIST is not supported. This bit is hardwired to 0.
6:0	0h RO	**Reserved**

4.1.11 Graphics Translation Table Memory Mapped Range Address (GTTMMADR0_0_2_0_PCI) — Offset 10h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device configuration space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V	**Memory Base Address (MBA_0):** Set by the OS, these bits correspond to address signals [63:24].
23:4	00000h RO	**Address Mask (ADM):** Hardwired to 0s to indicate at least 16MB address range.
3	0h RO	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**Memory Type (MEMTYP):** Hardwired to 2h to indicate 64 bit base address.
0	0h RO	**Memory I/O Space (MIOS):** Hardwired to 0 to indicate memory space.

4.1.12 Graphics Translation Table Memory Mapped Range Address (GTTMMADR1_0_2_0_PCI) — Offset 14h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device configuration space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Memory Base Address (MBA_1):** Set by the OS, these bits correspond to address signals [63:24].

4.1.13 Graphics Memory Range Address (GMADR0_0_2_0_PCI) — Offset 18h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 18h	0000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**4096MB Address Mask (ADMSK4096):** This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ4
30	0h RW/V/L	**2048MB Address Mask (ADMSK2048):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ3
29	0h RW/V/L	**1024MB Address Mask (ADMSK1024):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ2
28	0h RW/V/L	**512MB Address Mask (ADMSK512):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ1

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/V/L	**256MB Address Mask (ADMSK256):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ0
26:4	000000h RO	**Address Mask (ADM):** Hardwired to 0s to indicate at least 128MB address range.
3	1h RO	**Prefetchable Memory (PREFMEM):** Hardwired to 1 to enable prefetching.
2:1	2h RO	**Memory Type (MEMTYP):** Hardwired to 2h to indicate 64 bit base address.
0	0h RO	**Memory I/O Space (MIOS):** Hardwired to 0 to indicate memory space.

4.1.14 Graphics Memory Range Address (GMADR1_0_2_0_PCI) — Offset 1Ch

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Memory Base Address (MBA):** Set by the OS, these bits correspond to address signals [63:32].

4.1.15 I/O Base Address (IOBAR_0_2_0_PCI) — Offset 20h

This register provides the Base offset of the I/O registers within Device #2.

Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space.

Bits 2:1 are fixed and return zero

Bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set.

Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled.

Note that access to this IO BAR is independent of VGA functionality within Device #2.

If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.

This IO BAR can be disabled and hidden from system software via DEV2CTL[0] IOBARDIS at offset 0x58.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 20h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:6	000h RW/V/L	**IO Base Address (IOBASE):** Set by the OS, these bits correspond to address signals [15:6]. Note: This field is RO 0's if DEV2CTL[0] IOBARDIS is 1b. **Locked by:** DEV2CTL_0_2_0_PCI.IOBARDIS
5:3	0h RO	**Reserved**
2:1	0h RO	**Memory Type (MEMTYPE):** Hardwired to 0s to indicate 32-bit address.
0	1h RO	**Memory I/O Space (MIOS):** Hardwired to '1' to indicate IO space. Note: This field is RO 0's if DEV2CTL[0] IOBARDIS is 1b.

4.1.16 Subsystem Vendor Identification (SVID2_0_2_0_PCI) — Offset 2Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Subsystem Vendor Id (SUBVID):** This value is used to identify the vendor of the subsystem.

4.1.17 Subsystem Identification (SID2_0_2_0_PCI) — Offset 2Eh

This register is used to uniquely identify the subsystem where the PCI device resides.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Subsystem ID (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up.

4.1.18 Video BIOS ROM Base Address (ROMADR_0_2_0_PCI) — Offset 30h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0000h RO	**ROM Base Address (RBA):** Hardwired to 0's.
17:11	00h RO	**Address Mask (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	0h RO	**Reserved**
0	0h RO	**ROM BIOS Enable (RBE):** Hardwired to 0 to indicate ROM not accessible.

4.1.19 Capabilities Pointer (CAPPOINT_0_2_0_PCI) — Offset 34h

This register points to a linked list of capabilities implemented by this device.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 34h	40h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RO	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.

4.1.20 Interrupt Line (INTRLINE_0_2_0_PCI) — Offset 3Ch

This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Connection (INTCON):** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

4.1.21 Interrupt Pin (INTRPIN_0_2_0_PCI) — Offset 3Dh

This register tells which interrupt pin the device uses.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**Interrupt Pin Value (INTPIN):** As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.

4.1.22 Minimum Grant (MINGNT_0_2_0_PCI) — Offset 3Eh

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Minimum Grant Value (MGV):** Hardwired to 0s because the IGD does not burst as a PCI compliant master.

4.1.23 Maximum Latency (MAXLAT_0_2_0_PCI) — Offset 3Fh

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Maximum Latency Value (MLV):** Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

4.1.24 Capability Identifier (CAPID0_0_2_0_PCI) — Offset 40h

PCI standard Capability Identifier

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 40h	7009h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RO	**Next Capability Pointer (NEXT_CAP):** This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
7:0	09h RO	**Capability Identifier (CAP_ID):** This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

4.1.25 Capabilities Control (CAPCTRL0_0_2_0_PCI) — Offset 42h

Capabilities Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 42h	010Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	1h RO	**CAPID Version (CAPID_VER):** This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
7:0	0Ch RO	**CAPID Length (CAPIDLEN):** This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).

4.1.26 Capabilities A (CAPID0_A_0_2_0_PCI) — Offset 44h

Various Capabilities of the device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO/V	**Display FuSa Disabled (DISPLAY_FUSA_DIS):** 0: Display FuSa is enabled 1: Display FuSa is disabled Note: FuSa is an acronym for Functional Safety.
23:4	0h RO	**Reserved**
3	0h RO/V	**VGT Enabled (VGT_EN):** 0: VGT is disabled 1: VGT is enabled
2	0h RO	**Reserved**
1	0h RO/V	**SVM Disabled (SVMD):** 0: SVM is enabled 1: SVM is disabled
0	0h RO/V	**VTD Disable (VTDD):** 0: VTD is enabled 1: VTD is disabled

4.1.27 Capabilities B (CAPID0_B_0_2_0_PCI) — Offset 48h

Various Capabilities of the device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

4.1.28 PCI Mirror of GMCH Graphics Control (MGGC0_0_2_0_PCI) — Offset 50h

Mirror of GGC register from GTTMMADR Space at offset 0x108040.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 50h	0500h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	05h RO/V	**Graphics Memory Size (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h: 0MB 01h - 10h: 32MB, 64MB, 96MB, ..., 512MB 11h - 1Fh: Reserved 20h: 1024MB 21h - 2Fh: Reserved 30h: 1536MB 31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved F0h - FEh: 4MB, 8MB, 12MB, ..., 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
7:6	0h RO/V	**Graphics Translation Table Memory Size (GGMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0:No Preallocated Memory 0x1:2MB of Preallocated Memory 0x2:4MB of Preallocated Memory 0x3:8MB of Preallocated Memory
5:3	0h RO	**Reserved**
2	0h RO/V	**Versatile Acceleration Mode Enable (VAMEN):** Enables the use of the iGFX engines for Versatile Acceleration. 0: iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h. 1: iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 038000h.
1	0h RO/V	**IVD:** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO) BIOS Requirement: If a value of 1 is written, GGC[VAMEN] (ie. bit 2 in this register) should be also written to '1 so the sub-class field changes to 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved**

4.1.29 Mirror of Device Enable (DEVEN0_0_2_0_PCI) — Offset 54h

Mirror of DEVEN_0_0_0_PCI.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 54h	00BFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RO/V	**CHAP Enable (D7EN):** 0: Device 7 is disabled 1: Device 7 is enabled
13	0h RO	**Device 6 Enable (D6EN):** 0: Device 6 is disabled 1: Device 6 is enabled
12:11	0h RO	**Reserved**
10	0h RO	**Device 5 Enable (D5EN):** 0: Device 5 is disabled 1: Device 5 is enabled
9:8	0h RO	**Reserved**
7	1h RO/V	**Device 4 Enable (D4EN):** 0: Device 4 is disabled 1: Device 4 is enabled
6	0h RO	**Reserved**
5	1h RO/V	**Device 3 Enable For Display HD Audio (D3EN):** 0: Device 3 is disabled 1: Device 3 is enabled
4	1h RO/V	**Internal Graphics Engine (D2EN):** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
3	1h RO/V	**PEG10 Enable (D1F0EN):** Device 1, Function 0 is enabled

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**PEG11 Enable (D1F1EN):** Device 1, Function 1 is enabled
1	1h RO/V	**PEG12 Enable (D1F2EN):** Device 1, Function 2 is enabled
0	1h RO	**Host Bridge Enable (D0EN):** Device 0, Function 0 is enabled

4.1.30 Device 2 Control (DEV2CTL_0_2_0_PCI) — Offset 58h

This register implements a control bit to disable and hide the IOBAR register in systems that do not require legacy IOBAR access to Gfx MMIO registers.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 58h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW	**IO BAR Disable (IOBARDIS):** System BIOS can choose to disable and hide the IOBAR for systems that do not require legacy IOBAR access to GFX MMIO registers. 0b: IOBAR is enabled and exposed at offset 0x20 in Device 2 Configuration space (Default). 1b: IOBAR is disabled and not visible in PCI Configuration Space. Behaves as if hardwired to zeros.

4.1.31 Multi Size Aperture Control (MSAC_0_2_0_PCI) — Offset 60h

This register contains MSAC register which determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register.

Bits [20:16] 00000b: 128MB, GMADR[26:4] is hardwired to all 0

Bits [20:16] 00001b: 256MB, GMADR[27:4] overridden to all 0

Bits [20:16] 00010b: illegal (hardware will treat this as 00011b)

Bits [20:16] 00011b: 512MB, GMADR[28:27] overridden to all 0

Bits [20:16] 00100-00110b: illegal (hardware will treat this as 00111b)

Bits [20:16] 00111b: 1024MB, GMADR[29:27] overridden to all 0

Bits [20:16] 01000-01110b: illegal (hardware will treat this as 01111b)

Bits [20:16] 01111b: 2048MB, GMADR[30:27] overridden to all 0

Bits [20:16] 10000-11110b: illegal (hardware will treat this as 11111b)

Bits [20:16] 11111b: 4096MB, GMADR[31:27] overridden to all 0

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/V	**Untrusted Aperture Size Bit 4 (APSZ4):** Untrusted Aperture Size Bit 4
19	0h RW/V	**Untrusted Aperture Size Bit 3 (APSZ3):** Untrusted Aperture Size Bit 3
18	0h RW/V	**Untrusted Aperture Size Bit 2 (APSZ2):** Untrusted Aperture Size Bit 2
17	0h RW/V	**Untrusted Aperture Size Bit 1 (APSZ1):** Untrusted Aperture Size Bit 1
16	0h RW/V	**Untrusted Aperture Size Bit 0 (APSZ0):** Untrusted Aperture Size Bit 0
15:0	0h RO	**Reserved**

4.1.32 Push Aperture (PUSHAP_0_2_0_PCI) — Offset 68h

GT writes this Push Aperture register to ensure aperture writes have been pushed to DRAM.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Token Value (TOKEN_VALUE):** 32 bit Token Value. GT (GuC) writes a DWORD Token value to this field. A write to this register triggers a write response to GT. The response write will use the value written into this register.

4.1.33 VTd Status (VTD_STATUS_0_2_0_PCI) — Offset 6Ch

This register contains indicator bits for Graphics VTd mode.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 6Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RO	**GFX VTd Active (VTACT):** Reflects GFX VTd Mode is active. 1: GFX VTd Mode is active 0: GFX VTd Mode is inactive.

4.1.34 PCI Express Capability Header (PCIECAPHDR_0_2_0_PCI) — Offset 70h

PCI Express Capability Header

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 70h	AC10h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	ACh RO	**Next Capability Pointer (NEXT_PTR):** This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
7:0	10h RO	**Capability Identifier (CAP_ID):** This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

4.1.35 PCI Express Capability (PCIECAP_0_2_0_PCI) — Offset 72h

PCI Express Capability

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 72h	0092h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:9	00h RO	**Interrupt Message Number (INTRMSG):** This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure.Since this device only supports one MSI vector, this field is hardwired to 0.
8	0h RO	**Slot Implemented (SLOTIMP):** This field is hardwired to 0 for an endpoint device.
7:4	9h RO	**Device Type (DEV_TYPE):** This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.
3:0	2h RO	**Capability Version (CAP_VER):** This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.

4.1.36 Device Capabilities (DEVICECAP_0_2_0_PCI) — Offset 74h

PCI Express Device Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 74h	10008000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**Functional Level Reset Capability (FLRCAP):** Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
27:26	0h RO	**Captured Slot Power Limit Scale (PWR_LIM_SCALE):** Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b
25:18	00h RO	**Captured Slot Power Limit Value (CSPLS):** Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Reserved**
15	1h RO	**Role-Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14:12	0h RO	**Reserved**
11:9	0h RO	**Endpoint L1 Acceptable Latency (EPL1AL):** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state.This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 1 us).
8:6	0h RO	**Endpoint L0S Acceptable Latency (EPL0AL):** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state.This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 64 ns).
5	0h RO	**Extended Tag Field Supported (ETFS):** This bit indicates the maximum supported size of the Tag field as a Requester.This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).
4:3	0h RO	**Phantom Functions Supported (PFS):** This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices.This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.
2:0	0h RO	**Max Payload Size Supported (MPSS):** This field indicates the maximum payload size that the Function can support for TLPs.Hardwired to 000b to represents 128 bytes, the minimum allowed value.

4.1.37 PCI Express Device Control (DEVICECTL_0_2_0_PCI) — Offset 78h

PCI Express Device Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 78h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**Initiate Function Level Reset (INIT_FLR):** A write of 1b initiates Function Level Reset to the Function.During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.

Bit Range	Default & Access	Field Name (ID): Description
14:12	0h RO	**Max Read Request Size (MRRS):** Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
11	0h RO	**Enable No Snoop (ENS):** This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates.The graphics device never generates a PCI Express TLP.
10	0h RO	**Aux Power PM Enable (APPME):** Functions that do not implement this capability hardwire this bit to 0b.
9	0h RO	**Phantom Functions Enable (PFE):** Functions that do not implement this capability hardwire this bit to 0b.
8	0h RO	**Extended Tag Field Enable (ETFE):** Functions that do not implement this capability hardwire this bit to 0b.
7:5	0h RO	**Max Payload Size (MPS):** Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
4	0h RO	**Enable Relaxed Ordering (ERO):** A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester.The graphics device never generates a PCI Express TLP.
3	0h RO	**Unsupported Request Response Enable (URRE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
2	0h RW/V	**Fatal Error Enable (FEE):** This bit, in conjunction with other bits, controls sending ERR_FATAL Messages.
1	0h RW/V	**Non-Fatal Error Enable (NFEE):** This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages.
0	0h RW/V	**Correctable Error Enable (CEE):** This bit, in conjunction with other bits, controls sending ERR_COR Messages.

4.1.38 PCI Express Capability Structure (DEVICESTS_0_2_0_PCI) — Offset 7Ah

PCI Express Capability Structure

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 7Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Transactions Pending (TP):** When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed.A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
4	0h RO	**Aux Power Detected (APD):** Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
3	0h RO	**Unsupported Request Detected (URD):** This bit indicates the Function received an Unsupported Request.Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
2	0h RW/V	**Fatal Error Detected (FED):** This bit indicates status of fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.
1	0h RW/V	**Non-Fatal Error Detected (NFED):** This bit indicates status of non fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.
0	0h RW/V	**Correctable Error Detected (CED):** This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.

4.1.39 Message Signaled Interrupts Capability ID (MSI_CAPID_0_2_0_PCI) — Offset ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + ACh	D005h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	D0h RO	**Pointer To Next Capability (POINTNEXT):** This is a hardwired pointer to the next item in the capabilities list.
7:0	05h RO	**Capability ID (CAPID):** This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

4.1.40 Message Control (MC_0_2_0_PCI) — Offset AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + AEh	0100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	1h RO	**Per Vector Mask Capable (PVMASKCAP):** SR-IOV requires this capability.
7	0h RO	**64BIT Capable (CAP64B):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.
6:4	0h RW/V	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested.Value: Number of requests000: 1001: 2010: 4011: 8100: 16101: 32110: Reserved111: Reserved
3:1	0h RO	**Multiple Message Capable (MMC):** System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.
0	0h RW/V	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs.

4.1.41 Message Address (MA_0_2_0_PCI) — Offset B0h

This register contains the Message Address for MSIs sent by the device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW/V	**Message Address Field (MESSADD):** Used by system software to assign an MSI address to the device.The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	0h RO	**Force DWORD Align (FDWORD):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

4.1.42 Message Data (MD_0_2_0_PCI) — Offset B4h

This register contains the Message Data for MSIs sent by the device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + B4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**Message Data (MESSDATA):** Base message data pattern assigned by system software and used to handle an MSI from the device.When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

4.1.43 MSI Mask Bits (MSI_MASK_0_2_0_PCI) — Offset B8h

This register contains the MSI Mask Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/V	**Mask Bit For Vector 0 (MASKBIT):** For each Mask bit that is set, the function is prohibited from sending the associated message.

4.1.44 MSI Pending Bits (MSI_PEND_0_2_0_PCI) — Offset BCh

This register contains the MSI Pending Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**Pending Bit For Vector 0 (PENDBIT):** For each Pending bit that is set, the function has a pending associated message. If this bit is set when the corresponding vector's Mask bit is cleared, the function will send an MSI and then clear the Pending bit.

4.1.45 Mirror of Base Data of Stolen Memory (BDSM0_0_2_0_PCI) — Offset C0h

Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO/V	**Graphics Base Of Stolen Memory LSB (BDSM_LSB):** This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.
19:0	0h RO	**Reserved**

4.1.46 Mirror of Base Data of Stolen Memory (BDSM1_0_2_0_PCI) — Offset C4h

Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**Graphics Base Of Stolen Memory MSB (BDSM_MSB):** This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.

4.1.47 Graphics VTD Base Address LSB (GFXVTDBAR_LSB_0_2_0_PCI) — Offset C8h

This is the base address for the Graphics VTD configuration space.

There is no physical memory within this 4KB window that can be addressed.

The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN.

None of the bits in this register are writable in Intel TXT mode.

BIOS programs this register, after which the register cannot be altered.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**GFX-VTD Base Address Lower DWORD (GFXVTDBAR):** This field corresponds to bits 31 to 12 of the base address GFX-VTD configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set.
11:1	0h RO	**Reserved**
0	0h RW/V	**GFX-VTBAR Enable (GFXVTDBAREN):** 0: GFX-VTBAR is disabled and does not claim any memory. 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled.

4.1.48 Graphics VTD Base Address MSB (GFXVTDBAR_MSB_0_2_0_PCI) — Offset CCh

This is the base address for the Graphics VTD configuration space.

There is no physical memory within this 4KB window that can be addressed.

The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN.

None of the bits in this register are writable in Intel TXT mode.

BIOS programs this register, after which the register cannot be altered.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFX-VTD Base Address Upper DWORD (GFXVTDBAR):** This field corresponds to bits 63 to 32 of the base address GFX-VTD configuration space. BIOS will program this register, resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set.

4.1.49 Power Management Capabilities ID (PMCAPID_0_2_0_PCI) — Offset D0h

This register contains the PCI Power Management Capability ID and the next capability pointer.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + D0h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Capability Pointer (NEXT_PTR):** This is a hardwired pointer to the next item in the capabilities list.
7:0	01h RO	**Capability Identifier (CAP_ID):** Hardwired to 01h for power management.

4.1.50 Power Management Capabilities (PMCAP_0_2_0_PCI) — Offset D2h

This register provides information on the capabilities of the function related to power management.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + D2h	0022h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RO	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	0h RO	**D2 Support (D2):** Hardwired to 0 to indicate the D2 power management state is not supported.
9	0h RO	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	0h RO	**Reserved**
5	1h RO	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	2h RO	**Power Management Interface Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

4.1.51 Power Management Control and Status (PMCS_0_2_0_PCI) — Offset D4h

Power Management Control and Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + D4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PME Status (PMESTS):** This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSCALE):** This field is hardwired to 00 to indicate IGD does not support data register.
12:9	0h RO	**Data Select (DSEL):** This field is hardwired to 0h to indicate IGD does not support data register.
8	0h RO	**PME Enable (PMEEN):** This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	0h RO	**Reserved**
1:0	0h RW/V	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec.Bits[1:0]Power state00:D0Default01:D1Not Supported10:D2Not Supported11:D3

4.1.52 Software SMI (SWSMI_0_2_0_PCI) — Offset E0h

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0 address E0h-E1h must be reserved for this register.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + E0h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**Software Scratch Bits (SWSB):** Software Scratch Bits
7:1	00h RW	**Software Flag (SWF):** Used to indicate caller and SMI function desired, as well as return result.
0	0h RW	**Software SMI Event (GSSMIE):** When Set this bit will trigger an SMI. Software must write a '0' to clear this bit.SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.

4.1.53 Graphics System Event (GSE_0_2_0_PCI) — Offset E4h

This register can be accessed by either Byte, Word, or DWORD PCI configuration cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Graphics System Event Scratch Trigger 3 (GSE3):** Graphics System Event Scratch Trigger 3
23:16	00h RW	**Graphics System Event Scratch Trigger 2 (GSE2):** Graphics System Event Scratch Trigger 2
15:8	00h RW	**Graphics System Event Scratch Trigger 1 (GSE1):** Graphics System Event Scratch Trigger 1
7:0	00h RW	**Graphics System Event Scratch Trigger 0 (GSE0):** Graphics System Event Scratch Trigger 0

4.1.54 Software SCI (SWSCI_0_2_0_PCI) — Offset E8h

This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) SCI Event trigger (GSSCIE - bit 0). To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a '0' to '1' subsequent transition in bit 0 of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a '0' to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + E8h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**SMI Or SCI Event Select (SMISCISEL):** 0 = SMI (default)1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.
14:1	0000h RW	**Software Scratch Bits (SCISB):** Read/write bits not used by hardware.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Software SCI Event (GSSCIE):** If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.

4.1.55 Device 2 Mirror of Protected Audio Video Path Control (PAVPC0_0_2_0_PCI) — Offset F0h

Device 2 Mirror of Protected Audio Video Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO/V	**WOPCM Base LSB (WOPCMBASE_LSB):** Base value programmed (from Top of Stolen Memory). The programmed value must be consistent with the WOPCM Size programming.
19:7	0h RO	**Reserved**
6	0h RO/V	**ASMF Method Enable (ASMFEN):** 0: Disable ASMF 1: Enable ASMF
5	0h RO	**Reserved**
4	0h RO/V	**Override Terminate Attack (OVTATTACK):** Override of unsolicited connection state attack and terminate 0: Disable override; attack terminate allowed 1: Enable override; attack terminate disallowed
3	0h RO/V	**Heavy Mode Select (HVYMODSEL):** Heavy/light encryption mode select 0: Surface encryption is disabled - Light mode 1: Surface encryption is enabled
2	0h RO/V	**Lock Bit (LOCK):** BIOS will set this bit with bit 0 and/or bit 1.
1	0h RO/V	**PAVP Enable (PAVPE):** 0: PAVP functionality disabled 1: PAVP functionality enabled
0	0h RO/V	**PCM Enable (PCME):** Protected content memory enable.

4.1.56 Device 2 Mirror of Protected Audio Video Path Control (PAVPC1_0_2_0_PCI) — Offset F4h

Device 2 Mirror of Protected Audio Video Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**WOPCM Base MSB (WOPCMBASE_MSB):** Base value programmed (from Top of Stolen Memory). The programmed value must be consistent with the WOPCM Size programming.

4.1.57 Stepping Revision ID (SRID_0_2_0_PCI) — Offset F8h

Stepping Revision ID of this device

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**Stepping Revision ID MSB (SRID_MSB):** Upper 4 bit of the Stepping Revision ID.
19:16	0h RO	**Stepping Revision ID LSB (SRID_LSB):** Lower 4 bit of the Stepping Revision ID.
15:0	0h RO	**Reserved**

4.1.58 ASL Storage (ASLS_0_2_0_PCI) — Offset FCh

This is a software scratch register.

The exact bit register usage must be worked out in common between System BIOS and driver software.

For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/Non-VGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Device Switching Storage (DSS):** Software controlled usage to support device switching.

4.1.59 PASID Extended Capability Header (PASID_EXTCAP_0_2_0_PCI) — Offset 100h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 100h	2001001Bh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	200h RO	**Next Capability Offset (NCO):** This is a hardwired pointer to the next item in the capabilities list.
19:16	1h RO	**Version ID (V):** Hardwired to capability version 1.
15:0	001Bh RO	**Capability ID (CAPID):** Hardwired to the PASID Extended Capability ID

4.1.60 PASID Capability (PASID_CAP_0_2_0_PCI) — Offset 104h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 104h	1400h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:8	14h RO	**Maximum PASID Width (MPW):** Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).
7:3	0h RO	**Reserved**
2	0h RO	**Privilege Mode Supported (PMS):** Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.
1	0h RO	**Execute Permission Supported (EPS):** Hardwired to 0, the Endpoint supports requests-with-PASID that requests execute permission.
0	0h RO	**Reserved**

4.1.61 PASID Control (PASID_CTRL_0_2_0_PCI) — Offset 106h

Process Address Space ID (PASID) control for Device-2.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 106h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2	0h RO	**Privileged Mode Enable (PME):** Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Execute Permission Enable (EPE):** If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set.Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.
0	0h RW	**PASID Enable (PE):** If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If privileged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0).Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.

4.1.62 ATS Extended Capability Header (ATS_EXTCAP_0_2_0_PCI) — Offset 200h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 200h	3001000Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	300h RO	**Next Capability Offset (NCO):** This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
19:16	1h RO	**Version ID (V):** Hardwired to capability version 1.
15:0	000Fh RO	**Capability ID (CAPID):** Hardwired to the ATS Extended Capability ID

4.1.63 ATS Capability (ATS_CAP_0_2_0_PCI) — Offset 204h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 204h	0060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	1h RO	**Global Invalidate Supported (GIS):** If Set, the Function supports Invalidation Requests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate requests.Reserved
5	1h RO	**Page Aligned Request (PAR):** Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.
4:0	00h RO	**Invalidate Queue Depth (IQE):** The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.

4.1.64 ATS Control (ATS_CTRL_0_2_0_PCI) — Offset 206h

ATS Control register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 206h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**ATS Enable (AE):** When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemented as RW as software can read it to determine ATS enable status.
14:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:0	00h RW	**Smallest Translation Unit (STU):** This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^STU. A value of 0 indicates one block and value 1F indicates 2^31 blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.

4.1.65 Page Request Extended Capability Header (PR_EXTCAP_0_2_0_PCI) — Offset 300h

Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 300h	00010013h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO/V	**Next Capability Offset (NCO):** This is a hardwired pointer to the next item in the capabilities list. Value 000h (Default) indicates that this is the end of the PCI-Express Extended capability Linked List. When Graphics Virtualization is enabled, this field is hardwired to point to the next PCI Capability structure, the SRIOV Extended Capability Header at 320h. When Graphics Virtualization is disabled, this field will be hardwired to 000h to indicate the end of PCI-Express Extended capability Linked List.
19:16	1h RO	**Version ID (V):** Hardwired to capability version 1.
15:0	0013h RO	**Capability ID (CAPID):** Hardwired to the Page Request Extended Capability ID

4.1.66 Page Request Control (PR_CTRL_0_2_0_PCI) — Offset 304h

Page Request Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 304h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**RST:** When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).
0	0h RW	**Page-Request Enable (PRE):** When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.

4.1.67 Page Request Status (PR_STATUS_0_2_0_PCI) — Offset 306h

Page Request Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 306h	8100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**PRG Response PASID Required (PRPR):** If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.

Bit Range	Default & Access	Field Name (ID): Description
14:9	0h RO	**Reserved**
8	1h RO	**S:** When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.
7:2	0h RO	**Reserved**
1	0h RW/V	**Unexpected Page Request Group Index (UPGRI):** When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.
0	0h RW/V	**Response Failure (RF):** When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.

4.1.68 Outstanding Page Request Capacity (OPRC_0_2_0_PCI) — Offset 308h

Outstanding Page Request Capacity

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 308h	00008000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00008000h RO	**Outstanding Page Request Capacity (OPRC):** This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

4.1.69 Outstanding Page Request Allocation (OPRA_0_2_0_PCI) — Offset 30Ch

Outstanding Page Request Allocation

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 30Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Outstanding Page Request Allocation (OPRA):** This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

4.1.70 SRIOV Extended Capability Header (SRIOV_ECAPHDR_0_2_0_PCI) — Offset 320h

SR-IOV Extended Capability Header.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 320h	00010010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**Next Capability Offset (NEXT_0):** Next capability Offset. Value = 0x000 to indicate the end of the Extended Capability List
19:16	1h RO	**Capability Version (CAP_VER):** Capability Version
15:0	0010h RO	**PCIE Extended Capability ID (PCIE_ECAP_ID):** PCIE Extended capability ID

4.1.71 SRIOV Capabilities (SRIOV_CAP_0_2_0_PCI) — Offset 324h

Defines SR-IOV Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 324h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	000h RO	**VF Migration Interrupt Message Number (VF_MIG_INTR_MSG_NUM):** Value: 0. VF Migration is not supported.
20:2	0h RO	**Reserved**
1	0h RO	**ARI Capable Hierarchy Preserved (ARI_CAP_HIER_PRESERVED):** Value: Always 0. ARI is not supported.
0	0h RO	**VF Migration Capable (VF_MIG_CAP):** Value:0. VF Migration not supported.

4.1.72 SRIOV Status (SRIOV_STS_0_2_0_PCI) — Offset 32Ah

SR-IOV Status Register.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 32Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VF Migration Status (VF_MIG_STS):** VF Migration Status

4.1.73 SRIOV Initial VFs (SRIOV_INITVFS_0_2_0_PCI) — Offset 32Ch

Defines Initial number of VFs available to the VMM.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 32Ch	0007h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0007h RO/V	**Initial VFs (INITIAL_VFS):** For SR-IOV implementation, this value must exactly match the Total VFs

4.1.74 SRIOV Total VFs (SRIOV_TOTVFS_0_2_0_PCI) — Offset 32Eh

Defines the Total number of VFs available to the VMM.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 32Eh	0007h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0007h RO	**Total VFs (TOTAL_VFS):** Indicates the maximum number of VFs that could be associated with the PF

4.1.75 First VF Offset (FIRST_VF_OFFSET_0_2_0_PCI) — Offset 334h

Defines the offset of the function number from the PF to the first VF.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 334h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0001h RO	**First VF Offset Value (FIRST_VF_OFFSET):** Defines the routing ID offset of the first VF that is associated with the PF that contains this Capability structure. The first VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the PF containing this field ignoring any carry, using unsigned, 16-bit arithmetic. The value of this field is hardwired to 0001h.

4.1.76 VF Stride (VF_STRIDE_0_2_0_PCI) — Offset 336h

Defines the stride of the function number from one VF to the next.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 336h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0001h RO	**VF Stride Value (VF_STRIDE):** Defines the Routing ID offset from one VF to the next one for all VFs associated with the PF that contains this Capability structure. The next VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the current VF, ignoring any carry, using unsigned 16-bit arithmetic. The value of this field is hardwired to 0001h.

4.1.77 VF Device ID (VF_DEVICEID_0_2_0_PCI) — Offset 33Ah

Defines the Device ID to be used by all Virtual Functions

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 33Ah	9A40h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	9A40h RO/V	**VF Device ID (VF_DEVICEID):** Mirror the same device ID as the PF

4.1.78 Supported Page Sizes (SUPPORTED_PAGE_SIZES_0_2_0_PCI) — Offset 33Ch

Defines the System Page Sizes supported by this SR-IOV implementation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 33Ch	00000553h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000553h RO	**Supported Page Sizes Value (PAGE_SIZES):** This field indicates the page sizes supported by the PF. This PF supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the PF supports 4-KB page sizes. PFs are required to support 4-KB, 8-KB, 64-KB, 256-KB, 1-MB, and 4-MB page sizes. All other page sizes are optional, and not supported in this implementation.

4.1.79 System Page Sizes (SYSTEM_PAGE_SIZES_0_2_0_PCI) — Offset 340h

Defines the System Page Size chosen by the VMM.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 340h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RO	**Graphics System Event Scratch Trigger (SYS_PAGE_SIZES):** This field defines the page size the system will use to map the VFs memory addresses. Software must set the value of the System Page Size to one of the page sizes set in the Supported Page Sizes field. As with Supported Page Sizes, if bit nis Set in System Page Size, the VFs associated with this PF are required to support a page size of 2^(n+12). For example, if bit 1 is Set, the system is using an 8-KB page size. The results are undefined if System Page Size is zero. The results are undefined if more than one bit is set in System Page Size. The results are undefined if a bit is Set in System Page Size that is not Set in Supported Page Sizes. When System Page Size is set, the VF associated with this PF is required to align all BAR resources 20 on a System Page Size boundary. Each VF BARn or VF BARn pair shall be aligned on a System Page Size boundary. Each VF BARn or VF BARn pair defining a non-zero address space shall be sized to consume an integer multiple of System Page Size bytes. All data structures requiring page size alignment within a VF shall be aligned on a System Page Size boundary. VF Enable must be zero when System Page Size is written. The results are undefined if System Page Size is written when VF Enable is Set. Default value is 1h (i.e. 4KB), and that is the only value allowed for this implementation

4.1.80 VF BAR0 Lower DWORD (VF_BAR0_LDW_0_2_0_PCI) — Offset 344h

Lower DWORD of the BAR that defines the base Host Physical Address (HPA) of GTTMMADR for all VFs.

The HPA of the GTTMMADR for Virtual Function n = VF GTTMMADDR (Upper and Lower DWORD) + (n - 1) * (16MB * num Tiles)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 344h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V	**VF GTTMMADDR Lower DWORD (VF_GTTMMADDR_LDW):** VF GTTMMADDR Lower DWORD
23:4	00000h RO	**VF GTTMMADDR Lower DWORD Mask (VF_GTTMMADDR_LDW_MASK):** VF GTTMMADDR Lower DWORD Mask
3	0h RO	**BAR is Prefetchable (PREFETCHABLE):** BAR is Prefetchable
2:1	2h RO	**BAR Type (BAR_TYPE):** A value of 10 indicates a 64 bit BAR.
0	0h RO	**Memory Space Indicator (MEM_SPACE_IND):** A value 0 indicates a memory space.

4.1.81 VF BAR0 Upper DWORD (VF_BAR0_UDW_0_2_0_PCI) — Offset 348h

Upper DWORD of the BAR that defines the base Host Physical Address of the GTTMMADR for all VFs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 348h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**VF GTTMMADDR Upper DWORD (VF_GTTMMADDR_UDW):** VF GTTMMADDR Upper DWORD

4.1.82 VF BAR1 LDW (VF_BAR1_LDW_0_2_0_PCI) — Offset 34Ch

Lower DWORD of the BAR that defines the base Host Physical Address of GMADR for all VFs.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 34Ch	0000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW/V	**VF GMADDR Lower DWORD (VF_GMADDR_LDW):** VF GMADDR Lower DWORD
28:4	0000000h RO	**VF GMADDR Lower DWORD Mask (VF_GMADDR_LDW_MASK):** VF GMADDR Lower DWORD Mask
3	1h RO	**BAR is Prefetchable (PREFETCHABLE):** BAR is Prefetchable
2:1	2h RO	**BAR Type (BAR_TYPE):** A value of 10 indicates a 64 bit BAR.
0	0h RO	**Memory Space Indicator (MEM_SPACE_IND):** A value 0 indicates a memory space.

4.1.83 VF BAR1 UDW (VF_BAR1_UDW_0_2_0_PCI) — Offset 350h

Upper DWORD of the BAR that defines the base Host Physical Address of GMADR for all VFs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 350h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**VF GMADDR Upper DWORD (VF_GMADDR_UDW):** VF GMADDR Upper DWORD

4.1.84 VF Migration State Array Offset (VF_MIGST_OFFSET_0_2_0_PCI) — Offset 35Ch

Defines offset from a PF BAR to the VF Migration State Array. VF Migration not supported in this implementation

Note: Bit definitions are the same as CAPID0_B_0_2_0_PCI, offset 48h.

5 PCI Express* Controller Registers (D1:F0-1)

This chapter documents the registers of the processor PCIe Gen5 Controller devices. The processor contains multiple PCIe controller devices:

- Bus: 0, Device: 1, Function: 0 (PCI0 x16)
- Bus: 0, Device: 1, Function: 1 (PCI1 x8)

Note: Register default values are taken from device PCI0 only. Consult Volume 1 of this document for Device IDs

Table 5-1. Summary of Bus: 0, Device: 1, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Identifiers (ID)	00008086h
4h	2	Device Command (CMD)	0000h
6h	2	Primary Status (PSTS)	0010h
8h	4	Revision ID (RID_CC)	060400F0h
Ch	1	Cache Line Size (CLS)	00h
Dh	1	Primary Latency Timer (PLT)	00h
Eh	1	Header Type (HTYPE)	81h
10h	4	Base Address Register 0 (BAR0)	00000000h
14h	4	Base Address Register 1 (BAR1)	00000000h
18h	4	Bus Numbers (BNUM_SLT)	00000000h
1Ch	2	I/O Base And Limit (IOBL)	0000h
1Eh	2	Secondary Status (SSTS)	0000h
20h	4	Memory Base And Limit (MBL)	00000000h
24h	4	Prefetchable Memory Base And Limit (PMBL)	00010001h
28h	4	Prefetchable Memory Base Upper 32 Bits (PMBU32)	00000000h
2Ch	4	Prefetchable Memory Limit Upper 32 Bits (PMLU32)	00000000h
34h	1	Capabilities List Pointer (CAPP)	40h
3Ch	1	Interrupt Information Byte 0 (INTRB0)	00h
3Dh	1	Interrupt Information Byte 1 (INTRB1)	01h
3Eh	2	Bridge Control (BCTRL)	0000h
40h	2	Capabilities List (CLIST)	8010h
42h	2	PCI Express Capabilities (XCAP)	0042h
44h	4	Device Capabilities (DCAP)	00008001h
48h	2	Device Control (DCTL)	0020h
4Ah	2	Device Status (DSTS)	0010h
4Ch	4	Link Capabilities (LCAP)	01714C10h
50h	2	Link Control (LCTL)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
52h	2	Link Status (LSTS)	1011h
54h	4	Slot Capabilities (SLCAP)	00040060h
58h	2	Slot Control (SLCTL)	0000h
5Ah	2	Slot Status (SLSTS)	0000h
5Ch	2	Root Control (RCTL)	0000h
5Eh	2	Root Capabilities (ROOTCAP)	0000h
60h	4	Root Status (RSTS)	00000000h
64h	4	Device Capabilities 2 (DCAP2)	00B80837h
68h	2	Device Control 2 (DCTL2)	0000h
6Ah	2	Device Status 2 (DSTS2)	0000h
6Ch	4	Link Capabilities 2 (LCAP2)	0180000Eh
70h	2	Link Control 2 (LCTL2)	0001h
72h	2	Link Status 2 (LSTS2)	0000h
74h	4	Slot Capabilities 2 (SLCAP2)	00000000h
78h	2	Slot Control 2 (SLCTL2)	0000h
7Ah	2	Slot Status 2 (SLSTS2)	0000h
80h	2	Message Signaled Interrupt Identifiers (MID)	9005h
82h	2	Message Signaled Interrupt Message (MC)	0080h
84h	4	Message Signaled Interrupt Message Address (MA)	00000000h
88h	4	Message Signaled Interrupt Message Upper Address (MUA)	00000000h
8Ch	2	Message Signaled Interrupt Message Data (MD)	0000h
98h	2	Subsystem Vendor Capability (SVCAP)	A00Dh
9Ch	4	Subsystem Vendor IDs (SVID)	00000000h
A0h	2	Power Management Capability (PMCAP)	0001h
A2h	2	PCI Power Management Capabilities (PMC)	C803h
A4h	4	PCI Power Management Control (PMCS)	00000008h
100h	4	Advanced Error Extended (AECH)	00000000h
104h	4	Uncorrectable Error Status (UES)	00000000h
108h	4	Uncorrectable Error Mask (UEM)	00000000h
10Ch	4	Uncorrectable Error Severity (UEV)	00060010h
110h	4	Correctable Error Status (CES)	00000000h
114h	4	Correctable Error Mask (CEM)	00002000h
118h	4	Advanced Error Capabilities And Control (AECC)	00000000h
11Ch	4	Header Log (HL_DW1)	00000000h
120h	4	Header Log (HL_DW2)	00000000h
124h	4	Header Log (HL_DW3)	00000000h
128h	4	Header Log (HL_DW4)	00000000h
12Ch	4	Root Error Command (REC)	00000000h
130h	4	Root Error Status (RES)	00000000h
134h	4	Error Source Identification (ESID)	00000000h
138h	4	TLP Prefix Log 1 (TLPPL1)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
13Ch	4	TLP Prefix Log 2 (TLPPL2)	00000000h
140h	4	TLP Prefix Log 3 (TLPPL3)	00000000h
144h	4	TLP Prefix Log 4 (TLPPL4)	00000000h
150h	4	PTM Extended Capability Header (PTMECH)	00000000h
154h	4	PTM Capability (PTMCAPR)	00000410h
158h	4	PTM Control (PTMCTLR)	00000000h
200h	4	L1 Sub-States Extended Capability Header (L1SECH)	00000000h
204h	4	L1 Sub-States Capabilities (L1SCAP)	0028281Fh
208h	4	L1 Sub-States Control 1 (L1SCTL1)	00000000h
20Ch	4	L1 Sub-States Control 2 (L1SCTL2)	00000028h
220h	4	ACS Extended Capability Header (ACSECH)	00000000h
224h	2	ACS Capability (ACSCAPR)	001Fh
226h	2	ACS Control (ACSCTLR)	0000h
284h	4	Port VC Capability Register 1 (PVCCR1)	00000000h
288h	4	Port VC Capability 2 (PVCC2)	00000000h
28Ch	2	Port VC Control (PVCC)	0000h
28Eh	2	Port VC Status (PVCS)	0000h
290h	4	Virtual Channel 0 Resource Capability (V0VCRC)	00000000h
294h	4	Virtual Channel 0 Resource Control (V0CTL)	80000001h
29Ah	2	Virtual Channel 0 Resource Status (V0STS)	0000h
29Ch	4	Virtual Channel 1 Resource Capability (V1VCRC)	00000000h
2A0h	4	Virtual Channel 1 Resource Control (V1CTL)	00000000h
2A6h	2	Virtual Channel 1 Resource Status (V1STS)	0000h
A00h	4	DPC Extended Capability Header (DPCECH)	00000000h
A04h	2	DPC Capability (DPCCAPR)	14E0h
A06h	2	DPC Control (DPCCTLR)	0000h
A08h	2	DPC Status (DPCSR)	1F00h
A0Ah	2	DPC Error Source ID (DPCESIDR)	0000h
A0Ch	4	RP PIO Status (RPPIOSR)	00000000h
A10h	4	RP PIO Mask (RPPIOMR)	00070707h
A14h	4	RP PIO Severity (RPPIOVR)	00000000h
A18h	4	RP PIO SysError (RPPIOSER)	00000000h
A1Ch	4	RP PIO Exception (RPPIOER)	00000000h
A20h	4	RP PIO Header Log DW1 (RPPIOHLR_DW1)	00000000h
A24h	4	RP PIO Header Log DW2 (RPPIOHLR_DW2)	00000000h
A28h	4	RP PIO Header Log DW3 (RPPIOHLR_DW3)	00000000h
A2Ch	4	RP PIO Header Log DW4 (RPPIOHLR_DW4)	00000000h
A30h	4	Secondary PCI Express Extended Capability Header (SPEECH)	00000000h
A34h	4	Link Control 3 (LCTL3)	00000000h
A38h	4	Lane Error Status (LES)	00000000h
A3Ch	4	Lane 0 And Lane 1 Equalization Control (L01EC)	7F7F7F7Fh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A40h	4	Lane 2 And Lane 3 Equalization Control (L23EC)	7F7F7F7Fh
A44h	4	Lane 4 And Lane 5 Equalization Control (L45EC)	7F7F7F7Fh
A48h	4	Lane 6 And Lane 7 Equalization Control (L67EC)	7F7F7F7Fh
A4Ch	4	Lane 8 And Lane 9 Equalization Control (L89EC)	7F7F7F7Fh
A50h	4	Lane 10 And Lane 11 Equalization Control (L1011EC)	7F7F7F7Fh
A54h	4	Lane 12 And Lane 13 Equalization Control (L1213EC)	7F7F7F7Fh
A58h	4	Lane 14 And Lane 15 Equalization Control (L1415EC)	7F7F7F7Fh
A90h	4	Data Link Feature Extended Capability Header (DLFECH)	00000000h
A94h	4	Data Link Feature Capabilities (DLFCAP)	80000001h
A98h	4	Data Link Feature Status (DLFSTS)	00000000h
A9Ch	4	Physical Layer 16.0 GT/s Extended Capability Header (PL16GECH)	00000000h
AA0h	4	Physical Layer 16.0 GT/s Capability (PL16CAP)	00000000h
AA4h	4	Physical Layer 16.0 GT/s Control (PL16CTL)	00000000h
AA8h	4	Physical Layer 16.0 GT/s Status (PL16S)	00000000h
AACh	4	Physical Layer 16.0 GT/s Local Data Parity Mismatch Status (PL16LDPMS)	00000000h
AB0h	4	Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status (PL16FRDPMS)	00000000h
AB4h	4	Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status (PL16SRDPMS)	00000000h
AB8h	4	Physical Layer 16.0 GT/s Extra Status (PL16ES)	00000000h
ABCh	2	Physical Layer 16.0 GT/s Lane 01 Equalization Control (PL16L01EC)	FFFFh
ABEh	2	Physical Layer 16.0 GT/s Lane 23 Equalization Control (PL16L23EC)	FFFFh
AC0h	2	Physical Layer 16.0 GT/s Lane 45 Equalization Control (PL16L45EC)	FFFFh
AC2h	2	Physical Layer 16.0 GT/s Lane 67 Equalization Control (PL16L67EC)	FFFFh
AC4h	2	Physical Layer 16.0 GT/s Lane 89 Equalization Control (PL16L89EC)	FFFFh
AC6h	2	Physical Layer 16.0 GT/s Lane 1011 Equalization Control (PL16L1011EC)	FFFFh
AC8h	2	Physical Layer 16.0 GT/s Lane 1213 Equalization Control (PL16L1213EC)	FFFFh
ACAh	2	Physical Layer 16.0 GT/s Lane 1415 Equalization Control (PL16L1415EC)	FFFFh
ADCh	4	Physical Layer 32.0 GT/s Extended Capability Header (G5ECH)	0000002Ah
AE0h	4	Physical Layer 32.0 GT/s Capability (G5CAP)	00000100h
AE4h	4	Physical Layer 32.0 GT/s Control (G5CTL)	00000002h
AE8h	4	Physical Layer 32.0 GT/s Status (G5STS)	00000000h
AECh	4	Receiver Modified TS Data 1 (RCVDMODTSDATA1)	00000000h
AF0h	4	Receiver Modified TS Data 2 (RCVDMODTSDATA2)	00000000h
AF4h	4	Transmitted Modified TS Data 1 (TRNSMODTSDATA1)	00000000h
AF8h	4	Transmitted Modified TS Data 2 (TRNSMODTSDATA2)	00000000h
AFCh	4	32.0 GT/s Lane 0123 Equalization Control (G5LANEEQCTL_0)	FFFFFFFFh
B00h	4	32.0 GT/s Lane 4567 Equalization Control (G5LANEEQCTL_4)	FFFFFFFFh
B04h	4	32.0 GT/s Lane 891011 Equalization Control (G5LANEEQCTL_8)	FFFFFFFFh
B08h	4	32.0 GT/s Lane 12131415 Equalization Control (G5LANEEQCTL_12)	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B0Ch	4	Alternate Protocol Extended Capability Header (APEC)	0000002Bh
B10h	4	Alternate Protocol Capabilities (APCAPR)	00000000h
B14h	4	Alternate Protocol Control (APCTRLR)	000000FFh
B18h	4	Alternate Protocol Data 1 (APD1R)	FFFF0000h
B1Ch	4	Alternate Protocol Data 2 (APD2R)	00000000h
B20h	4	Alternate Protocol Selective Enable Mask (APSEMR)	00000001h
C00h	4	Multicast Extended Capability Header (MCECH)	00000000h
C04h	2	Multicast Extended Capability (MCAPR)	0000h
C06h	2	Multicast Control (MCCTLR)	0000h
C08h	4	Multicast Base Address Register 1 (MCBADRR1)	00000000h
C0Ch	4	Multicast Base Address Register 2 (MCBADRR2)	00000000h
C10h	4	Multicast Receive (MCRR)	00000000h
C18h	4	Multicast Block All (MCBAR)	00000000h
C20h	4	Multicast Block Untranslated (MCBUR)	00000000h
C28h	4	Multicast Overlay BAR 1 (MCOB1)	00000000h
C2Ch	4	Multicast Overlay BAR 2 (MCOB2)	00000000h
C70h	4	VNN Removal Control (VNNREMCTL)	00000001h
C74h	4	VNN Removal Save And Restore Hardware Contexts 1 (VNNRSNRC1)	00000000h
EDCh	4	Physical Layer 16.0 GT/s Margining Extended Capability Header (PL16MECH)	00010027h
EE0h	2	Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status Byte 0 & 1 (PL16MPCPSB01)	0000h
EE2h	2	Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status Byte 2 & 3 (PL16MPCPSB23)	0000h
EE4h	4	Physical Layer 16.0 GT/s Lane0 Margin Control and Status (PL16L0MCS)	00009C38h
EE8h	4	Physical Layer 16.0 GT/s Lane1 Margin Control and Status (PL16L1MCS)	00009C38h
EECh	4	Physical Layer 16.0 GT/s Lane2 Margin Control and Status (PL16L2MCS)	00009C38h
EF0h	4	Physical Layer 16.0 GT/s Lane3 Margin Control and Status (PL16L3MCS)	00009C38h
EF4h	4	Physical Layer 16.0 GT/s Lane4 Margin Control and Status (PL16L4MCS)	00009C38h
EF8h	4	Physical Layer 16.0 GT/s Lane5 Margin Control and Status (PL16L5MCS)	00009C38h
EFCh	4	Physical Layer 16.0 GT/s Lane6 Margin Control and Status (PL16L6MCS)	00009C38h
F00h	4	Physical Layer 16.0 GT/s Lane7 Margin Control and Status (PL16L7MCS)	00009C38h
F04h	4	Physical Layer 16.0 GT/s Lane8 Margin Control and Status (PL16L8MCS)	00009C38h
F08h	4	Physical Layer 16.0 GT/s Lane9 Margin Control and Status (PL16L9MCS)	00009C38h
F0Ch	4	Physical Layer 16.0 GT/s Lane10 Margin Control and Status (PL16L10MCS)	00009C38h
F10h	4	Physical Layer 16.0 GT/s Lane11 Margin Control and Status (PL16L11MCS)	00009C38h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F14h	4	Physical Layer 16.0 GT/s Lane12 Margin Control and Status (PL16L12MCS)	00009C38h
F18h	4	Physical Layer 16.0 GT/s Lane13 Margin Control and Status (PL16L13MCS)	00009C38h
F1Ch	4	Physical Layer 16.0 GT/s Lane14 Margin Control and Status (PL16L14MCS)	00009C38h
F20h	4	Physical Layer 16.0 GT/s Lane15 Margin Control and Status (PL16L15MCS)	00009C38h

5.1 Device Identifiers (ID) — Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Device Identification (DID):** See the Device ID table in the first volume of this document.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel.

5.2 Device Command (CMD) — Offset 4h

Device Command

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** This field is reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** This field is reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** This field is reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** This field is reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** This field is reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone.

5.3 Primary Status (PSTS) — Offset 6h

Primary Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCMD.PERE is not set.
14	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
13	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
12	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
11	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	0h RO	**Primary DEVSEL# Timing Status (PDTS):** This field is reserved per PCI-Express spec
8	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and PCMD.PERE is set.
7	0h RO	**Primary Fast Back to Back Capable (PFBC):** This field is reserved per PCI-Express spec.
6	0h RO	**Reserved**
5	0h RO	**Primary 66 MHz Capable (PC66):** This field is reserved per PCI-Express spec.
4	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
3	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
2:0	0h RO	**Reserved**

5.4 Revision ID (RID_CC) — Offset 8h

Revision ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 8h	060400F0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	04h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a 1 for a Host Bridge, this register reads 00h.
15:8	00h RO/V	**Programming Interface (PI):** PCI-to-PCI bridge.
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

5.5 Cache Line Size (CLS) — Offset Ch

Cache Line Size

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:1, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

5.6 Primary Latency Timer (PLT) — Offset Dh

Primary Latency Timer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:1, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Latency Count (CT):** This field is reserved per PCI-Express spec
2:0	0h RO	**Reserved**

5.7 Header Type (HTYPE) — Offset Eh

Header Type

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:1, F:0] + Eh	81h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-function Device (MFD):** This bit is 1 to indicate a multi-function device.
6:0	01h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a 1 for a Host Bridge, this register reads 00h.

5.8 Base Address Register 0 (BAR0) — Offset 10h

Base Address Register 0

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	00000h RW/V2	**Lower Base Address (LBA):** The base address[31:13] of the BAR.
12:4	0h RO	**Reserved**
3	0h RO	**Prefetchable Memory (P):** This BAR is not prefetchable.
2:1	0h RW/O	**Memory Mapping Type (MMT):** If the BAR is enabled, this field should be written to 10b, else write 00b to this field.
0	0h RO	**Memory Space Indicator (MSI):** Hardwired to 0 to indicate memory space.

5.9 Base Address Register 1 (BAR1) — Offset 14h

Base Address Register 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V2	**Upper Base Address (UBA):** The base address[63:32] of the BAR.

5.10 Bus Numbers (BNUM_SLT) — Offset 18h

Bus Numbers

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is a RW register - else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	00h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	00h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	00h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

5.11 I/O Base And Limit (IOBL) — Offset 1Ch

I/O Base And Limit

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 1Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

5.12 Secondary Status (SSTS) — Offset 1Eh

Secondary Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 1Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
14	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
13	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with Unsupported Request status from the device.
12	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with Completion Abort status from the device.
11	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with Completion Abort status to the device.
10:9	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** This field is reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
8	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
7	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** This field is reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
6	0h RO	**Reserved**
5	0h RO	**Secondary 66 MHz Capable (SC66):** This field is reserved per PCI Express spec
4:0	0h RO	**Reserved**

5.13 Memory Base And Limit (MBL) — Offset 20h

Memory Base And Limit

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved**
15:4	000h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved**

5.14 Prefetchable Memory Base And Limit (PMBL) — Offset 24h

Prefetchable Memory Base And Limit

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 24h	00010001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	000h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

5.15 Prefetchable Memory Base Upper 32 Bits (PMBU32) — Offset 28h

Prefetchable Memory Base Upper 32 Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

5.16 Prefetchable Memory Limit Upper 32 Bits (PMLU32) — Offset 2Ch

Prefetchable Memory Limit Upper 32 Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

5.17 Capabilities List Pointer (CAPP) — Offset 34h

Capabilities List Pointer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:1, F:0] + 34h	40h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Capability Linked List (Default Settings)** Offset | Capability | Next Pointer 40h | PCI Express | 80h 80h | Message Signaled Interrupt (MSI) | 90h 90h | Subsystem Vendor | A0h A0h | PCI Power Management | 00h **Extended PCIe Capability Linked List** Offset | Capability | Next Pointer 100h | Advanced Error Reporting | 000h 140h | Access Control Services | 000h 200h | L1 Sub-states | 000h 220h | Secondary PCI Express Capability | 000h

5.18 Interrupt Information Byte 0 (INTRB0) — Offset 3Ch

Interrupt Information Byte 0

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:1, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

5.19 Interrupt Information Byte 1 (INTRB1) — Offset 3Dh

Interrupt Information Byte 1

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:1, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG.PxIP field: Port Bits[15:12] Bits[11:08] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP ... X 0h STRPFUSECFG.PxIP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.

5.20 Bridge Control (BCTRL) — Offset 3Eh

Bridge Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 3Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
10	0h RO	**Discard Timer Status (DTS):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
9	0h RW/V2	**Secondary Discard Timer (SDT):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
8	0h RW/V2	**Primary Discard Timer (PDT):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
7	0h RO	**Fast Back to Back Enable (FBE):** This field is reserved per PCI-Express spec.
6	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
5	0h RW/V2	**Master Abort Mode (MAM):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
4	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
3	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h - 3BBh and 3C0h - 3DFh, and all aliases of bits 15:10 in any combination of 1's
2	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
1	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
0	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.

5.21 Capabilities List (CLIST) — Offset 40h

Capabilities List

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 40h	8010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

5.22 PCI Express Capabilities (XCAP) — Offset 42h

PCI Express Capabilities

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 42h	0042h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:9	00h RO	**Interrupt Message Number (IMN):** The Root Port does not have multiple MSI interrupt numbers.
8	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
3:0	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 and 3.0 specification which incorporates the Register Expansion ECN.

5.23 Device Capabilities (DCAP) — Offset 44h

Device Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 44h	00008001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported.
25:18	00h RO	**Captured Slot Power Limit Value (CSPV):** Not supported.
17:16	0h RO	**Reserved**
15	1h RO	**Role Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:12	0h RO	**Reserved**
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** This field is reserved for root ports.
8:6	0h RO	**Endpoint L0s Acceptable Latency (E0AL):** This field is reserved for root ports.
5	0h RW/O	**Extended Tag Field Supported (ETFS):** The Root Port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported

Bit Range	Default & Access	Field Name (ID): Description
2:0	1h RW/L	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. **Locked by:** LPCRE.IPCL

5.24 Device Control (DCTL) — Offset 48h

Device Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 48h	0020h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** Must be RW for OS testing. The OS will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
7:5	1h RW	**Max Payload Size (MPS):** The root port supports up to 256B max payload. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

5.25 Device Status (DSTS) — Offset 4Ah

Device Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 4Ah	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
4	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
3	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
2	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed TLP
1	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout
0	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

5.26 Link Capabilities (LCAP) — Offset 4Ch

Link Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 4Ch	01714C10h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	01h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port# Value of PN field 1 01h 2 02h 3 03h : : X 0Xh Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
23	0h RO	**Reserved**
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to 0 to indicate the Root Port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** 0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b: Less than 1 us 001b: 1 us to less than 2 us 010b: 2 us to less than 4 us 011b: 4 us to less than 8 us 100b: 8 us to less than 16 us 101b: 16 us to less than 32 us 110b: 32 us to 64 us 111b: More than 64 us Note: If power management (e.g PLL shutdown) is enabled, BIOS should program this latency to comprehend PLL lock latency.

Bit Range	Default & Access	Field Name (ID): Description
14:12	4h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00b: No ASPM Support 01b: L0s Supported 10b: L1 Supported 11b: L0s and L1 Supported
9:4	01h RO/V	**Maximum Link Width (MLW):** Indicates the maximum link width of the link 0x1: x1 Link Width 0x2: x2 Link Width 0x4: x4 Link Width 0x8: x8 Link Width
3:0	0h RO/V	**Max Link Speed (MLS):** This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This field reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through PCI Express Speed Limit setting or MPC.PCIESD register. This field reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through PCI Express Speed Limit setting or MPC.PCIESD register. Otherwise, this field reports a value of 0011b.

5.27 Link Control (LCTL) — Offset 50h

Link Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 50h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets. Default value of this bit is 0b.
8	0h RO	**Enable Clock Power Management (ECPM):** Not supported on Root Ports.
7	0h RW	**Extended Sync (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the Root Port and device are operating with a distributed common reference clock.
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns 0 when read. Software uses LSTS.LT and LSTS.LTE to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is 1, hardware will always see 00 as an output from this register. BIOS reading this register should always return the correct value.

5.28 Link Status (LSTS) — Offset 52h

Link Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 52h	1011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
14	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
13	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.

Bit Range	Default & Access	Field Name (ID): Description
12	1h RO/V	**Slot Clock Configuration (SCC):** In normal mode, Root Port uses the same reference clock as on the platform and does not generate its own clock. Note: When operating in PCI Express mode, the default of this register bit is dependent on the PCIe Non-Common Clock With SSC Mode Enable Strap. If the strap enables non-common clock with SSC support, this bit shall default to 0. Otherwise, this bit shall default to 1.
11	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
10	0h RO	**Reserved**
9:4	01h RO/V	**Negotiated Link Width (NLW):** Negotiated link width. 0x1: x1 Link Width 0x2: x2 Link Width 0x4: x4 Link Width 0x8: x8 Link Width 0x10: x16 Link Width The value of this register is undefined if the link has not successfully trained.
3:0	1h RO/V	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.

5.29 Slot Capabilities (SLCAP) — Offset 54h

Slot Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 54h	00040060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1h RW/O	**No Command Completed Support (NCCS):** Set to 1 as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RW/O	**Electromechanical Interlock Present (EMIP):** Indicates whether an Electromechanical Interlock is present for this slot. 0b: Indicates that an Electromechanical Interlock is not present. 1b: Indicates that an Electromechanical Interlock is present.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	00h RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RW/O	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RW/O	**Attention Indicator Present (AIP):** Indicates whether an Attention Indicator LED is present for this slot. 0b: Indicates that an Attention Indicator is not present. 1b: Indicates that an Attention Indicator is present.
2	0h RW/O	**MRL Sensor Present (MSP):** Indicates whether an MRL Sensor is present for this slot. 0b: Indicates that an MRL Sensor is not present. 1b: Indicates that an MRL Sensor is present.
1	0h RW/O	**Power Controller Present (PCP):** Indicates whether a Power Controller is implemented for this slot. 0b: Indicates that a Power Controller is not present. 1b: Indicates that a Power Controller is present.
0	0h RW/O	**Attention Button Present (ABP):** Indicates whether an Attention Button is implemented for this slot. 0b: Indicates that an Attention Button is not present. 1b: Indicates that an Attention Button is present.

5.30 Slot Control (SLCTL) — Offset 58h

Slot Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 58h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13	0h RW	**Auto Slot Power Limit Disable (ASPLD):** When set, this bit disables automatic sending of Set_Slot_Power_Limit message when the link transitions from non-DL_Up status to DL_Up status.
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed.
11	0h RW	**Electromechanical Interlock Control (EMIC):** When software writes either a 1 to this bit, The PCIe port pulses the EMIL pin per PCI Express Server/Workstation Module Electromechanical Spec Rev 1.0. Write of 0 has no effect. This bit always returns a 0 when read. If electromechanical lock is not implemented, then either a write of 1 or 0 to this register has no effect.
10	0h RW	**Power Controller Control (PCC):** This bit indicates the current state of the Power applied to the slot of the PCI Express port. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 0: Power On 1: Power Off
9:8	0h RW	**Power Indicator Control (PIC):** If a Power Indicator is implemented, writes to this register set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00: Reserved. 01: On 10: Blink (The PCIe cluster drives 1.5 Hz square wave for Chassis mounted LEDs in the case of legacy card form factor for PCI-Express devices) 11: Off When this register is written, the event is signaled via the virtual pins of the switch over the SMBus port. The switch does not generated the Power_Indicator_On/Off/Blink messages on PCI Express when this field is written to by software.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**Attention Indicator Control (AIC):** If an Attention Indicator is implemented, writes to this register sets the Attention Indicator to the written state. Reads of this field reflect the value from the latest write, even if the corresponding hot-plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00: Reserved. 01: On 10: Blink (The switch drives 1.5 Hz square wave) 11: Off When this register is written, the event is signaled via the virtual pins of the switch over the SMBus port.
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RW	**Command Completed Interrupt Enable (CCE):** This field enables the generation of Hot-plug interrupts when a command is completed by the Hot-plug controller connected to the PCI-Express port. 0: Disables hot-plug interrupts on a command completion by a hot-plug Controller 1: Enables hot-plug interrupts on a command completion by a hot-plug Controller
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RW	**MRL Sensor Changed Enable (MSE):** This bit enables the generation of hot-plug interrupts or wake messages via a MRL Sensor changed event. 0: Disables generation of hot-plug interrupts or wake messages when an MRL Sensor changed event happens. 1: Enables generation of hot-plug interrupts or wake messages when an MRL Sensor changed event happens.
1	0h RW	**Power Fault Detected Enable (PFE):** This bit enables the generation of hot-plug interrupts or wake messages via a power fault event. 0: Disables generation of hot-plug interrupts or wake messages when a power fault event happens. 1: Enables generation of hot-plug interrupts or wake messages when a power fault event happens.
0	0h RW	**Attention Button Pressed Enable (ABE):** This bit enables the generation of hot-plug interrupts or wake messages via an attention button pressed event. 0: Disables generation of hot-plug interrupts or wake messages when the attention button is pressed. 1: Enables generation of hot-plug interrupts or wake messages when the attention button is pressed.

5.31 Slot Status (SLSTS) — Offset 5Ah

Slot Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 5Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
7	0h RO/V	**Electromechanical Interlock Status (EMIS):** A read to this register returns the current state of the Electromechanical Interlock (the EMILS pin) which has the defined encodings as: 0: Electromechanical Interlock Disengaged 1: Electromechanical Interlock Engaged
6	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected (1) or empty (0). If XCAP.SI is cleared, this bit is a 1.
5	0h RO/V	**MRL Sensor State (MS):** This bit reports the status of an MRL sensor if it is implemented. 0: MRL Closed 1: MRL Open If Hotplug is implemented through VPP, the correct polarity of the external MRL sensor in the motherboard should be translated to map to the encodings as defined in this register field.
4	0h RW/1C/V	**Command Completed (CC):** This bit is set when the hot-plug controller completes an issued command and is ready to accept a new command. It is subsequently cleared by software after the field has been read and processed. If Command Completed notification is supported, then the No Command Completed Support bit in the Slot Capabilities register should be 0.
3	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the PD bit changes state.
2	0h RW/1C/V	**MRL Sensor Changed (MSC):** This bit is set when an MRL Sensor Changed event is detected. It is subsequently cleared by software after the field has been read and processed. On-board logic per slot must set the VPP signal corresponding to this bit inactive if the FF/system does not support out-of-band presence detect.
1	0h RW/1C/V	**Power Fault Detected (PFD):** This bit is set when a power fault event is detected by the power controller. It is subsequently cleared by software after the field has been read and processed. On-board logic per slot must set the VPP signal corresponding to this bit inactive if the FF/system does not support out-of-band presence detect.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1C/V	**Attention Button Pressed (ABP):** This bit is set when the Attention Button is pressed. It is subsequently cleared by software after the field has been read and processed. On-board logic per slot must set the VPP signal corresponding to this bit inactive if the FF/system does not support out-of-band presence detect. Design should implement this as an edge detection logic in the chipset/platform to recognize a 0 -> 1 transition as an ABP event. Due to the long time frames for human interaction, software could potentially have serviced and cleared this event while the operator is pressing the Attention Button. For instance, if the user presses the Attention Button that lasts for 2ms and the VPP sampling rate is, say 100us and if the Interrupt Service routine (ISR) processes and clears the ABP in 100us, there could be up to 10 (i.e 2000/(100+100)) different interrupts for the same event. Hardware must only generate 1 interrupt for every ABP event by treating it as edge based rather than level based event.

5.32 Root Control (RCTL) — Offset 5Ch

Root Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 5Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	**Reserved**
4	0h RW	**CRS Software Visibility Enable (CRSSVE):** This bit, when set, enables the Root Port to return Configuration Retry Status (CRS) Completion status to software. 1: Enable software to received a CRS status. This allows software to make the decision to re-issue the configuration request or move on and re-issue the request at a later time. 0: Disable software from receiving a CRS response. The PCIe will wait and re-issue the configuration request until it receives a response other than CRS without notifying software.
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

5.33 Root Capabilities (ROOTCAP) — Offset 5Eh

Root Capabilities

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 5Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RW/O	**CRS Software Visibility (CRSSV):** This bit, when set, indicates that the Root Port is capable of returning Configuration Retry Status (CRS) on completions to software.

5.34 Root Status (RSTS) — Offset 60h

Root Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requester ID will be updated, and this bit will be cleared. Root Ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requester ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0000h RO/V	**PME Requester ID (RID):** Indicates the PCI requester ID of the last PME requester. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

5.35 Device Capabilities 2 (DCAP2) — Offset 64h

Device Capabilities 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 64h	00B80837h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	2h RW/O	**Max End-End TLP Prefixes (MEETLPP):** Indicates the maximum number of End-End TLP Prefixes supported by this Function. TLPs received by this Function that contain more End-End TLP Prefixes than are supported must be handled as Malformed TLPs. Values are: 01b: 1 End-End TLP Prefix 10b: 2 End-End TLP Prefixes 11b: 3 End-End TLP Prefixes 00b: 4 End-End TLP Prefixes If End-End TLP Prefix Supported is Clear, this field is RsvdP.
21	1h RW/O	**End-End TLP Prefix Supported (EETLPPS):** Indicates whether End-End TLP Prefix support is offered by a Function. Values are: 0b: No Support. 1b: Support is provided to receive TLPs containing End-End TLP Prefixes.
20	1h RW/O	**Extended Fmt Field Supported (EFFS):** If Set, the Function supports the 3 bit definition of the Fmt field. If Clear, the Function supports a 2 bit definition of the Fmt field. Must be Set for Functions that support End-End TLP Prefixes. All Functions in an Upstream Port must have the same value for this bit. Each Downstream Port of a component may have a different value for this bit. It is strongly recommended that Functions support the 3 bit definition of the Fmt field.
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b: OBFF is not supported. 01b: OBFF is supported using Message signaling only. 10b: OBFF is supported using WAKE# signaling only. 11b: OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. Note: OBFF is not supported. BIOS should program this field to 00b.
17	0h RW/O	**10-Bit Tag Requester Supported (PX10BTRS):** If this bit is Set, the Function supports 10-Bit Tag Requester capability - otherwise, the Function does not. This bit must not be Set if the 10-Bit Tag Completer Supported bit is Clear.
16	0h RW/O	**10-Bit Tag Completer Supported (PX10BTCS):** If this bit is Set, the Function supports 10-Bit Tag Completer capability - otherwise, the Function does not.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a 1 or a 0 to enable/disable the root port from declaring support for the LTR capability.
10	0h RO	**Reserved**
9	0h RW/O	**CAS Completer 128-bit Supported (AC128BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability.
8	0h RW/O	**AtomicOp Completer 64-bit Supported (AC64BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability
7	0h RW/O	**AtomicOp Completer 32-bit Supported (AC32BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability
6	0h RW/O	**Atomic Routing Supported (ARS):** This bit must be set to 1b if the Port supports this optional capability
5	1h RO	**ARI Forwarding Supported (AFS):** Applicable only to Switch Downstream Ports and Root Ports - must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this bit 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A & B 0110b Ranges B & C 0111b Ranges A, B & C <-- This is what Root Port supports 1110b Ranges B, C & D 1111b Ranges A, B, C & D All other values are reserved.

5.36 Device Control 2 (DCTL2) — Offset 68h

Device Control 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 68h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**End-End TLP Prefix Blocking (EETLPPB):** Controls whether the routing function is permitted to forward TLPs containing an End-End TLP Prefix. Values are: 0b: Forwarding Enabled Function is permitted to send TLPs with End-End TLP Prefixes. 1b: Forwarding Blocked Function is not permitted to send TLPs with End-End TLP Prefixes. This bit affects TLPs that exit the Switch / Root Complex using the associated Port. It does not affect TLPs forwarded internally within the Switch / Root Complex. It does not affect TLPs that enter through the associated Port, that originate in the associated Port or originate in a Root Complex Integrated Device integrated with the associated Port. Asdescribed in Section 2.2.10.2, blocked TLPs are reported by the TLP Prefix Blocked Error.
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** Optimized Buffer Flush/Fill Enable (OBFFEN): 00b: Disable OBFF mechanism. 01b: Enable OBFF mechanism using Message signaling (Variation A). 10b: Enable OBFF mechanism using Message signaling (Variation B). 11b: Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12	0h RW/V2	**10-Bit Tag Requester Enable (PX10BTRE):** This bit, in combination with the Extended Tag Field Enable bit in the Device Control register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is Set, the Requester is permitted to use 10-Bit Tags. Software should not change the value of this bit while the Function has outstanding Non-Posted Requests - otherwise, the result is undefined. Functions that do not implement 10-Bit Tag Requester capability must hardwire this bit to 0b.
11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**AtomicOp Egress Blocking (AEB):** Applicable and mandatory for Switch Upstream Ports, Switch Downstream Ports, and Root Ports that implement AtomicOp routing capability - otherwise must be hardwired to 0b. When this bit is Set, AtomicOp Requests that target going out this Egress Port must be blocked.
6	0h RW	**AtomicOp Requester Enable (ARE):** Applicable only to Endpoints and Root Ports - must be hardwired to 0b for other Function types. The Function is allowed to initiate AtomicOp Requests only if this bit and the Bus Master Enable bit in the Command register are both Set. This bit is required to be RW if the Endpoint or Root Port is capable of initiating AtomicOp Requests, but otherwise is permitted to be hardwired to 0b. This bit does not serve as a capability bit. This bit is permitted to be RW even if no AtomicOp Requester capabilities are supported by the Endpoint or Root Port.
5	0h RW	**ARI Forwarding Enable (AFE):** When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The Root Port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50us to 100us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

5.37 Device Status 2 (DSTS2) — Offset 6Ah

Device Status 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 6Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

5.38 Link Capabilities 2 (LCAP2) — Offset 6Ch

Link Capabilities 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 6Ch	0180000Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RW/O	**Two Retimers Presence Detect Supported (TRPDS):** When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit must be set to 1b in a Downstream Port when the Supported Link Speeds Vector of the Link Capabilities 2 register indicates support for a Link speed of 16.0 GT/s or higher. It is permitted to be set to 1b regardless of the supported Link speeds, and in Upstream Ports, if the Retimer Presence Detect Supported bit is also set to 1b.
23	1h RW/O	**Retimer Presence Detect Supported (RPDS):** When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit must be set to 1b in a Downstream Port when the Supported Link Speeds Vector of the Link Capabilities 2 register indicates support for a Link speed of 16.0 GT/s or higher. It is permitted to be set to 1b regardless of the supported Link speeds and in Upstream Ports.
22:16	00h RW/O	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bits 6:4 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector. This register is Read-Only if LPCR.SRL field is set. **Locked by:** LPCR.SRL
15:9	00h RW/O	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0GT/s Bits 6:4 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector. This register is Read-Only if LPCR.SRL field is set. **Locked by:** LPCR.SRL
8	0h RO	**Crosslink Supported (CS):** No support for Crosslink.

Bit Range	Default & Access	Field Name (ID): Description
7:1	07h RO/V	**Supported Link Speeds Vector (SLSV):** This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported - otherwise, the Link speed is not supported. Bit definitions within this field for PCI Express are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bit 3: 16.0 GT/s. Bit 4: 32.0 GT/s. Bits 5-6: Reserved.
0	0h RO	**Reserved**

5.39 Link Control 2 (LCTL2) — Offset 70h

Link Control 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 70h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is operating at 2.5 GT/s, the setting of this field has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Reserved**
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
3:0	1h RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

5.40 Link Status 2 (LSTS2) — Offset 72h

Link Status 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 72h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO/V/P	**Two Retimers Presence Detected (PX2RPD):** When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation. The default value of this bit is 0b. This bit is required for Ports that have the Two Retimers Presence Detect Supported bit of the Link Capabilities 2 register set to 1b. Ports that have the Two Retimers Presence Detect Supported bit set to 0b are permitted to hardwire this bit to 0b.
6	0h RO/V/P	**Retimer Presence Detected (RPD):** When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation. The default value of this bit is 0b. This bit is required for Ports that have the Retimer Presence Detect Supported bit Set. Ports that have the Retimer Presence Detect Supported bit of the Link Capabilities 2 register set to 0b are permitted to hardwire this bit to 0b.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C/V/P	**Link Equalization Request (LER):** This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link.
4	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** When set to 1, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
3	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** When set to 1, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
2	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** When set to 1, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
1	0h RO/V/P	**Equalization Complete (EQC):** When set to 1, this bit indicates that the Transmitter Equalization procedure at the 8.0GT/s data rate has completed.
0	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

5.41 Slot Capabilities 2 (SLCAP2) — Offset 74h

Slot Capabilities 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

5.42 Slot Control 2 (SLCTL2) — Offset 78h

Slot Control 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

5.43 Slot Status 2 (SLSTS2) — Offset 7Ah

Slot Status 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

5.44 Message Signaled Interrupt Identifiers (MID) — Offset 80h

Message Signaled Interrupt Identifiers

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 80h	9005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

5.45 Message Signaled Interrupt Message (MC) — Offset 82h

Message Signaled Interrupt Message

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 82h	0080h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	1h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
3:1	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

5.46 Message Signaled Interrupt Message Address (MA) — Offset 84h

Message Signaled Interrupt Message Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	**Reserved**

5.47 Message Signaled Interrupt Message Upper Address (MUA) — Offset 88h

Message Signaled Interrupt Message Upper Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Address (UADDR):** System-specified message upper address. This register is implemented only if the Function supports a 64-bit message address (bit 7 in Message Control register Set). This register is required for PCI Express Endpoints and is optional for other Function types. If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (Address[63:32]). If the contents of this register are zero, the Function uses the 32 bit address specified by the Message Address register

5.48 Message Signaled Interrupt Message Data (MD) — Offset 8Ch

Message Signaled Interrupt Message Data

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 8Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

5.49 Subsystem Vendor Capability (SVCAP) — Offset 98h

Subsystem Vendor Capability

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 98h	A00Dh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

5.50 Subsystem Vendor IDs (SVID) — Offset 9Ch

Subsystem Vendor IDs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

5.51 Power Management Capability (PMCAP) — Offset A0h

Power Management Capability

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + A0h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	01h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

5.52 PCI Power Management Capabilities (PMC) — Offset A2h

PCI Power Management Capabilities

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + A2h	C803h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:11	19h RO	**PMES:** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Windows operating systems to enable PME# in devices connected behind this root port.
10	0h RO	**D2S:** The D2 state is not supported.
9	0h RO	**D1S:** The D1 state is not supported.
8:6	0h RO	**AC:** Reports 375mA maximum suspend well current required when in the D3COLD state.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification.

5.53 PCI Power Management Control (PMCS) — Offset A4h

PCI Power Management Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A4h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DTA:** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** This field is reserved per PCI Express specification

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**B2/B3 Support (B23S):** This field is reserved per PCI Express specification.
21:16	0h RO	**Reserved**
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Windows operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved**
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00: D0 state 11: D3HOT state When in the D3HOT state, the controllers configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a 10 or 01 to these bits, the write will be ignored.

5.54 Advanced Error Extended (AECH) — Offset 100h

Advanced Error Extended

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

5.55 Uncorrectable Error Status (UES) — Offset 104h

Uncorrectable Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/1C/V/P	**Poisoned TLP Egress Blocked Status (PTLPEBS):** Indicates that poisoned TLP Egress Blocked error has occurred. Note: This bit can only be set if DPCCAPR.PTLPEBS = 1 and DPCCTLR.PTLPEBE = 1.
25	0h RW/1C/V/P	**TLP Prefix Blocked Error Status (TLPPBES):** When set indicates that TLP Prefix Blocked Error has been detected.
24	0h RW/1C/V/P	**AtomicOp Egress Blocked Status (AEBS):** AtomicOp Egress Blocked Status
23	0h RW/1C/V/P	**MC Blocked TLP Status (MCBTLPS):** Indicates that a TLP that fails MC_Blocked_TLP error check has been received.
22	0h RW/1C/V/P	**Uncorrectable Internal Error Status (UIES):** Indicate Uncorrectable Internal Error Occurs.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Indicates an ACS Violation is logged.
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RW/1C/V/P	**ECRC Error Status (EE):** ECRC error has occurred.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RW/1C/V/P	**Flow Control Protocol Error Status (FCPE):** Indicates a Flow Control Protocol Error has occurred.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved**
5	0h RW/1C/V/P	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Status (TE):** Not supported.

5.56 Uncorrectable Error Mask (UEM) — Offset 108h

Uncorrectable Error Mask

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Mask (PTLPEBM):** Mask for Poisoned TLP Egress Blocked error.
25	0h RW/P	**TLP Prefix Blocked Error Mask (TLPPBEM):** Mask for TLP Prefix Blocked Error.
24	0h RW/P	**AtomicOp Egress Blocked Mask (AEBM):** Mask for AtomicOp Egress Blocked
23	0h RW/P	**MC Blocked TLP Mask (MCBTLPM):** Mask bit for MC Blocked TLP error.
22	0h RW/P	**Uncorrectable Internal Error Mask (UIEM):** Mask for uncorrectable errors.
21	0h RW/P	**ACS Violation Mask (AVM):** Mask for ACS Violation errors.
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RW/P	**ECRC Error Mask (EE):** Mask for ECRC errors.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RW/P	**Flow Control Protocol Error Mask (FCPE):** Mask for Flow Control Protocol Error.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved**
5	0h RW/P	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Mask (TE):** Not supported.

5.57 Uncorrectable Error Severity (UEV) — Offset 10Ch

Uncorrectable Error Severity

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 10Ch	00060010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Severity (PTLPEBS):** Severity for Poisoned TLP Egress Blocked error.
25	0h RW/P	**TLP Prefix Blocked Error Severity (TLPPBES):** Severity for TLP Prefix Blocked errors.
24	0h RW/P	**AtomicOp Egress Blocked Severity (AEBS):** AtomicOp Egress Blocked Severity
23	0h RW/P	**MC Blocked TLP Severity (MCBTLPS):** Severity for MC Blocked TLP Error.
22	0h RW/P	**Uncorrectable Internal Error Severity (UIES):** Severity for Uncorrectable Internal Error.
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS Violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RW/P	**ECRC Error Severity (EE):** ECRC error severity.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/P	**Flow Control Protocol Error Severity (FCPE):** Severity for Flow Control Protocol Error.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved**
5	0h RW/P	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Severity (TE):** TE not supported.

5.58 Correctable Error Status (CES) — Offset 110h

Correctable Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V/P	**Header Log Overflow Status (HLOS):** When set, indicate that Header Log Overflow Status had occurred.
14	0h RW/1C/V/P	**Corrected Internal Error Status (CIES):** When set, indicate that Correctable Internal Error Status had occurred.
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

5.59 Correctable Error Mask (CEM) — Offset 114h

Correctable Error Mask

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 114h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/P	**Header Log Overflow Mask (HLOM):** Mask for Header Log Overflow.
14	0h RW/P	**Corrected Internal Error Mask (CIEM):** Masks for Correctable Internal Error.
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved**
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved**
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

5.60 Advanced Error Capabilities And Control (AECC) — Offset 118h

Advanced Error Capabilities And Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**Completion Timeout Prefix/Header Log Capable (CTPHLC):** If set, this bit indicates that port records the prefix/header of Request TLPs that experience a Completion Timeout error. Note: BIOS should program this bit before enable the Completion Timeout mechanism.
11	0h RO/V/P	**TLP Prefix Log Present (TLPPLP):** If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.
10:9	0h RO	**Reserved**
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	00h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

5.61 Header Log (HL_DW1) — Offset 11Ch

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 11Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st DWORD of TLP (DW1):** Byte0 && Byte1 && Byte2 && Byte3

5.62 Header Log (HL_DW2) — Offset 120h

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd DWORD of TLP (DW2):** Byte4 && Byte5 && Byte6 && Byte7

5.63 Header Log (HL_DW3) — Offset 124h

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd DWORD of TLP (DW3):** Byte8 && Byte9 && Byte10 && Byte11

5.64 Header Log (HL_DW4) — Offset 128h

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th DWORD of TLP (DW4):** Byte12 && Byte13 && Byte14 && Byte15

5.65 Root Error Command (REC) — Offset 12Ch

Root Error Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 12Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

5.66 Root Error Status (RES) — Offset 130h

Root Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved
26:7	0h RO	**Reserved**
6	0h RW/1C/V/P	**Fatal Error Messages Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

5.67 Error Source Identification (ESID) — Offset 134h

Error Source Identification

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requester ID if an internally detected error.
15:0	0000h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error.

5.68 TLP Prefix Log 1 (TLPPL1) — Offset 138h

TLP Prefix Log 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 138h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st dWord of TLP Prefix (DW1):** TLP Prefix DW logging.

5.69 TLP Prefix Log 2 (TLPPL2) — Offset 13Ch

TLP Prefix Log 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 13Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd dWord of TLP Prefix (DW2):** TLP Prefix DW logging.

5.70 TLP Prefix Log 3 (TLPPL3) — Offset 140h

TLP Prefix Log 3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd dWord of TLP Prefix (DW3):** TLP Prefix DW logging.

5.71 TLP Prefix Log 4 (TLPPL4) — Offset 144h

TLP Prefix Log 4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th dWord of TLP Prefix (DW4):** TLP Prefix DW logging.

5.72 PTM Extended Capability Header (PTMECH) — Offset 150h

PTM Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

5.73 PTM Capability (PTMCAPR) — Offset 154h

PTM Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 154h	00000410h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	04h RW/O	**Local Clock Granularity (LCG):** 0000 0000b: Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Source's local clock in ns. 1111 1111b: Indicates the period of this Time Source's local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:5	0h RO	**Reserved**
4	1h RW/O	**PTM Propagation Delay Adaptation Capable (PTMPDAC):** When Set, this field indicates the Port supports the PTM Propagation Delay Adaptation Capability.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Reserved**
2	0h RW/O	**PTM Root Capable (PTMRC):** Root Ports must set this bit to 1b.
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Role is not supported by Root Port.

5.74 PTM Control (PTMCTLR) — Offset 158h

PTM Control Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Effective Granularity (EG):** Root Port does not support PTM Requester role.
7:3	0h RO	**Reserved**
2	0h RW	**PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB):** If PTM Propagation Delay Adaptation Capable is Set, then this bit when Set selects interpretation B of the Propagation Delay[31:0] field in the PTM ResponseD Message For a Switch, if a specific Port is permanently attached such that this control is not required, it is permitted for that Port for this bit to be RsvdP. Default value is 0b.
1	0h RW	**Root Select (RS):** When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register.

5.75 L1 Sub-States Extended Capability Header (L1SECH) — Offset 200h

L1 Sub-States Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh.

5.76 L1 Sub-States Capabilities (L1SCAP) — Offset 204h

L1 Sub-States Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 204h	0028281Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:19	05h RW/O	**Port Tpower_on Value (PTV):** Along with the Port Tpower_on Scale field in the L1 Sub-states Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved**
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Sub-states Capabilities register. 00b: 2 us 01b: 10 us 10b: 100 us 11b: Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7	0h RO	**Reserved**
6	0h RW/1C/V	**CLKREQ# Acceleration Interrupt Status (L1SSEIS):** For a Downstream Port that has both the CLKREQ# Acceleration Supported and CLKREQ# Acceleration Interrupt Enable bits Set, when set this bit indicates that the Port has completed the CLKREQ# Acceleration Link Activation process, and that the Link has reached L0. Software must then clear this bit by writing a 1b to this bit. Must be hardwired to 0b for Upstream Ports. Default value is 0b.
5	0h RW/O	**CLKREQ# Acceleration Supported (L1SSES):** When set this bit indicates that this Port supports CLKREQ# acceleration.
4	1h RW/O	**L1 PM Sub-states Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Sub-states. For compatibility with possible future extensions, software must not enable L1 PM Sub-states unless this bit is set. This RWO field must be programmed prior to enabling ASPM. Required for both Upstream and Downstream Ports.
3	1h RW/O	**ASPM L1.1 Supported (AL11S):** When set, this bit indicates ASPM L1.SNOOZ is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM.
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that PCI-PM L1.SNOOZ is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM.
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that PCI-PM L1.OFF is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM.

5.77 L1 Sub-States Control 1 (L1SCTL1) — Offset 208h

L1 Sub-States Control 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency Scale Value (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular Root Port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF.
28:26	0h RO	**Reserved**
25:16	000h RW	**L1.2 LTR Threshold Latency Value (L12LTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular Root Port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF.

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time(in us) the Root Port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF.
7:6	0h RO	**Reserved**
5	0h RW	**L1 Substate Exit Control (L1SSEC):** L1.Substate the Port must initiate the CLKREQ# Acceleration Link Activation process. Apart from that, once the Link reaches L0, the Port must continue to attempt to maintain the Link in L0 for as long as this bit remains Set. However if the Upstream Port request for L1 entry, the Downstream Port will proceed to allow L1 entry but will not re-enter L1.1 or L1.2.
4	0h RW	**CLKREQ# Acceleration Interrupt Enable (L1SSEIE):** When set this bit enables the generation of an interrupt to indicate the completion of the CLKREQ# acceleration Link Activation process
3	0h RW	**ASPM L1.1 Enable (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ sub-states are enabled. Required for both upstream and downstream ports. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled. Required for both upstream and downstream ports. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
1	0h RW	**PCI-PM L1.1 Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.

5.78 L1 Sub-States Control 2 (L1SCTL2) — Offset 20Ch

L1 Sub-States Control 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 20Ch	00000028h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	05h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserted in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF.
2	0h RO	**Reserved**
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. 00b: 2 us 01b: 10 us 10b: 100us 11b: Reserved. Required for all Ports that support L1.OFF.

5.79 ACS Extended Capability Header (ACSECH) — Offset 220h

ACS Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Capability ID (CID):** For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

5.80 ACS Capability (ACSCAPR) — Offset 224h

ACS Capability Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 224h	001Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control is not supported.
4	1h RW/O	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding.
3	1h RW/O	**ACS P2P Completion Redirect (C):** Required for all Functions that support ACS P2P Request Redirect - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** Required for Root Ports that support peer-to-peer traffic with other Root Ports - required for Switch Downstream Ports - required for multi-function device Functions that support peer-to-peer traffic with other Functions - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** Required for Root Ports and Switch Downstream Ports - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** Required for Root Ports and Switch Downstream Ports - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

5.81 ACS Control (ACSCTLR) — Offset 226h

ACS Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 226h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	0h RO	**ACS Direct Translated P2P Enable (TE):** ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (EE):** ACS P2P Egress Control is not supported.
4	0h RW	**ACS Upstream Forwarding Enable (UE):** ACS Upstream Forwarding.
3	0h RW	**ACS P2P Completion Redirect Enable (CE):** Determines when the component redirects peer-to-peer Completions upstream - applicable only to Read Completions whose Relaxed Ordering Attribute is clear. Requests are never affected by ACS P2P Completion Redirect. Default value of this field is 0b.
2	0h RW	**ACS P2P Request Redirect Enable (RE):** Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect. Default value of this field is 0b.
1	0h RW	**ACS Translation Blocking Enable (BE):** When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking. Default value of this field is 0b.
0	0h RW	**ACS Source Validation Enable (VE):** When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation. Default value of this field is 0b.

5.82 Port VC Capability Register 1 (PVCCR1) — Offset 284h

Port VC Capability Register 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 284h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RO	**Function Arbitration Table Entry Size (FARES):** Indicates the size (in bits) of Function Arbitration table entry in the device. Defined encodings are: 00b Size of Function Arbitration table entry is 1 bit 01b Size of Function Arbitration table entry is 2 bits 10b Size of Function Arbitration table entry is 4 bits 11b Size of Function Arbitration table entry is 8 bits
9:8	0h RO	**Reference Clock (RC):** Indicates the reference clock for Virtual Channels that support time-based WRR Function Arbitration. Defined encodings are: 00b 100 ns reference clock 01b 11b Reserved
7	0h RO	**Reserved**
6:4	0h RO	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict priority VC Arbitration. The minimum value of this field is 000b and the maximum value is Extended VC Count.
3	0h RO	**Reserved**
2:0	0h RW/O	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The minimum value of this field is zero (for devices that only support the default VC). The maximum value is seven.

5.83 Port VC Capability 2 (PVCC2) — Offset 288h

Port VC Capability 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 288h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.
23:8	0h RO	**Reserved**
7:0	00h RO	**VC Arbitration Capability (VCAC):** Indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid for all devices that report a Low Priority Extended VC Count greater than 0. Each bit location within this field corresponds to a VC Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the device can be configured to provide different VC arbitration services. Defined bit positions are: Bit 0: Hardware fixed arbitration scheme (e.g., Round Robin). Bit 1: Weighted Round Robin (WRR) arbitration with 32 phases. Bit 2: WRR arbitration with 64 phases. Bit 3: WRR arbitration with 128 phases. Bits 4-7: Reserved.

5.84 Port VC Control (PVCC) — Offset 28Ch

Port VC Control.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 28Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RW	**VC Arbitration Select (VCAS):** Used by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability register 2. The permissible values of this field are numbers corresponding to one of the asserted bits in the VC Arbitration Capability field. This field cannot be modified when more than one VC in the LPVC group is enabled.
0	0h WO	**Load VC Arbitration Table (LVCAT):** Used by software to update the VC Arbitration Table. This bit is valid when the selected VC Arbitration uses the VC Arbitration Table. Software Sets this bit to request hardware to apply new values programmed into VC Arbitration Table - Clearing this bit has no effect. Software checks the VC Arbitration Table Status bit to confirm that new values stored in the VC Arbitration Table are latched by the VC arbitration logic. This bit always returns 0b when read.

5.85 Port VC Status (PVCS) — Offset 28Eh

Port VC Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 28Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VC Arbitration Table Status (VCATS):** Indicates the coherency status of the VC Arbitration Table. This bit is valid when the selected VC uses the VC Arbitration Table. This bit is Set by hardware when any entry of the VC Arbitration Table is written by software. This bit is Cleared by hardware when hardware finishes loading values stored in the VC Arbitration Table after software sets the Load VC Arbitration Table bit in the Port VC Control register. Default value of this bit is 0b.

5.86 Virtual Channel 0 Resource Capability (V0VCRC) — Offset 290h

Virtual Channel 0 Resource Capability

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 290h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Function Arbitration Table Offset (FATO):** Indicates the location of the Function Arbitration Table associated with the VC resource. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.
23	0h RO	**Reserved**
22:16	00h RW/O	**Maximum Time Slots (MTS):** Indicates the maximum number of time slots (minus 1) that the VC resource is capable of supporting when it is configured for time-based WRR Function Arbitration. For example, a value of 000 0000b in this field indicates the supported maximum number of time slots is 1 and a value of 111 1111b indicates the supported maximum number of time slots is 128. This field is valid only when the Function Arbitration Capability indicates that the VC resource supports time-based WRR Function Arbitration.
15:8	0h RO	**Reserved**
7:0	00h RO	**Function Arbitration Capability (FAC):** Indicates types of Function Arbitration supported by the VC resource. Each bit location within this field corresponds to a Function Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Function Arbitration Select field. Defined bit positions are: Bit 0: Non-configurable hardware-fixed arbitration scheme (e.g. Round Robin). Bit 1: Weighted Round Robin (WRR) arbitration with 32 phases. Bit 2: WRR arbitration with 64 phases. Bit 3: WRR arbitration with 128 phases. Bit 4: Time-based WRR with 128 phases. Bit 5: WRR arbitration with 256 phases. Bits 6-7: Reserved.

5.87 Virtual Channel 0 Resource Control (V0CTL) — Offset 294h

Virtual Channel 0 Resource Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 294h	80000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** When Set, this bit enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. Default value of this bit is 1b for the first VC resource and 0b for other VC resource(s). Notes: 1. This bit is hardwired to 1b for the default VC (VC0), i.e., writing to this field has no effect for VC0. 2. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Set in both components on a Link. 3. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Cleared in both components on a Link. 4. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 5. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel.
30:27	0h RO	**Reserved**
26:24	0h RO	**Virtual Channel Identifier (ID):** This field assigns a VC ID to the VC resource. This field cannot be modified when the VC is already enabled. Note: For the first VC resource (default VC), this field is a read-only field that must be hardwired to 000b.
23:20	0h RO	**Reserved**
19:17	0h RW	**Function Arbitration Select (FAS):** This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.
16	0h RW	**Load Function Arbitration Table (LFAT):** When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table - clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. **Locked by:** LPCR.SRL
9:8	0h RO	**Reserved**
7:1	00h RW	**Transaction Class / Virtual Channel Map (TVM):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.
0	1h RO	**Transaction Class / Virtual Channel Map TC0 (TVMT0):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.

5.88 Virtual Channel 0 Resource Status (V0STS) — Offset 29Ah

Virtual Channel 0 Resource Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + 29Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO/V	**VC Negotiation Pending (NP):** This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. When this bit is Set by hardware, it indicates that the VC resource is still in the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete. For a nondefault Virtual Channel, software may use this bit when enabling or disabling the VC. For the default VC, this bit indicates the status of the process of Flow Control initialization. Before using a Virtual Channel, software must check whether the VC Negotiation Pending bits for that Virtual Channel are Clear in both components on a Link.
0	0h RO	**Function Arbitration Table Status (FATS):** This bit indicates the coherency status of the Function Arbitration Table associated with the VC resource. This bit is valid only when the Function Arbitration Table is used by the selected Function Arbitration for the VC resource. This bit is Set by hardware when any entry of the Function Arbitration Table is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the Function Arbitration Table after software sets the Load FunctionArbitration Table bit. Default value of this bit is 0b

5.89 Virtual Channel 1 Resource Capability (V1VCRC) — Offset 29Ch

Virtual Channel 1 Resource Capability

Note: Bit definitions are the same as V0VCRC, offset 290h.

5.90 Virtual Channel 1 Resource Control (V1CTL) — Offset 2A0h

Virtual Channel 1 Resource Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + 2A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared. **Locked by:** LPCR.SRL
30:28	0h RO	**Reserved**
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel Note: BIOS is required to program VCID[3] to 0 when operating at DMI2. **Locked by:** LPCR.SRL

Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RO	**Reserved**
19:17	0h RW	**Function Arbitration Select (FAS):** This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.
16	0h RW	**Load Function Arbitration Table (LFAT):** When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table - clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. **Locked by:** LPCR.SRL
9:8	0h RO	**Reserved**
7:1	00h RW	**Transaction Class / Virtual Channel Map (TVM):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.
0	0h RO	**Reserved**

5.91 Virtual Channel 1 Resource Status (V1STS) — Offset 2A6h

Virtual Channel 1 Resource Status

Note: Bit definitions are the same as V0STS, offset 29Ah.

5.92 DPC Extended Capability Header (DPCECH) — Offset A00h

DPC Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support DPC Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** For systems that support DPC Extended Capability, BIOS should write a 001Dh to this register else it should write 0.

5.93 DPC Capability (DPCCAPR) — Offset A04h

DPC Capability Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + A04h	14E0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12	1h RW/O	**DL_Active ERR_COR Signaling Supported (DLAECSS):** This field when set, indicates that the Root Port supports the ability to signal with ERR_COR when the link transitions to the DL_Active state. Root Port that supports RP Extensions for DPC must set this bit.
11:8	4h RW/O	**RP PIO Log Size (RPPIOLS):** This field indicates how many DWORDs are allocated for the RP PIO log registers, comprised by the RP PIO Header Log, RP PIO ImpSpec Log and RP PIO TLP Prefix Log. If the Root Port supports RP Extensions for DPC, the value of this field must be 4 or greater - otherwise the value of this field must be 0.
7	1h RW/O	**DPC Software Triggering Supported (DPCSTS):** This field when set, indicates that the Root Port supports the ability for software to trigger DPC. Root Ports that support RP Extensions for DPC must set this bit.
6	1h RW/O	**Poisoned TLP Egress Blocking Supported (PTLPEBS):** This field when set, indicates that the Root Port supports the ability to block the transmission of a poisoned TLP from its Egress port. Root Ports that support RP Extensions for DPC must set this bit.

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW/O	**RP Extensions For DPC (RPEFDPC):** This field when set, indicates that a Root Port supports a defined set of DPC Extensions that are specific to Root Ports.
4:0	00h RW/O	**DPC Interrupt Message Number (DPCIMN):** This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with the DPC Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: BIOS is expected to update this field with the right value before enabling DPC interrupt.

5.94 DPC Control (DPCCTLR) — Offset A06h

DPC Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + A06h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RW	**DL_Active ERR_COR Enable (DLAECE):** This bit when set, enables the downstream port to signal ERR_COR when the link transitions to the DL_Active state.
6	0h RW/1S/V	**DPC Software Trigger (DPCST):** If DPC Trigger is enabled and the DPC Trigger Status bit is clear, software writing a 1b to this bit will cause DPC to be triggered. If DPC Trigger is not enabled or DPC Trigger Status is set, software writing a 1b to this bit has no effect. Note: It is permitted to write 1b to this bit while simultaneously writing updated values to other fields in this register, notably the DPC Trigger Enable field. For this case, the DPC Software Trigger semantics are based on the updated value of the DPC Trigger Enable field. *Note: This bit always return 0b when read.
5	0h RW	**Poisoned TLP Egress Blocking Enable (PTLPEBE):** This bit, when set, enables the associated Egress Port to block the transmission of poisoned TLP.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**DPC ERR_COR Enable (DPCECE):** When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered.
3	0h RW	**DPC Interrupt Enable (DPCIE):** When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered.
2	0h RW	**DPC Completion Control (DPCCC):** This bit controls the Completion Status for completions formed during DPC. 0b: Completer Abort (CA) Completion Status. 1b: Unsupported Request (UR) Completion Status.
1:0	0h RW	**DPC Trigger Enable (DPCTE):** This field enables DPC and controls the conditions that cause DPC to be triggered. 00b: DPC is disabled. 01b: DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_FATAL message. 10b: DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_NONFATAL or ERR_FATAL message. 11b: Reserved.

5.95 DPC Status (DPCSR) — Offset A08h

DPC Status Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + A08h	1F00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:8	1Fh RO/V/P	**RP PIO First Error Pointer (RPPIOFEP):** The value of this field identifies a bit position in the RP PIO Status register, and this field is considered valid when that bit is set. When this field is valid, and software writes a 1b to the indicated RP PIO Status bit (thus clearing it), this field must revert to its default value. This field is applicable only for Root Ports that support RP Extensions for DPC, and is otherwise reserved. If this field is not reserved, the default value is 11111b.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RO/V/P	**DPC Trigger Extension (DPCTE):** This field serves as an extension to the DPC Trigger Reason field. When that field is valid and has a value of 11b, this field indicates why DPC has been triggered. 00b: DPC was triggered due to RP PIO error. 01b: DPC was triggered due to DPC Software Trigger bit. 10b: Reserved. 11b: Reserved. This field is valid only when the DPC Trigger Status bit is set and the value of the DPC Trigger Reason field is 11b. Otherwise the value of this field is undefined.
4	0h RO/V	**DPC RP Busy (DPCRPB):** When the DPC Trigger Status bit is Set and this bit is Set, the Root Port is busy with internal activity that must complete before software is permitted to clear the DPC Trigger Status bit. If software Clears the DPC Trigger Status bit while this bit is set, the behavior is undefined. This field is valid only when the DPC Trigger Status bit is Set - otherwise the value of this field is undefined. This bit is applicable only for Root Ports that support RP Extensions for DPC, and is Reserved otherwise.
3	0h RW/1C/V/P	**DPC Interrupt Status (DPCIS):** This bit is set if DPC is triggered while the DPC Interrupt Enable bit is set.
2:1	0h RO/V/P	**DPC Trigger Reason (DPCTR):** This field indicates why DPC has been triggered. 00b: DPC was triggered due to an unmasked uncorrectable error. 01b: DPC was triggered due to receiving an ERR_NONFATAL. 10b: DPC was triggered due to receiving an ERR_FATAL. 11b: DPC was triggered due to a reason that is indicated by the DPC Trigger Reason Extension field. Note: This field is only valid when DPC Trigger Status bit is set - otherwise the value of this field is undefined.
0	0h RW/1C/V/P	**DPC Trigger Status (DPCTS):** When set, indicates that DPC has been triggered. DPC is event triggered. While this bit is set, hardware must direct the LTSSM to the Disabled state. This bit must be cleared before the LTSSM can be released from Disabled state. Once the requirements for how long software must leave the downstream port in DPC is met, software is permitted to clear this bit regardless of the state of other status bits associated with the triggering event. Refer to PCIe Base specification 3.0 for more timing requirements pertaining to this bit.

5.96 DPC Error Source ID (DPCESIDR) — Offset A0Ah

DPC Error Source ID Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + A0Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V/P	**DPC Error Source ID (DPCESID):** When the DPC Trigger Reason field indicates that DPC was triggered due to the reception of an ERR_NONFATAL or ERR_FATAL message, this register field contains the Requester ID of the received messages. Otherwise, the value of this register is undefined.

5.97 RP PIO Status (RPPIOSR) — Offset A0Ch

RP PIO Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A0Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/1C/V/P	**Memory Completion Timeout Status (MCTS):** Non-posted memory request completion times out.
17	0h RW/1C/V/P	**Memory Completer Abort Completion Status (MCACS):** Non-posted memory request received CA completion.
16	0h RW/1C/V/P	**Memory Unsupported Request Completion Status (MURCS):** Non-posted Memory request received UR completion.
15:11	0h RO	**Reserved**
10	0h RW/1C/V/P	**I/O Completion Timeout Status (IOCTS):** I/O request completion times out.
9	0h RW/1C/V/P	**I/O Completer Abort Completion Status (IOCACS):** I/O request received CA completion.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**I/O Unsupported Request Completion Status (IOURCS):** I/O request received UR completion.
7:3	0h RO	**Reserved**
2	0h RW/1C/V/P	**Configuration Completion Timeout Status (CCTS):** Configuration request completion times out.
1	0h RW/1C/V/P	**Configuration Completer Abort Completion Status (CCACS):** Configuration request received CA completion.
0	0h RW/1C/V/P	**Configuration Unsupported Request Completion Status (CURCS):** Configuration request received UR completion.

5.98 RP PIO Mask (RPPIOMR) — Offset A10h

RP PIO Mask Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A10h	00070707h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	1h RW/P	**Memory Completion Timeout Mask (MCTM):** Mask bit for Memory Completion Timeout Status.
17	1h RW/P	**Memory Completer Abort Completion Mask (MCACM):** Mask bit for Memory Completer Abort Completion Status.
16	1h RW/P	**Memory Unsupported Request Completion Mask (MURCM):** Mask bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	1h RW/P	**I/O Completion Timeout Mask (IOCTM):** Mask bit for I/O Completion Timeout Status.
9	1h RW/P	**I/O Completer Abort Completion Mask (IOCACM):** Mask bit for I/O Completer Abort Completion Status.
8	1h RW/P	**I/O Unsupported Request Completion Mask (IOURCM):** Mask bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/P	**Configuration Completion Timeout Mask (CCTM):** Mask bit for Configuration Completion Timeout Status.
1	1h RW/P	**Configuration Completer Abort Completion Mask (CCACM):** Mask bit for Configuration Completer Abort Status.
0	1h RW/P	**Configuration Unsupported Request Completion Mask (CURCM):** Mask bit for Configuration Unsupported Request Completion Status.

5.99 RP PIO Severity (RPPIOVR) — Offset A14h

RP PIO Severity Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout Severity (MCTSV):** Severity bit for Memory Completion Timeout Status.
17	0h RW/P	**Memory Completer Abort Completion Severity (MCACSV):** Severity bit for Memory Completer Abort Completion Status.
16	0h RW/P	**Memory Unsupported Request Completion Severity (MURCSV):** Severity bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout Severity (IOCTSV):** Severity bit for I/O Completion Timeout Status.
9	0h RW/P	**I/O Completer Abort Completion Severity (IOCACSV):** Severity bit for I/O Completer Abort Completion Status.
8	0h RW/P	**I/O Unsupported Request Completion Severity (IOURCSV):** Severity bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout Severity (CCTSV):** Severity bit for Configuration Completion Timeout Status.
1	0h RW/P	**Configuration Completer Abort Completion Severity (CCACSV):** Severity bit for Configuration Completer Abort Status.
0	0h RW/P	**Configuration Unsupported Request Completion Severity (CURCSV):** Severity bit for Configuration Unsupported Request Completion Status.

5.100 RP PIO SysError (RPPIOSER) — Offset A18h

RP PIO SysError Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout SysErr (MCTSE):** SysErr bit for Memory Completion Timeout Status.
17	0h RW/P	**Memory Completer Abort Completion SysErr (MCACSE):** SysErr bit for Memory Completer Abort Completion Status.
16	0h RW/P	**Memory Unsupported Request Completion SysErr (MURCSE):** SysErr bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout SysErr (IOCTSE):** SysErr bit for I/O Completion Timeout Status.
9	0h RW/P	**I/O Completer Abort Completion SysErr (IOCACSE):** SysErr bit for I/O Completer Abort Completion Status.
8	0h RW/P	**I/O Unsupported Request Completion SysErr (IOURCSE):** SysErr bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout SysErr (CCTSE):** SysErr bit for Configuration Completion Timeout Status.
1	0h RW/P	**Configuration Completer Abort Completion SysErr (CCACSE):** SysErr bit for Configuration Completer Abort Status.
0	0h RW/P	**Configuration Unsupported Request Completion SysErr (CURCSE):** SysErr bit for Configuration Unsupported Request Completion Status.

5.101 RP PIO Exception (RPPIOER) — Offset A1Ch

RP PIO Exception Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout Exception (MCTE):** Exception bit for Memory Completion Timeout Status.
17	0h RW/P	**Memory Completer Abort Completion Exception (MCACE):** Exception bit for Memory Completer Abort Completion Status.
16	0h RW/P	**Memory Unsupported Request Completion Exception (MURCE):** Exception bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout Exception (IOCTE):** Exception bit for I/O Completion Timeout Status.
9	0h RW/P	**I/O Completer Abort Completion Exception (IOCACE):** Exception bit for I/O Completer Abort Completion Status.
8	0h RW/P	**I/O Unsupported Request Completion Exception (IOURCE):** Exception bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout Exception (CCTE):** Exception bit for Configuration Completion Timeout Status.
1	0h RW/P	**Configuration Completer Abort Completion Exception (CCACE):** Exception bit for Configuration Completer Abort Status.
0	0h RW/P	**Configuration Unsupported Request Completion Exception (CURCE):** Exception bit for Configuration Unsupported Request Completion Status.

5.102 RP PIO Header Log DW1 (RPPIOHLR_DW1) — Offset A20h

RP PIO Header Log DW1 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st DWORD of TLP (DW1):** Byte0 AND Byte1 AND Byte2 AND Byte3.

5.103 RP PIO Header Log DW2 (RPPIOHLR_DW2) — Offset A24h

RP PIO Header Log DW2 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd DWORD of TLP (DW2):** Byte4 AND Byte5 AND Byte6 AND Byte7.

5.104 RP PIO Header Log DW3 (RPPIOHLR_DW3) — Offset A28h

RP PIO Header Log DW3 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd DWORD of TLP (DW3):** Byte8 AND Byte9 AND Byte10 AND Byte11.

5.105 RP PIO Header Log DW4 (RPPIOHLR_DW4) — Offset A2Ch

RP PIO Header Log DW4 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th DWORD of TLP (DW4):** Byte12 AND Byte13 AND Byte14 AND Byte15.

5.106 Secondary PCI Express Extended Capability Header (SPEECH) — Offset A30h

Secondary PCI Express Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

5.107 Link Control 3 (LCTL3) — Offset A34h

Link Control 3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RW	**Enable Lower SKP OS Generation Vector (ELSOSGV):** When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bits 6:4 Rsvd Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved**
1	0h RW/P	**Link Equalization Request Interrupt Enable (LERIE):** When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW/1S/V	**Perform Equalization (PE):** When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization Phase 1.

5.108 Lane Error Status (LES) — Offset A38h

Lane Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V/P	**Lane 15 Error Status (L15ES):** Lane 15 detected a Lane-based error.
14	0h RW/1C/V/P	**Lane 14 Error Status (L14ES):** Lane 14 detected a Lane-based error.
13	0h RW/1C/V/P	**Lane 13 Error Status (L13ES):** Lane 13 detected a Lane-based error.
12	0h RW/1C/V/P	**Lane 12 Error Status (L12ES):** Lane 12 detected a Lane-based error.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C/V/P	**Lane 11 Error Status (L11ES):** Lane 11 detected a Lane-based error.
10	0h RW/1C/V/P	**Lane 10 Error Status (L10ES):** Lane 10 detected a Lane-based error.
9	0h RW/1C/V/P	**Lane 9 Error Status (L9ES):** Lane 9 detected a Lane-based error.
8	0h RW/1C/V/P	**Lane 8 Error Status (L8ES):** Lane 8 detected a Lane-based error.
7	0h RW/1C/V/P	**Lane 7 Error Status (L7ES):** Lane 7 detected a Lane-based error.
6	0h RW/1C/V/P	**Lane 6 Error Status (L6ES):** Lane 6 detected a Lane-based error.
5	0h RW/1C/V/P	**Lane 5 Error Status (L5ES):** Lane 5 detected a Lane-based error.
4	0h RW/1C/V/P	**Lane 4 Error Status (L4ES):** Lane 4 detected a Lane-based error.
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 detected a Lane-based error.

5.109 Lane 0 And Lane 1 Equalization Control (L01EC) — Offset A3Ch

Lane 0 And Lane 1 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A3Ch	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.110 Lane 2 And Lane 3 Equalization Control (L23EC) — Offset A40h

Lane 2 And Lane 3 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A40h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset Hint (UPL3TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.111 Lane 4 And Lane 5 Equalization Control (L45EC) — Offset A44h

Lane 4 And Lane 5 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A44h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 5 Receiver Preset Hint (UPL5RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 5 Transmitter Preset (UPL5TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 5 Receiver Preset Hint (DPL5RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 5 Transmitter Preset (DPL5TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 4 Receiver Preset Hint (UPL4RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 4 Transmitter Preset (UPL4TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 4 Receiver Preset Hint (DPL4RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 4 Transmitter Preset (DPL4TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.112 Lane 6 And Lane 7 Equalization Control (L67EC) — Offset A48h

Lane 6 And Lane 7 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A48h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 7 Receiver Preset Hint (UPL7RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
27:24	Fh RW	**Upstream Port Lane 7 Transmitter Preset (UPL7TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 7 Receiver Preset Hint (DPL7RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 7 Transmitter Preset (DPL7TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 6 Receiver Preset Hint (UPL6RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 6 Transmitter Preset (UPL6TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 6 Receiver Preset Hint (DPL6RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 6 Transmitter Preset (DPL6TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.113 Lane 8 And Lane 9 Equalization Control (L89EC) — Offset A4Ch

Lane 8 And Lane 9 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A4Ch	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 9 Receiver Preset Hint (UPL9RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 9 Transmitter Preset (UPL9TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 9 Receiver Preset Hint (DPL9RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 9 Transmitter Preset (DPL9TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 8 Receiver Preset Hint (UPL8RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 8 Transmitter Preset (UPL8TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 8 Receiver Preset Hint (DPL8RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 8 Transmitter Preset (DPL8TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.114 Lane 10 And Lane 11 Equalization Control (L1011EC) — Offset A50h

Lane 10 And Lane 11 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A50h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 11 Receiver Preset Hint (UPL11RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 11 Transmitter Preset (UPL11TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 11 Receiver Preset Hint (DPL11RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 11 Transmitter Preset (DPL11TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 10 Receiver Preset Hint (UPL10RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Upstream Port Lane 10 Transmitter Preset (UPL10TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 10 Receiver Preset Hint (DPL10RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 10 Transmitter Preset (DPL10TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.115 Lane 12 And Lane 13 Equalization Control (L1213EC) — Offset A54h

Lane 12 And Lane 13 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A54h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 13 Receiver Preset Hint (UPL13RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 13 Transmitter Preset (UPL13TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 13 Receiver Preset Hint (DPL13RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 13 Transmitter Preset (DPL13TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 12 Receiver Preset Hint (UPL12RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 12 Transmitter Preset (UPL12TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 12 Receiver Preset Hint (DPL12RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 12 Transmitter Preset (DPL12TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.116 Lane 14 And Lane 15 Equalization Control (L1415EC) — Offset A58h

Lane 14 And Lane 15 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A58h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 15 Receiver Preset Hint (UPL15RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
27:24	Fh RW	**Upstream Port Lane 15 Transmitter Preset (UPL15TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 15 Receiver Preset Hint (DPL15RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 15 Transmitter Preset (DPL15TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 14 Receiver Preset Hint (UPL14RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 14 Transmitter Preset (UPL14TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 14 Receiver Preset Hint (DPL14RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 14 Transmitter Preset (DPL14TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.117 Data Link Feature Extended Capability Header (DLFECH) — Offset A90h

Data Link Feature Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability.

5.118 Data Link Feature Capabilities (DLFCAP) — Offset A94h

Data Link Feature Capabilities Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A94h	80000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/O	**Data Link Feature Exchange Enable (DLFEE):** If set, this bit indicates that this Port will enter the DL_Feature negotiation state. Default is 1b.
30:23	0h RO	**Reserved**
22:1	000000h RW/O	**Local Feature Supported (LFS):** These bits indicate that the Downstream Port supports the associated Data Link Feature. For this version of this specification, this field is hardwired to 0.
0	1h RW/O	**Local Scaled Flow Control Supported (LSFCS):** This bit indicates that the Port supports the Scaled Flow Control Feature.

5.119 Data Link Feature Status (DLFSTS) — Offset A98h

Data Link Feature Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Data Link Feature Status Valid (DLFSV):** This bit indicates that the Downstream Port has received a Data Link Feature DLLP after the Link entered L0. When this bit is 1b, bits 23:0 are frozen. Software must clear this bit to re-enable capturing information. This bit is cleared on DL_Down.
30:23	0h RO	**Reserved**
22:1	000000h RO/V	**Remote Feature Supported (RFS):** These bits indicate that the Remote Port supports the corresponding Data Link Feature. These bits capture all information from the Data Link Feature DLLP even when this Port does not support the corresponding feature.
0	0h RO/V	**Remote Scaled Flow Control Supported (RSFCS):** This bit indicates that the Remote Port indicated it supports the Scaled Flow Control Feature

5.120 Physical Layer 16.0 GT/s Extended Capability Header (PL16GECH) — Offset A9Ch

Physical Layer 16.0 GT/s Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + A9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Physical Layer 16.0 GT/s Capability

5.121 Physical Layer 16.0 GT/s Capability (PL16CAP) — Offset AA0h

Physical Layer 16.0 GT/s Capability Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

5.122 Physical Layer 16.0 GT/s Control (PL16CTL) — Offset AA4h

Physical Layer 16.0 GT/s Control Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

5.123 Physical Layer 16.0 GT/s Status (PL16S) — Offset AA8h

Physical Layer 16.0 GT/s Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW/1C/V/P	**Link Equalization Request 16.0 GT/s (LERG4):** This bit is Set by hardware to request the 16.0 GT/s Link equalization process to be performed on the Link. The default value of this bit is 0b.
3	0h RO/V/P	**Equalization 16.0 GT/s Phase 3 Successful (EQP3SG4):** When set to 1b, this bit indicates that Phase 3 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V/P	**Equalization 16.0 GT/s Phase 2 Successful (EQP2SG4):** When set to 1b, this bit indicates that Phase 2 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.
1	0h RO/V/P	**Equalization 16.0 GT/s Phase 1 Successful (EQP1SG4):** When set to 1b, this bit indicates that Phase 1 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.
0	0h RO/V/P	**Equalization 16.0 GT/s Complete (EQG4):** When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 16.0 GT/s data rate has completed. The default value of this bit is 0b.

5.124 Physical Layer 16.0 GT/s Local Data Parity Mismatch Status (PL16LDPMS) — Offset AACh

Physical Layer 16.0 GT/s Local Data Parity Mismatch Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**Local Data Parity Mismatch Status (LDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

5.125 Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status (PL16FRDPMS) — Offset AB0h

Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AB0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**First Retimer Data Parity Mismatch Status (FRDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

5.126 Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status (PL16SRDPMS) — Offset AB4h

Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AB4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**Second Retimer Data Parity Mismatch Status (SRDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

5.127 Physical Layer 16.0 GT/s Extra Status (PL16ES) — Offset AB8h

Physical Layer 16.0 GT/s Extra Status Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

5.128 Physical Layer 16.0 GT/s Lane 01 Equalization Control (PL16L01EC) — Offset ABCh

Physical Layer 16.0 GT/s Lane 01 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + ABCh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 1 Transmitter Preset (UP16L1TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 1 Transmitter Preset (DP16L1TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 0 Transmitter Preset (UP16L0TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 0 Transmitter Preset (DP16L0TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.129 Physical Layer 16.0 GT/s Lane 23 Equalization Control (PL16L23EC) — Offset ABEh

Physical Layer 16.0 GT/s Lane 23 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + ABEh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 3 Transmitter Preset (UP16L3TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 3 Transmitter Preset (DP16L3TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 2 Transmitter Preset (UP16L2TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 2 Transmitter Preset (DP16L2TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.130 Physical Layer 16.0 GT/s Lane 45 Equalization Control (PL16L45EC) — Offset AC0h

Physical Layer 16.0 GT/s Lane 45 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + AC0h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 5 Transmitter Preset (UP16L5TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 5 Transmitter Preset (DP16L5TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 4 Transmitter Preset (UP16L4TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 4 Transmitter Preset (DP16L4TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.131 Physical Layer 16.0 GT/s Lane 67 Equalization Control (PL16L67EC) — Offset AC2h

Physical Layer 16.0 GT/s Lane 67 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + AC2h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 7 Transmitter Preset (UP16L7TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 7 Transmitter Preset (DP16L7TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 6 Transmitter Preset (UP16L6TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 6 Transmitter Preset (DP16L6TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.132 Physical Layer 16.0 GT/s Lane 89 Equalization Control (PL16L89EC) — Offset AC4h

Physical Layer 16.0 GT/s Lane 89 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + AC4h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 9 Transmitter Preset (UP16L9TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 9 Transmitter Preset (DP16L9TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 8 Transmitter Preset (UP16L8TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 8 Transmitter Preset (DP16L8TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.133 Physical Layer 16.0 GT/s Lane 1011 Equalization Control (PL16L1011EC) — Offset AC6h

Physical Layer 16.0 GT/s Lane 1011 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + AC6h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 11 Transmitter Preset (UP16L11TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 11 Transmitter Preset (DP16L11TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 10 Transmitter Preset (UP16L10TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 10 Transmitter Preset (DP16L10TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.134 Physical Layer 16.0 GT/s Lane 1213 Equalization Control (PL16L1213EC) — Offset AC8h

Physical Layer 16.0 GT/s Lane 1213 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + AC8h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 13 Transmitter Preset (UP16L13TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 13 Transmitter Preset (DP16L13TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 12 Transmitter Preset (UP16L12TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 12 Transmitter Preset (DP16L12TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.135 Physical Layer 16.0 GT/s Lane 1415 Equalization Control (PL16L1415EC) — Offset ACAh

Physical Layer 16.0 GT/s Lane 1415 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + ACAh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 15 Transmitter Preset (UP16L15TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 15 Transmitter Preset (DP16L15TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 14 Transmitter Preset (UP16L14TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 14 Transmitter Preset (DP16L14TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

5.136 Physical Layer 32.0 GT/s Extended Capability Header (G5ECH) — Offset ADCh

Physical Layer 32.0 GT/s Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + ADCh	0000002Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: Lock Key bit is located in the Personality Lock Key Control Register. Software will need to program this field appropriately for linked capabilities list if default is not supported.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.
15:0	002Ah RW/O	**PCI Express Extended Capability ID (ECID):** This field is a PCISIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 32.0 GT/s Capability is 002Ah.

5.137 Physical Layer 32.0 GT/s Capability (G5CAP) — Offset AE0h

Physical Layer 32.0 GT/s Capability

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AE0h	00000100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:11	00h RO	**Modified TS Reserved Usage Modes (MODTSUSGMDRSVRVD):** This field is reserved for future Usage Modes defined by the PCISIG. Must be 0.
10	0h RW/O	**Modified TS Usage Mode 2 Supported - Alternate Protocol (MODTSUSGMD2SUP):** This bit indicates that this Port supports sending and recieving vendor specific Training Set Messages (Modified TS Usage 001b).

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/O	**Modified TS Usage Mode 1 Supported - Training Set Message (MODTSUSGMD1SUP):** This bit indicates that this Port supports sending and recieving vendor specific Training Set Messages (Modified TS Usage 001b).
8	1h RO	**Modified TS Usage Mode 0 Supported - PCI Express (MODTSUSGMD0SUP):** his bit indicates that this Port supports PCI Express (Modified TS Usage 000b). This bit must be 1b.
7:2	0h RO	**Reserved**
1	0h RW/O	**No Equalization Needed Supported (NOEQSUP):** When Set, this Port supports controlling whether or not Equalization is needed.
0	0h RW/O	**Equalization bypass to highest rate Supported (EQBYPSUP):** When Set, this Port supports controlling whether the Port negotiates to skip equalization for speeds other than the highest common supported speed. Must be 1b for Ports that support 32.0 GT/s or higher data rates.

5.138 Physical Layer 32.0 GT/s Control (G5CTL) — Offset AE4h

Physical Layer 32.0 GT/s Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AE4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10:8	0h RW/P	**Modified TS Usage Mode Selected (MODTSUSGSEL):** This field indicates which Usage Mode will be used by this Downstream Port the next time the Link enters LTSSM State. Behavior is undefined if this field indicates a Usage Mode that is not supported (i.e. associated Modified TS Usage Mode Supported bit is Clear). This field is present in Downstream Ports. In Upstream Ports, this field is RsvdP.
7:2	0h RO	**Reserved**
1	1h RW/P	**No Equalization Needed Disable (NOEQDIS):** When Clear, this Port is permitted to indicate that it does not require equalization. When Set, this Port must always indicate that it requires equalization. No Equalization Needed Supported is Set, this bit is RWS with a default value of 0b. No Equalization Needed Supported is Clear, this bit is permitted to be hardwired to 0b. If this bit is Set, Equalization bypass to highest rate Disable must also be Set.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/P	**Equalization bypass to highest rate Disable (EQBYPDIS):** When Clear, this Port indicates during Link Training that is wishes to train to the highest common link data rate and skip equalization of intermediate data rates. Equalization bypass to highest rate Supported is Set, this bit is RWS with a default value of 0b. Equalization bypass to highest rate Supported is Clear, this bit is permitted to be hardwired to 0b.

5.139 Physical Layer 32.0 GT/s Status (G5STS) — Offset AE8h

Physical Layer 32.0 GT/s Status.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AE8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**No Equalization Needed Received (NOEQR):** When Set, this Port either received a Modified TS1/TS2 with the No Equalization Needed bit Set or received a non-modified TS1/TS2 was recieved with the No Equalization Needed encoding (also reported in the Received Enhanced Link Behavior Control field). Default is 0b.
9	0h RO/V	**Transmitter Precode Request (TXPRECODER):** When Set, this Port will request the transmitter to use Precoding by setting the Precoding Request bit in the TS1s/TS2s it transmits prior to entry to Recovery.Speed Default is Implementation Specific.
8	0h RO/V	**Transmitter Precoding On (TXPRECODEO):** This field indicates whether the Receiver asked this transmitter to enable Precoding. This bit is cleared on DL_Down.
7:6	0h RO/V	**Received Enhanced Link Behavior Control (RCVDELBCTL):** This field contains the Enhanced Link Behavior Control bits from the most recent TS1 or TS2 received in the Polling or Configuration states. This field is Cleared on DL_Down.
5	0h RO/V	**Modified TS Received (MODTSRCVD):** If Set, Received Modified TS Data 1 Register and Received Modified TS Data 2 Register contain meaningful data. This bit is Cleared when the Link is Down. This bit is Set when the Modified TS1/TS2 Ordered Set is received
4	0h RW/1C/V/P	**Link Equalization Request 32.0 GT/s (LERG5):** This bit is Set by hardware to request the 32.0 GT/s Link equalization process to be performed on the Link. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V/P	**Equalization 32.0 GT/s Phase 3 Successfu (EQ32PH3SUCC):** When set to 1b, this bit indicates that Phase 3 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.
2	0h RO/V/P	**Equalization 32.0 GT/s Phase 2 Successful (EQ32PH2SUCC):** When set to 1b, this bit indicates that Phase 2 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.
1	0h RO/V/P	**Equalization 32.0 GT/s Phase 1 Successful (EQ32PH1SUCC):** When set to 1b, this bit indicates that Phase 1 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. he default value of this bit is 0b. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.
0	0h RO/V/P	**Equalization 32.0 GT/s Complete (EQ32CMPLT):** When Set, this bit indicates that the 32.0 GT/s Transmitter Equalization procedure has completed. For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.

5.140 Receiver Modified TS Data 1 (RCVDMODTSDATA1) — Offset AECh

Receiver Modified TS Data 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Received Modified TS Vendor ID (RCVDMTSVID):** If Modified TS Received is Set, this field contains the Modified TS Vendor ID field from the Modified TS1/TS2 Ordered Set received If Modified TS Received is Clear, this field contains 0000h. Bits 15:8 contain the value of Symbol 10. Bits 7:0 contain the value of Symbol 11. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0000h.
15:3	0000h RO/V	**Received Modified TS Information 1 (RCVDMTSINFO1):** If Modified TS Received is Set, this field contains the Modified TS Information 1 field from the Modified TS1/TS2 Ordered Set If Modified TS Received is Clear, this field contains 0 0000 0000 0000b. Bits 15:8 contain the value of Symbol 12. Bits 16:8 contain the value of Symbol 13. Bits 7:0 contain the value of Symbol 14. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0 0000 0000 0000b.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO/V	**Received Modified TS Usage Mode (RCVDMTSUSAGEMD):** If Modified TS Received is Set, this field contains the Modified TS Usage field from the Modified TS1/TS2 Ordered Set If Modified TS Received is Clear, this field contains 000b. Unused bits in this field are permitted to he hardwired to 0b. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 000b.

5.141 Receiver Modified TS Data 2 (RCVDMODTSDATA2) — Offset AF0h

Receiver Modified TS Data 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AF0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	0h RO/V	**Alternate Protocol Negotation Status (ALTPROTNEGSTS):** Indicates the status of the Apternate Protocol Negotiaiton. Encodings are: Alternate Protocol Negotiation not supported Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear. Alternate Protocol Negotiation disabled - Modified TS Usage Mode 2 Supported - Alternate Protoco is Set but Modified TS Usage Mode Selected was not 2 during the appropriate LTSSM State. Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. Alternate protocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the ownstream Port selected one of those protocols for use. If Set, Alternate Protocol Negotiation completed succesfully. If Clear, alternate protocol negotiation negotiation has not completed succesfully. If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h. If Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear, this bit is hardwired to 0b. If Modified TS Usage Mode Selected does not equal 2, this bit contains 0b. This bit is Cleared on XXX LTSSM State

Bit Range	Default & Access	Field Name (ID): Description
23:0	000000h RO/V	**Received Modified TS Information 2 (RCVDMTSINFO2):** If Modified TS Received is Set, this field contains the Modified TS Information 2 field from the received Modified TS1/TS2 Ordered Set If Modified TS Received is Clear, this field contains 00 0000h. Bits 23:16 contain the value of Symbol 12. Bits 16:8 contain the value of Symbol 13. Bits 7:0 contain the value of Symbol 14. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 00 0000h.

5.142 Transmitted Modified TS Data 1 (TRNSMODTSDATA1) — Offset AF4h

Transmitted Modified TS Data 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AF4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Transmitted Modified TS Vendor ID (TRNSMTSVID):** If Modified TS Received is Set, this field contains the Modified TS Vendor ID field from the last Modified TS1/TS2 Ordered Set transmitted during the most recent LTSSM State. Bits 15:8 contain the value of Symbol 10. Bits 7:0 contain the value of Symbol 11. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0000h.
15:3	0000h RO/V	**Transmitted Modified TS Information 1 (TRNSMTSINFO1):** Transmitted Modified TS Information 1- If Modified TS Received is Set, this field contains the Modified TS Information 1 field from the last Modified TS1/TS2 Ordered Set transmitted during the most recent LTSSM State. Bits 15:8 contain the value of Symbol 12. Bits 16:8 contain the value of Symbol 13. Bits 7:0 contain the value of Symbol 14. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0 0000 0000 0000b.
2:0	0h RO/V	**Transmitted Modified TS Usage Mode (TRNSMTSUSAGEMD):** If Modified TS Received is Set, this field contains the Modified TS Usage field from the last Modified TS1/TS2 Ordered Set transmitted during the most recent LTSSM State. Unused bits in this field are permitted to he hardwired to 0b. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 000b.

5.143 Transmitted Modified TS Data 2 (TRNSMODTSDATA2) — Offset AF8h

Transmitted Modified TS Data 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AF8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	0h RO/V	**Alternate Protocol Negotation Status (ALTPROTNEGSTS):** Alternate Protocol Negotation Status - Indicates the status of the Apternate Protocol Negotiaiton. Encodings are Alternate Protocol Negotiation not supported - Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear. Alternate Protocol Negotiation disabled - Modified TS Usage Mode 2 Supported - Alternate Protocol is Set but Modified TS Usage Mode Selected was not 2 during the appropriate LTSSM State. Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. Alternate rotocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the Downstream Port selected one of those protocols for use. If Set, Alternate Protocol Negotiation completed succesfully. If Clear, alternate protocol negotiation negotiation has not completed succesfully. If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h. If Modified TS Usage Mode 2 Supported - Alternate Protocol is Clear, this bit is hardwired to 0b. If Modified TS Usage Mode Selected does not equal 2, this bit contains 0b. This bit is Cleared on XXX LTSSM State.
23:0	000000h RO/V	**Transmitted Modified TS Information 2 (TRNSMTSINFO2):** If Modified TS Received is Set, this field contains the Modified TS Information 2 field from the last Modified TS1/TS2 Ordered Set transmitted during the most recent LTSSM State. Bits 23:16 contain the value of Symbol 12. Bits 16:8 contain the value of Symbol 13. Bits 7:0 contain the value of Symbol 14. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 00 0000h.

5.144 32.0 GT/s Lane 0123 Equalization Control (G5LANEEQCTL_0) — Offset AFCh

32.0 GT/s Lane 0123 Equalization Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + AFCh	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>31:28</td><td>Fh
RW</td><td>**Lane 3 Upstream Port 32.0 GT/s Transmitter Preset (L3UPTP):**
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstram	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>27:24</td><td>Fh
RW</td><td>**Lane 3 Downstream Port 32.0 GT/s Transmitter Preset (L3DPTP):**
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>23:20</td><td>Fh
RW</td><td>Lane 2 Upstream Port 32.0 GT/s Transmitter Preset (L2UPTP):
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstram	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>19:16</td><td>Fh
RW</td><td>Lane 2 Downstream Port 32.0 GT/s Transmitter Preset (L2DPTP):
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Lane 1 Upstream Port 32.0 GT/s Transmitter Preset (L1UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
11:8	Fh RW	**Lane 1 Downstream Port 32.0 GT/s Transmitter Preset (L1DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>7:4</td><td>Fh
RW</td><td>Lane 0 Upstream Port 32.0 GT/s Transmitter Preset (L0UPTP):
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstram	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>3:0</td><td>Fh
RW</td><td>Lane 0 Downstream Port 32.0 GT/s Transmitter Preset (L0DPTP):
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

5.145 32.0 GT/s Lane 4567 Equalization Control (G5LANEEQCTL_4) — Offset B00h

32.0 GT/s Lane 4567 Equalization Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B00h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**Lane 7 Upstream Port 32.0 GT/s Transmitter Preset (L7UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
27:24	Fh RW	**Lane 7 Downstream Port 32.0 GT/s Transmitter Preset (L7DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>23:20</td><td>Fh
RW</td><td>Lane 6 Upstream Port 32.0 GT/s Transmitter Preset (L6UPTP):
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstream	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>19:16</td><td>Fh
RW</td><td>Lane 6 Downstream Port 32.0 GT/s Transmitter Preset (L6DPTP):
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>15:12</td><td>Fh
RW</td><td>Lane 5 Upstream Port 32.0 GT/s Transmitter Preset (L5UPTP):
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstram	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>11:8</td><td>Fh
RW</td><td>Lane 5 Downstream Port 32.0 GT/s Transmitter Preset (L5DPTP):
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

Bit Range	Default & Access	Field Name (ID): Description
7:4	Fh RW	**Lane 4 Upstream Port 32.0 GT/s Transmitter Preset (L4UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
3:0	Fh RW	**Lane 4 Downstream Port 32.0 GT/s Transmitter Preset (L4DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

5.146 32.0 GT/s Lane 891011 Equalization Control (G5LANEEQCTL_8) — Offset B04h

32.0 GT/s Lane 891011 Equalization Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B04h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**Lane 11 Upstream Port 32.0 GT/s Transmitter Preset (L11UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
27:24	Fh RW	**Lane 11 Downstream Port 32.0 GT/s Transmitter Preset (L11DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

Bit Range	Default & Access	Field Name (ID): Description
23:20	Fh RW	**Lane 10 Upstream Port 32.0 GT/s Transmitter Preset (L10UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
19:16	Fh RW	**Lane 10 Downstream Port 32.0 GT/s Transmitter Preset (L10DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>15:12</td><td>Fh
RW</td><td>Lane 9 Upstream Port 32.0 GT/s Transmitter Preset (L9UPTP):
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstram	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>11:8</td><td>Fh
RW</td><td>Lane 9 Downstream Port 32.0 GT/s Transmitter Preset (L9DPTP):
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

Bit Range	Default & Access	Field Name (ID): Description
7:4	Fh RW	**Lane 8 Upstream Port 32.0 GT/s Transmitter Preset (L8UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
3:0	Fh RW	**Lane 8 Downstream Port 32.0 GT/s Transmitter Preset (L8DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

5.147 32.0 GT/s Lane 12131415 Equalization Control (G5LANEEQCTL_12) — Offset B08h

32.0 GT/s Lane 12131415 Equalization Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B08h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**Lane 15 Upstream Port 32.0 GT/s Transmitter Preset (L15UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
27:24	Fh RW	**Lane 15 Downstream Port 32.0 GT/s Transmitter Preset (L15DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

Bit Range	Default & Access	Field Name (ID): Description
23:20	Fh RW	**Lane 14 Upstream Port 32.0 GT/s Transmitter Preset (L14UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
19:16	Fh RW	**Lane 14 Downstream Port 32.0 GT/s Transmitter Preset (L14DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Lane 13 Upstream Port 32.0 GT/s Transmitter Preset (L13UPTP):** Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows: | | Operating | Crosslink | Usage | | | Port | Supported | | | | Direction | | | | A | Downstream | Any | Field Contains The Value | | | Port | | sent on the associoated lane | | | | | during Link Equalization. | | B | Upstream | 0b | Field is intended for debug | | | Port | | and diagnostics. It Contains | | | | | the value captured From the | | | | | associated Lane during Link | | | | | Equalization | | | | | | | | | | When Crosslink are supported,| | | | | Case C (below) applies and | | | | | this captured information | | | | | is not visible to software. | | | | | Vendor are encourage to | | | | | provide an alternate | | | | | mechanism to obtain this | | | | | informations. | | C | Upstram | 1b | Field is not used or | | | Port | | affectedby the current Link | | | | | Equalization. | | | | | | | | | | Field value will be used if | | | | | negotiation a future | | | | | crosslink switches the | | | | | operating port Direction | | | | | so that case A (above) | | | | | applies. |
11:8	Fh RW	**Lane 13 Downstream Port 32.0 GT/s Transmitter Preset (L13DPTP):** Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>7:4</td><td>Fh
RW</td><td>Lane 12 Upstream Port 32.0 GT/s Transmitter Preset (L12UPTP):
Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization.
Field usage varies as follows:
| | Operating | Crosslink | Usage |
	Port	Supported	
	Direction		
A	Downstream	Any	Field Contains The Value
	Port		sent on the associoated lane
			during Link Equalization.
B	Upstream	0b	Field is intended for debug
	Port		and diagnostics. It Contains
			the value captured From the
			associated Lane during Link
			Equalization
			When Crosslink are supported,
			Case C (below) applies and
			this captured information
			is not visible to software.
			Vendor are encourage to
			provide an alternate
			mechanism to obtain this
			informations.
C	Upstram	1b	Field is not used or
	Port		affectedby the current Link
			Equalization.
			Field value will be used if
			negotiation a future
			crosslink switches the
			operating port Direction
			so that case A (above)
			applies. |</td></tr>
<tr><td>3:0</td><td>Fh
RW</td><td>Lane 12 Downstream Port 32.0 GT/s Transmitter Preset (L12DPTP):
Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit</td></tr>
</table>

5.148 Alternate Protocol Extended Capability Header (APEC) — Offset B0Ch

Alternate Protocol Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B0Ch	0000002Bh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	002Bh RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Alternate Protocol Capability is 002Bh.

5.149 Alternate Protocol Capabilities (APCAPR) — Offset B10h

Alternate Protocol Capabilities.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW/O	**Alternate Protocol Selective Enable Supported (APSES):** If Set, the Alternate Protocol Selective Enable Mask Register is present. If Clear, the Alternate Protocol Selective Enable Mask Register is not present and alternate protocol negotiation is controlled soley by the Alternate Protocol Negotiation Global Enable bit. In Upstream Ports, this bit is hardwired to 0b. In Downstream Ports, this bit is HwInit with an implementation specific default value.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Alternate Protocol Count (APC):** Indicates the number of Alternate Protocols supported by one or more Lanes of this Link. Since support for PCI Express is mandatory, the value of this field must be greater than or equal to 1. **Locked by:** LPCRE.IPCL

5.150 Alternate Protocol Control (APCTRLR) — Offset B14h

Alternate Protocol Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B14h	000000FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	FFh RW	**Alternate Protocol Index Select (APIS):** This field determines which Lane and which Alternate Protocol of that Lane is visible in Alternate Protocol Data 1 Register and Alternate Protocol Data 2 Register. The default value of this field is 00h. Unused bits in this field are permitted to be hardwired to 0b. If Alternate Protocol Count is 01h, this field is permitted to be hardwired to 00h. Behavior is undefined if this field is greater than Alternate Protocol Count. Specific Alternate Protocol Index Select values are permitted to be disabled without renumbering other protocol index values. Disabled entries return an Alternate Protocol Vendor ID of FFFFh.

5.151 Alternate Protocol Data 1 (APD1R) — Offset B18h

Alternate Protocol Data 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B18h	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RW/O	**Alternate Protocol Vendor ID (APVID):** This field contains the Vendor ID associated alternate protocol associated with the Alternate Protocol Index Select value. Bits 7:0 of this field contain bits 7:0 of Vendor ID (Symbol 10). Bits 15:8 of this field contain bits 15:8 of Vendor ID (Symbol 11). If Alternate Protocol Index Select is greater than or equal to Alternate Protocol Count, this field contains FFFFh. If Alternate Protocol Index Select is associated with a disabled alternate protocol, this field contains FFFFh.
15:5	000h RW/O	**Alternate Protocol Details (APD):** This field contains the Alternate Protocol Details associated alternate protocol associated with the Alternate Protocol Index Select value. If Alternate Protocol Vendor ID is FFFFh, the value of this field is undefined.
4:3	0h RO	**Reserved**
2:0	0h RW/O	**Alternate Protocol Usage Information (APUI):** This field contains the Modified TS Usage Information associated alternate protocol associated with the Alternate Protocol Index Select value.

5.152 Alternate Protocol Data 2 (APD2R) — Offset B1Ch

Alternate Protocol Data 2 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23:0	000000h RO	**Modified TS Information 2 (MTSI2):** This field contains the value for symbols 12 throught 14 for the alternate protocol associated with the Alternate Protocol Index Select value. If Alternate Protocol Vendor ID is FFFFh, the value of this field is undefined. Bits 7:0 contain the value of Symbol 12. Bits 16:8 contain the value of Symbol 13. Bits 23:16 contain the value of Symbol 14.

5.153 Alternate Protocol Selective Enable Mask (APSEMR) — Offset B20h

Alternate Protocol Selective Enable Mask Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + B20h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RW/P	**Alternate Protocol Selective Enable Mask - Others (APEMO):** Other bits in this register represent protocols other than PCI Express. The default values of these other bits is implementation specific. The width of this field is shown here as 32 bits. The actual width derpends on Alternate Protocol Count. Bits in this field corresponding to disabled Alternate Protocol Index values are permitted to be hardwired to 0b. Bits in this field corresponding to Alternate Protocol Index Select values above Alternate Protocol Count are permitted to be hardwired to 0b.
0	1h RW/P	**Alternate Protocol Selective Enable Mask - PCI Express (APEMPCIE):** The PCI Express Protocol is always index 00h. The default value of this bit is 1b (i.e., PCI Express is always enabled by default). This bit is permitted to be hardwired to 1b.

5.154 Multicast Extended Capability Header (MCECH) — Offset C00h

Multicast Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For system that supports Multicast, the Capability Version would show the value of 1h else the value of this register is 0
15:0	0000h RW/O	**Capability ID (CID):** For system that supports Multicast, the Capability ID would show the value of 0012h else the value of this register is 0

5.155 Multicast Extended Capability (MCAPR) — Offset C04h

Multicast Extended Capability Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + C04h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/O	**MC ECRC Regeneration Support (MCECRCRS):** If set, indicates that ECRC regeneration is supported
14	0h RO	**Reserved**
13:8	00h RO	**MC Window Size Request (MCWSR):** This field is reserved in Switch and Root Port. For Endpoint, the log2 of the Multicast Window Size is requested
7:6	0h RO	**Reserved**
5:0	00h RW/O	**MC Max Group (MCMG):** Indicates the maximum number of Multicast Groups that the component supports, encoded as M-1. A value of 00h indicates that one Multicast Group is supported.

5.156 Multicast Control (MCCTLR) — Offset C06h

Multicast Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + C06h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MC Enabled (MCE):** When set, Multicast Capability is enabled for the port
14:6	0h RO	**Reserved**
5:0	00h RW	**MC Number Group (MCNG):** Indicates the number of multicast groups configured for use, encoded as N-1. THe default value of 00h indicates that one Multicast Group is configured for use. Behavior is undefined if value exceeds MCAPR.MCMG

5.157 Multicast Base Address Register 1 (MCBADRR1) — Offset C08h

Multicast Base Address Register 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**MC Base Address Lower (MCBADRL):** The base address (Lower) of the Multicast address range. The behavior is undefined if MC Enable is set and bits in this field corresponding to address bits that contain the Multicast Group number or address bits less than MC Index Position are non-zero
11:6	0h RO	**Reserved**
5:0	00h RW	**MC Index Position (MCIP):** The location of the LSB of the Multicast Group Number within the address. Behavior is undefined if this value is less than 12 and MC Enable is set

5.158 Multicast Base Address Register 2 (MCBADRR2) — Offset C0Ch

Multicast Base Address Register 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C0Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MC Base Address Higher (MCBADRH):** The base address (Higher) of the Multicast address range. The behavior is undefined if MC Enable is set and bits in this field corresponding to address bits that contain the Multicast Group number or address bits less than MC Index Position are non-zero

5.159 Multicast Receive (MCRR) — Offset C10h

Multicast Receive Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MC Receive (MCRR):** For each bit that is set, this function gets a copy of any Multicast TLPs for the associated Multicast Group. Bits above MC Num Group are ignored by hardware

5.160 Multicast Block All (MCBAR) — Offset C18h

Multicast Block All Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MC Block All (MCBA):** For each bit that is set, this function is blocked from sending TLPs to the associated Multicast Group. Bits above MC Num Group are ignored by hardware

5.161 Multicast Block Untranslated (MCBUR) — Offset C20h

Multicast Block Untranslated Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MC Block Untranslated (MBU):** For each bit that is set, this function is blocked from sending TLPs containing Untranslated Addresses to the associated Multicast Group. Bits above MC Num Group are ignored by hardware.

5.162 Multicast Overlay BAR 1 (MCOB1) — Offset C28h

Multicast Overlay BAR 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**MC Overlay BAR Lower (MCOBL):** Specifies the Base Address (Lower) of the window onto which MC TLPs passes through this function will be overlaid
5:0	00h RW	**MC Overlay Size (MCOS):** For 6 or greater, specifies the size in Bytes of the overlay aperture as a power of 2. If less than 6, disables the overlay mechanism

5.163 Multicast Overlay BAR 2 (MCOB2) — Offset C2Ch

Multicast Overlay BAR 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MC Overlay BAR Higher (MCOBH):** Specifies the Base Address (Higher) of the window onto which MC TLPs passes through this function will be overlaid

5.164 VNN Removal Control (VNNREMCTL) — Offset C70h

VNN Removal Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C70h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Receiver Eye Margin Error Tracking Mechanism Disable (REMETMD):** When this bit is set MAC will not track Error count during Receiver Equalization (EQ Phase 2 - PDMI, EQ Phase 3 - PCIe). Preset/Coeff evaluation will be based on FOM returned by PHY alone. This bit must be configured before training to GEN3 data rate.
30:9	0h RO	**Reserved**
8	0h RW	**Function Disable VNN Removal (FDVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link is function disable, so that VNN is allow to be remove when platform permitted.
7	0h RW	**Hot Plug VNN Removal Enable (HPVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when clkreq_b deassetion in Detect state, so that VNN is allow to be remove when platform permitted.
6	0h RW	**Detect Not PCIe VNN Removal Enable (DNPVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering Detect Not PCIe when link is unown, so that VNN is allow to be remove when platform permitted.
5	0h RW	**RTD3 VNN Removal Enable (RTD3VNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering L23 due to RTD3, so that VNN is allow to be remove when platform permitted.
4	0h RW	**Link Disable VNN Removal Enable (LDVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering Link Disable, so that VNN is allow to be remove when platform permitted.
3:2	0h RW	**Internal States Propagation Latency For VNN Removal Exit (ISPLFVNNRE):** This register configure internal delay of IP to allow boundary lock to deassert. This counter will start count after contexts propagation is done and early boundary lock is deassert. 00 8 osc clocks 01 16 osc clocks 10 32 osc clocks 11 64 osc clocks Note: For each x4 instance, only the value from Port 1 is used. This is a per controller register
1:0	1h RW	**Link Reset Suppression Latency For VNN Removal Exit (LRSLFVNNRE):** This register configure the Link Reset Suppression latency after pmc had deassert restore_b during VNN Removal, and link clock pll had achieved lock. Link reset will be suppress upon IP Inaccessible exit with restore_b assertion, and the counter will start count when restore_b deassert with link clock had achieved lock. After timer expire, link reset will be deassert. 00 4 osc clocks 01 8 osc clocks 10 16 osc clocks 11 32 osc clocks Note: For each x4 instance, only the value from Port 1 is used. This is a per controller register

5.165 VNN Removal Save And Restore Hardware Contexts 1 (VNNRSNRC1) — Offset C74h

VNN Removal Save And Restore Hardware Contexts 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + C74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Spare 31 State Contexts (VNNS31SC):** Spare Flag for VNN Removal
30	0h RW	**VNN Spare 30 State Contexts (VNNS30SC):** Spare Flag for VNN Removal
29	0h RW	**VNN Spare 29 State Contexts (VNNS29SC):** Spare Flag for VNN Removal
28	0h RW	**VNN Spare 28 State Contexts (VNNS28SC):** Spare Flag for VNN Removal
27	0h RW	**VNN Spare 27 State Contexts (VNNS27SC):** Spare Flag for VNN Removal
26	0h RW	**VNN Spare 26 State Contexts (VNNS26SC):** Spare Flag for VNN Removal
25	0h RW	**VNN Spare 25 State Contexts (VNNS25SC):** Spare Flag for VNN Removal
24	0h RW	**VNN Spare 24 State Contexts (VNNS24SC):** Spare Flag for VNN Removal
23	0h RW	**VNN Spare 23 State Contexts (VNNS23SC):** Spare Flag for VNN Removal
22	0h RW	**VNN Spare 22 State Contexts (VNNS22SC):** Spare Flag for VNN Removal
21	0h RW	**VNN Spare 21 State Contexts (VNNS21SC):** Spare Flag for VNN Removal
20	0h RW	**VNN Spare 20 State Contexts (VNNS20SC):** Present Detect State Flag (PDS) information stored to this flag, so that link will restore back PDS upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
19	0h RW	**VNN Spare 19 State Contexts (VNNS19SC):** Spare Flag for VNN Removal
18	0h RW	**VNN Spare 18 State Contexts (VNNS18SC):** Spare Flag for VNN Removal
17	0h RW	**VNN Spare 17 State Contexts (VNNS17SC):** Spare Flag for VNN Removal
16	0h RW	**VNN Spare 16 State Contexts (VNNS16SC):** Spare Flag for VNN Removal

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**VNN Spare 15 State Contexts (VNNS15SC):** Spare Flag for VNN Removal
14	0h RW	**VNN Spare 14 State Contexts (VNNS14SC):** Spare Flag for VNN Removal
13	0h RW	**VNN Spare 13 State Contexts (VNNS13SC):** Spare Flag for VNN Removal
12	0h RW	**VNN Spare 12 State Contexts (VNNS12SC):** Spare Flag for VNN Removal
11	0h RW	**VNN Spare 11 State Contexts (VNNS11SC):** Spare Flag for VNN Removal
10	0h RW	**VNN Spare 10 State Contexts (VNNS10SC):** Spare Flag for VNN Removal
9	0h RW	**VNN Spare 9 State Contexts (VNNS9SC):** Spare Flag for VNN Removal
8	0h RW	**VNN Spare 8 State Contexts (VNNS8SC):** Spare Flag for VNN Removal
7	0h RW	**VNN Spare 7 State Contexts (VNNS7SC):** Spare Flag for VNN Removal
6	0h RW	**VNN Spare 6 State Contexts (VNNS6SC):** Spare Flag for VNN Removal
5	0h RW	**VNN Spare 5 State Contexts (VNNS5SC):** Link Down indicaton will be reflected here.
4	0h RW	**VNN Spare 4 State Contexts (VNNS4SC):** DL_ACTIVE (LA) information stored to this flag, so that link will restore back LA upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
3	0h RW	**VNN Spare 3 State Contexts (VNNS3SC):** Legacy Present Detect State Flag (PDS) information stored to this flag, so that link will restore back Legacy PDS Flag upon VNN Removal restoration. Based on PCIEALC.PDSP, this information or New PDS Implementation Context[20] will be selected. Writing to this registers have no effect unless restore_b is assert. Legacy Present Detect State Flag (PDS) information stored to this flag, so that link will restore back Legacy PDS Flag upon VNN Removal restoration. Based on PCIEALC.PDSP, this information or New PDS Implementation Context[20] will be selected. Writing to this registers have no effect unless restore_b is assert.
2	0h RW	**VNN Detect Not PCIe State Contexts (VNNDNPSC):** When Link entered Detect Not PCIe state, LTSSM will push the link Detect Not PCIe state information to this flag, so that link will restore back to Detect Not PCIe state behavior upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
1	0h RW	**VNN L23 State Contexts (VNNL23SC):** When Link entered L23 state, LTSSM will push the link L23 state information to this flag, so that link will restore back to L23 state behavior (Actual State restore to Detect Quiet PG) upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
0	0h RW	**VNN Link Disable State Contexts (VNNLDSC):** When Link entered Link Disable state, LTSSM will push the link disable state information to this flag, so that link will restore back to disable state behavior (Actual State restore to Detect Quiet PG) upon VNN Removal restoration.

5.166 Physical Layer 16.0 GT/s Margining Extended Capability Header (PL16MECH) — Offset EDCh

Physical Layer 16.0 GT/s Margining Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + EDCh	00010027h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.
19:16	1h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0027h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Physical Layer 16.0 GT/s Margining Capability

5.167 Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status Byte 0 & 1 (PL16MPCPSB01) — Offset EE0h

Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status Byte 0 & 1.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + EE0h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/O	**Margining uses Driver Software (MARGINDRISW):** If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. In this case the value read from Margining Software Ready is undefined

5.168 Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status Byte 2 & 3 (PL16MPCPSB23) — Offset EE2h

Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status Byte 2 & 3.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:1, F:0] + EE2h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO/V	**Margining Software Ready (MARGINSWRDY):** When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear.
0	0h RO/V	**Margining Ready (MARGINRDY):** Indicates when the Margining feature is ready to accept margining commands. Behavior is undefined if this bit is Clear and, for any Lane, any of the Receiver Number, Margin Type, Usage Model, or Margin Payload fields are written. If Margining uses Driver Software is Set, Margining Ready must be Set no later than 100 ms after the later of Margining Software Ready becoming Set or the link training to 16.0 GT/s. If Margining uses Driver Software is Clear, Margining Ready must be Set no later than 100 ms after the Link trains to 16.0 GT/s.

5.169 Physical Layer 16.0 GT/s Lane0 Margin Control and Status (PL16L0MCS) — Offset EE4h

Physical Layer 16.0 GT/s Lane0 Margin Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:1, F:0] + EE4h	00009C38h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO/V	**Margin Payload Status (MPSTS):** This field is only meaningful, when the Margin Type This field must be reset to the default value if the Port goes to DL_Down status.
23	0h RO	**Reserved**
22	0h RO/V	**Usage Model Status (UMS):** This field must be reset to the default value if the Port goes to DL_Down status.
21:19	0h RO/V	**Margin Type Status (MTS):** This field must be reset to the default value if the Port goes to DL_Down status.
18:16	0h RO/V	**Receiver Number Status (RNS):** This field must be reset to the default value if the Port goes to DL_Down status.
15:8	9Ch RW	**Margin Payload (MP):** This fields value is used in conjunction with the Margin Type field. The default value is 9Ch. This field must be reset to the default value if the Port goes to DL_Down status.
7	0h RO	**Reserved**
6	0h RW	**Usage Model (UM):** The default value is 0b. This field must be reset to the default value if the Port goes to DL_Down status.
5:3	7h RW	**Margin Type (MT):** The default value is 111b. This field must be reset to the default value if the Port goes to DL_Down status.
2:0	0h RW	**Receiver Number (RN):** The default value is 000b. This field must be reset to the default value if the Port goes to DL_Down status.

5.170 Physical Layer 16.0 GT/s Lane1 Margin Control and Status (PL16L1MCS) — Offset EE8h

Physical Layer 16.0 GT/s Lane1 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.171 Physical Layer 16.0 GT/s Lane2 Margin Control and Status (PL16L2MCS) — Offset EECh

Physical Layer 16.0 GT/s Lane2 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.172 Physical Layer 16.0 GT/s Lane3 Margin Control and Status (PL16L3MCS) — Offset EF0h

Physical Layer 16.0 GT/s Lane3 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.173 Physical Layer 16.0 GT/s Lane4 Margin Control and Status (PL16L4MCS) — Offset EF4h

Physical Layer 16.0 GT/s Lane4 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.174 Physical Layer 16.0 GT/s Lane5 Margin Control and Status (PL16L5MCS) — Offset EF8h

Physical Layer 16.0 GT/s Lane5 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.175 Physical Layer 16.0 GT/s Lane6 Margin Control and Status (PL16L6MCS) — Offset EFCh

Physical Layer 16.0 GT/s Lane6 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.176 Physical Layer 16.0 GT/s Lane7 Margin Control and Status (PL16L7MCS) — Offset F00h

Physical Layer 16.0 GT/s Lane7 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.177 Physical Layer 16.0 GT/s Lane8 Margin Control and Status (PL16L8MCS) — Offset F04h

Physical Layer 16.0 GT/s Lane8 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.178 Physical Layer 16.0 GT/s Lane9 Margin Control and Status (PL16L9MCS) — Offset F08h

Physical Layer 16.0 GT/s Lane9 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.179 Physical Layer 16.0 GT/s Lane10 Margin Control and Status (PL16L10MCS) — Offset F0Ch

Physical Layer 16.0 GT/s Lane10 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.180 Physical Layer 16.0 GT/s Lane11 Margin Control and Status (PL16L11MCS) — Offset F10h

Physical Layer 16.0 GT/s Lane11 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.181 Physical Layer 16.0 GT/s Lane12 Margin Control and Status (PL16L12MCS) — Offset F14h

Physical Layer 16.0 GT/s Lane12 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.182 Physical Layer 16.0 GT/s Lane13 Margin Control and Status (PL16L13MCS) — Offset F18h

Physical Layer 16.0 GT/s Lane13 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.183 Physical Layer 16.0 GT/s Lane14 Margin Control and Status (PL16L14MCS) — Offset F1Ch

Physical Layer 16.0 GT/s Lane14 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

5.184 Physical Layer 16.0 GT/s Lane15 Margin Control and Status (PL16L15MCS) — Offset F20h

Physical Layer 16.0 GT/s Lane15 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6 PCI Express* Controller Registers (D6:F0)

This chapter documents the registers of the processor PCIe Gen4 Controller device (x4).

Table 6-1. Summary of Bus: 0, Device: 6, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Identifiers (ID)	00008086h
4h	2	Device Command (CMD)	0000h
6h	2	Primary Status (PSTS)	0010h
8h	4	Revision ID (RID_CC)	060400F0h
Ch	1	Cache Line Size (CLS)	00h
Dh	1	Primary Latency Timer (PLT)	00h
Eh	1	Header Type (HTYPE)	81h
18h	4	Bus Numbers (BNUM_SLT)	00000000h
1Ch	2	I/O Base And Limit (IOBL)	0000h
1Eh	2	Secondary Status (SSTS)	0000h
20h	4	Memory Base And Limit (MBL)	00000000h
24h	4	Prefetchable Memory Base And Limit (PMBL)	00010001h
28h	4	Prefetchable Memory Base Upper 32 Bits (PMBU32)	00000000h
2Ch	4	Prefetchable Memory Limit Upper 32 Bits (PMLU32)	00000000h
34h	1	Capabilities List Pointer (CAPP)	40h
3Ch	2	Interrupt Information (INTR)	0100h
3Eh	2	Bridge Control (BCTRL)	0000h
40h	2	Capabilities List (CLIST)	8010h
42h	2	PCI Express Capabilities (XCAP)	0042h
44h	4	Device Capabilities (DCAP)	00008001h
48h	2	Device Control (DCTL)	0020h
4Ah	2	Device Status (DSTS)	0010h
4Ch	4	Link Capabilities (LCAP)	01714C10h
50h	2	Link Control (LCTL)	0000h
52h	2	Link Status (LSTS)	1011h
54h	4	Slot Capabilities (SLCAP)	00040060h
58h	2	Slot Control (SLCTL)	0000h
5Ah	2	Slot Status (SLSTS)	0000h
5Ch	2	Root Control (RCTL)	0000h
60h	4	Root Status (RSTS)	00000000h
64h	4	Device Capabilities 2 (DCAP2)	00080837h
68h	2	Device Control 2 (DCTL2)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6Ah	2	Device Status 2 (DSTS2)	0000h
6Ch	4	Link Capabilities 2 (LCAP2)	0000000Eh
70h	2	Link Control 2 (LCTL2)	0001h
72h	2	Link Status 2 (LSTS2)	0000h
74h	4	Slot Capabilities 2 (SLCAP2)	00000000h
78h	2	Slot Control 2 (SLCTL2)	0000h
7Ah	2	Slot Status 2 (SLSTS2)	0000h
80h	2	Message Signaled Interrupt Identifiers (MID)	9005h
82h	2	Message Signaled Interrupt Message (MC)	0000h
84h	4	Message Signaled Interrupt Message Address (MA)	00000000h
88h	2	Message Signaled Interrupt Message Data (MD)	0000h
90h	2	Subsystem Vendor Capability (SVCAP)	A00Dh
94h	4	Subsystem Vendor IDs (SVID)	00000000h
A0h	2	Power Management Capability (PMCAP)	0001h
A2h	2	PCI Power Management Capabilities (PMC)	C803h
A4h	4	PCI Power Management Control (PMCS)	00000008h
100h	4	Advanced Error Extended (AECH)	00000000h
104h	4	Uncorrectable Error Status (UES)	00000000h
108h	4	Uncorrectable Error Mask (UEM)	00000000h
10Ch	4	Uncorrectable Error Severity (UEV)	00060010h
110h	4	Correctable Error Status (CES)	00000000h
114h	4	Correctable Error Mask (CEM)	00002000h
118h	4	Advanced Error Capabilities And Control (AECC)	00000000h
11Ch	4	Header Log (HL_DW1)	00000000h
120h	4	Header Log (HL_DW2)	00000000h
124h	4	Header Log (HL_DW3)	00000000h
128h	4	Header Log (HL_DW4)	00000000h
12Ch	4	Root Error Command (REC)	00000000h
130h	4	Root Error Status (RES)	00000000h
134h	4	Error Source Identification (ESID)	00000000h
150h	4	PTM Extended Capability Header (PTMECH)	00000000h
154h	4	PTM Capability (PTMCAPR)	00000400h
158h	4	PTM Control (PTMCTLR)	00000000h
200h	4	L1 Sub-States Extended Capability Header (L1SECH)	00000000h
204h	4	L1 Sub-States Capabilities (L1SCAP)	0028281Fh
208h	4	L1 Sub-States Control 1 (L1SCTL1)	00000000h
20Ch	4	L1 Sub-States Control 2 (L1SCTL2)	00000028h
220h	4	ACS Extended Capability Header (ACSECH)	00000000h
224h	2	ACS Capability (ACSCAPR)	001Fh
226h	2	ACS Control (ACSCTLR)	0000h
284h	4	Port VC Capability Register 1 (PVCCR1)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
288h	4	Port VC Capability 2 (PVCC2)	00000000h
28Ch	2	Port VC Control (PVCC)	0000h
28Eh	2	Port VC Status (PVCS)	0000h
290h	4	Virtual Channel 0 Resource Capability (V0VCRC)	00000000h
294h	4	Virtual Channel 0 Resource Control (V0CTL)	80000001h
29Ah	2	Virtual Channel 0 Resource Status (V0STS)	0000h
29Ch	4	Virtual Channel 1 Resource Capability (V1VCRC)	00000000h
2A0h	4	Virtual Channel 1 Resource Control (V1CTL)	00000000h
2A6h	2	Virtual Channel 1 Resource Status (V1STS)	0000h
A00h	4	DPC Extended Capability Header (DPCECH)	00000000h
A04h	2	DPC Capability (DPCCAPR)	14E0h
A06h	2	DPC Control (DPCCTLR)	0000h
A08h	2	DPC Status (DPCSR)	1F00h
A0Ah	2	DPC Error Source ID (DPCESIDR)	0000h
A0Ch	4	RP PIO Status (RPPIOSR)	00000000h
A10h	4	RP PIO Mask (RPPIOMR)	00070707h
A14h	4	RP PIO Severity (RPPIOVR)	00000000h
A18h	4	RP PIO SysError (RPPIOSER)	00000000h
A1Ch	4	RP PIO Exception (RPPIOER)	00000000h
A20h	4	RP PIO Header Log DW1 (RPPIOHLR_DW1)	00000000h
A24h	4	RP PIO Header Log DW2 (RPPIOHLR_DW2)	00000000h
A28h	4	RP PIO Header Log DW3 (RPPIOHLR_DW3)	00000000h
A2Ch	4	RP PIO Header Log DW4 (RPPIOHLR_DW4)	00000000h
A30h	4	Secondary PCI Express Extended Capability Header (SPEECH)	00000000h
A34h	4	Link Control 3 (LCTL3)	00000000h
A38h	4	Lane Error Status (LES)	00000000h
A3Ch	4	Lane 0 And Lane 1 Equalization Control (L01EC)	7F7F7F7Fh
A40h	4	Lane 2 And Lane 3 Equalization Control (L23EC)	7F7F7F7Fh
A44h	4	Lane 4 And Lane 5 Equalization Control (L45EC)	7F7F7F7Fh
A48h	4	Lane 6 And Lane 7 Equalization Control (L67EC)	7F7F7F7Fh
A4Ch	4	Lane 8 And Lane 9 Equalization Control (L89EC)	7F7F7F7Fh
A50h	4	Lane 10 And Lane 11 Equalization Control (L1011EC)	7F7F7F7Fh
A54h	4	Lane 12 And Lane 13 Equalization Control (L1213EC)	7F7F7F7Fh
A58h	4	Lane 14 And Lane 15 Equalization Control (L1415EC)	7F7F7F7Fh
A90h	4	Data Link Feature Extended Capability Header (DLFECH)	00000000h
A94h	4	Data Link Feature Capabilities (DLFCAP)	80000000h
A98h	4	Data Link Feature Status (DLFSTS)	00000000h
A9Ch	4	Physical Layer 16.0 GT/s Extended Capability Header (PL16GECH)	00000000h
AA0h	4	Physical Layer 16.0 GT/s Capability (PL16CAP)	00000000h
AA4h	4	Physical Layer 16.0 GT/s Control (PL16CTL)	00000000h
AA8h	4	Physical Layer 16.0 GT/s Status (PL16S)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
AACh	4	Physical Layer 16.0 GT/s Local Data Parity Mismatch Status (PL16LDPMS)	00000000h
AB0h	4	Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status (PL16FRDPMS)	00000000h
AB4h	4	Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status (PL16SRDPMS)	00000000h
AB8h	4	Physical Layer 16.0 GT/s Extra Status (PL16ES)	00000000h
ABCh	2	Physical Layer 16.0 GT/s Lane 01 Equalization Control (PL16L01EC)	FFFFh
ABEh	2	Physical Layer 16.0 GT/s Lane 23 Equalization Control (PL16L23EC)	FFFFh
AC0h	2	Physical Layer 16.0 GT/s Lane 45 Equalization Control (PL16L45EC)	FFFFh
AC2h	2	Physical Layer 16.0 GT/s Lane 67 Equalization Control (PL16L67EC)	FFFFh
AC4h	2	Physical Layer 16.0 GT/s Lane 89 Equalization Control (PL16L89EC)	FFFFh
AC6h	2	Physical Layer 16.0 GT/s Lane 1011 Equalization Control (PL16L1011EC)	FFFFh
AC8h	2	Physical Layer 16.0 GT/s Lane 1213 Equalization Control (PL16L1213EC)	FFFFh
ACAh	2	Physical Layer 16.0 GT/s Lane 1415 Equalization Control (PL16L1415EC)	FFFFh
C70h	4	VNN Removal Control (VNNREMCTL)	00000001h
C74h	4	VNN Removal Save And Restore Hardware Contexts 1 (VNNRSNRC1)	00000000h
EDCh	4	Physical Layer 16.0 GT/s Margining Extended Capability Header (PL16MECH)	00010027h
EE0h	4	Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status (PL16MPCPS)	00000000h
EE4h	4	Physical Layer 16.0 GT/s Lane0 Margin Control and Status (PL16L0MCS)	00009C38h
EE8h	4	Physical Layer 16.0 GT/s Lane1 Margin Control and Status (PL16L1MCS)	00009C38h
EECh	4	Physical Layer 16.0 GT/s Lane2 Margin Control and Status (PL16L2MCS)	00009C38h
EF0h	4	Physical Layer 16.0 GT/s Lane3 Margin Control and Status (PL16L3MCS)	00009C38h
EF4h	4	Physical Layer 16.0 GT/s Lane4 Margin Control and Status (PL16L4MCS)	00009C38h
EF8h	4	Physical Layer 16.0 GT/s Lane5 Margin Control and Status (PL16L5MCS)	00009C38h
EFCh	4	Physical Layer 16.0 GT/s Lane6 Margin Control and Status (PL16L6MCS)	00009C38h
F00h	4	Physical Layer 16.0 GT/s Lane7 Margin Control and Status (PL16L7MCS)	00009C38h
F04h	4	Physical Layer 16.0 GT/s Lane8 Margin Control and Status (PL16L8MCS)	00009C38h
F08h	4	Physical Layer 16.0 GT/s Lane9 Margin Control and Status (PL16L9MCS)	00009C38h
F0Ch	4	Physical Layer 16.0 GT/s Lane10 Margin Control and Status (PL16L10MCS)	00009C38h
F10h	4	Physical Layer 16.0 GT/s Lane11 Margin Control and Status (PL16L11MCS)	00009C38h
F14h	4	Physical Layer 16.0 GT/s Lane12 Margin Control and Status (PL16L12MCS)	00009C38h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F18h	4	Physical Layer 16.0 GT/s Lane13 Margin Control and Status (PL16L13MCS)	00009C38h
F1Ch	4	Physical Layer 16.0 GT/s Lane14 Margin Control and Status (PL16L14MCS)	00009C38h
F20h	4	Physical Layer 16.0 GT/s Lane15 Margin Control and Status (PL16L15MCS)	00009C38h

6.1 Device Identifiers (ID) — Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Device Identification (DID):** See the Device ID table in the first volume of this document.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel.

6.2 Device Command (CMD) — Offset 4h

Device Command

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** This field is reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** This field is reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** This field is reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** This field is reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** This field is reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone.

6.3 Primary Status (PSTS) — Offset 6h

Primary Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCMD.PERE is not set.
14	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
13	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
12	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
11	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	0h RO	**Primary DEVSEL# Timing Status (PDTS):** This field is reserved per PCI-Express spec
8	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and PCMD.PERE is set.
7	0h RO	**Primary Fast Back to Back Capable (PFBC):** This field is reserved per PCI-Express spec.
6	0h RO	**Reserved**
5	0h RO	**Primary 66 MHz Capable (PC66):** This field is reserved per PCI-Express spec.
4	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
3	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
2:0	0h RO	**Reserved**

6.4 Revision ID (RID_CC) — Offset 8h

Revision ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 8h	060400F0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	04h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a 1 for a Host Bridge, this register reads 00h.
15:8	00h RO/V	**Programming Interface (PI):** PCI-to-PCI bridge.
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

6.5 Cache Line Size (CLS) — Offset Ch

Cache Line Size

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:6, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

6.6 Primary Latency Timer (PLT) — Offset Dh

Primary Latency Timer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:6, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Latency Count (CT):** This field is reserved per PCI-Express spec
2:0	0h RO	**Reserved**

6.7 Header Type (HTYPE) — Offset Eh

Header Type

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:6, F:0] + Eh	81h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-function Device (MFD):** This bit is 1 to indicate a multi-function device.
6:0	01h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a 1 for a Host Bridge, this register reads 00h.

6.8 Bus Numbers (BNUM_SLT) — Offset 18h

Bus Numbers

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is a RW register - else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	00h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	00h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	00h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

6.9 I/O Base And Limit (IOBL) — Offset 1Ch

I/O Base And Limit

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 1Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

6.10 Secondary Status (SSTS) — Offset 1Eh

Secondary Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 1Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
14	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
13	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with Unsupported Request status from the device.
12	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with Completion Abort status from the device.
11	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with Completion Abort status to the device.
10:9	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** This field is reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
8	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
7	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** This field is reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
6	0h RO	**Reserved**
5	0h RO	**Secondary 66 MHz Capable (SC66):** This field is reserved per PCI Express spec
4:0	0h RO	**Reserved**

6.11 Memory Base And Limit (MBL) — Offset 20h

Memory Base And Limit

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved**
15:4	000h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved**

6.12 Prefetchable Memory Base And Limit (PMBL) — Offset 24h

Prefetchable Memory Base And Limit

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 24h	00010001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	000h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

6.13 Prefetchable Memory Base Upper 32 Bits (PMBU32) — Offset 28h

Prefetchable Memory Base Upper 32 Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

6.14 Prefetchable Memory Limit Upper 32 Bits (PMLU32) — Offset 2Ch

Prefetchable Memory Limit Upper 32 Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

6.15 Capabilities List Pointer (CAPP) — Offset 34h

Capabilities List Pointer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:6, F:0] + 34h	40h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Capability Linked List (Default Settings)** Offset | Capability | Next Pointer 40h | PCI Express | 80h 80h | Message Signaled Interrupt (MSI) | 90h 90h | Subsystem Vendor | A0h A0h | PCI Power Management | 00h **Extended PCIe Capability Linked List** Offset | Capability | Next Pointer 100h | Advanced Error Reporting | 000h 140h | Access Control Services | 000h 200h | L1 Sub-states | 000h 220h | Secondary PCI Express Capability | 000h

6.16 Interrupt Information (INTR) — Offset 3Ch

Interrupt Information

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 3Ch	0100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG.PxIP field: Port Bits[15:12] Bits[11:08] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP ... X 0h STRPFUSECFG.PxIP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

6.17 Bridge Control (BCTRL) — Offset 3Eh

Bridge Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 3Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**Discard Timer Status (DTS):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
9	0h RW/V2	**Secondary Discard Timer (SDT):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
8	0h RW/V2	**Primary Discard Timer (PDT):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
7	0h RO	**Fast Back to Back Enable (FBE):** This field is reserved per PCI-Express spec.
6	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
5	0h RW/V2	**Master Abort Mode (MAM):** This field is reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
4	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
3	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h - 3BBh and 3C0h - 3DFh, and all aliases of bits 15:10 in any combination of 1's
2	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
1	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
0	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.

6.18 Capabilities List (CLIST) — Offset 40h

Capabilities List

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 40h	8010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

6.19 PCI Express Capabilities (XCAP) — Offset 42h

PCI Express Capabilities

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 42h	0042h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:9	00h RO	**Interrupt Message Number (IMN):** The Root Port does not have multiple MSI interrupt numbers.
8	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
3:0	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 and 3.0 specification which incorporates the Register Expansion ECN.

6.20 Device Capabilities (DCAP) — Offset 44h

Device Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 44h	00008001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported.
25:18	00h RO	**Captured Slot Power Limit Value (CSPV):** Not supported.
17:16	0h RO	**Reserved**
15	1h RO	**Role Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:12	0h RO	**Reserved**
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** This field is reserved for root ports.
8:6	0h RO	**Endpoint L0s Acceptable Latency (E0AL):** This field is reserved for root ports.
5	0h RW/O	**Extended Tag Field Supported (ETFS):** The Root Port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported

Bit Range	Default & Access	Field Name (ID): Description
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

6.21 Device Control (DCTL) — Offset 48h

Device Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 48h	0020h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** Must be RW for OS testing. The OS will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
7:5	1h RW	**Max Payload Size (MPS):** The root port supports up to 256B max payload. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

6.22 Device Status (DSTS) — Offset 4Ah

Device Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 4Ah	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
4	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
3	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
2	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed TLP
1	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout
0	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

6.23 Link Capabilities (LCAP) — Offset 4Ch

Link Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 4Ch	01714C10h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	01h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port# Value of PN field 1 01h 2 02h 3 03h : : X 0Xh Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
23	0h RO	**Reserved**
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to 0 to indicate the Root Port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** 0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b: Less than 1 us 001b: 1 us to less than 2 us 010b: 2 us to less than 4 us 011b: 4 us to less than 8 us 100b: 8 us to less than 16 us 101b: 16 us to less than 32 us 110b: 32 us to 64 us 111b: More than 64 us Note: If power management (e.g PLL shutdown) is enabled, BIOS should program this latency to comprehend PLL lock latency.

Bit Range	Default & Access	Field Name (ID): Description
14:12	4h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00b: No ASPM Support 01b: L0s Supported 10b: L1 Supported 11b: L0s and L1 Supported
9:4	01h RO/V	**Maximum Link Width (MLW):** Indicates the maximum link width of the link 0x1: x1 Link Width 0x2: x2 Link Width 0x4: x4 Link Width 0x8: x8 Link Width 0x10: x16 Link Width
3:0	0h RO/V	**Max Link Speed (MLS):** This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This field reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through PCI Express Speed Limit setting or MPC.PCIESD register. This field reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through PCI Express Speed Limit setting or MPC.PCIESD register. Otherwise, this field reports a value of 0011b.

6.24 Link Control (LCTL) — Offset 50h

Link Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 50h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets. Default value of this bit is 0b.
8	0h RO	**Enable Clock Power Management (ECPM):** Not supported on Root Ports.
7	0h RW	**Extended Sync (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the Root Port and device are operating with a distributed common reference clock.
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns 0 when read. Software uses LSTS.LT and LSTS.LTE to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is 1, hardware will always see 00 as an output from this register. BIOS reading this register should always return the correct value.

6.25 Link Status (LSTS) — Offset 52h

Link Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 52h	1011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
14	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
13	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.

Bit Range	Default & Access	Field Name (ID): Description
12	1h RO/V	**Slot Clock Configuration (SCC):** In normal mode, Root Port uses the same reference clock as on the platform and does not generate its own clock. Note: When operating in PCI Express mode, the default of this register bit is dependent on the PCIe Non-Common Clock With SSC Mode Enable Strap. If the strap enables non-common clock with SSC support, this bit shall default to 0. Otherwise, this bit shall default to 1.
11	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
10	0h RO	**Reserved**
9:4	01h RO/V	**Negotiated Link Width (NLW):** Negotiated link width. 0x1: x1 Link Width 0x2: x2 Link Width 0x4: x4 Link Width 0x8: x8 Link Width 0x10: x16 Link Width The value of this register is undefined if the link has not successfully trained.
3:0	1h RO/V	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.

6.26 Slot Capabilities (SLCAP) — Offset 54h

Slot Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 54h	00040060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1h RO	**No Command Completed Support (NCCS):** Set to 1 as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	00h RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

6.27 Slot Control (SLCTL) — Offset 58h

Slot Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 58h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13	0h RW	**Auto Slot Power Limit Disable (ASPLD):** When set, this bit disables automatic sending of Set_Slot_Power_Limit message when the link transitions from non-DL_Up status to DL_Up status.
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed.
11	0h RO	**Electromechanical Interlock Control (EMIC):** This port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller.
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller.
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller.
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller.
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller.
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller.

6.28 Slot Status (SLSTS) — Offset 5Ah

Slot Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 5Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
7	0h RO	**Electromechanical Interlock Status (EMIS):** This port does not support and electromechanical interlock.
6	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected (1) or empty (0). If XCAP.SI is cleared, this bit is a 1.
5	0h RO	**MRL Sensor State (MS):** MRL sensor is not implemented.
4	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller.
3	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the PD bit changes state.
2	0h RO	**MRL Sensor Changed (MSC):** MRL sensor is not implemented.
1	0h RO	**Power Fault Detected (PFD):** Power controller is not implemented.
0	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button.

6.29 Root Control (RCTL) — Offset 5Ch

Root Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 5Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

6.30 Root Status (RSTS) — Offset 60h

Root Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requester ID will be updated, and this bit will be cleared. Root Ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requester ID in RID. Subsequent PMEs are kept pending until this bit is cleared.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**PME Requester ID (RID):** Indicates the PCI requester ID of the last PME requester. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

6.31 Device Capabilities 2 (DCAP2) — Offset 64h

Device Capabilities 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 64h	00080837h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b: OBFF is not supported. 01b: OBFF is supported using Message signaling only. 10b: OBFF is supported using WAKE# signaling only. 11b: OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. Note: OBFF is not supported. BIOS should program this field to 00b.
17	0h RW/O	**10-Bit Tag Requester Supported (PX10BTRS):** If this bit is Set, the Function supports 10-Bit Tag Requester capability - otherwise, the Function does not. This bit must not be Set if the 10-Bit Tag Completer Supported bit is Clear.
16	0h RW/O	**10-Bit Tag Completer Supported (PX10BTCS):** If this bit is Set, the Function supports 10-Bit Tag Completer capability - otherwise, the Function does not.
15:12	0h RO	**Reserved**
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a 1 or a 0 to enable/disable the root port from declaring support for the LTR capability.
10	0h RO	**Reserved**
9	0h RW/O	**CAS Completer 128-bit Supported (AC128BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/O	**AtomicOp Completer 64-bit Supported (AC64BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability
7	0h RW/O	**AtomicOp Completer 32-bit Supported (AC32BS):** Applicable to Functions with Memory Space BARs as well as all Root Ports - must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability
6	0h RW/O	**Atomic Routing Supported (ARS):** This bit must be set to 1b if the Port supports this optional capability
5	1h RO	**ARI Forwarding Supported (AFS):** Applicable only to Switch Downstream Ports and Root Ports - must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this bit 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A & B 0110b Ranges B & C 0111b Ranges A, B & C <-- This is what Root Port supports 1110b Ranges B, C & D 1111b Ranges A, B, C & D All other values are reserved.

6.32 Device Control 2 (DCTL2) — Offset 68h

Device Control 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 68h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** Optimized Buffer Flush/Fill Enable (OBFFEN): 00b: Disable OBFF mechanism. 01b: Enable OBFF mechanism using Message signaling (Variation A). 10b: Enable OBFF mechanism using Message signaling (Variation B). 11b: Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12	0h RW/V2	**10-Bit Tag Requester Enable (PX10BTRE):** This bit, in combination with the Extended Tag Field Enable bit in the Device Control register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is Set, the Requester is permitted to use 10-Bit Tags. Software should not change the value of this bit while the Function has outstanding Non-Posted Requests - otherwise, the result is undefined. Functions that do not implement 10-Bit Tag Requester capability must hardwire this bit to 0b.
11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:8	0h RO	**Reserved**
7	0h RW	**AtomicOp Egress Blocking (AEB):** Applicable and mandatory for Switch Upstream Ports, Switch Downstream Ports, and Root Ports that implement AtomicOp routing capability - otherwise must be hardwired to 0b. When this bit is Set, AtomicOp Requests that target going out this Egress Port must be blocked.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**AtomicOp Requester Enable (ARE):** Applicable only to Endpoints and Root Ports - must be hardwired to 0b for other Function types. The Function is allowed to initiate AtomicOp Requests only if this bit and the Bus Master Enable bit in the Command register are both Set. This bit is required to be RW if the Endpoint or Root Port is capable of initiating AtomicOp Requests, but otherwise is permitted to be hardwired to 0b. This bit does not serve as a capability bit. This bit is permitted to be RW even if no AtomicOp Requester capabilities are supported by the Endpoint or Root Port.
5	0h RW	**ARI Forwarding Enable (AFE):** When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The Root Port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50us to 100us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

6.33 Device Status 2 (DSTS2) — Offset 6Ah

Device Status 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 6Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

6.34 Link Capabilities 2 (LCAP2) — Offset 6Ch

Link Capabilities 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 6Ch	0000000Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/O	**Two Retimers Presence Detect Supported (TRPDS):** When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit must be set to 1b in a Downstream Port when the Supported Link Speeds Vector of the Link Capabilities 2 register indicates support for a Link speed of 16.0 GT/s or higher. It is permitted to be set to 1b regardless of the supported Link speeds, and in Upstream Ports, if the Retimer Presence Detect Supported bit is also set to 1b.
23	0h RW/O	**Retimer Presence Detect Supported (RPDS):** When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit must be set to 1b in a Downstream Port when the Supported Link Speeds Vector of the Link Capabilities 2 register indicates support for a Link speed of 16.0 GT/s or higher. It is permitted to be set to 1b regardless of the supported Link speeds and in Upstream Ports.

Bit Range	Default & Access	Field Name (ID): Description
22:16	00h RW/O	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bits 6:4 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector. This register is Read-Only if LPCR.SRL field is set. **Locked by:** LPCR.SRL
15:9	00h RW/O	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0GT/s Bits 6:4 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector. This register is Read-Only if LPCR.SRL field is set. **Locked by:** LPCR.SRL
8	0h RO	**Crosslink Supported (CS):** No support for Crosslink.
7:1	07h RO/V	**Supported Link Speeds Vector (SLSV):** This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported - otherwise, the Link speed is not supported. Bit definitions within this field for PCI Express are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bit 3: 16.0 GT/s. Bits 4-6: Reserved.
0	0h RO	**Reserved**

6.35 Link Control 2 (LCTL2) — Offset 70h

Link Control 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 70h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is operating at 2.5 GT/s, the setting of this field has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Reserved**
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	1h RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

6.36 Link Status 2 (LSTS2) — Offset 72h

Link Status 2

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 72h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO/V/P	**Two Retimers Presence Detected (PX2RPD):** When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation. The default value of this bit is 0b. This bit is required for Ports that have the Two Retimers Presence Detect Supported bit of the Link Capabilities 2 register set to 1b. Ports that have the Two Retimers Presence Detect Supported bit set to 0b are permitted to hardwire this bit to 0b.
6	0h RO/V/P	**Retimer Presence Detected (RPD):** When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation. The default value of this bit is 0b. This bit is required for Ports that have the Retimer Presence Detect Supported bit Set. Ports that have the Retimer Presence Detect Supported bit of the Link Capabilities 2 register set to 0b are permitted to hardwire this bit to 0b.
5	0h RW/1C/V/P	**Link Equalization Request (LER):** This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link.
4	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** When set to 1, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
3	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** When set to 1, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
2	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** When set to 1, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed.
1	0h RO/V/P	**Equalization Complete (EQC):** When set to 1, this bit indicates that the Transmitter Equalization procedure at the 8.0GT/s data rate has completed.
0	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

6.37 Slot Capabilities 2 (SLCAP2) — Offset 74h

Slot Capabilities 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

6.38 Slot Control 2 (SLCTL2) — Offset 78h

Slot Control 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

6.39 Slot Status 2 (SLSTS2) — Offset 7Ah

Slot Status 2

Note: Bit definitions are the same as DSTS2, offset 6Ah.

6.40 Message Signaled Interrupt Identifiers (MID) — Offset 80h

Message Signaled Interrupt Identifiers

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 80h	9005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

6.41 Message Signaled Interrupt Message (MC) — Offset 82h

Message Signaled Interrupt Message

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 82h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
3:1	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

6.42 Message Signaled Interrupt Message Address (MA) — Offset 84h

Message Signaled Interrupt Message Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**ADDR:** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	**Reserved**

6.43 Message Signaled Interrupt Message Data (MD) — Offset 88h

Message Signaled Interrupt Message Data

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 88h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**DATA:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

6.44 Subsystem Vendor Capability (SVCAP) — Offset 90h

Subsystem Vendor Capability

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 90h	A00Dh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

6.45 Subsystem Vendor IDs (SVID) — Offset 94h

Subsystem Vendor IDs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

6.46 Power Management Capability (PMCAP) — Offset A0h

Power Management Capability

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + A0h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	01h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

6.47 PCI Power Management Capabilities (PMC) — Offset A2h

PCI Power Management Capabilities

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + A2h	C803h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:11	19h RO	**PMES:** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Windows operating systems to enable PME# in devices connected behind this root port.
10	0h RO	**D2S:** The D2 state is not supported.
9	0h RO	**D1S:** The D1 state is not supported.
8:6	0h RO	**AC:** Reports 375mA maximum suspend well current required when in the D3COLD state.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	**Reserved**
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**VS:** Indicates support for Revision 1.2 of the PCI Power Management Specification.

6.48 PCI Power Management Control (PMCS) — Offset A4h

PCI Power Management Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A4h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DTA:** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** This field is reserved per PCI Express specification

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**B2/B3 Support (B23S):** This field is reserved per PCI Express specification.
21:16	0h RO	**Reserved**
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Windows operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved**
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00: D0 state 11: D3HOT state When in the D3HOT state, the controllers configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a 10 or 01 to these bits, the write will be ignored.

6.49 Advanced Error Extended (AECH) — Offset 100h

Advanced Error Extended

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

6.50 Uncorrectable Error Status (UES) — Offset 104h

Uncorrectable Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/1C/V/P	**Poisoned TLP Egress Blocked Status (PTLPEBS):** Indicates that poisoned TLP Egress Blocked error has occurred. Note: This bit can only be set if DPCCAPR.PTLPEBS = 1 and DPCCTLR.PTLPEBE = 1.
25	0h RO	**Reserved**
24	0h RW/1C/V/P	**AtomicOp Egress Blocked Status (AEBS):** AtomicOp Egress Blocked Status
23:22	0h RO	**Reserved**
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Indicates an ACS Violation is logged.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Status (TE):** Not supported.

6.51 Uncorrectable Error Mask (UEM) — Offset 108h

Uncorrectable Error Mask

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Mask (PTLPEBM):** Mask for Poisoned TLP Egress Blocked error.
25	0h RO	**Reserved**
24	0h RW/P	**AtomicOp Egress Blocked Mask (AEBM):** Mask for AtomicOp Egress Blocked
23:22	0h RO	**Reserved**
21	0h RW/P	**ACS Violation Mask (AVM):** Mask for ACS Violation errors.
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Training Error Mask (TE):** Not supported.

6.52 Uncorrectable Error Severity (UEV) — Offset 10Ch

Uncorrectable Error Severity

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 10Ch	00060010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Poisoned TLP Egress Blocked Severity (PTLPEBS):** Severity for Poisoned TLP Egress Blocked error.
25	0h RO	**Reserved**
24	0h RW/P	**AtomicOp Egress Blocked Severity (AEBS):** AtomicOp Egress Blocked Severity
23:22	0h RO	**Reserved**
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS Violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**Reserved**
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved**
0	0h RO	**Training Error Severity (TE):** TE not supported.

6.53 Correctable Error Status (CES) — Offset 110h

Correctable Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

6.54 Correctable Error Mask (CEM) — Offset 114h

Correctable Error Mask

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 114h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved**
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	**Reserved**
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

6.55 Advanced Error Capabilities And Control (AECC) — Offset 118h

Advanced Error Capabilities And Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**Completion Timeout Prefix/Header Log Capable (CTPHLC):** If set, this bit indicates that port records the prefix/header of Request TLPs that experience a Completion Timeout error. Note: BIOS should program this bit before enable the Completion Timeout mechanism.
11:9	0h RO	**Reserved**
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capable (EGC):** ECRC is not supported.
4:0	00h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

6.56 Header Log (HL_DW1) — Offset 11Ch

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 11Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st DWORD of TLP (DW1):** Byte0 && Byte1 && Byte2 && Byte3

6.57 Header Log (HL_DW2) — Offset 120h

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd DWORD of TLP (DW2):** Byte4 && Byte5 && Byte6 && Byte7

6.58 Header Log (HL_DW3) — Offset 124h

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd DWORD of TLP (DW3):** Byte8 && Byte9 && Byte10 && Byte11

6.59 Header Log (HL_DW4) — Offset 128h

Header Log

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th DWORD of TLP (DW4):** Byte12 && Byte13 && Byte14 && Byte15

6.60 Root Error Command (REC) — Offset 12Ch

Root Error Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 12Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

6.61 Root Error Status (RES) — Offset 130h

Root Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved
26:7	0h RO	**Reserved**
6	0h RW/1C/V/P	**Fatal Error Messages Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

6.62 Error Source Identification (ESID) — Offset 134h

Error Source Identification

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requester ID if an internally detected error.
15:0	0000h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error.

6.63 PTM Extended Capability Header (PTMECH) — Offset 150h

PTM Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**Capability ID (CID):** For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

6.64 PTM Capability (PTMCAPR) — Offset 154h

PTM Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 154h	00000400h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	04h RW/O	**Local Clock Granularity (LCG):** 0000 0000b: Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Source's local clock in ns. 1111 1111b: Indicates the period of this Time Source's local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved**
2	0h RW/O	**PTM Root Capable (PTMRC):** Root Ports must set this bit to 1b.
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Role is not supported by Root Port.

6.65 PTM Control (PTMCTLR) — Offset 158h

PTM Control Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Effective Granularity (EG):** Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved**
1	0h RW	**Root Select (RS):** When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register.

6.66 L1 Sub-States Extended Capability Header (L1SECH) — Offset 200h

L1 Sub-States Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh.

6.67 L1 Sub-States Capabilities (L1SCAP) — Offset 204h

L1 Sub-States Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 204h	0028281Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:19	05h RW/O	**Port Tpower_on Value (PTV):** Along with the Port Tpower_on Scale field in the L1 Sub-states Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved**
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Sub-states Capabilities register. 00b: 2 us 01b: 10 us 10b: 100 us 11b: Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7	0h RO	**Reserved**
6	0h RW/1C/V	**CLKREQ# Acceleration Interrupt Status (L1SSEIS):** For a Downstream Port that has both the CLKREQ# Acceleration Supported and CLKREQ# Acceleration Interrupt Enable bits Set, when set this bit indicates that the Port has completed the CLKREQ# Acceleration Link Activation process, and that the Link has reached L0. Software must then clear this bit by writing a 1b to this bit. Must be hardwired to 0b for Upstream Ports. Default value is 0b.
5	0h RW/O	**CLKREQ# Acceleration Supported (L1SSES):** When set this bit indicates that this Port supports CLKREQ# acceleration.

Bit Range	Default & Access	Field Name (ID): Description
4	1h RW/O	**L1 PM Sub-states Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Sub-states. For compatibility with possible future extensions, software must not enable L1 PM Sub-states unless this bit is set. This RWO field must be programmed prior to enabling ASPM. Required for both Upstream and Downstream Ports.
3	1h RW/O	**ASPM L1.1 Supported (AL11S):** When set, this bit indicates ASPM L1.SNOOZ is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM.
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM.
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that PCI-PM L1.SNOOZ is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM.
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that PCI-PM L1.OFF is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM.

6.68 L1 Sub-States Control 1 (L1SCTL1) — Offset 208h

L1 Sub-States Control 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency Scale Value (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular Root Port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF.

Bit Range	Default & Access	Field Name (ID): Description
28:26	0h RO	**Reserved**
25:16	000h RW	**L1.2 LTR Threshold Latency Value (L12LTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular Root Port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF.
15:8	00h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time(in us) the Root Port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF.
7:6	0h RO	**Reserved**
5	0h RW	**L1 Substate Exit Control (L1SSEC):** L1.Substate the Port must initiate the CLKREQ# Acceleration Link Activation process. Apart from that, once the Link reaches L0, the Port must continue to attempt to maintain the Link in L0 for as long as this bit remains Set. However if the Upstream Port request for L1 entry, the Downstream Port will proceed to allow L1 entry but will not re-enter L1.1 or L1.2.
4	0h RW	**CLKREQ# Acceleration Interrupt Enable (L1SSEIE):** When set this bit enables the generation of an interrupt to indicate the completion of the CLKREQ# acceleration Link Activation process
3	0h RW	**ASPM L1.1 Enable (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ sub-states are enabled. Required for both upstream and downstream ports. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF sub-states are enabled. Required for both upstream and downstream ports. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
1	0h RW	**PCI-PM L1.1 Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Note: If STRPFUSECFG.mPHYIOPMDIS is 1, hardware will always see 0 as an output from this register. BIOS reading this register should always return the correct value.

6.69 L1 Sub-States Control 2 (L1SCTL2) — Offset 20Ch

L1 Sub-States Control 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 20Ch	00000028h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	05h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserted in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF.
2	0h RO	**Reserved**
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. 00b: 2 us 01b: 10 us 10b: 100us 11b: Reserved. Required for all Ports that support L1.OFF.

6.70 ACS Extended Capability Header (ACSECH) — Offset 220h

ACS Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Capability ID (CID):** For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

6.71 ACS Capability (ACSCAPR) — Offset 224h

ACS Capability Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 224h	001Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control is not supported.
4	1h RW/O	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding.
3	1h RW/O	**ACS P2P Completion Redirect (C):** Required for all Functions that support ACS P2P Request Redirect - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** Required for Root Ports that support peer-to-peer traffic with other Root Ports - required for Switch Downstream Ports - required for multi-function device Functions that support peer-to-peer traffic with other Functions - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** Required for Root Ports and Switch Downstream Ports - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** Required for Root Ports and Switch Downstream Ports - must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

6.72 ACS Control (ACSCTLR) — Offset 226h

ACS Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 226h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	0h RO	**ACS Direct Translated P2P Enable (TE):** ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (EE):** ACS P2P Egress Control is not supported.
4	0h RW	**ACS Upstream Forwarding Enable (UE):** ACS Upstream Forwarding.
3	0h RW	**ACS P2P Completion Redirect Enable (CE):** Determines when the component redirects peer-to-peer Completions upstream - applicable only to Read Completions whose Relaxed Ordering Attribute is clear. Requests are never affected by ACS P2P Completion Redirect. Default value of this field is 0b.
2	0h RW	**ACS P2P Request Redirect Enable (RE):** Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect. Default value of this field is 0b.
1	0h RW	**ACS Translation Blocking Enable (BE):** When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking. Default value of this field is 0b.
0	0h RW	**ACS Source Validation Enable (VE):** When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation. Default value of this field is 0b.

6.73 Port VC Capability Register 1 (PVCCR1) — Offset 284h

Port VC Capability Register 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 284h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RO	**Function Arbitration Table Entry Size (FARES):** Indicates the size (in bits) of Function Arbitration table entry in the device. Defined encodings are: 00b Size of Function Arbitration table entry is 1 bit 01b Size of Function Arbitration table entry is 2 bits 10b Size of Function Arbitration table entry is 4 bits 11b Size of Function Arbitration table entry is 8 bits
9:8	0h RO	**Reference Clock (RC):** Indicates the reference clock for Virtual Channels that support time-based WRR Function Arbitration. Defined encodings are: 00b 100 ns reference clock 01b 11b Reserved
7	0h RO	**Reserved**
6:4	0h RO	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict priority VC Arbitration. The minimum value of this field is 000b and the maximum value is Extended VC Count.
3	0h RO	**Reserved**
2:0	0h RW/O	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The minimum value of this field is zero (for devices that only support the default VC). The maximum value is seven.

6.74 Port VC Capability 2 (PVCC2) — Offset 288h

Port VC Capability 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 288h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.
23:8	0h RO	**Reserved**
7:0	00h RO	**VC Arbitration Capability (VCAC):** Indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid for all devices that report a Low Priority Extended VC Count greater than 0. Each bit location within this field corresponds to a VC Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the device can be configured to provide different VC arbitration services. Defined bit positions are: Bit 0: Hardware fixed arbitration scheme (e.g., Round Robin). Bit 1: Weighted Round Robin (WRR) arbitration with 32 phases. Bit 2: WRR arbitration with 64 phases. Bit 3: WRR arbitration with 128 phases. Bits 4-7: Reserved.

6.75 Port VC Control (PVCC) — Offset 28Ch

Port VC Control.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 28Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RW	**VC Arbitration Select (VCAS):** Used by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability register 2. The permissible values of this field are numbers corresponding to one of the asserted bits in the VC Arbitration Capability field. This field cannot be modified when more than one VC in the LPVC group is enabled.
0	0h WO	**Load VC Arbitration Table (LVCAT):** Used by software to update the VC Arbitration Table. This bit is valid when the selected VC Arbitration uses the VC Arbitration Table. Software Sets this bit to request hardware to apply new values programmed into VC Arbitration Table - Clearing this bit has no effect. Software checks the VC Arbitration Table Status bit to confirm that new values stored in the VC Arbitration Table are latched by the VC arbitration logic. This bit always returns 0b when read.

6.76 Port VC Status (PVCS) — Offset 28Eh

Port VC Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 28Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VC Arbitration Table Status (VCATS):** Indicates the coherency status of the VC Arbitration Table. This bit is valid when the selected VC uses the VC Arbitration Table. This bit is Set by hardware when any entry of the VC Arbitration Table is written by software. This bit is Cleared by hardware when hardware finishes loading values stored in the VC Arbitration Table after software sets the Load VC Arbitration Table bit in the Port VC Control register. Default value of this bit is 0b.

6.77 Virtual Channel 0 Resource Capability (V0VCRC) — Offset 290h

Virtual Channel 0 Resource Capability

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 290h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Function Arbitration Table Offset (FATO):** Indicates the location of the Function Arbitration Table associated with the VC resource. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the MFVC Capability structure. A value of 00h indicates that the table is not present.
23	0h RO	**Reserved**
22:16	00h RW/O	**Maximum Time Slots (MTS):** Indicates the maximum number of time slots (minus 1) that the VC resource is capable of supporting when it is configured for time-based WRR Function Arbitration. For example, a value of 000 0000b in this field indicates the supported maximum number of time slots is 1 and a value of 111 1111b indicates the supported maximum number of time slots is 128. This field is valid only when the Function Arbitration Capability indicates that the VC resource supports time-based WRR Function Arbitration.
15:8	0h RO	**Reserved**
7:0	00h RO	**Function Arbitration Capability (FAC):** Indicates types of Function Arbitration supported by the VC resource. Each bit location within this field corresponds to a Function Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Function Arbitration Select field. Defined bit positions are: Bit 0: Non-configurable hardware-fixed arbitration scheme (e.g. Round Robin). Bit 1: Weighted Round Robin (WRR) arbitration with 32 phases. Bit 2: WRR arbitration with 64 phases. Bit 3: WRR arbitration with 128 phases. Bit 4: Time-based WRR with 128 phases. Bit 5: WRR arbitration with 256 phases. Bits 6-7: Reserved.

6.78 Virtual Channel 0 Resource Control (V0CTL) — Offset 294h

Virtual Channel 0 Resource Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 294h	80000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** When Set, this bit enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. Default value of this bit is 1b for the first VC resource and 0b for other VC resource(s). Notes: 1. This bit is hardwired to 1b for the default VC (VC0), i.e., writing to this field has no effect for VC0. 2. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Set in both components on a Link. 3. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Cleared in both components on a Link. 4. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 5. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel.
30:27	0h RO	**Reserved**
26:24	0h RO	**Virtual Channel Identifier (ID):** This field assigns a VC ID to the VC resource. This field cannot be modified when the VC is already enabled. Note: For the first VC resource (default VC), this field is a read-only field that must be hardwired to 000b.
23:20	0h RO	**Reserved**
19:17	0h RW	**Function Arbitration Select (FAS):** This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.
16	0h RW	**Load Function Arbitration Table (LFAT):** When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table - clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
9:8	0h RO	**Reserved**
7:1	00h RW	**Transaction Class / Virtual Channel Map (TVM):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.
0	1h RO	**Transaction Class / Virtual Channel Map TC0 (TVMT0):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.

6.79 Virtual Channel 0 Resource Status (V0STS) — Offset 29Ah

Virtual Channel 0 Resource Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 29Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO/V	**VC Negotiation Pending (NP):** This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. When this bit is Set by hardware, it indicates that the VC resource is still in the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete. For a nondefault Virtual Channel, software may use this bit when enabling or disabling the VC. For the default VC, this bit indicates the status of the process of Flow Control initialization. Before using a Virtual Channel, software must check whether the VC Negotiation Pending bits for that Virtual Channel are Clear in both components on a Link.
0	0h RO	**Function Arbitration Table Status (FATS):** This bit indicates the coherency status of the Function Arbitration Table associated with the VC resource. This bit is valid only when the Function Arbitration Table is used by the selected Function Arbitration for the VC resource. This bit is Set by hardware when any entry of the Function Arbitration Table is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the Function Arbitration Table after software sets the Load FunctionArbitration Table bit.

6.80 Virtual Channel 1 Resource Capability (V1VCRC) — Offset 29Ch

Virtual Channel 1 Resource Capability

Note: Bit definitions are the same as V0VCRC, offset 290h.

6.81 Virtual Channel 1 Resource Control (V1CTL) — Offset 2A0h

Virtual Channel 1 Resource Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + 2A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
30:28	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel Note: BIOS is required to program VCID[3] to 0 when operating at DMI2. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
23:20	0h RO	**Reserved**
19:17	0h RW	**Function Arbitration Select (FAS):** This field configures the VC resource to provide a particular Function Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Function Arbitration Capability field of the VC resource.
16	0h RW	**Load Function Arbitration Table (LFAT):** When Set, this bit updates the Function Arbitration logic from the Function Arbitration Table for the VC resource. This bit is only valid when the Function Arbitration Table is used by the selected Function Arbitration scheme (that is indicated by a Set bit in the Function Arbitration Capability field selected by Function Arbitration Select). Software sets this bit to signal hardware to update Function Arbitration logic with new values stored in the Function Arbitration Table - clearing this bit has no effect. Software uses the Function Arbitration Table Status bit to confirm whether the new values of Function Arbitration Table are completely latched by the arbitration logic. This bit always returns 0b when read. Default value of this bit is 0b.
15:10	00h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if LPCR.SRL field is set **Locked by:** LPCR.SRL
9:8	0h RO	**Reserved**
7:1	00h RW	**Transaction Class / Virtual Channel Map (TVM):** This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. Default value of this field is FFh for the first VC resource and is 00h for other VC resources. Note: Bit 0 of this field is read-only. It must be hardwired to 1b for the default VC0 and hardwired to 0b for all other enabled VCs.
0	0h RO	**Reserved**

6.82 Virtual Channel 1 Resource Status (V1STS) — Offset 2A6h

Virtual Channel 1 Resource Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + 2A6h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO/V	**VC Negotiation Pending (NP):** This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. When this bit is Set by hardware, it indicates that the VC resource is still in the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete. For a nondefault Virtual Channel, software may use this bit when enabling or disabling the VC. For the default VC, this bit indicates the status of the process of Flow Control initialization. Before using a Virtual Channel, software must check whether the VC Negotiation Pending bits for that Virtual Channel are Clear in both components on a Link.
0	0h RO	**Function Arbitration Table Status (FATS):** This bit indicates the coherency status of the Function Arbitration Table associated with the VC resource. This bit is valid only when the Function Arbitration Table is used by the selected Function Arbitration for the VC resource. This bit is Set by hardware when any entry of the Function Arbitration Table is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the Function Arbitration Table after software sets the Load FunctionArbitration Table bit. Default value of this bit is 0b

6.83 DPC Extended Capability Header (DPCECH) — Offset A00h

DPC Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support DPC Extended Capability, BIOS should write a 1h to this register else it should write 0.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Capability ID (CID):** For systems that support DPC Extended Capability, BIOS should write a 001Dh to this register else it should write 0.

6.84 DPC Capability (DPCCAPR) — Offset A04h

DPC Capability Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + A04h	14E0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12	1h RW/O	**DL_Active ERR_COR Signaling Supported (DLAECSS):** This field when set, indicates that the Root Port supports the ability to signal with ERR_COR when the link transitions to the DL_Active state. Root Port that supports RP Extensions for DPC must set this bit.
11:8	4h RW/O	**RP PIO Log Size (RPPIOLS):** This field indicates how many DWORDs are allocated for the RP PIO log registers, comprised by the RP PIO Header Log, RP PIO ImpSpec Log and RP PIO TLP Prefix Log. If the Root Port supports RP Extensions for DPC, the value of this field must be 4 or greater - otherwise the value of this field must be 0.
7	1h RW/O	**DPC Software Triggering Supported (DPCSTS):** This field when set, indicates that the Root Port supports the ability for software to trigger DPC. Root Ports that support RP Extensions for DPC must set this bit.
6	1h RW/O	**Poisoned TLP Egress Blocking Supported (PTLPEBS):** This field when set, indicates that the Root Port supports the ability to block the transmission of a poisoned TLP from its Egress port. Root Ports that support RP Extensions for DPC must set this bit.
5	1h RW/O	**RP Extensions For DPC (RPEFDPC):** This field when set, indicates that a Root Port supports a defined set of DPC Extensions that are specific to Root Ports.

Bit Range	Default & Access	Field Name (ID): Description
4:0	00h RW/O	**DPC Interrupt Message Number (DPCIMN):** This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with the DPC Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: BIOS is expected to update this field with the right value before enabling DPC interrupt.

6.85 DPC Control (DPCCTLR) — Offset A06h

DPC Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + A06h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RW	**DL_Active ERR_COR Enable (DLAECE):** This bit when set, enables the downstream port to signal ERR_COR when the link transitions to the DL_Active state.
6	0h RW/1S/V	**DPC Software Trigger (DPCST):** If DPC Trigger is enabled and the DPC Trigger Status bit is clear, software writing a 1b to this bit will cause DPC to be triggered. If DPC Trigger is not enabled or DPC Trigger Status is set, software writing a 1b to this bit has no effect. Note: It is permitted to write 1b to this bit while simultaneously writing updated values to other fields in this register, notably the DPC Trigger Enable field. For this case, the DPC Software Trigger semantics are based on the updated value of the DPC Trigger Enable field. *Note: This bit always return 0b when read.
5	0h RW	**Poisoned TLP Egress Blocking Enable (PTLPEBE):** This bit, when set, enables the associated Egress Port to block the transmission of poisoned TLP.
4	0h RW	**DPC ERR_COR Enable (DPCECE):** When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**DPC Interrupt Enable (DPCIE):** When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered.
2	0h RW	**DPC Completion Control (DPCCC):** This bit controls the Completion Status for completions formed during DPC. 0b: Completer Abort (CA) Completion Status. 1b: Unsupported Request (UR) Completion Status.
1:0	0h RW	**DPC Trigger Enable (DPCTE):** This field enables DPC and controls the conditions that cause DPC to be triggered. 00b: DPC is disabled. 01b: DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_FATAL message. 10b: DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR_NONFATAL or ERR_FATAL message. 11b: Reserved.

6.86 DPC Status (DPCSR) — Offset A08h

DPC Status Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + A08h	1F00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:8	1Fh RO/V/P	**RP PIO First Error Pointer (RPPIOFEP):** The value of this field identifies a bit position in the RP PIO Status register, and this field is considered valid when that bit is set. When this field is valid, and software writes a 1b to the indicated RP PIO Status bit (thus clearing it), this field must revert to its default value. This field is applicable only for Root Ports that support RP Extensions for DPC, and is otherwise reserved. If this field is not reserved, the default value is 11111b.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RO/V/P	**DPC Trigger Extension (DPCTE):** This field serves as an extension to the DPC Trigger Reason field. When that field is valid and has a value of 11b, this field indicates why DPC has been triggered. 00b: DPC was triggered due to RP PIO error. 01b: DPC was triggered due to DPC Software Trigger bit. 10b: Reserved. 11b: Reserved. This field is valid only when the DPC Trigger Status bit is set and the value of the DPC Trigger Reason field is 11b. Otherwise the value of this field is undefined.
4	0h RO/V	**DPC RP Busy (DPCRPB):** When the DPC Trigger Status bit is Set and this bit is Set, the Root Port is busy with internal activity that must complete before software is permitted to clear the DPC Trigger Status bit. If software Clears the DPC Trigger Status bit while this bit is set, the behavior is undefined. This field is valid only when the DPC Trigger Status bit is Set - otherwise the value of this field is undefined. This bit is applicable only for Root Ports that support RP Extensions for DPC, and is Reserved otherwise.
3	0h RW/1C/V/P	**DPC Interrupt Status (DPCIS):** This bit is set if DPC is triggered while the DPC Interrupt Enable bit is set.
2:1	0h RO/V/P	**DPC Trigger Reason (DPCTR):** This field indicates why DPC has been triggered. 00b: DPC was triggered due to an unmasked uncorrectable error. 01b: DPC was triggered due to receiving an ERR_NONFATAL. 10b: DPC was triggered due to receiving an ERR_FATAL. 11b: DPC was triggered due to a reason that is indicated by the DPC Trigger Reason Extension field. Note: This field is only valid when DPC Trigger Status bit is set - otherwise the value of this field is undefined.
0	0h RW/1C/V/P	**DPC Trigger Status (DPCTS):** When set, indicates that DPC has been triggered. DPC is event triggered. While this bit is set, hardware must direct the LTSSM to the Disabled state. This bit must be cleared before the LTSSM can be released from Disabled state. Once the requirements for how long software must leave the downstream port in DPC is met, software is permitted to clear this bit regardless of the state of other status bits associated with the triggering event. Refer to PCIe Base specification 3.0 for more timing requirements pertaining to this bit.

6.87 DPC Error Source ID (DPCESIDR) — Offset A0Ah

DPC Error Source ID Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + A0Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V/P	**DPC Error Source ID (DPCESID):** When the DPC Trigger Reason field indicates that DPC was triggered due to the reception of an ERR_NONFATAL or ERR_FATAL message, this register field contains the Requester ID of the received messages. Otherwise, the value of this register is undefined.

6.88 RP PIO Status (RPPIOSR) — Offset A0Ch

RP PIO Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A0Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/1C/V/P	**Memory Completion Timeout Status (MCTS):** Non-posted memory request completion times out.
17	0h RW/1C/V/P	**Memory Completer Abort Completion Status (MCACS):** Non-posted memory request received CA completion.
16	0h RW/1C/V/P	**Memory Unsupported Request Completion Status (MURCS):** Non-posted Memory request received UR completion.
15:11	0h RO	**Reserved**
10	0h RW/1C/V/P	**I/O Completion Timeout Status (IOCTS):** I/O request completion times out.
9	0h RW/1C/V/P	**I/O Completer Abort Completion Status (IOCACS):** I/O request received CA completion.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**I/O Unsupported Request Completion Status (IOURCS):** I/O request received UR completion.
7:3	0h RO	**Reserved**
2	0h RW/1C/V/P	**Configuration Completion Timeout Status (CCTS):** Configuration request completion times out.
1	0h RW/1C/V/P	**Configuration Completer Abort Completion Status (CCACS):** Configuration request received CA completion.
0	0h RW/1C/V/P	**Configuration Unsupported Request Completion Status (CURCS):** Configuration request received UR completion.

6.89 RP PIO Mask (RPPIOMR) — Offset A10h

RP PIO Mask Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A10h	00070707h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	1h RW/P	**Memory Completion Timeout Mask (MCTM):** Mask bit for Memory Completion Timeout Status.
17	1h RW/P	**Memory Completer Abort Completion Mask (MCACM):** Mask bit for Memory Completer Abort Completion Status.
16	1h RW/P	**Memory Unsupported Request Completion Mask (MURCM):** Mask bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	1h RW/P	**I/O Completion Timeout Mask (IOCTM):** Mask bit for I/O Completion Timeout Status.
9	1h RW/P	**I/O Completer Abort Completion Mask (IOCACM):** Mask bit for I/O Completer Abort Completion Status.
8	1h RW/P	**I/O Unsupported Request Completion Mask (IOURCM):** Mask bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/P	**Configuration Completion Timeout Mask (CCTM):** Mask bit for Configuration Completion Timeout Status.
1	1h RW/P	**Configuration Completer Abort Completion Mask (CCACM):** Mask bit for Configuration Completer Abort Status.
0	1h RW/P	**Configuration Unsupported Request Completion Mask (CURCM):** Mask bit for Configuration Unsupported Request Completion Status.

6.90 RP PIO Severity (RPPIOVR) — Offset A14h

RP PIO Severity Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout Severity (MCTSV):** Severity bit for Memory Completion Timeout Status.
17	0h RW/P	**Memory Completer Abort Completion Severity (MCACSV):** Severity bit for Memory Completer Abort Completion Status.
16	0h RW/P	**Memory Unsupported Request Completion Severity (MURCSV):** Severity bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout Severity (IOCTSV):** Severity bit for I/O Completion Timeout Status.
9	0h RW/P	**I/O Completer Abort Completion Severity (IOCACSV):** Severity bit for I/O Completer Abort Completion Status.
8	0h RW/P	**I/O Unsupported Request Completion Severity (IOURCSV):** Severity bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout Severity (CCTSV):** Severity bit for Configuration Completion Timeout Status.
1	0h RW/P	**Configuration Completer Abort Completion Severity (CCACSV):** Severity bit for Configuration Completer Abort Status.
0	0h RW/P	**Configuration Unsupported Request Completion Severity (CURCSV):** Severity bit for Configuration Unsupported Request Completion Status.

6.91 RP PIO SysError (RPPIOSER) — Offset A18h

RP PIO SysError Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout SysErr (MCTSE):** SysErr bit for Memory Completion Timeout Status.
17	0h RW/P	**Memory Completer Abort Completion SysErr (MCACSE):** SysErr bit for Memory Completer Abort Completion Status.
16	0h RW/P	**Memory Unsupported Request Completion SysErr (MURCSE):** SysErr bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout SysErr (IOCTSE):** SysErr bit for I/O Completion Timeout Status.
9	0h RW/P	**I/O Completer Abort Completion SysErr (IOCACSE):** SysErr bit for I/O Completer Abort Completion Status.
8	0h RW/P	**I/O Unsupported Request Completion SysErr (IOURCSE):** SysErr bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout SysErr (CCTSE):** SysErr bit for Configuration Completion Timeout Status.
1	0h RW/P	**Configuration Completer Abort Completion SysErr (CCACSE):** SysErr bit for Configuration Completer Abort Status.
0	0h RW/P	**Configuration Unsupported Request Completion SysErr (CURCSE):** SysErr bit for Configuration Unsupported Request Completion Status.

6.92 RP PIO Exception (RPPIOER) — Offset A1Ch

RP PIO Exception Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/P	**Memory Completion Timeout Exception (MCTE):** Exception bit for Memory Completion Timeout Status.
17	0h RW/P	**Memory Completer Abort Completion Exception (MCACE):** Exception bit for Memory Completer Abort Completion Status.
16	0h RW/P	**Memory Unsupported Request Completion Exception (MURCE):** Exception bit for Memory Unsupported Request Completion Status.
15:11	0h RO	**Reserved**
10	0h RW/P	**I/O Completion Timeout Exception (IOCTE):** Exception bit for I/O Completion Timeout Status.
9	0h RW/P	**I/O Completer Abort Completion Exception (IOCACE):** Exception bit for I/O Completer Abort Completion Status.
8	0h RW/P	**I/O Unsupported Request Completion Exception (IOURCE):** Exception bit for I/O Unsupported Request Completion Status.
7:3	0h RO	**Reserved**
2	0h RW/P	**Configuration Completion Timeout Exception (CCTE):** Exception bit for Configuration Completion Timeout Status.
1	0h RW/P	**Configuration Completer Abort Completion Exception (CCACE):** Exception bit for Configuration Completer Abort Status.
0	0h RW/P	**Configuration Unsupported Request Completion Exception (CURCE):** Exception bit for Configuration Unsupported Request Completion Status.

6.93 RP PIO Header Log DW1 (RPPIOHLR_DW1) — Offset A20h

RP PIO Header Log DW1 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**1st DWORD of TLP (DW1):** Byte0 AND Byte1 AND Byte2 AND Byte3.

6.94 RP PIO Header Log DW2 (RPPIOHLR_DW2) — Offset A24h

RP PIO Header Log DW2 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**2nd DWORD of TLP (DW2):** Byte4 AND Byte5 AND Byte6 AND Byte7.

6.95 RP PIO Header Log DW3 (RPPIOHLR_DW3) — Offset A28h

RP PIO Header Log DW3 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**3rd DWORD of TLP (DW3):** Byte8 AND Byte9 AND Byte10 AND Byte11.

6.96 RP PIO Header Log DW4 (RPPIOHLR_DW4) — Offset A2Ch

RP PIO Header Log DW4 Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**4th DWORD of TLP (DW4):** Byte12 AND Byte13 AND Byte14 AND Byte15.

6.97 Secondary PCI Express Extended Capability Header (SPEECH) — Offset A30h

Secondary PCI Express Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIEECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

6.98 Link Control 3 (LCTL3) — Offset A34h

Link Control 3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RW	**Enable Lower SKP OS Generation Vector (ELSOSGV):** When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bits 6:4 Rsvd Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved**
1	0h RW/P	**Link Equalization Request Interrupt Enable (LERIE):** When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW/1S/V	**Perform Equalization (PE):** When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization Phase 1.

6.99 Lane Error Status (LES) — Offset A38h

Lane Error Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V/P	**Lane 15 Error Status (L15ES):** Lane 15 detected a Lane-based error.
14	0h RW/1C/V/P	**Lane 14 Error Status (L14ES):** Lane 14 detected a Lane-based error.
13	0h RW/1C/V/P	**Lane 13 Error Status (L13ES):** Lane 13 detected a Lane-based error.
12	0h RW/1C/V/P	**Lane 12 Error Status (L12ES):** Lane 12 detected a Lane-based error.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C/V/P	**Lane 11 Error Status (L11ES):** Lane 11 detected a Lane-based error.
10	0h RW/1C/V/P	**Lane 10 Error Status (L10ES):** Lane 10 detected a Lane-based error.
9	0h RW/1C/V/P	**Lane 9 Error Status (L9ES):** Lane 9 detected a Lane-based error.
8	0h RW/1C/V/P	**Lane 8 Error Status (L8ES):** Lane 8 detected a Lane-based error.
7	0h RW/1C/V/P	**Lane 7 Error Status (L7ES):** Lane 7 detected a Lane-based error.
6	0h RW/1C/V/P	**Lane 6 Error Status (L6ES):** Lane 6 detected a Lane-based error.
5	0h RW/1C/V/P	**Lane 5 Error Status (L5ES):** Lane 5 detected a Lane-based error.
4	0h RW/1C/V/P	**Lane 4 Error Status (L4ES):** Lane 4 detected a Lane-based error.
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 detected a Lane-based error.

6.100 Lane 0 And Lane 1 Equalization Control (L01EC) — Offset A3Ch

Lane 0 And Lane 1 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A3Ch	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.101 Lane 2 And Lane 3 Equalization Control (L23EC) — Offset A40h

Lane 2 And Lane 3 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A40h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset Hint (UPL3TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.102 Lane 4 And Lane 5 Equalization Control (L45EC) — Offset A44h

Lane 4 And Lane 5 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A44h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 5 Receiver Preset Hint (UPL5RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 5 Transmitter Preset (UPL5TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 5 Receiver Preset Hint (DPL5RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 5 Transmitter Preset (DPL5TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 4 Receiver Preset Hint (UPL4RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 4 Transmitter Preset (UPL4TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 4 Receiver Preset Hint (DPL4RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 4 Transmitter Preset (DPL4TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.103 Lane 6 And Lane 7 Equalization Control (L67EC) — Offset A48h

Lane 6 And Lane 7 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A48h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 7 Receiver Preset Hint (UPL7RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
27:24	Fh RW	**Upstream Port Lane 7 Transmitter Preset (UPL7TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 7 Receiver Preset Hint (DPL7RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 7 Transmitter Preset (DPL7TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 6 Receiver Preset Hint (UPL6RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 6 Transmitter Preset (UPL6TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 6 Receiver Preset Hint (DPL6RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 6 Transmitter Preset (DPL6TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.104 Lane 8 And Lane 9 Equalization Control (L89EC) — Offset A4Ch

Lane 8 And Lane 9 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A4Ch	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 9 Receiver Preset Hint (UPL9RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 9 Transmitter Preset (UPL9TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 9 Receiver Preset Hint (DPL9RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 9 Transmitter Preset (DPL9TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 8 Receiver Preset Hint (UPL8RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 8 Transmitter Preset (UPL8TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 8 Receiver Preset Hint (DPL8RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 8 Transmitter Preset (DPL8TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.105 Lane 10 And Lane 11 Equalization Control (L1011EC) — Offset A50h

Lane 10 And Lane 11 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A50h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 11 Receiver Preset Hint (UPL11RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 11 Transmitter Preset (UPL11TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 11 Receiver Preset Hint (DPL11RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 11 Transmitter Preset (DPL11TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 10 Receiver Preset Hint (UPL10RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Upstream Port Lane 10 Transmitter Preset (UPL10TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 10 Receiver Preset Hint (DPL10RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 10 Transmitter Preset (DPL10TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.106 Lane 12 And Lane 13 Equalization Control (L1213EC) — Offset A54h

Lane 12 And Lane 13 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A54h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 13 Receiver Preset Hint (UPL13RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
27:24	Fh RW	**Upstream Port Lane 13 Transmitter Preset (UPL13TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 13 Receiver Preset Hint (DPL13RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 13 Transmitter Preset (DPL13TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 12 Receiver Preset Hint (UPL12RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 12 Transmitter Preset (UPL12TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 12 Receiver Preset Hint (DPL12RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 12 Transmitter Preset (DPL12TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.107 Lane 14 And Lane 15 Equalization Control (L1415EC) — Offset A58h

Lane 14 And Lane 15 Equalization Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A58h	7F7F7F7Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	7h RW	**Upstream Port Lane 15 Receiver Preset Hint (UPL15RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.

Bit Range	Default & Access	Field Name (ID): Description
27:24	Fh RW	**Upstream Port Lane 15 Transmitter Preset (UPL15TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
23	0h RO	**Reserved**
22:20	7h RW	**Downstream Port Lane 15 Receiver Preset Hint (DPL15RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 15 Transmitter Preset (DPL15TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved**
14:12	7h RW	**Upstream Port Lane 14 Receiver Preset Hint (UPL14RPH):** Field contains the Receiver Preset Hint value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Upstream Port Lane 14 Transmitter Preset (UPL14TP):** Field contains the Transmitter Preset value sent or received during Port 8 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
7	0h RO	**Reserved**
6:4	7h RW	**Downstream Port Lane 14 Receiver Preset Hint (DPL14RPH):** Receiver Preset Hint may be used as a hint for 8 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 14 Transmitter Preset (DPL14TP):** Transmitter Preset used for 8 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.108 Data Link Feature Extended Capability Header (DLFECH) — Offset A90h

Data Link Feature Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability.

6.109 Data Link Feature Capabilities (DLFCAP) — Offset A94h

Data Link Feature Capabilities Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A94h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/O	**Data Link Feature Exchange Enable (DLFEE):** If set, this bit indicates that this Port will enter the DL_Feature negotiation state. Default is 1b.
30:23	0h RO	**Reserved**
22:1	000000h RW/O	**Local Feature Supported (LFS):** These bits indicate that the Downstream Port supports the associated Data Link Feature. For this version of this specification, this field is hardwired to 0.
0	0h RW/O	**Local Scaled Flow Control Supported (LSFCS):** This bit indicates that the Port supports the Scaled Flow Control Feature.

6.110 Data Link Feature Status (DLFSTS) — Offset A98h

Data Link Feature Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Data Link Feature Status Valid (DLFSV):** This bit indicates that the Downstream Port has received a Data Link Feature DLLP after the Link entered L0. When this bit is 1b, bits 23:0 are frozen. Software must clear this bit to re-enable capturing information. This bit is cleared on DL_Down.
30:23	0h RO	**Reserved**
22:1	000000h RO/V	**Remote Feature Supported (RFS):** These bits indicate that the Remote Port supports the corresponding Data Link Feature. These bits capture all information from the Data Link Feature DLLP even when this Port does not support the corresponding feature.
0	0h RO/V	**Remote Scaled Flow Control Supported (RSFCS):** This bit indicates that the Remote Port indicated it supports the Scaled Flow Control Feature

6.111 Physical Layer 16.0 GT/s Extended Capability Header (PL16GECH) — Offset A9Ch

Physical Layer 16.0 GT/s Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + A9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0000h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Physical Layer 16.0 GT/s Capability

6.112 Physical Layer 16.0 GT/s Capability (PL16CAP) — Offset AA0h

Physical Layer 16.0 GT/s Capability Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

6.113 Physical Layer 16.0 GT/s Control (PL16CTL) — Offset AA4h

Physical Layer 16.0 GT/s Control Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

6.114 Physical Layer 16.0 GT/s Status (PL16S) — Offset AA8h

Physical Layer 16.0 GT/s Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + AA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW/1C/V/P	**Link Equalization Request 16.0 GT/s (LERG4):** This bit is Set by hardware to request the 16.0 GT/s Link equalization process to be performed on the Link. The default value of this bit is 0b.
3	0h RO/V/P	**Equalization 16.0 GT/s Phase 3 Successful (EQP3SG4):** When set to 1b, this bit indicates that Phase 3 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V/P	**Equalization 16.0 GT/s Phase 2 Successful (EQP2SG4):** When set to 1b, this bit indicates that Phase 2 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.
1	0h RO/V/P	**Equalization 16.0 GT/s Phase 1 Successful (EQP1SG4):** When set to 1b, this bit indicates that Phase 1 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. The default value of this bit is 0b.
0	0h RO/V/P	**Equalization 16.0 GT/s Complete (EQG4):** When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 16.0 GT/s data rate has completed. The default value of this bit is 0b.

6.115 Physical Layer 16.0 GT/s Local Data Parity Mismatch Status (PL16LDPMS) — Offset AACh

Physical Layer 16.0 GT/s Local Data Parity Mismatch Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + AACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**Local Data Parity Mismatch Status (LDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

6.116 Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status (PL16FRDPMS) — Offset AB0h

Physical Layer 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + AB0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**First Retimer Data Parity Mismatch Status (FRDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

6.117 Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status (PL16SRDPMS) — Offset AB4h

Physical Layer 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + AB4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C/V/P	**Second Retimer Data Parity Mismatch Status (SRDPMS):** Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The default value of each bit is 0b.

6.118 Physical Layer 16.0 GT/s Extra Status (PL16ES) — Offset AB8h

Physical Layer 16.0 GT/s Extra Status Register

Note: Bit definitions are the same as DSTS2, offset 6Ah.

6.119 Physical Layer 16.0 GT/s Lane 01 Equalization Control (PL16L01EC) — Offset ABCh

Physical Layer 16.0 GT/s Lane 01 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + ABCh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 1 Transmitter Preset (UP16L1TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 1 Transmitter Preset (DP16L1TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 0 Transmitter Preset (UP16L0TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 0 Transmitter Preset (DP16L0TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.120 Physical Layer 16.0 GT/s Lane 23 Equalization Control (PL16L23EC) — Offset ABEh

Physical Layer 16.0 GT/s Lane 23 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + ABEh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 3 Transmitter Preset (UP16L3TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 3 Transmitter Preset (DP16L3TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 2 Transmitter Preset (UP16L2TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 2 Transmitter Preset (DP16L2TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.121 Physical Layer 16.0 GT/s Lane 45 Equalization Control (PL16L45EC) — Offset AC0h

Physical Layer 16.0 GT/s Lane 45 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + AC0h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 5 Transmitter Preset (UP16L5TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 5 Transmitter Preset (DP16L5TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 4 Transmitter Preset (UP16L4TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 4 Transmitter Preset (DP16L4TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.122 Physical Layer 16.0 GT/s Lane 67 Equalization Control (PL16L67EC) — Offset AC2h

Physical Layer 16.0 GT/s Lane 67 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + AC2h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 7 Transmitter Preset (UP16L7TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 7 Transmitter Preset (DP16L7TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 6 Transmitter Preset (UP16L6TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 6 Transmitter Preset (DP16L6TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.123 Physical Layer 16.0 GT/s Lane 89 Equalization Control (PL16L89EC) — Offset AC4h

Physical Layer 16.0 GT/s Lane 89 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + AC4h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 9 Transmitter Preset (UP16L9TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 9 Transmitter Preset (DP16L9TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 8 Transmitter Preset (UP16L8TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 8 Transmitter Preset (DP16L8TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.124 Physical Layer 16.0 GT/s Lane 1011 Equalization Control (PL16L1011EC) — Offset AC6h

Physical Layer 16.0 GT/s Lane 1011 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + AC6h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 11 Transmitter Preset (UP16L11TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 11 Transmitter Preset (DP16L11TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 10 Transmitter Preset (UP16L10TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 10 Transmitter Preset (DP16L10TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.125 Physical Layer 16.0 GT/s Lane 1213 Equalization Control (PL16L1213EC) — Offset AC8h

Physical Layer 16.0 GT/s Lane 1213 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + AC8h	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 13 Transmitter Preset (UP16L13TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 13 Transmitter Preset (DP16L13TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 12 Transmitter Preset (UP16L12TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 12 Transmitter Preset (DP16L12TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.126 Physical Layer 16.0 GT/s Lane 1415 Equalization Control (PL16L1415EC) — Offset ACAh

Physical Layer 16.0 GT/s Lane 1415 Equalization Control Register

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:6, F:0] + ACAh	FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RW	**Upstream Port 16 GT/s Port Lane 15 Transmitter Preset (UP16L15TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
11:8	Fh RW	**Downstream Port 16 GT/s Lane 15 Transmitter Preset (DP16L15TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
7:4	Fh RW	**Upstream Port 16 GT/s Port Lane 14 Transmitter Preset (UP16L14TP):** Field contains the Transmitter Preset value sent or received during Port 16 GT/s Link Equalization. Port Direction: Downstream Port Crosslink Supported: Any Usage: Contains value sent on the associated Lane during Link EQ.
3:0	Fh RW	**Downstream Port 16 GT/s Lane 14 Transmitter Preset (DP16L14TP):** Transmitter Preset used for 16 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

6.127 VNN Removal Control (VNNREMCTL) — Offset C70h

VNN Removal Control

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + C70h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Receiver Eye Margin Error Tracking Mechanism Disable (REMETMD):** When this bit is set MAC will not track Error count during Receiver Equalization (EQ Phase 2 - PDMI, EQ Phase 3 - PCIe). Preset/Coeff evaluation will be based on FOM returned by PHY alone. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
30:9	0h RO	**Reserved**
8	0h RW	**Function Disable VNN Removal (FDVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link is function disable, so that VNN is allow to be remove when platform permitted.
7	0h RW	**Hot Plug VNN Removal Enable (HPVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when clkreq_b deassetion in Detect state, so that VNN is allow to be remove when platform permitted.
6	0h RW	**Detect Not PCIe VNN Removal Enable (DNPVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering Detect Not PCIe when link is unown, so that VNN is allow to be remove when platform permitted.
5	0h RW	**RTD3 VNN Removal Enable (RTD3VNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering L23 due to RTD3, so that VNN is allow to be remove when platform permitted.
4	0h RW	**Link Disable VNN Removal Enable (LDVNNRE):** When assert, controller will assert vnnremoval_en_b to SOC when link entering Link Disable, so that VNN is allow to be remove when platform permitted.
3:2	0h RW	**Internal States Propagation Latency For VNN Removal Exit (ISPLFVNNRE):** This register configure internal delay of IP to allow boundary lock to deassert. This counter will start count after contexts propagation is done and early boundary lock is deassert. 00 8 osc clocks 01 16 osc clocks 10 32 osc clocks 11 64 osc clocks Note: For each x4 instance, only the value from Port 1 is used. This is a per controller register
1:0	1h RW	**Link Reset Suppression Latency For VNN Removal Exit (LRSLFVNNRE):** This register configure the Link Reset Suppression latency after pmc had deassert restore_b during VNN Removal, and link clock pll had achieved lock. Link reset will be suppress upon IP Inaccessible exit with restore_b assertion, and the counter will start count when restore_b deassert with link clock had achieved lock. After timer expire, link reset will be deassert. 00 4 osc clocks 01 8 osc clocks 10 16 osc clocks 11 32 osc clocks Note: For each x4 instance, only the value from Port 1 is used. This is a per controller register

6.128 VNN Removal Save And Restore Hardware Contexts 1 (VNNRSNRC1) — Offset C74h

VNN Removal Save And Restore Hardware Contexts 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + C74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Spare 31 State Contexts (VNNS31SC):** Spare Flag for VNN Removal
30	0h RW	**VNN Spare 30 State Contexts (VNNS30SC):** Spare Flag for VNN Removal
29	0h RW	**VNN Spare 29 State Contexts (VNNS29SC):** Spare Flag for VNN Removal
28	0h RW	**VNN Spare 28 State Contexts (VNNS28SC):** Spare Flag for VNN Removal
27	0h RW	**VNN Spare 27 State Contexts (VNNS27SC):** Spare Flag for VNN Removal
26	0h RW	**VNN Spare 26 State Contexts (VNNS26SC):** Spare Flag for VNN Removal
25	0h RW	**VNN Spare 25 State Contexts (VNNS25SC):** Spare Flag for VNN Removal
24	0h RW	**VNN Spare 24 State Contexts (VNNS24SC):** Spare Flag for VNN Removal
23	0h RW	**VNN Spare 23 State Contexts (VNNS23SC):** Spare Flag for VNN Removal
22	0h RW	**VNN Spare 22 State Contexts (VNNS22SC):** Spare Flag for VNN Removal
21	0h RW	**VNN Spare 21 State Contexts (VNNS21SC):** Spare Flag for VNN Removal
20	0h RW	**VNN Spare 20 State Contexts (VNNS20SC):** Present Detect State Flag (PDS) information stored to this flag, so that link will restore back PDS upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
19	0h RW	**VNN Spare 19 State Contexts (VNNS19SC):** Spare Flag for VNN Removal
18	0h RW	**VNN Spare 18 State Contexts (VNNS18SC):** Spare Flag for VNN Removal
17	0h RW	**VNN Spare 17 State Contexts (VNNS17SC):** Spare Flag for VNN Removal
16	0h RW	**VNN Spare 16 State Contexts (VNNS16SC):** Spare Flag for VNN Removal
15	0h RW	**VNN Spare 15 State Contexts (VNNS15SC):** Spare Flag for VNN Removal
14	0h RW	**VNN Spare 14 State Contexts (VNNS14SC):** Spare Flag for VNN Removal

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**VNN Spare 13 State Contexts (VNNS13SC):** Spare Flag for VNN Removal
12	0h RW	**VNN Spare 12 State Contexts (VNNS12SC):** Spare Flag for VNN Removal
11	0h RW	**VNN Spare 11 State Contexts (VNNS11SC):** Spare Flag for VNN Removal
10	0h RW	**VNN Spare 10 State Contexts (VNNS10SC):** Spare Flag for VNN Removal
9	0h RW	**VNN Spare 9 State Contexts (VNNS9SC):** Spare Flag for VNN Removal
8	0h RW	**VNN Spare 8 State Contexts (VNNS8SC):** Spare Flag for VNN Removal
7	0h RW	**VNN Spare 7 State Contexts (VNNS7SC):** Spare Flag for VNN Removal
6	0h RW	**VNN Spare 6 State Contexts (VNNS6SC):** Spare Flag for VNN Removal
5	0h RW	**VNN Spare 5 State Contexts (VNNS5SC):** Link Down indicaton will be reflected here.
4	0h RW	**VNN Spare 4 State Contexts (VNNS4SC):** DL_ACTIVE (LA) information stored to this flag, so that link will restore back LA upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
3	0h RW	**VNN Spare 3 State Contexts (VNNS3SC):** Legacy Present Detect State Flag (PDS) information stored to this flag, so that link will restore back Legacy PDS Flag upon VNN Removal restoration. Based on PCIEALC.PDSP, this information or New PDS Implementation Context[20] will be selected. Writing to this registers have no effect unless restore_b is assert. Legacy Present Detect State Flag (PDS) information stored to this flag, so that link will restore back Legacy PDS Flag upon VNN Removal restoration. Based on PCIEALC.PDSP, this information or New PDS Implementation Context[20] will be selected. Writing to this registers have no effect unless restore_b is assert.
2	0h RW	**VNN Detect Not PCIe State Contexts (VNNDNPSC):** When Link entered Detect Not PCIe state, LTSSM will push the link Detect Not PCIe state information to this flag, so that link will restore back to Detect Not PCIe state behavior upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
1	0h RW	**VNN L23 State Contexts (VNNL23SC):** When Link entered L23 state, LTSSM will push the link L23 state information to this flag, so that link will restore back to L23 state behavior (Actual State restore to Detect Quiet PG) upon VNN Removal restoration. Writing to this registers have no effect unless restore_b is assert.
0	0h RW	**VNN Link Disable State Contexts (VNNLDSC):** When Link entered Link Disable state, LTSSM will push the link disable state information to this flag, so that link will restore back to disable state behavior (Actual State restore to Detect Quiet PG) upon VNN Removal restoration.

6.129 Physical Layer 16.0 GT/s Margining Extended Capability Header (PL16MECH) — Offset EDCh

Physical Layer 16.0 GT/s Margining Extended Capability Header

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + EDCh	00010027h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.
19:16	1h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15:0	0027h RW/O	**PCI Express Extended Capability ID (PCIECID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Physical Layer 16.0 GT/s Margining Capability

6.130 Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status (PL16MPCPS) — Offset EE0h

Physical Layer 16.0 GT/s Margining Port Capabilities and Port Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + EE0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**Margining Software Ready (MARGINSWRDY):** When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO/V	**Margining Ready (MARGINRDY):** Indicates when the Margining feature is ready to accept margining commands. Behavior is undefined if this bit is Clear and, for any Lane, any of the Receiver Number, Margin Type, Usage Model, or Margin Payload fields are written. If Margining uses Driver Software is Set, Margining Ready must be Set no later than 100 ms after the later of Margining Software Ready becoming Set or the link training to 16.0 GT/s. If Margining uses Driver Software is Clear, Margining Ready must be Set no later than 100 ms after the Link trains to 16.0 GT/s.
15:1	0h RO	**Reserved**
0	0h RW/O	**Margining uses Driver Software (MARGINDRISW):** If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. In this case the value read from Margining Software Ready is undefined

6.131 Physical Layer 16.0 GT/s Lane0 Margin Control and Status (PL16L0MCS) — Offset EE4h

Physical Layer 16.0 GT/s Lane0 Margin Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:6, F:0] + EE4h	00009C38h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO/V	**Margin Payload Status (MPSTS):** This field is only meaningful, when the Margin Type This field must be reset to the default value if the Port goes to DL_Down status.
23	0h RO	**Reserved**
22	0h RO/V	**Usage Model Status (UMS):** This field must be reset to the default value if the Port goes to DL_Down status.
21:19	0h RO/V	**Margin Type Status (MTS):** This field must be reset to the default value if the Port goes to DL_Down status.
18:16	0h RO/V	**Receiver Number Status (RNS):** This field must be reset to the default value if the Port goes to DL_Down status.
15:8	9Ch RW	**Margin Payload (MP):** This fields value is used in conjunction with the Margin Type field. The default value is 9Ch. This field must be reset to the default value if the Port goes to DL_Down status.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Usage Model (UM):** The default value is 0b. This field must be reset to the default value if the Port goes to DL_Down status.
5:3	7h RW	**Margin Type (MT):** The default value is 111b. This field must be reset to the default value if the Port goes to DL_Down status.
2:0	0h RW	**Receiver Number (RN):** The default value is 000b. This field must be reset to the default value if the Port goes to DL_Down status.

6.132 Physical Layer 16.0 GT/s Lane1 Margin Control and Status (PL16L1MCS) — Offset EE8h

Physical Layer 16.0 GT/s Lane1 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.133 Physical Layer 16.0 GT/s Lane2 Margin Control and Status (PL16L2MCS) — Offset EECh

Physical Layer 16.0 GT/s Lane2 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.134 Physical Layer 16.0 GT/s Lane3 Margin Control and Status (PL16L3MCS) — Offset EF0h

Physical Layer 16.0 GT/s Lane3 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.135 Physical Layer 16.0 GT/s Lane4 Margin Control and Status (PL16L4MCS) — Offset EF4h

Physical Layer 16.0 GT/s Lane4 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.136 Physical Layer 16.0 GT/s Lane5 Margin Control and Status (PL16L5MCS) — Offset EF8h

Physical Layer 16.0 GT/s Lane5 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.137 Physical Layer 16.0 GT/s Lane6 Margin Control and Status (PL16L6MCS) — Offset EFCh

Physical Layer 16.0 GT/s Lane6 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.138 Physical Layer 16.0 GT/s Lane7 Margin Control and Status (PL16L7MCS) — Offset F00h

Physical Layer 16.0 GT/s Lane7 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.139 Physical Layer 16.0 GT/s Lane8 Margin Control and Status (PL16L8MCS) — Offset F04h

Physical Layer 16.0 GT/s Lane8 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.140 Physical Layer 16.0 GT/s Lane9 Margin Control and Status (PL16L9MCS) — Offset F08h

Physical Layer 16.0 GT/s Lane9 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.141 Physical Layer 16.0 GT/s Lane10 Margin Control and Status (PL16L10MCS) — Offset F0Ch

Physical Layer 16.0 GT/s Lane10 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.142 Physical Layer 16.0 GT/s Lane11 Margin Control and Status (PL16L11MCS) — Offset F10h

Physical Layer 16.0 GT/s Lane11 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.143 Physical Layer 16.0 GT/s Lane12 Margin Control and Status (PL16L12MCS) — Offset F14h

Physical Layer 16.0 GT/s Lane12 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.144 Physical Layer 16.0 GT/s Lane13 Margin Control and Status (PL16L13MCS) — Offset F18h

Physical Layer 16.0 GT/s Lane13 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.145 Physical Layer 16.0 GT/s Lane14 Margin Control and Status (PL16L14MCS) — Offset F1Ch

Physical Layer 16.0 GT/s Lane14 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

6.146 Physical Layer 16.0 GT/s Lane15 Margin Control and Status (PL16L15MCS) — Offset F20h

Physical Layer 16.0 GT/s Lane15 Margin Control and Status Register

Note: Bit definitions are the same as PL16L0MCS, offset EE4h.

7 Dynamic Tuning Technology Registers (D4:F0)

Dynamic Tuning Technology device. This chapter documents the registers in Bus: 0, Device: 4, Function: 0.

Table 7-1. Summary of Bus: 0, Device: 4, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID_0_4_0_PCI)	8086h
2h	2	Device ID (DID_0_4_0_PCI)	461Dh
4h	2	PCI Command (PCICMD_0_4_0_PCI)	0000h
6h	2	PCI Status (PCISTS_0_4_0_PCI)	0090h
8h	1	Revision ID (RID_0_4_0_PCI)	00h
9h	1	Class Code (CC_0_4_0_PCI)	00h
Ah	2	Extended Class Code (CC_0_4_0_NOPI_PCI)	1180h
Ch	1	Cache Line Size Register (CLS_0_4_0_PCI)	00h
Dh	1	Master Latency Timer (MLT_0_4_0_PCI)	00h
Eh	1	Header Type (HDR_0_4_0_PCI)	00h
Fh	1	Built In Self Test (BIST_0_4_0_PCI)	00h
10h	8	Thermal Controller Base Address (TMBAR_0_4_0_PCI)	0000000000000004h
2Ch	2	Subsystem Vendor ID (SVID_0_4_0_PCI)	0000h
2Eh	2	Subsystem ID (SID_0_4_0_PCI)	0000h
34h	1	Capability Pointer (CAPPOINT_0_4_0_PCI)	90h
3Ch	1	Interrupt Line Register (INTRLINE_0_4_0_PCI)	00h
3Dh	1	Interrupt Pin Register (INTRPIN_0_4_0_PCI)	01h
3Eh	1	Minimum Guaranteed (MINGNT_0_4_0_PCI)	00h
3Fh	1	Maximum Latency (MAXLAT_0_4_0_PCI)	00h
54h	4	Device Enable (DEVEN_0_4_0_PCI)	0003D4DFh
E4h	4	Capabilities A (CAPID0_A_0_4_0_PCI)	00000000h
E8h	4	Capabilities B (CAPID0_B_0_4_0_PCI)	00000000h

7.1 Vendor ID (VID_0_4_0_PCI) — Offset 0h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VID:** PCI standard identification for Intel.

7.2 Device ID (DID_0_4_0_PCI) — Offset 2h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 2h	461Dh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	461Dh RW/V/L	**DID:** Identifier assigned to the Thermal Management Controller.

7.3 PCI Command (PCICMD_0_4_0_PCI) — Offset 4h

This register provides basic control over the DTT devices ability to respond to PCI cycles.

The PCICMD Register in the DTT disables the DTT PCI compliant master accesses to main memory.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**INTDIS:** This bit, when set, disables the device from asserting INTA#.
9	0h RO	**FB2B:** The DTT device does not implement this bit and it is hardwired to a 0.
8	0h RO	**SERRE:** The DTT device does not implement this bit and it is hardwired to a 0.
7	0h RO	**ADSTEP:** The DTT device does not implement this bit and it is hardwired to a 0.
6	0h RO	**PERRE:** This bit is hardwired to 0. The DTT Device belongs to the category of devices that does not corrupt programs or data in system memory or hard drives. It therefore ignores any parity error that it detects and continues with normal operation.
5	0h RO	**VGASNOOP:** The DTT device does not implement this bit and it is hardwired to a 0.
4	0h RO	**MWIE:** This bit is hardwired to 0. The DTT Device will never issue memory write and invalidate commands, and therefore has no need to implement this bit.
3	0h RO	**SCE:** The DTT device does not implement this bit and it is hardwired to a 0.
2	0h RW	**BME:** The DTT Device is enabled to function as a PCI-compliant bus master when this bit is set. If it is not set, bus mastering is disabled.
1	0h RW	**MAE:** The DTT Device will allow access to thermal registers when this bit is set. If it is not set, access to memory mapped thermal registers is disabled.
0	0h RO	**IOAE:** The DTT device does not implement this bit and it is hardwired to a 0.

7.4 PCI Status (PCISTS_0_4_0_PCI) — Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant Master Abort (MA) and PCI compliant Target Abort (TA).

PCISTS also indicates the DEVSEL# timing that has been set by the DTT Device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 6h	0090h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**DPE:** The DTT device does not implement this bit and it is hardwired to a 0.
14	0h RO	**SSE:** This bit is hardwired to zero. The DTT Device never asserts SERR#, and therefore it has no need to implement this bit.
13	0h RO	**RURS:** The DTT device does not implement this bit and it is hardwired to a 0.
12	0h RO	**RCAS:** The DTT device does not implement this bit and it is hardwired to a 0.
11	0h RO	**STAS:** This bit is hardwired to 0. The DTT Device will not generate a Target Abort DMI completion packet or Special Cycle, and therefore it has no need to implement this bit.
10:9	0h RO	**DEVT:** These bits are hardwired to 0. Device 4 does not physically connect to PCI_A.
8	0h RO	**DPD:** This bit is hardwired to 0. PERR signaling and messaging are not implemented by the DTT Device, and therefore it has no need to implement this bit.
7	1h RO	**FB2B:** This bit is hardwired to 1. Device 4 does not physically connect to PCI_A, so this bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the DTT Device.
6	0h RO	**Reserved**
5	0h RO	**PCI66M:** The DTT device does not implement this bit and it is hardwired to a 0.
4	1h RO	**CLIST:** This bit is set to 1 to indicate that the register at 34h provides an offset into the function. PCI Configuration Space containing a pointer to the location of the first item in the list.
3	0h RW/V/L	**IS:** Reflects the state of the INTA# signal at the input of the enable/disable circuit. This bit is set by HW to 1 when the INTA# is asserted and reset by HW to 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the 0.4.0.PCICMD register).
2:0	0h RO	**Reserved**

7.5 Revision ID (RID_0_4_0_PCI) — Offset 8h

This register contains the revision number of the DTT Device.

This is an 8-bit value that indicates the revision identification number for the device.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Revision ID Upper Bits (RID_MSB):** DTT device Revision ID 4 upper bits.
3:0	0h RW/L	**Revision ID Lower Bits (RID):** DTT device Revision ID 4 lower bits.

7.6 Class Code (CC_0_4_0_PCI) — Offset 9h

This register contains the device programming interface information related to the Sub-Class Code and

Base Class Code definition for the DTT Device. This register also contains the Base Class Code and the

function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 9h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**PI:** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

7.7 Extended Class Code (CC_0_4_0_NOPI_PCI) — Offset Ah

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the DTT Device.

This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + Ah	1180h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	11h RO	**BCC:** This is an 8-bit value that indicates the base class code for the DTT Thermal Controller. This code has the value 11h, indicating a device that is used for data acquisition and signal processing.
7:0	80h RO	**SUBCC:** The code is 80h which indicates Other Data Acquisition and Signal Processing Controllers.

7.8 Cache Line Size Register (CLS_0_4_0_PCI) — Offset Ch

The DTT Device does not support this register as a PCI subordinate.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**CLS:** This field is hardwired to 0. The DTT as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

7.9 Master Latency Timer (MLT_0_4_0_PCI) — Offset Dh

The DTT Device does not support the programmability of the master latency timer because it does

not perform bursts.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MLT:** This field is hardwired to 0. The DTT Device does not support perform bursts.

7.10 Header Type (HDR_0_4_0_PCI) — Offset Eh

This register identifies the header layout of the configuration space.

No physical register exists at this location.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**HDR:** This field always returns 0 to indicate that the DTT device is a single function device with standard header layout.

7.11 Built In Self Test (BIST_0_4_0_PCI) — Offset Fh

This register is used for control and status of Built In Self Test (BIST).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BS:** This bit is hardwired to zero. The DTT Device does not support BIST.
6:0	0h RO	**Reserved**

7.12 Thermal Controller Base Address (TMBAR_0_4_0_PCI) — Offset 10h

This is the base address for the Thermal Controller Memory Mapped space.

There is no physical memory within this 32KB window that can be addressed.

The 32KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space.

All TMBAR space maps the access to this memory space towards MCHBAR space.

For details of this BAR, refer to the MCHBAR specifications.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:4, F:0] + 10h	0000000000000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:43	0h RO	**Reserved**
42:17	0000000h RW	**TMMBA:** This field corresponds to bits 41 to 16 of the base address TMBAR address space. BIOS will program this register resulting in a base address for a 64KB block of contiguous memory address space. This register ensures that a naturally aligned 64KB space is allocated within total addressable memory space. The DTT driver uses this base address to program all Thermal and Throttling control register set.
16:4	0000h RO	**ADM:** Hardwired to 0s to indicate at least 128KB address range.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**PM:** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**MT:** Hardwired to 10 to indicate 64-bit address.
0	0h RO	**MIOS:** Hardwired to 0 to indicate memory space.

7.13 Subsystem Vendor ID (SVID_0_4_0_PCI) — Offset 2Ch

This value is used to identify the vendor of the subsystem.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SUBVID:** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only. **Locked by:** WRITE_ONCE_LOCK.SUBVID_WOL

7.14 Subsystem ID (SID_0_4_0_PCI) — Offset 2Eh

This value is used to identify a particular subsystem.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SUBID:** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only. **Locked by:** WRITE_ONCE_LOCK.SUBID_WOL

7.15 Capability Pointer (CAPPOINT_0_4_0_PCI) — Offset 34h

CAPPOINT provides the offset that is the pointer to the location of the first device capability in the capability list.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 34h	90h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	90h RW/V/L	**CAPPV:** This field contains an offset into the functions PCI Configuration Space for the first item in the New Capabilities Linked List which is the MSI Capabilities ID register at address 90h or the Power Management Capabilities ID registers at address D0h. The value is determined by CAPL[0].

7.16 Interrupt Line Register (INTRLINE_0_4_0_PCI) — Offset 3Ch

Used to communicate interrupt line routing information.

BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system.

The value indicates to which input of the system interrupt controller this devices interrupt pin is connected.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**INTCON:** Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this devices interrupt pin is connected.

7.17 Interrupt Pin Register (INTRPIN_0_4_0_PCI) — Offset 3Dh

This register specifies which interrupt pin this device uses.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**INTPIN:** As a single function device, the DTT device specifies INTA as its interrupt pin. 01h = INTA.

7.18 Minimum Guaranteed (MINGNT_0_4_0_PCI) — Offset 3Eh

This register is hardwired to zero.

The DTT Device does not burst as a PCI compliant master.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MGV:** These bits are hardwired to zero. The DTT Device does not burst as a PCI compliant master.

7.19 Maximum Latency (MAXLAT_0_4_0_PCI) — Offset 3Fh

This register are hardwired to zero.

The DTT Device has no specific requirements for how often it needs to access the PCI bus.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MLV:** These bits are hardwired to zero. The DTT Device has no specific requirements for how often it needs to access the PCI bus.

7.20 Device Enable (DEVEN_0_4_0_PCI) — Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:4, F:0] + 54h	0003D4DFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/L	**D6F1EN:** 0: Bus 0 Device 6 Function 1 is disabled and not visible. 1: Bus 0 Device 6 Function 1 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 1 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG61D
17	1h RW/L	**D10EN:** 0: Bus 0 Device 10 is disabled and not visible. 1: Bus 0 Device 10 is enabled and visible. This bit will be set to 0b and remain 0b if Device 10 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.DEV10_DISABLED
16	1h RW/L	**D6F2EN:** 0: Bus 0 Device 6 Function 2 is disabled and not visible. 1: Bus 0 Device 6 Function 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 2 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG62D

Bit Range	Default & Access	Field Name (ID): Description
15	1h RW/L	**D8EN:** 0: Bus 0 Device 8 is disabled and not visible. 1: Bus 0 Device 8 is enabled and visible. This bit will be set to 0b and remain 0b if Device 8 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.GMM_DIS
14	1h RW/L	**D14F0EN:** VMD Enable - 0: Bus 0 Device 14 Function 0 is disabled and hidden. 1: Bus 0 Device 14 Function 0 is enabled and visible. **Locked by:** CAPID0_B_0_0_0_PCI.VMD_DIS
13	0h RW/L	**D6F0EN:** 0: Bus 0 Device 6 Function 0 is disabled and not visible. 1: Bus 0 Device 6 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 0 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG60D
12	1h RW/L	**D9EN:** 0: Bus 0 Device 9 is disabled and not visible. 1: Bus 0 Device 9 is enabled and visible. This bit will be set to 0b and remain 0b if Device 9 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.NPK_DIS
11	0h RO	**Reserved**
10	1h RW/L	**D5EN:** 0: Bus 0 Device 5 is disabled and not visible. 1: Bus 0 Device 5 is enabled and visible. This bit will be set to 0b and remain 0b if Device 5 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.IMGU_DIS
9:8	0h RO	**Reserved**
7	1h RW/L	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.CDD
6	1h RW/L	**D3F7EN:** NVMe - Device 3 function 7 enable. 0: Bus 0 Device 3 function 7 is disabled and hidden. 1: Bus 0 Device 3 function 7 is enabled and visible. This bit will be set to 0b and remain 0b if Device 3 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F7D
5	0h RW/L	**D3F0EN:** NVMe - Device 3 function 0 enable. 0: Bus 0 Device 3 function 0 is disabled and hidden. 1: Bus 0 Device 3 function 0 is enabled and visible. This bit will be set to 0b and remain 0b if Device 3 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F0D
4	1h RW/L	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.IGD

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW/L	**D1F0EN:** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if PEG10 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG10D
2	1h RW/L	**D1F1EN:** 0: Bus 0 Device 1 Function 1 is disabled and hidden. 1: Bus 0 Device 1 Function 1 is enabled and visible. **Locked by:** CAPID0_A_0_0_0_PCI.PEG11D
1	1h RW/L	**D1F2EN:** 0: Bus 0 Device 1 Function 2 is disabled and hidden. 1: Bus 0 Device 1 Function 2 is enabled and visible. **Locked by:** CAPID0_A_0_0_0_PCI.PEG12D
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

7.21 Capabilities A (CAPID0_A_0_4_0_PCI) — Offset E4h

Processor capability enumeration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:4, F:0] + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**NVME Device 3 Function 0 Disable (NVME_F0D):** 0: Device 3 Function 0 and associated memory spaces are accessible. 1: Device 3 Function 0 (NVMe F0) and associated memory space are disabled by hardwiring the D3F0EN field, bit 5 of the SoC Device Enable register
30	0h RW/L	**PCIe Device 1 Function 2 Disable (PEG12D):** 0: Device 1 Function 2 and associated memory spaces are accessible. 1: Device 1 Function 2 and associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
29	0h RW/L	**PCIe Device 1 Function 1 Disable (PEG11D):** 0: Device 1 Function 1 and associated memory spaces are accessible. 1: Device 1 Function 1 and associated memory and IO spaces are disabled by hardwiring the D1F1EN field, bit 2 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
28	0h RW/L	**PCIe Device 1 Function 0 Disable (PEG10D):** 0: Device 1 Function 0 and associated memory spaces are accessible. 1: Device 1 Function 0 and associated memory and IO spaces are disabled by hardwiring the D1F0EN field, bit 3 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/L	**PCIe Link Width Up-config Disable (PELWUD):** 0: Link width upconfig is supported. The Processor advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The Processor does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	0h RW/L	**DMI Width (DW):** 0: DMI x4 1: DMI x2
25	0h RW/L	**DRAM ECC Disable (ECCDIS):** 0: ECC is supported 1: ECC is not supported
24	0h RW/L	**Force DRAM ECC Enable (FDEE):** 0: DRAM ECC optional via software. 1: DRAM ECC enabled. MCHBAR C0MISCCTL bit [0] and C1MISCCTL bit [0] are forced to 1 and Read-Only. Note that FDEE and ECCDIS must not both be set to 1.
23	0h RW/L	**VT-d Disable (VTDD):** 0: VT-d is supported 1: VT-d is not supported
22	0h RW/L	**DMI GEN2 Disable (DMIG2DIS):** 0: Capable of running DMI in Gen 2 mode 1: Not capable of running DMI in Gen 2 mode
21	0h RO	**Reserved**
20:19	0h RW/L	**DRAM Maximum Size per Channel (DDRSZ):** This field defines the maximum allowed memory size per channel. • 0: Unlimited (64GB per channel) • 1: Maximum 8GB per channel • 2: Maximum 4GB per channel • 3: Maximum 2GB per channel
18	0h RW/L	**PCIe Controller Device 6 Function 0 Disabled (PEG60D):** PCIe Controller Device 6 Function 0 is disabled 0: Device 6 Function 0 is supported 1: Device 6 Function 0 is not supported
17	0h RW/L	**DRAM 1N Timing Disable (D1NM):** 0: Part is capable of supporting 1n mode timings on the DDR interface. 1: Part is not capable of supporting 1n mode. Only supported timings are 2n or greater.
16	0h RO	**Reserved**
15	0h RW/L	**DTT Device Disable (CDD):** 0: DTT Device enabled. 1: DTT Device disabled.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/L	**2 DIMMs Per Channel Enable (DDPCD):** Allows Dual Channel operation but only supports 1 DIMM per channel. 0: 2 DIMMs per channel enabled 1: 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero. (MCHBAR offset 260h, bits 22-23 for channel 0 and MCHBAR offset 660h, bits 22-23 for channel 1)
13	0h RW/L	**X2APIC Enable (X2APIC_EN):** Extended Interrupt Mode. 0b: Hardware does not support Extended APIC mode. 1b: Hardware supports Extended APIC mode.
12	0h RW/L	**Dual Memory Channel Support (PDCD):** 0: Capable of Dual Channel 1: Not Capable of Dual Channel - only single channel capable.
11	0h RW/L	**Internal Graphics Disable (IGD):** 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RW/L	**DID0 Override Enable (DID0OE):** 0: Disable ability to override DID0 - For production 1: Enable ability to override DID - For debug and samples only
9	0h RO	**Reserved**
8	0h RW/L	**2 Level Memory Support (2LM_SUPPORTED):** 0: 2 Level Memory (2LM) is not supported. Only 1LM is supported. 1: 2 Level Memory (2LM) is supported
7:4	0h RW/L	**Compatibility Revision ID (CRID):** Compatibility Revision ID
3	0h RW/L	**Memory Overclocking (DDR_OVERCLOCK):** Memory Overclocking support 0: Memory Overclocking is not supported 1: Memory Overclocking is supported
2	0h RO	**Reserved**
1	0h RW/L	**NVME F7D (NVME_F7D):** 0: Device 3 Function 7 and associated memory spaces are accessible. 1: Device 3 Function 7 (NVMe F7) and associated memory space are disabled by hardwiring the D3F7EN field, bit 6 of the SoC Device Enable register
0	0h RO	**Reserved**

7.22 Capabilities B (CAPID0_B_0_4_0_PCI) — Offset E8h

Processor capability enumeration.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:4, F:0] + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Image Processing Unit (IPU) Disable (IPU_DIS):** 0: Device 5 associated memory spaces are accessible. 1: Device 5 associated memory and IO spaces are disabled.
30	0h RW/L	**Trace Hub Disable (TRACE_HUB_DIS):** 0: Trace Hub associated memory spaces are accessible. 1: Trace Hub associated memory and IO spaces are disabled.
29	0h RW/L	**Overclocking Enabled (OC_ENABLED):** 0: Overclocking is Disabled 1: Overclocking is Enabled If overclocking is enabled, MSR FLEX_RATIO.OC_BINS contains how many bits of over-clocking are supported. The encoding is as follows: 0: Overclocking is Disabled 1-6: Turbo ratio limits can be incremented by this amount 7: Unlimited If overclocking is disabled, FLEX_RATIO.OC_BINS is meaningless.
28	0h RW/L	**SMT Capability (SMT):** This setting indicates whether the processor is SMT (HyperThreading) capable.
27:25	0h RW/L	**Cache Size (CACHESZ):** This setting indicates the supporting cache sizes.
24	0h RW/L	**SVM Disable (SVM_DISABLE):** 0: SVM enabled 1: SVM disabled
23:21	0h RW/L	**Memory 100MHz Reference Clock (PLL_REF100_CFG):** DDR Maximum Frequency Capability with 100MHz memory reference clock (ref_clk). 0: 100 MHz memory reference clock is not supported 1-6: Reserved 7: Unlimited
20	0h RW/L	**PCIe Gen 3 Disable (PEGG3_DIS):** 0: Capable of running any of the Gen 3-compliant PCIe controllers in Gen 3 mode (Devices 0/1/x, 0/6/x) 1: Not capable of running any of the PCIe controllers in Gen 3 mode
19	0h RW/L	**Processor Package Type (PKGTYP):** This setting indicates the CPU Package Type.
18:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/L	**PCIe x16 Disable (PEGX16D):** 0: Capable of x16 PCIe Port 1: Not Capable of x16 PCIe port, instead PCIe limited to x8 and below. Causes PCIe port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down (unless in use by the other PEG port or the embedded Display Port), and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down.)
15	0h RW/L	**DMI Gen 3 Disable (DMIG3DIS):** DMI Gen 3 Disable
14:12	0h RW/L	**2 Level Memory Technology Support (LTECH):** 0: 1LM 1: EDRAM0 3: EDRAM0+1 4: 2LM Other values are reserved.
11	0h RW/L	**HDCP Disable (HDCPD):** 0: Capable of HDCP 1: HDCP Disabled
10	0h RW/L	**Device 10 Disable (DEV10_DISABLED):** Indicates if Device 10 (Crash Log/Telemetry) is disabled. 0: Device 10 capability is present 1: Device 10 is disabled and locked from further enabling
9	0h RO	**Reserved**
8	0h RW/L	**GNA (GMM) Disable (GNA_DIS):** 0: Device 8 associated memory spaces are accessible. 1: Device 8 associated memory and IO spaces are disabled by hardwiring the D8EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
7	0h RW/L	**DDD:** 0: Debug mode 1: Production mode
6:4	0h RO	**Reserved**
3	0h RW/L	**S/H OPI Enable (SH_OPI_EN):** Specifies if OPI or DMI are enabled for S/H models. 0: DMI is enabled 1: OPI is enabled
2	0h RW/L	**VMD Disable (VMD_DIS):** Indicates if VMD is disabled.
1	0h RW/L	**Global Single PCIe Lane (DPEGFX1):** This bit has no effect on Device 1 unless Device 1 is configured for at least two ports via PEG0CFGSEL strap. 0: All PCIe port widths do not depend on their respective BCTRL[VGAEN]. 1: Each PCIe port width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.
0	0h RW/L	**Single PCIe Lane (SPEGFX1):** This bit has no effect on Device 1 unless Device 1 is configured for a single port via PEG0CFGSEL strap. 0: Device 1 Function 0 width does not depend on its BCTRL[VGAEN]. 1: Device 1 Function 0 width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1.

8 Volume Management Device (D14:F0)

This chapter documents the Volume Management Device Registers.

Table 8-1. Summary of Volume Management Device (D14:F0)

Volume Management Device (D14:F0)
Volume Management Device MEMBAR2 Registers

8.1 Volume Management Device (D14:F0)

This section describes the registers in Bus: 0, Device: 14, Function: 0.

8.1.1 Summary of Registers

Table 8-2. Summary of Bus: 0, Device: 14, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID_0_14_0_PCI)	8086h
2h	2	Device ID (DID_0_14_0_PCI)	0000h
4h	2	PCI Command (PCICMD_0_14_0_PCI)	0000h
6h	2	PCI Status (PCISTS_0_14_0_PCI)	0010h
8h	1	Revision ID (RID_0_14_0_PCI)	00h
9h	1	Class Code Register Interface (CCRIF_0_14_0_PCI)	00h
Ah	2	Class Code Register Classes (CCRC_0_14_0_PCI)	0104h
Ch	1	Cache Line Size (CLSR_0_14_0_PCI)	00h
Eh	1	Header Type (HDR_0_14_0_PCI)	80h
10h	8	VMD Configuration Base Address (CFGBAR_0_14_0_PCI)	000000000000000Ch
18h	8	VMD Memory Base Address Range 1 (MEMBAR1_0_14_0_PCI)	000000000000000Ch
20h	8	VMD Memory Base Address Range 2 (MEMBAR2_0_14_0_PCI)	000000000000000Ch
2Ch	2	Subsystem Vendor ID (SVID_0_14_0_PCI)	8086h
2Eh	2	Subsystem ID (SSID_0_14_0_PCI)	0000h
34h	1	Capability Pointer (CAPPTR_0_14_0_PCI)	80h
3Ch	1	Interrupt Line Register (INTL_0_14_0_PCI)	00h
3Dh	1	Interrupt Pin Register (INTPIN_0_14_0_PCI)	00h

8.1.2 Vendor ID (VID_0_14_0_PCI) — Offset 0h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor Identification Number (VENDOR_IDENTIFICATION_NUMBER):** The value is assigned by PCI-SIG to Intel.

8.1.3 Device ID (DID_0_14_0_PCI) — Offset 2h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 2h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Device Identification Number (DEVICE_IDENTIFICATION_NUMBER):** The value in this register specifies the Device ID for the volume Management Device. This value is the same for all instances of the VMD. The value of this register is selected by the DEVID_SELECT field in the VMCONFIG register. Volume Management Device v2.0 for Server uses Device ID values 0x28C0 to 0x28CF.

8.1.4 PCI Command (PCICMD_0_14_0_PCI) — Offset 4h

This register provides basic control over the VMD devices ability to respond to PCI cycles.

The PCICMD Register in the VMD disables the VMD PCI compliant master accesses to main memory.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**INTx Interrupt Disable (INTERRUPT_DISABLE):** VMD does not support the generation of INTx, but VMD-owned devices may. This bit has no effect in hardware. 1: INTx Legacy Interrupt generation is disabled 0: INTx Legacy Interrupt generation is enabled Notes: INTx message received from VMD-owned Root Ports will be routed to the system using the same rules defined in the Root Ports as though they were not VMD-owned. If the VMD driver expects INTx, then the INTPIN registers in the VMD-owned Root Ports and Switches must be programmed by the VMD driver. A write to this register will trigger an interrupt to the VMD driver using the MSI table entry 0.
9	0h RO	**Fast Back To Back Enable (FAST_BACK_TO_BACK_ENABLE):** Not applicable to PCI Express and is hardwired to 0
8	0h RO	**SERR Reporting Enable (SERRE):** SERR Reporting Enable Not supported for VMD. VMD-Owned Root Ports may be programmed by the VMD driver to signal a system error.
7	0h RO	**IDSEL Stepping Wait Cycle Control (IDSEL_STEPPING_WAIT_CYCLE_CONTROL):** Not applicable to internal IIO devices. Hardwired to 0.
6	0h RO	**Parity Error Reporting Enable (PERRE):** Parity Error Reporting Enable Not supported for VMD. VMD-Owned Root Ports still report parity errors separately.
5	0h RO	**VGA Palette Snoop Enable (VGA_PALETTE_SNOOP_ENABLE):** Not applicable to internal IIO devices. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Memory Write and Invalidate Enable Not applicable to internal IIO devices. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Special Cycle Enable Not applicable to DMI/PCI Express devices. Hardwired to 0
2	0h RW	**Bus Master Enable (BME):** Bus Master Enable Virtually, this bit is meant to enable the VMD to master requests to the system. This bit has no effect in hardware. The VMD driver reads this bit to decide how to set corresponding BME bits in the VMD-Owned Root Ports and Endpoint devices. 1: If this bit is set, the VMD driver may allow VMD-Owned Root Ports and Endpoint devices to master requests to the Root Complex. 0: If this bit is clear, the VMD driver must prevent VMD-Owned Root Ports and Endpoint devices from mastering requests to the Root Complex. Notes: A write to this register will trigger an interrupt to the VMD driver using the MSI table entry 0.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable Virtually, this bit is meant to enable the VMD memory BARs. In hardware, this bit will enable CFGBAR and the MEMBAR2 MSI-X table. It has no effect on MEMBAR1 and the rest of MEMBAR2 (which are decoded by the VMD-Owned Root Ports). The VMD driver reads this bit to decide how to set corresponding MSE bits in the VMD-Owned Root Ports and/or Endpoint devices. 1: If this bit is set, CFGBAR and MSI-X tables are enabled for access. The VMD driver may enable VMD-Owned Root Port and Endpoint device BAR regions. 0: If this bit is clear, CFGBAR and MSI-X tables are disabled and inaccessible. The VMD driver must disable VMD-Owned Root Port and Endpoint device BAR regions. Notes: A write to this register will trigger an interrupt to the VMD driver using the MSI table entry 0.
0	0h RO	**I/O Space Enable (IOSE):** I/O Space Enable Not supported by VMD. VMD driver must not enable I/O regions in VMD-Owned Root Port or Endpoint devices.

8.1.5 PCI Status (PCISTS_0_14_0_PCI) — Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant Master Abort (MA)

and PCI compliant Target Abort (TA). PCISTS also indicates the DEVSEL# timing that has been set by the VMD.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Detected Parity Error. Not used by VMD.
14	0h RO	**Signaled System Error (SSE):** Signaled System Error. Not used by VMD.
13	0h RO	**Received Master Abort (RMA):** Received Master Abort. Not used by VMD.
12	0h RO	**Received Target Abort (RTA):** Received Target Abort. Not used by VMD.
11	0h RO	**Signaled Target Abort (STA):** Signaled Target Abort. Not used by VMD.
10:9	0h RO	**Device Select Timing (DEVSEL_TIMING):** Not applicable to PCI Express. Hardwired to 0.
8	0h RO	**Master Data Parity Error (MDPE):** Master Data Parity Error. Not used by VMD.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Fast Back To Back (FAST_BACK_TO_BACK):** Not applicable to VMD. Hardwired to 0.
6	0h RO	**Reserved**
5	0h RO	**PCI66MHz Capable (PCI66MHZ_CAPABLE):** Not applicable to VMD. Hardwired to 0.
4	1h RO	**Capabilities List (CAPABILITIES_LIST):** This bit indicates the presence of a capabilities list structure.
3	0h RO	**INTx Status (INTX_STATUS):** Indicates a pending INTx interrupt. Not used by VMD.
2:0	0h RO	**Reserved**

8.1.6 Revision ID (RID_0_14_0_PCI) — Offset 8h

This register contains the revision number of the VMD Device. This is an 8-bit value that

indicates the revision identification number for the device.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (REVISION_ID):** Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to this register.

8.1.7 Class Code Register Interface (CCRIF_0_14_0_PCI) — Offset 9h

Class Code Register Interface

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 9h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Programming Interface (INTERFACE_F):** VMD can be any value. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK

8.1.8 Class Code Register Classes (CCRC_0_14_0_PCI) — Offset Ah

Class Code Register Classes

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + Ah	0104h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RW/L	**Base Class Code (BASE_CLASS):** VMD can represent itself as any Base Class. Initial Base Class is Mass Storage Device. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
7:0	04h RW/L	**Sub Class (SUB_CLASS):** VMD can be represented with any Sub Class. Initial Sub Class is RAID device. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK

8.1.9 Cache Line Size (CLSR_0_14_0_PCI) — Offset Ch

Cache Line Size Register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** This register is set as RW for compatibility reasons only. Cacheline size is 64B.

8.1.10 Header Type (HDR_0_14_0_PCI) — Offset Eh

This register identifies the header layout of the configuration space.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + Eh	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi function Device (MULTI_FUNCTION_DEVICE):** Set to 1b to indicate functions 1-7 may exist for the device
6:0	00h RO	**Configuration Layout (CONFIGURATION_LAYOUT):** This field identifies the format of the configuration header layout. It is Type 0 for all this device. The default is 00h, indicating a 'endpoint device'.

8.1.11 VMD Configuration Base Address (CFGBAR_0_14_0_PCI) — Offset 10h

VMD Configuration Base Address

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:14, F:0] + 10h	000000000000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW/V	**Memory Base Address (MEMORY_BASE_ADDRESS):** Sets the location of the CFGBAR in memory space. The size is programmed in CFGBARSZ by BIOS. CFGBARSZ specifies the lowest order address bit that is writable. The minimum granularity is 1MB. If CFGBAR.Type = 10b, then bits 63:32 are writable. If CFGBAR.Type = 00b, then bits 63:32 are read-only.
19:4	0h RO	**Reserved**
3	1h RW/L	**BAR is Prefetchable (PREFETCHABLE):** BAR points to Prefetchable memory. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
2:1	2h RW/L	**Memory Type (TYPE_F):** Memory type claimed by this BAR is 64-bit addressable **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
0	0h RO	**Memory Space Indicator (MEMORY_SPACE_INDICATOR):** BAR resource is memory (as opposed to I/O).

8.1.12 VMD Memory Base Address Range 1 (MEMBAR1_0_14_0_PCI) — Offset 18h

VMD Memory Base Address Range 1

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:14, F:0] + 18h	000000000000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
41:12	00000000h RW/V	**Memory Base Address (MEMORY_BASE_ADDRESS):** Sets the location of the MEMBARx in memory space. The size is programmed in MEMBARxSZ by BIOS. MEMBARxSZ specifies the lowest order address bit that is writable. The minimum granularity is 4kB. If MEMBARx.Type = 10b, then bits 63:32 are writable. If MEMBARx.Type = 00b, then bits 63:32 are read-only. If MEMBARxSZ = 0, then all address bits are read-only. If MEMBARxSZ < 12, then the effective value is 12.
11:4	0h RO	**Reserved**
3	1h RW/L	**MEMBAR1 is Prefetchable (PREFETCHABLE):** BAR points to Prefetchable memory. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
2:1	2h RW/L	**Memory Type (TYPE_F):** Memory type claimed by this BAR is 64-bit addressable **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
0	0h RO	**Memory Space Indicator (MEMORY_SPACE_INDICATOR):** BAR resource is memory (as opposed to I/O).

8.1.13 VMD Memory Base Address Range 2 (MEMBAR2_0_14_0_PCI) — Offset 20h

VMD Memory Base Address Range 2

Note: Bit definitions are the same as MEMBAR1_0_14_0_PCI, offset 18h.

8.1.14 Subsystem Vendor ID (SVID_0_14_0_PCI) — Offset 2Ch

Subsystem Vendor ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 2Ch	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RW/L	**Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID):** The default value specifies Intel but can be set to any value once after reset. **Locked by:** IOP_WRITE_ONCE_LOCK_0_14_0_CR.VMD_SVID_WOL

8.1.15 Subsystem ID (SSID_0_14_0_PCI) — Offset 2Eh

This register contain the VMD Subsystem ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**Subsystem_ ID (SUBSYSTEM_ID):** The default value specifies Intel but can be set to any value once after reset. **Locked by:** IOP_WRITE_ONCE_LOCK_0_14_0_CR.VMD_SID_WOL

8.1.16 Capability Pointer (CAPPTR_0_14_0_PCI) — Offset 34h

This register contain the VMD Capability Pointer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 34h	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RO	**Capability Pointer (CAPABILITY_POINTER):** Points to the first capability structure for the device which is the PCIe capability (for devices that support 4kB extended configuration space). A value of zero indicates there are no capability structures (and no extended configuration space).

8.1.17 Interrupt Line Register (INTL_0_14_0_PCI) — Offset 3Ch

Interrupt Line Register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Interrupt Line (INTERRUPT_LINE):** N/A for these devices

8.1.18 Interrupt Pin Register (INTPIN_0_14_0_PCI) — Offset 3Dh

Interrupt Pin Register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 3Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Interrupt Pin (INTP):** Interrupt Pin. N/A since these devices do not generate any interrupt on their own

8.2 Volume Management Device MEMBAR2 Registers

This chapter documents the Volume Management Device's MEMBAR2 registers.

Base address of these registers are defined in the MEMBAR2_0_14_0_PCI register in Bus: 0, Device: 14, Function: 0.

8.2.1 Summary of Registers

Table 8-3. Summary of MEMBER2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	8	MSI-X Table Address Register 0 (MSIXADDR_0_14_0_MEMBAR2[0])	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	MSI-X Message Data Register 0 (MSIXDATA_0_14_0_MEMBAR2[0])	00000000h
Ch	4	MSI-X Vector Control Register 0 (MSIXVCTL_0_14_0_MEMBAR2[0])	00000001h
1000h	8	MSI-X Pending Bit Array (MSIXPBA_0_14_0_MEMBAR2)	0000000000000000h

8.2.2 MSI-X Table Address Register 0 (MSIXADDR_0_14_0_MEMBAR2[0]) — Offset 0h

MSI-X Table Address Register

Note: There are 19 instances of this register. The offset between instances is 16.

Type	Size	Offset	Default
MMIO	64 bit	MEMBER2 + 0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:32	00000000h RW	**MSI-X Upper Address (MSI_X_UPPER_ADDRESS):** Upper address bits used when generating an MSI.
31:2	00000000h RW	**MSI-X Address (MSI_X_ADDRESS):** System-specified message lower address. For MSI-X messages, the contents of this field from an MSI-X Table entry specifies the lower portion of the DWORD-aligned address (AD[31:02]) for the memory write transaction.
1:0	0h RO	**MSG ADD10 (MSG_ADD10):** For proper DWORD alignment, these bits need to be 0's.

8.2.3 MSI-X Message Data Register 0 (MSIXDATA_0_14_0_MEMBAR2[0]) — Offset 8h

MSI-X Message Data Register

Note: There are 19 instances of this register. The offset between instances is 16.

Type	Size	Offset	Default
MMIO	32 bit	MEMBER2 + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Data (MESSAGE_DATA):** System-specified message data.

8.2.4 MSI-X Vector Control Register 0 (MSIXVCTL_0_14_0_MEMBAR2[0]) — Offset Ch

MSI-X Vector Control Register

Note: There are 19 instances of this register. The offset between instances is 16.

Type	Size	Offset	Default
MMIO	32 bit	MEMBER2 + Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RW	**MSI-X Mask (MSI_X_MASK):** When this bit is set, the NTB is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked.

8.2.5 MSI-X Pending Bit Array (MSIXPBA_0_14_0_MEMBAR2) — Offset 1000h

MSI-X Pending Bit Array

Type	Size	Offset	Default
MMIO	64 bit	MEMBER2 + 1000h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18	0h RO/V	**IntPending 18 (INTPENDING_18):** Represents MSI entry 18
17	0h RO/V	**IntPending 17 (INTPENDING_17):** Bit 17 represents MSI entry 17
16	0h RO/V	**IntPending 16 (INTPENDING_16):** Bit 16 represents MSI entry 16
15	0h RO/V	**IntPending 15 (INTPENDING_15):** Bit 15 represents MSI entry 15
14	0h RO/V	**IntPending 14 (INTPENDING_14):** Bit 14 represents MSI entry 14
13	0h RO/V	**IntPending 13 (INTPENDING_13):** Bit 13 represents MSI entry 13
12	0h RO/V	**IntPending 12 (INTPENDING_12):** Bit 12 represents MSI entry 12
11	0h RO/V	**IntPending 11 (INTPENDING_11):** Bit 11 represents MSI entry 11
10	0h RO/V	**IntPending 10 (INTPENDING_10):** Bit 10 represents MSI entry 10
9	0h RO/V	**IntPending 9 (INTPENDING_9):** Bit 9 represents MSI entry 9
8	0h RO/V	**IntPending 8 (INTPENDING_8):** Bit 8 represents MSI entry 8
7	0h RO/V	**IntPending 7 (INTPENDING_7):** Bit 7 represents MSI entry 7
6	0h RO/V	**IntPending 6 (INTPENDING_6):** Bit 6 represents MSI entry 6
5	0h RO/V	**IntPending 5 (INTPENDING_5):** Bit 5 represents MSI entry 5
4	0h RO/V	**IntPending 4 (INTPENDING_4):** Bit 4 represents MSI entry 4
3	0h RO/V	**IntPending 3 (INTPENDING_3):** Bit 3 represents MSI entry 3
2	0h RO/V	**IntPending 2 (INTPENDING_2):** Bit 2 represents MSI entry 2
1	0h RO/V	**IntPending 1 (INTPENDING_1):** Bit 1 represents MSI entry 1

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/V	**IntPending 0 (INTPENDING_0):** Bit 0 represents MSI entry 0

9 Gauss Newton Algorithm Registers (D8:F0)

Gaussian Mixture Model and Neural Network Accelerator. This chapter documents the registers in: Bus 0, Device 8, Function 0.

Table 9-1. Summary of Bus: 0, Device: 8, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Vendor & Device ID (IDENTIFICATION)	00008086h
4h	2	Device Control (DCTRL)	0000h
6h	2	Device Status (DSTS)	0010h
8h	4	Revision ID & Class Codes (RID_DLCO)	08800000h
Ch	1	Cache Line Size (CLS)	00h
Eh	1	Header Type (HTYPE)	00h
Fh	1	Built-in Self Test (BIST)	00h
10h	4	GNA Base Address Low (GNABAL)	00000004h
14h	4	GNA Base Address High (GNABAH)	00000000h
2Ch	2	Sub System Vendor Identifiers (SSVI)	0000h
2Eh	2	Sub System Identifiers (SSI)	0000h
34h	4	Capabilities Pointers (CAPP)	00000090h
3Ch	1	Interrupt Line (INTL)	00h
3Dh	1	Interrupt Pin Register (INTP)	01h
3Eh	2	Min Grant And Min Latency Register (MINGNTLAT)	0000h
40h	4	Override Configuration Control (OVRCFGCTL)	00000000h
90h	2	Message Signaled Interrupt Capability ID (MSICAPID)	A005h
92h	2	Message Signaled Interrupt Message Control (MC)	0000h
94h	4	Message Signaled Interrupt Message Address (MA)	00000000h
98h	4	Message Signaled Interrupt Message Data (MD)	00000000h
A0h	2	D0i3 Capability ID (D0I3CAPID)	DC09h
A2h	2	D0i3 Capability (D0I3CAP)	F014h
A4h	4	D0i3 Vendor Extended Capability Register (D0I3VSEC)	01400010h
A8h	4	D0i3 SW LTR Pointer Register (D0I3SWLTRPTR)	00000000h
ACh	4	D0i3 DevIdle Pointer Register (D0I3DEVIDLEPTR)	00000A81h
B0h	2	D0i3 DevIdle Power On Latency (D0I3DEVIDLEPOL)	0800h
B2h	2	D0i3 Power Control Enables Register (PCE)	0028h
DCh	2	Power Management Capability ID (PMCAPID)	F001h
DEh	2	Power Management Capability (PMCAP)	0002h
E0h	2	Power Management Control Status (PMCS)	0000h
F0h	2	FLR Capability ID (FLRCAPID)	0013h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F2h	2	FLR Capability Length And Version (FLRMISC)	0306h
F4h	1	FLR Control Register (FLRCTL)	00h
F5h	1	FLR Status Register (FLRSTS)	00h

9.1 Vendor & Device ID (IDENTIFICATION) — Offset 0h

Device ID assigned to GNA and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Device Identification Number (DID):** Indicates the device ID assigned to the GNA.
15:0	8086h RO	**Vendor Identification Number (VID):** Indicates Intel's identification

9.2 Device Control (DCTRL) — Offset 4h

The Command register provides coarse control over GMM's abilities such as:

- Unsupported Request Error Reporting Enable
- Poisoned TLP Error Reporting Enable
- Interrupt Disable
- Max Aligned Payload Size
- Max Aligned Read Request Size
- Special Cycle Enable
- Bus Master Enable
- Memory Space Enable

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RO	**Unsupported Request Error Reporting Enable (UNSPREQERREN):** Unsupported Request Error Reporting Enable
13	0h RO	**Poisoned TLP Error Reporting Enable (PTLPERREN):** Poisoned TLP Error Reporting Enable
12:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTDIS):** Interrupt Disable: Controls the ability of the function to generate INTx interrupts. 0: INTx allowed 1: INTx disabled
9:6	0h RO	**Reserved**
5	0h RO	**Max Aligned Payload Size (MXAPAYLDSZ):** Max Aligned Payload Size - Reserved
4	0h RO	**Max Aligned Read Request Size (MXARDREQSZ):** Max Aligned Read Request Size - Reserved
3	0h RO	**Special Cycle Enable (SCEN):** Special Cycle Enable - Reserved
2	0h RW	**Bus Master Enable (BME):** Bus Master Enable: 0: Disable (default). 1: Enabled. Device may generate bus master transactions depending on its mode of operation.
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable Controls the GMM devices response to memory space accesses. 0: Disabled (default) 1: Enabled. Device will respond to memory space accesses.
0	0h RO	**IO Space Enable (IOSE):** IO Space Enable. Not implemented.

9.3 Device Status (DSTS) — Offset 6h

The Status register to record status information for PCI related events

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** This bit is set by a function whenever it receives a Poisoned TLP, regardless of the state the parity Error Response bit in the Command register. On a Function with a Type 1 Configuration header, the bit is set when the Poisoned TLP is received by its primary side. Note: some implementations use this error type as non-fatal error indication This bit is typically RWC. Change to RO as this bit is not in use.
14	0h RO	**Signaled System Error (SSE):** This bit is set when a function sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR# enable bit in the command register is 1. Note: some implementations use this error for fatal. When received all operations are aborted. This bit is typically RWC. Change to RO as this bit is not in use
13	0h RW/1C/V	**Received Master Abort (RMA):** This bit is set when a requester receives a completion with Unsupported Request Completion status. On a function with a Type 1 configuration header, the bit is set when the Unsupported Request is received by its primary side.
12	0h RW/1C/V	**Received Target Abort (RTA):** This bit is set when a transaction abort is received to a GMM initiated transaction.
11	0h RW/1C/V	**Signaled Target Abort (STA):** This bit is set when a Function completes a Posted or Non-Posted Request as a Completer Abort Error. This applies to a function with a type 1 configuration header when the Completer Abort was generated by its primary side.
10:8	0h RO	**Reserved**
7	0h RO	**Fast Back-to-Back (FB2B):** Fast Back-to-Back (ignored by SW)
6:5	0h RO	**Reserved**
4	1h RO	**Capability List (CLIST):** Capability List 0: no capability list 1: the GMM contains a linked list of capabilities which is accessed via the CAPPTR register at offset 34h
3	0h RO/V	**Interrupt Status (INTSTS):** Reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will this device send a virtual INTA. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit is controlled by HW. 0: No interrupt pending 1: Interrupt pending

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO	**Reserved**

9.4 Revision ID & Class Codes (RID_DLCO) — Offset 8h

RID: This register indicates the stepping of this device.

DLCO: This register identify the type of device.

The values are as defined in PCI 3.0 bus specification in Appendix D.

The GMM is identified as an Other system Peripheral

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 8h	08800000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	08h RO	**Base Class Code (BCC):** Base Class (Generic system Peripherals)
23:16	80h RO	**Sub Class Code (SCC):** Code for Sub Class
15:8	00h RO	**Peripheral Interface (PROGINTERFACE):** Interface (other system peripheral)
7:0	00h RO/V	**Revision ID (RID):** Indicates the stepping of this device.

9.5 Cache Line Size (CLS) — Offset Ch

The system cache-line size in units of DWORDS

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CLS):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

9.6 Header Type (HTYPE) — Offset Eh

This byte identifies the layout of the second part of the predefined header and whether or not the device contains multiple functions (GMM is a single-function device of basic configuration space format, so this register is Read-Only and hardwired to 0).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi Function Device (MFD):** Hardwired to 0 indicating this device is not a multi-function device.
6:0	00h RO	**Header Type (HT):** The value 00h, indicates a basic (i.e. single function) configuration space format.

9.7 Built-in Self Test (BIST) — Offset Fh

This register describes the BIST capability of GMM and since GMM doesn't support BIST, the register is configured as Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BISTCAP):** BIST Capable. Hardwired to 0 since this device does not implement BIST.
6	0h RO	**Start BIST (BISTST):** Start BIST. Hardwired to 0 since this device does not implement BIST.
5:4	0h RO	**Reserved**
3:0	0h RO	**BIST Completion Code (BISTCC):** Hardwired to 0 since this device does not implement BIST.

9.8 GNA Base Address Low (GNABAL) — Offset 10h

GNA Base Address Low:

Lower 32-bits of the GNA Base Address register.

The GMM Base Address register may be accessed with Double Word (32bit) read/write operations.

In 32-bit OS, the address specified may be limited by 32-bit of space, and the renaming bits must stay with their default values.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Memory Base Address Low (BAL):** Base address of this device's memory mapped IO space. A page of 4KB of address is used.
11:4	00h RO	**Address Mask (ADDRMSK):** Hardwired to 0s to indicate at least 4KB address range
3	0h RO	**Prefetchable Memory (PREF):** Hardwired to 0 indicating that this range is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	2h RO	**Memory Type (MEMTY):** Memory Type: 00: 32 bit base address 01: reserved 10: 64-bit base address 11: reserved
0	0h RO	**Space Type (SPTY):** Space Type: Memory/IO Space Hardwired to 0 indicating that this is a Memory BAR.

9.9 GNA Base Address High (GNABAH) — Offset 14h

Upper 32-bits of the GNA Base Address register.

The GNA Base Address register may be accessed with Double Word (32bit) read/write operations.

In 32-bit OS, the address specified may be limited by 32-bit of space, and the renaming bits must stay with their default values.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Memory Base Address High (Reserved) (BAR):** These bits must be loaded with zeros.
6:0	00h RW	**Memory Base Address High (BAH):** Includes the high bits of the base address used by 64-bit OS. Must hold zero for 32-bit OS.

9.10 Sub System Vendor Identifiers (SSVI) — Offset 2Ch

This register is initialized to logic 0 by the assertion of reset. This register can be written only once after reset de-assertion it is locked for writes after that.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action taken on this value.

9.11 Sub System Identifiers (SSI) — Offset 2Eh

This register is initialized to logic 0 by the assertion of reset. This register can be written only once after reset de-assertion it is locked for writes after that.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem ID (SSID):** Subsystem ID (SSID): This is written by BIOS. No hardware action taken on this value.

9.12 Capabilities Pointers (CAPP) — Offset 34h

This register gives MSI capability pointer offset.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 34h	00000090h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	90h RO	**Capability Pointer (CAPP):** Indicates that the MSI capability pointer offset is offset 90h.

9.13 Interrupt Line (INTL) — Offset 3Ch

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Connection (INTCON):** Communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected.

9.14 Interrupt Pin Register (INTP) — Offset 3Dh

Tells which PCI legacy interrupt pin a device will use (GMM uses only IntA).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2:0	1h RO	**Legacy Interrupt (LEGINT):** When Legacy interrupts are used, function use legacy interrupt INTA.

9.15 Min Grant And Min Latency Register (MINGNTLAT) — Offset 3Eh

Specifies a device's desired settings for Latency Timer values.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 3Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Min Latency (MINLAT):** Reserved
7:0	00h RO	**Min Grant (MINGNT):** Reserved

9.16 Override Configuration Control (OVRCFGCTL) — Offset 40h

This register holds bits that may be used internal mechanisms in the GMM during debug operations. Special notes will be made to BIOS writers, if any 5 of these bits will need to be set to value other than default.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Sideband Clock Gating Enable (SBDCGEN):** This bit, when set, enables the sideband interface clock used for GMM bus interface operations (gated_side_clk) to be gated when conditions are met. When clear, clock gating is disabled.
7:0	0h RO	**Reserved**

9.17 Message Signaled Interrupt Capability ID (MSICAPID) — Offset 90h

This register contains a pointer to the next item in the capabilities list which is the Power Management Capability and also helps to identify linked list item (capability structure) as being for MSI registers.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 90h	A005h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RO	**Pointer to Next Capability (NXTPTR):** This contains a pointer to the next item in the capabilities list which is the Power Management Capability
7:0	05h RO	**Capability ID (CAPID):** Capability ID Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

9.18 Message Signaled Interrupt Message Control (MC) — Offset 92h

This register is defined to meet PCI Local Bus Specification 3.0 Section 6.8 definition of MSI messages.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 92h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RO	**Per-Vector Masking Capable (PVMCAP):** Per-Vector Masking Capable. 0: not supported by GMM.
7	0h RO	**64-bit Address Capable (ADDR64CAP):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32bit/4GB limit.
6:4	0h RW	**Multiple Message Enable (MMEN):** System software program this field to indicate the number of vectors allocated to the GMM. At least one vector must be allocated when the MSI interrupts are enabled. This value is ignored by HW as only a single vector is in use by GMM.
3:1	0h RO	**Multiple Message Capable (MMCAP):** Indicates to SW the number of vectors that the GMM module is requesting for use. Value Number of Messages requested 000 1 001 2 (reserved) 010 4 (reserved) 011 8 (reserved) 100 16(reserved) 101 32(reserved) Other reserved
0	0h RW	**MSI Enable (MSIEN):** MSI Enable Controls the ability of GMM to generate MSI Messages. A device driver is prohibited from writing this bit to mask a functions service request. 0: MSI will not be generated 1: MSI will be generated. INTA will not be generated and INTA status is not set.

9.19 Message Signaled Interrupt Message Address (MA) — Offset 94h

This register is defined to meet PCI Local Bus Specification 3.0 Section 6.8 definition of MSI messages.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MADDR):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	0h RO	**Reserved**

9.20 Message Signaled Interrupt Message Data (MD) — Offset 98h

This register is defined to meet PCI Local Bus Specification 3.0 Section 6.8 definition of MSI messages

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Message Data (MDAT):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

9.21 D0i3 Capability ID (D0I3CAPID) — Offset A0h

Pointer to next capability and capability ID.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + A0h	DC09h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	DCh RO	**Pointer to Next Capability (NXTPTR):** This contains a pointer to the next item in the capabilities list which is the Power Management Capability.
7:0	09h RO	**Capability ID (CAPID):** Value of 09h identifies this linked list item (capability structure) is a vendor specific capability.

9.22 D0i3 Capability (D0I3CAP) — Offset A2h

Vendor-Specific Capability ID.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + A2h	F014h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RO	**Vendor-Specific Capability ID (VSID):** Indicates that this Vendor Specific Capability is an Extended Capability, which use a VSEC 16-bit Extended Vendor Capability in the subsequent 4B., differentiating this from other vendor specific capabilities.
11:8	0h RO	**Vendor Specific Capability Revision (VSREV):** Reserved
7:0	14h RO	**Vendor Specific Capability Length (VSLEN):** This field indicates the number of bytes in this capability including the CapID and Cap registers.

9.23 D0i3 Vendor Extended Capability Register (D0I3VSEC) — Offset A4h

Vendor Specific Extended Capability Length.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + A4h	01400010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Extended Capability Length (VSECLEN):** Indicates that this Vendor Specific Capability is an Extended Capability, which use a VSEC 16-bit Extended Vendor Capability in the subsequent 4B., differentiating this from other vendor specific capabilities.
19:16	0h RO	**Vendor Specific Extended Capability Revision (VSREV):** For this revision of DevIdle, this field is 0h.
15:0	0010h RO	**Vendor Specific Extended Capability ID (VSECID):** DevIdle has been assigned the Intel VSEC ID of 10h.

9.24 D0i3 SW LTR Pointer Register (D0I3SWLTRPTR) — Offset A8h

SW LTR Update MMIO Offset Location.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** The value in this field is ignored as GMM does not support SW LTR.
3:1	0h RO	**Base Address Register Number (BARNUM):** The value in this field is ignored as GMM does not support SW LTR.
0	0h RO	**Valid Indicator (VALID):** Indicates the use of SW LTR by the function.GMM does not use SW LTR.

9.25 D0i3 DevIdle Pointer Register (D0I3DEVIDLEPTR) — Offset ACh

DevIdle MMIO Offset Location.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + ACh	00000A81h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:4	00000A8h RO	**DevIdle MMIO Offset Location (DEVIDLELOC):** This location pointer to the DevIdle register in MMIO space, as an offset from the BAR base.
3:1	0h RO	**Base Address Register Number (BARNUM):** The DevIdle is located in BAR0.
0	1h RO	**Valid Indicator (VALID):** GMM has a DevIdle register.

9.26 D0i3 DevIdle Power On Latency (D0I3DEVIDLEPOL) — Offset B0h

D0idle_5 Max_Power_On_Latency is set by BIOS at boot and read by device driver SW to calculate approximate cost of a D0idle entry + exit cycle. This allows driver to avoid idle entry in cases where device duty cycle is larger than D0idle entry + exit cycle.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + B0h	0800h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:10	2h RO	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. This field is a RO as there is no need for BIOS programing of it.
9:0	000h RO	**Power On Latency Value (POLV):** A value of 0 indicates a power on latency of less than 1us. This field is a RO as there is no need for BIOS programing of it.

9.27 D0i3 Power Control Enables Register (PCE) — Offset B2h

This register controls the D0i3 features like Hardware Autonomous Enable, sleep enable, D3-Hot Enable, I3 Enable and PMC Request Enable.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + B2h	0028h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	1h RW	**Hardware Autonomous Enable (HAE):** If set, then the IP may request a PG whenever it is idle. NOTE: If this bit is set, then bits[2:0] must be 000.
4	0h RO	**Reserved**
3	1h RW	**Sleep Enable (SE):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PGing. Note that some platforms may default this bit to 0, others to 1.
2	0h RW	**D3-Hot Enable (D3HE):** If set, then IP will PG when idle and the PMCSR[1:0] register in the IP =11.
1	0h RW	**I3 Enable (I3E):** If set, then IP will PG when idle and the D0i3 register (D0i3C[2] = 1) is set. NOTE: If bits [2:1] = 11, then the IP would PG whenever either PMCSR = 11 or the D0i3C.i3 bit is set.
0	0h RW	**PMC Request Enable (PMCRE):** If set, then IP will PG when idle and the PMC requests power gating by asserting the pmc_*_sw_pg_req_b signal.

9.28 Power Management Capability ID (PMCAPID) — Offset DCh

This register contains a pointer to next item in capabilities list and also helps to identify linked list item as being for

PCI Power Management registers.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + DCh	F001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	F0h RO	**Next Pointer (NXTPTR):** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	01h RO	**Capability Identifier (CAPID):** Identifies this linked list item as being for PCI Power Management registers. This is compliant with the PCI Power Management Interface Specification (section 3.2).

9.29 Power Management Capability (PMCAP) — Offset DEh

This register describes the Power Management Capability of GMM.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + DEh	0002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RO	**PME Support (PMES):** This device does not support PMEB signal.
10	0h RO	**D2 Support (D2S):** This device does not support D2.
9	0h RO	**D1 Support (D1S):** This device does not support D1.
8:6	0h RO	**Auxiliary Current (AUXC):** Reserved
5	0h RO	**Device Specific Initialization (DSI):** Indicates that this device requires device specific initialization before generic class device driver is to use it.
4	0h RO	**Auxiliary Power (AUXP):** This device does not use Aux power.
3	0h RO	**PME Clock (PMEC):** Indicate this device does NOT support PMEB generation.

Bit Range	Default & Access	Field Name (ID): Description
2:0	2h RO	**Version for PM (VER):** Hardwired to 010b to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

9.30 Power Management Control Status (PMCS) — Offset E0h

This register has the status of PME Generation from D3(cold), Data Scale, Data Select, PME Enable and Power State.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + E0h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PME Generation from D3 (cold) (PMEGD3):** Not supported.
14:13	0h RO	**Data Scale (DATSC):** No support for Power Management Data register.
12:9	0h RO	**Data Select (DATSEL):** No support for Power Management Data register.
8	0h RO	**PME Enable (PMEE):** PMEB is not supported.
7:2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Write of reserved values is ignored and state will not change. Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional.

9.31 FLR Capability ID (FLRCAPID) — Offset F0h

This register contains a pointer to next item in capabilities list and capability of Advanced Features.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + F0h	0013h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Pointer (NXTPTR):** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	13h RO	**Capability Identifier (CAPID):** A value that indicates FLR (Vendor specific value). 0: 09h (FLR in use) A value of 09h in this register indicates that this is a FLR capabilities field.

9.32 FLR Capability Length And Version (FLRMISC) — Offset F2h

This register describes the FLR Capability, TXP Capability and Capability Length.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + F2h	0306h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	1h RO	**FLR Capability (FLRCAP):** Indicates support for Function Level Reset (FLR).
8	1h RO	**TXP Capability (TXPCAP):** Indicates that TP bit is supported.
7:0	06h RO	**Capability Length (CAPLEN):** This bit indicates the number of bytes this vendor specified capability requires. it has a value of 06h for the FLR capability.

9.33 FLR Control Register (FLRCTL) — Offset F4h

This register controls the Functional Level reset operation of GMM.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + F4h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h WO	**Initiate FLR (INITFLR):** Writing 1 to this field starts the Functional Level Reset.This will act similar to the Abort + will bring all non-CFG registers to their reset value. The FLR is completed when the FLR status bit is cleared.

9.34 FLR Status Register (FLRSTS) — Offset F5h

This register helps to identify whether FLR is in progress.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + F5h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RO/V	**Transaction Pending (XPEND):** 0: FLR not in progress. 1: FLR is in progress (due to internal operation or waiting for the completion of a non-posted transaction).

10 CrashLog & Telemetry Registers (D10:F0)

CrashLog & Telemetry device registers.

The device has an SRAM that has the following data:

- CrashLog: records the system information during a crash/hang.
- Telemetry: records a snapshot of the system state.

This chapter documents the registers in Bus: 0, Device 10, Function 0.

Table 10-1. Summary of Bus: 0, Device: 10, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID (VENDOR_ID_DEVICE_ID)	9A0D8086h
4h	4	Command and Status (COMMAND_STATUS)	00100000h
8h	4	Revision ID (REVISION_ID)	11800001h
Ch	4	Cache Line Size (CACHE_LINE_SIZE)	00000000h
10h	8	PM Base Address (PM_BAR)	0000000000000004h
2Ch	4	Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID)	00000000h
34h	4	Capabilities Pointer (CAPABILITIES_POINTER)	00000070h
3Ch	4	Interrupt line (INTERRUPT_LINE)	00000000h
70h	4	PCIe Capability ID (PCIE_CAPID)	0092D010h
74h	4	Device Capabilities (DEV_CAP)	00000FE0h
78h	4	PCIE Device Control and Status (DEV_CTL_STS)	00000000h
D0h	4	Power Management Capabilities (PM_CAPID)	00030001h
D4h	4	Power Management Control Status (PM_CONTROL_STATUS)	00000008h
100h	4	Telemetry Capability Header (TELEM_CAPABILITY_HEADER)	11010023h
104h	4	Telemetry VSEC 0 (TELEM_VSEC_0)	01018086h
108h	4	Telemetry VSEC 1 (TELEM_VSEC_1)	04040002h
10Ch	4	Telemetry VSEC 2 (TELEM_VSEC_2)	000326C0h
110h	4	Watcher Capability Header (WATCHER_CAPABILITY_HEADER)	12010023h
114h	4	Watcher VSEC 0 (WATCHER_VSEC_0)	01018086h
118h	4	Watcher VSEC 1 (WATCHER_VSEC_1)	04020003h
11Ch	4	Watcher VSEC 2 (WATCHER_VSEC_2)	00030080h
120h	4	Crashlog Capability Header (CRASHLOG_CAPABILITY_HEADER)	00010023h
124h	4	Crashlog VSEC 0 (CRASHLOG_VSEC_0)	01018086h
128h	4	Crashlog VSEC 1 (CRASHLOG_VSEC_1)	0A010004h
12Ch	4	Crashlog VSEC 2 (CRASHLOG_VSEC_2)	00030180h

10.1 Device ID And Vendor ID (VENDOR_ID_DEVICE_ID) — Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the Device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 0h	9A0D8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	9A0Dh RO	**Device ID (DEVICE_ID):** Device ID identifies the particular PCI device.
15:0	8086h RO	**Vendor ID (VENDOR_ID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device.

10.2 Command and Status (COMMAND_STATUS) — Offset 4h

Command register to program interrupt disable, bus master enable and Memory space enable.

Status register to read the errors and aborts.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DETECTED_PARITY_ERROR):** Not implemented.
30	0h RO	**Signaled System Error (SIGNALED_SYSTEM_ERROR):** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register. This device does not implement this bit and it is hardwired to a 0.
29	0h RO	**Received Master Abort (RECEIVED_MASTER_ABORT_STATUS):** This bit is set when device receives a Completion transaction with Unsupported Request completion status. No error will be reported.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Received Target Abort (RECEIVED_TARGET_ABORT_STATUS):** This bit is set when device receives a Completion transaction with Completer Abort completion status. No error will be reported.
27	0h RO	**Signaled Target Abort (SIGNALED_TARGET_ABORT_STATUS):** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband. Device will not generate a Target Abort DMI completion packet or Special Cycle, and therefore it has no need to implement this bit.
26:25	0h RO	**Reserved**
24	0h RO	**Master Data Parity Error (MASTER_DATA_PARITY_ERROR):** This bit is Set by a Requester if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: * Requester receives a Completion marked poisoned * Requester poisons a write Request If the Parity Error Response bit is 0b, this bit is never Set.
23:21	0h RO	**Reserved**
20	1h RO	**Capabilities List (CAPABILITIES_LIST):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. This device does support capabilities.
19	0h RO	**Interrupt Status (INTERRUPT_STATUS):** Reflects the state of the interrupt pin at the input of the enable/disable circuit. When the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI.
18:11	0h RO	**Reserved**
10	0h RO	**Interrupt Disable (INTERRUPT_DISABLE):** Disables the function to generate INTx interrupt. A value of 0 enables the function to generate INTA messages. Note: this bit has no effect on MSI generation. Since this device does not generate interrupts, this bit is set to 0x0.
9	0h RO	**Reserved**
8	0h RO	**SERR Reporting Enable (SERR_ENABLE):** Setting this bit enables the generation of System Error messages. Not implemented by this device.
7	0h RO	**Reserved**
6	0h RO	**Parity Error Response (PARITY_ERROR_RESPONSE):** This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status register. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RO	**Reserved**
2	0h RO	**Bus Master Enable (BUS_MASTER_ENABLE):** Controls the ability of a PCI Express Endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write Requests in the Upstream direction. **Endpoints:** • When this bit is Set, the PCI Express Function is allowed to issue Memory or I/O Requests. • When this bit is Clear, the PCI Express Function is not allowed to issue any Memory or I/O Requests. • Note that as MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Requests other than Memory or I/O Requests are not controlled by this bit. Default value of this bit is 0b. This bit is hardwired to 0b if a Function does not generate Memory or I/O Requests.
1	0h RW	**Memory Space Enable (MEMORY_SPACE_ENABLE):** When set, Memory Space Decoding is enabled and memory transactions targeting the device are accepted Note: The MSE has to be set to accept any memory transaction on the primary interface targeting any of this device.
0	0h RO	**Reserved**

10.3 Revision ID (REVISION_ID) — Offset 8h

Revision ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 8h	11800001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	11h RO	**Base Class Code (CLASS_CODE):** This is an 8-bit value that indicates the base class code for the Power Management Controller. This code has the value 11h, indicating a device that is used for data acquisition and signal processing.
23:16	80h RO	**Sub Class (SUB_CLASS_CODE):** The code is 80h which indicates Other Data Acquisition and Signal Processing Controllers.
15:8	00h RO	**Programming Interface (PROGRAMMING_INTERFACE):** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**Revision ID (REVISION_ID):** Indicates the device specific revision identifier derived from and input strap.

10.4 Cache Line Size (CACHE_LINE_SIZE) — Offset Ch

Cache Line Size.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Builtin Self Test (BIST):** Hardwired to 0x0. This device does not support BIST.
30:24	0h RO	**Reserved**
23:16	00h RO	**Header Type (HEADER_TYPE):** This device implements a Type 0 configuration header.
15:8	00h RO	**Master Latency Timer (MASTER_LATENCY_TIMER):** This register is also referred to as Primary Latency Timer for Type 1 Configuration Space header Functions. The Latency Timer does not apply to PCI Express. This register must be hardwired to 00h.
7:0	00h RO	**Cache Line Size (CACHE_LINE_SIZE):** The Cache Line Size register is set by the system firmware or the operating system to system cache line size. However, note that legacy PCI 3.0 software may not always be able to program this field correctly especially in the case of Hot-Plug devices. This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

10.5 PM Base Address (PM_BAR) — Offset 10h

Base address register.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:10, F:0] + 10h	0000000000000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:15	000000h RW	**PMBAR Address (PMBAR):** This field corresponds to bits 38 to 15 of the base address PMBAR address space. BIOS will program this register resulting in a base address for a 32KB block of contiguous memory address space. This register ensures that a naturally aligned 32KB space is allocated within total addressable memory space.
14:4	000h RO	**Address Mask (ADDRESS_MASK):** Hardwired to 0s to indicate at least 32KB address range. Software typically writes all 1's to the BAR and then reads back the resulting value to assess the size of the BAR. Since bits 14:4 are read-only and zero, that indicates that the device is 32KB.
3	0h RO	**BAR is Prefetchable (PREFETCHABLE):** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h RO	**Address Range (ADDRESS_RANGE):** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing). This also indicates that the size of the BAR register is 64b.
0	0h RO	**Memory Space Indicator (SPACE_TYPE):** Value of 0 indicates the BAR is located in memory space.

10.6 Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID) — Offset 2Ch

This value is used to identify a particular subsystem.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Subsystem ID (SUBSYSTEM_ID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

10.7 Capabilities Pointer (CAPABILITIES_POINTER) — Offset 34h

Capabilities pointer.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 34h	00000070h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** Pointer to first capability structure.

10.8 Interrupt line (INTERRUPT_LINE) — Offset 3Ch

Interrupt line.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Interrupt Pin (INTERRUPT_PIN):** A value of 00h indicates that the Function uses no legacy interrupt Message(s).
7:0	00h RO	**Interrupt line (INTERRUPT_LINE):** Hardware does not use this field. Rather it is programmed by system software and device drivers to communicate interrupt line routing information.

10.9 PCIe Capability ID (PCIE_CAPID) — Offset 70h

Indicates the PCI Express Capability.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 70h	0092D010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Interrupt Message Number (INTERRUPT_MESSAGE_NUMBER):** This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Telemetry Aggregator doesn't currently generate interrupts, so this value is hardwired to 0.
24	0h RO	**Slot Implemented (SLOT_IMPLEMENTED):** Hardwired to 0 for any endpoint device.
23:20	9h RO	**Device Type (DEV_TYPE):** Device/Port Type Indicates the specific type of this PCI Express Function. 0x9 is Root Complex Integrated Endpoint.
19:16	2h RO	**Capability Version (CAP_VERSION):** Indicates PCI Express Capability structure version number. Must be hardwired to 0x2.
15:8	D0h RO	**Next Capability Pointer (NEXT_CAPABILITY_POINTER):** Pointer to next capability in the capabilities linked list.
7:0	10h RO	**Capability ID (CAPABILITY_ID):** 0x10 indicates that this is a PCI express capability structure.

10.10 Device Capabilities (DEV_CAP) — Offset 74h

Identifies PCI Express device Function specific capabilities.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 74h	00000FE0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Function Level Reset Capability (FLR_CAP):** A value of 1b indicates the Function supports the optional Function Level Reset mechanism.
27:12	0000h RO	**MISC:** Miscellaneous fields not relevant for Telemetry Aggregator device.
11:9	7h RO	**L1 Latency (L1_LAT):** Endpoint L1 Acceptable Latency. 0x7: No limit.
8:6	7h RO	**L0 Latency (L0_LAT):** Endpoint L0 Acceptable Latency. 0x7: No limit.
5	1h RO	**Extended Tag (EXT_TAG):** Extended Tag Field Supported This bit indicates the maximum supported size of the Tag field as a Requester. 0x1: 8-bit Tag field supported.
4:3	0h RO	**Phantom Functions (FANTOM_FUNC):** Phantom Functions Supported. 0x0: No Function Number bits are used for Phantom Functions.
2	0h RO	**Reserved**
1:0	0h RO	**Max Payload size (MAX_PAYLOAD_SIZE):** Max_Payload_Size Supported This field indicates the maximum payload size that the Function can support for TLPs. 0x0: 128 bytes max payload size.

10.11 PCIE Device Control and Status (DEV_CTL_STS) — Offset 78h

PCIE Device Control and Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 78h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Miscellaneous Status (MISC_STATUS):** Miscellaneous reserved and status bits. Telemetry Aggregator doesn't set any of the status bits.
15	0h RO	**Initiates FLR (INIT_FLR):** Initiates FLR for FLR-supporting devices. FLR not supported for Telemetry Aggregator. Hardwire to 0.
14:0	0000h RO	**Miscellaneous PCIE Device Control (MISC_CONTROL):** Miscellaneous PCIE device control settings. Telemetry Aggregator doesn't implement any of the contolled functionality and as such will not respond to the writes.

10.12 Power Management Capabilities (PM_CAPID) — Offset D0h

The Power Management Capabilities register is a read-only register which provides information on the capabilities of the function related to power management.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + D0h	00030001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME Support (PME_SUPPORT):** This field indicates the power states in which the device may assert PME#. It is hardwired to 0 to indicate that the device does not support nor assert the PME# signal.
26	0h RO	**D2:** Hardwired to 0 to indicate that the D2 power management state is not supported.
25	0h RO	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
24:22	0h RO	**Reserved**
21	0h RO	**Device Specific Initialization (DEVICE_SPECIFIC_INITIALIZATION):** Indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. This bit is not used by some operating systems. Windows OS, for instance, does not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this. 1b indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
20	0h RO	**Reserved**
19	0h RO	**PME Capability (PME_CAPABILITY):** When this bit is set, it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is clear, it indicates that no PCI clock is required for the function to generate PME#. Functions that do not support PME# generation in any state must return 0 for this field. Hardwired to 0 to indicate the device does not support PME# generation.
18:16	3h RO	**VERSION:** This device complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	00h RO	**Next Capability Pointer (NEXT_CAPABILITY_POINTER):** This field is hardwired to 00h, indicating the end of the capabilities linked list.
7:0	01h RO	**Capability ID (CAPABILITY_ID):** 01h indicates that this is a power management capability.

10.13 Power Management Control Status (PM_CONTROL_STATUS) — Offset D4h

The Data register is an optional, 8-bit read-only register that provides a mechanism for the function to report state dependent operating data such as power consumed or heat dissipation. Typically the data returned through the Data register is a static copy (look up table, for example) of the function's worst case 'DC characteristics' data sheet. This data, when made available to system software, could then be used to intelligently make decisions about power budgeting, cooling requirements, etc.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + D4h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DATA:** The data register, data scale and data select registers are not supported. Hardwired to zero.
23:16	0h RO	**Reserved**
15	0h RO	**PME# Status (PME_STATUS):** This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. This bit is hardwired to 0b to indicate that PME# assertion from D3 (cold) is not supported.
14:13	0h RO	**Data Scale (DATA_SCALE):** The data register, data scale and data select registers are not supported.
12:9	0h RO	**Data Select (DATA_SELECT):** The data register, data scale and data select registers are not supported.
8	0h RO	**PME Enable (PME_ENABLE):** This bit is hardwired to 0b to indicate that PME# assertion from D3 (cold) is disabled.
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** When set to 1 this bit indicates that the device is transitioning from D3hot to D0 because the power state commands do not perform a internal reset. Config context is preserved. Upon transition no additional operating system intervention is required to preserve configuration context beyond writing the power state bits. When clear the devices do not perform an internal reset upon transitioning from D3hot to D0 via software control of the power state bits. Regardless of this bit the devices that transition from a D3hot to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Power State (POWER_STATE):** This field indicates the current power state of the device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs.

10.14 Telemetry Capability Header (TELEM_CAPABILITY_HEADER) — Offset 100h

DVSEC header for telemetry capability.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 100h	11010023h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	110h RO	**Next Capability Offset (NEXT_CAPABILITY_OFFSET):** Points to the location of the next capability, unless this is the last one then the value is either 000h or a value within CFG range or greater than 0xFF if in the extended config space.
19:16	1h RO	**Capability Version (CAPABILITY_VERSION):** Indicates that this is version 1 of the PCIe capability header.
15:0	0023h RO	**PCIe Extended Capability Id (PCIE_EXTENDED_CAPID):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Designated Vendor-Specific Capability is 0023h.

10.15 Telemetry VSEC 0 (TELEM_VSEC_0) — Offset 104h

Telemetry VSEC 0.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 104h	01018086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	010h RO	**Header Size (DVSEC_LEN):** DVSEC number of bytes including this field and the PCIe Capability field.
19:16	1h RO	**Version ID (DVSEC_VER):** Indicates the revision of this header.
15:0	8086h RO	**Vendor ID (DVSEC_VENDOR_ID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device.

10.16 Telemetry VSEC 1 (TELEM_VSEC_1) — Offset 108h

Telemetry VSEC 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 108h	04040002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RO	**Entry Size (ENTRY_SIZE):** Entry Size in DWORDs.
23:16	04h RO	**Number of Entries (NUM_ENTRIES):** Number of entries, describes the number of telemetry aggregators that would exist in this capability lookup table.
15:0	0002h RO	**Discovery Type (DVSEC_ID):** Indicates the type of discovery entry. This is a telemetry capability.

10.17 Telemetry VSEC 2 (TELEM_VSEC_2) — Offset 10Ch

Telemetry VSEC 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 10Ch	000326C0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:3	000064D8h RO	**Discovery Table Offset (DISCOVERY_TABLE_OFFSET):** Base address of the discovery list for this capability space. This offset is relative to the device's MMIO address space (relative to the BAR).
2:0	0h RO	**BAR ID (BAR_ID):** The BAR to be used: 0h: 0x10 (BAR0).

10.18 Watcher Capability Header (WATCHER_CAPABILITY_HEADER) — Offset 110h

DVSEC header for watcher capability.

Note: Bit definitions are the same as TELEM_CAPABILITY_HEADER, offset 100h.

10.19 Watcher VSEC 0 (WATCHER_VSEC_0) — Offset 114h

Watcher VSEC 0.

Note: Bit definitions are the same as TELEM_VSEC_0, offset 104h.

10.20 Watcher VSEC 1 (WATCHER_VSEC_1) — Offset 118h

Watcher VSEC 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 118h	04020003h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RO	**Entry Size (ENTRY_SIZE):** Entry Size in DWORDs.

Bit Range	Default & Access	Field Name (ID): Description
23:16	02h RO	**Number of Entries (NUM_ENTRIES):** Number of entries, describes the number of telemetry aggregators that would exist in this capability lookup table.
15:0	0003h RO	**Discovery Type (DVSEC_ID):** Indicates the type of discovery entry. This is a watcher capability.

10.21 Watcher VSEC 2 (WATCHER_VSEC_2) — Offset 11Ch

Watcher VSEC 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 11Ch	00030080h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:3	00006010h RO	**Discovery Table Offset (DISCOVERY_TABLE_OFFSET):** Base address of the discovery list for this capability space. This offset is relative to the device's MMIO address space (relative to the BAR).
2:0	0h RO	**BAR ID (BAR_ID):** The BAR to be used: 0: 0x10 (BAR0).

10.22 Crashlog Capability Header (CRASHLOG_CAPABILITY_HEADER) — Offset 120h

DVSEC header for crashlog capability.

Note: Bit definitions are the same as TELEM_CAPABILITY_HEADER, offset 100h.

10.23 Crashlog VSEC 0 (CRASHLOG_VSEC_0) — Offset 124h

Crashlog VSEC 0.

Note: Bit definitions are the same as TELEM_VSEC_0, offset 104h.

10.24 Crashlog VSEC 1 (CRASHLOG_VSEC_1) — Offset 128h

Crashlog VSEC 1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:10, F:0] + 128h	0A010004h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ah RO	**Entry Size (ENTRY_SIZE):** Entry Size in DWORDs.
23:16	01h RO	**Number of Entries (NUM_ENTRIES):** Number of entries, describes the number of telemetry aggregators that would exist in this capability lookup table.
15:0	0004h RO	**Discovery Type (DVSEC_ID):** Indicates the type of discovery entry. This is a crashlog capability.

10.25 Crashlog VSEC 2 (CRASHLOG_VSEC_2) — Offset 12Ch

Crashlog VSEC 2.

Note: Bit definitions are the same as WATCHER_VSEC_2, offset 11Ch.