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## General Purpose NPN Transistor Array

The CA3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

### Ordering Information

| PART NUMBER (BRAND) | TEMP. RANGE ($^o$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CA3046 | -55 to 125 | 14 Ld PDIP | E14.3 |
| CA3046M (3046) | -55 to 125 | 14 Ld SOIC | M14.15 |
| CA3046M96 (3046) | -55 to 125 | 14 Ld SOIC Tape and Reel | M14.15 |

### Pinout

CA3046 (PDIP, SOIC)
TOP VIEW
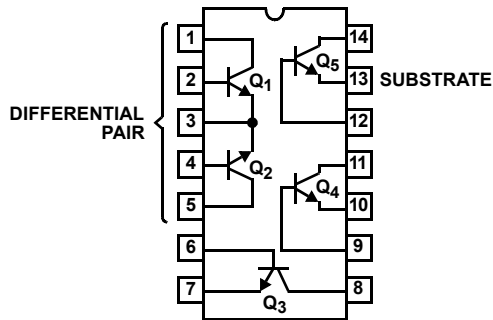


## Features

- Two Matched Transistors
  - $V_{BE}$ Match . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±5mV
  - $I_{IO}$ Match. . . . . . . . . . . . . . . . . . . . . . . . . . . .2µA (Max)

- Low Noise Figure . . . . . . . . . . . . . . . . 3.2dB (Typ) at 1kHz

- 5 General Purpose Monolithic Transistors

- Operation From DC to 120MHz

- Wide Operating Current Range

- Full Military Temperature Range

## Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range

- Custom Designed Differential Amplifiers

- Temperature Compensated Amplifiers

- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

## Absolute Maximum Ratings

Collector-to-Emitter Voltage ($V_{CEO}$) . . . . . . . . . . . . . . . . . . . . . 15V
Collector-to-Base Voltage ($V_{CBO}$). . . . . . . . . . . . . . . . . . . . . . . 20V
Collector-to-Substrate Voltage ($V_{CIO}$, Note 1). . . . . . . . . . . . . 20V
Emitter-to-Base Voltage ($V_{EBO}$) . . . . . . . . . . . . . . . . . . . . . . . . 5V
Collector Current ($I_C$). . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 50mA

## Operating Conditions

Temperature Range. . . . . . . . . . . . . . . . . . . . . . . . -55$^o$C to 125$^o$C

## Thermal Information

Thermal Resistance (Typical, Note 2)    $\theta_{JA}$ ($^o$C/W)   $\theta_{JC}$ ($^o$C/W)
  PDIP Package . . . . . . . . . . . . . . . . . . .    180       N/A
  SOIC Package . . . . . . . . . . . . . . . . . . .    220       N/A
Maximum Power Dissipation (Any One Transistor) . . . . . . . 300mW
Maximum Junction Temperature (Plastic Package) . . . . . . . .150$^o$C
Maximum Storage Temperature Range . . . . . . . . . -65$^o$C to 150$^o$C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . 300$^o$C
  (SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. The collector of each transistor of the CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

2. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications    $T_A = 25^oC$, characteristics apply for each transistor in CA3046 as specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| Collector-to-Base Breakdown Voltage | $V_{(BR)CBO}$ | $I_C = 10\mu A$, $I_E = 0$ | | 20 | 60 | - | V |
| Collector-to-Emitter Breakdown Voltage | $V_{(BR)CEO}$ | $I_C = 1mA$, $I_B = 0$ | | 15 | 24 | - | V |
| Collector-to-Substrate Breakdown Voltage | $V_{(BR)CIO}$ | $I_C = 10\mu A$, $I_{CI} = 0$ | | 20 | 60 | - | V |
| Emitter-to-Base Breakdown Voltage | $V_{(BR)EBO}$ | $I_E = 10\mu A$, $I_C = 0$ | | 5 | 7 | - | V |
| Collector Cutoff Current (Figure 1) | $I_{CBO}$ | $V_{CB} = 10V$, $I_E = 0$ | | - | 0.002 | 40 | nA |
| Collector Cutoff Current (Figure 2) | $I_{CEO}$ | $V_{CE} = 10V$, $I_B = 0$ | | - | See Fig. 2 | 0.5 | $\mu A$ |
| Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3) | $h_{FE}$ | $V_{CE} = 3V$ | $I_C = 10mA$ | - | 100 | - | - |
| | | | $I_C = 1mA$ | 40 | 100 | - | - |
| | | | $I_C = 10\mu A$ | - | 54 | - | - |
| Input Offset Current for Matched Pair $Q_1$ and $Q_2$. $\|I_{IO1} - I_{IO2}\|$ (Note 3) (Figure 4) | | $V_{CE} = 3V$, $I_C = 1mA$ | | - | 0.3 | 2 | $\mu A$ |
| Base-to-Emitter Voltage (Note 3) (Figure 5) | $V_{BE}$ | $V_{CE} = 3V$ | $I_E = 1mA$ | - | 0.715 | - | V |
| | | | $I_E = 10mA$ | - | 0.800 | - | V |
| Magnitude of Input Offet Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$ (Note 3) (Figures 5, 7) | | $V_{CE} = 3V$, $I_C = 1mA$ | | - | 0.45 | 5 | mV |
| Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$ (Note 3) (Figures 5, 7) | | $V_{CE} = 3V$, $I_C = 1mA$ | | - | 0.45 | 5 | mV |
| Temperature Coefficient of Base-to-Emitter Voltage (Figure 6) | $\dfrac{\Delta V_{BE}}{\Delta T}$ | $V_{CE} = 3V$, $I_C = 1mA$ | | - | -1.9 | - | mV/$^o$C |
| Collector-to-Emitter Saturation Voltage | $V_{CES}$ | $I_B = 1mA$, $I_C = 10mA$ | | - | 0.23 | - | V |
| Temperature Coefficient: Magnitude of Input Off-set Voltage (Figure 7) | $\dfrac{\|\Delta V_{IO}\|}{\Delta T}$ | $V_{CE} = 3V$, $I_C = 1mA$ | | - | 1.1 | - | $\mu V/^o C$ |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Low Frequency Noise Figure (Figure 9) | NF | $f = 1kHz$, $V_{CE} = 3V$, $I_C = 100\mu A$, Source Resistance = $1k\Omega$ | | - | 3.25 | - | dB |
| Low Frequency, Small Signal Equivalent Circuit Characteristics | | | | | | | |
|    Forward Current Transfer Ratio (Figure 11) | $h_{FE}$ | $f = 1kHz$, $V_{CE} = 3V$, $I_C = 1mA$ | | - | 110 | - | - |
|    Short Circuit Input Impedance (Figure 11) | $h_{IE}$ | $f = 1kHz$, $V_{CE} = 3V$, $I_C = 1mA$ | | - | 3.5 | - | $k\Omega$ |
|    Open Circuit Output Impedance (Figure 11) | $h_{OE}$ | $f = 1kHz$, $V_{CE} = 3V$, $I_C = 1mA$ | | - | 15.6 | - | $\mu S$ |

## Electrical Specifications  $T_A = 25^oC$, characteristics apply for each transistor in CA3046 as specified  **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Open Circuit Reverse Voltage Transfer Ratio (Figure 11) | $h_{RE}$ | f = 1kHz, $V_{CE}$ = 3V, $I_C$ = 1mA | - | $1.8 \times 10^{-4}$ | - | - |
| Admittance Characteristics | | | | | | |
| Forward Transfer Admittance (Figure 12) | $Y_{FE}$ | f = 1kHz, $V_{CE}$ = 3V, $I_C$ = 1mA | - | 31 - j1.5 | - | - |
| Input Admittance (Figure 13) | $Y_{IE}$ | f = 1kHz, $V_{CE}$ = 3V, $I_C$ = 1mA | - | 0.3 + j0.04 | - | - |
| Output Admittance (Figure 14) | $Y_{OE}$ | f = 1kHz, $V_{CE}$ = 3V, $I_C$ = 1mA | - | 0.001 + j0.03 | - | - |
| Reverse Transfer Admittance (Figure 15) | $Y_{RE}$ | f = 1kHz, $V_{CE}$ = 3V, $I_C$ = 1mA | - | See Fig. 14 | - | - |
| Gain Bandwidth Product (Figure 16) | $f_T$ | $V_{CE}$ = 3V, $I_C$ = 3mA | 300 | 550 | - | MHz |
| Emitter-to-Base Capacitance | $C_{EB}$ | $V_{EB}$ = 3V, $I_E$ = 0 | - | 0.6 | - | pF |
| Collector-to-Base Capacitance | $C_{CB}$ | $V_{CB}$ = 3V, $I_C$ = 0 | - | 0.58 | - | pF |
| Collector-to-Substrate Capacitance | $C_{CI}$ | $V_{CS}$ = 3V, $I_C$ = 0 | - | 2.8 | - | pF |

NOTE:

3. Actual forcing current is via the emitter for this test.

## *Typical Performance Curves*
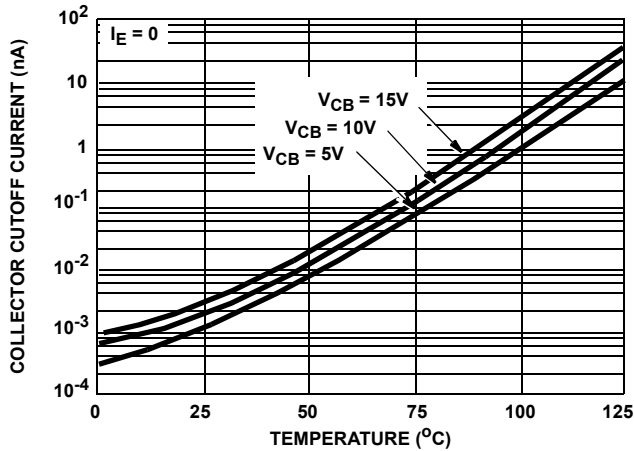


FIGURE 1.  TYPICAL COLLECTOR-TO-BASE CUTOFF CUR-
RENT vs TEMPERATURE FOR EACH TRANSISTOR
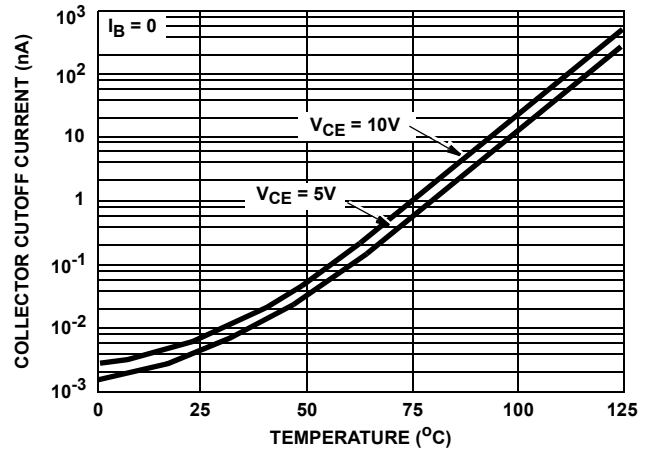


FIGURE 2.  TYPICAL COLLECTOR-TO-EMITTER CUTOFF
CURRENT vs TEMPERATURE FOR EACH
TRANSISTOR
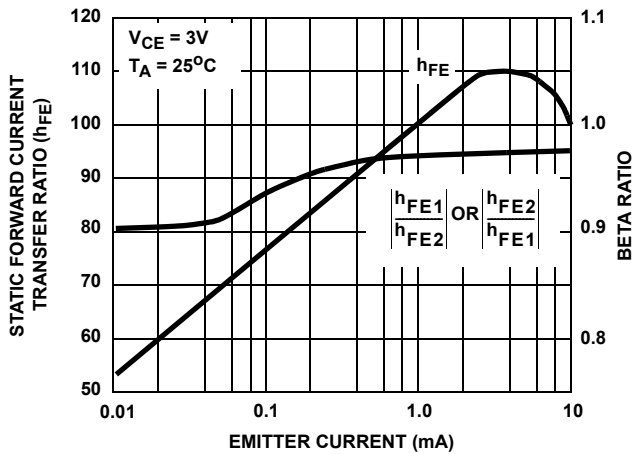


FIGURE 3.  TYPICAL STATIC FORWARD CURRENT TRANSFER
RATIO AND BETA RATIO FOR $Q_1$ AND $Q_2$ vs
EMITTER CURRENT
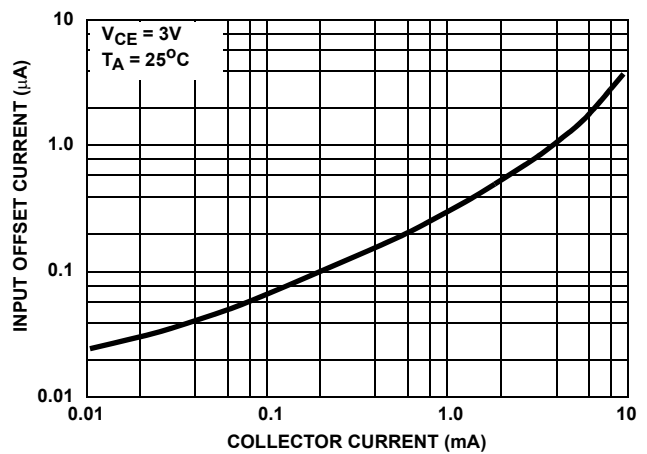


FIGURE 4.  TYPICAL INPUT OFFSET CURRENT FOR
MATCHED TRANSISTOR PAIR $Q_1Q_2$ vs
COLLECTOR CURRENT

## *Typical Performance Curves*  (Continued)
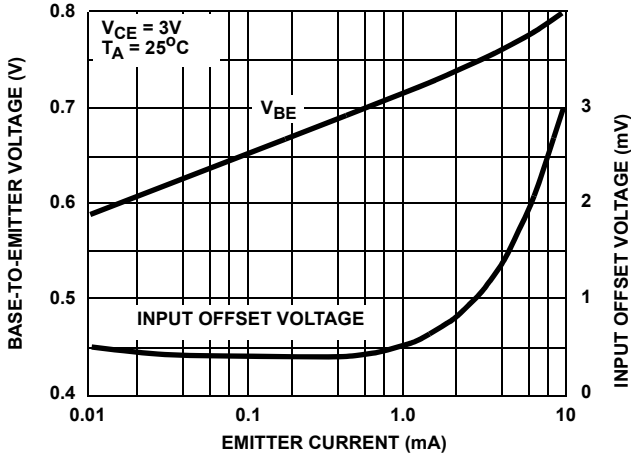


FIGURE 5.  TYPICAL STATIC BASE-TO-EMITTER VOLTAGE
CHARACTERISTICS AND INPUT OFFSET VOLT-
AGE FOR DIFFERENTIAL PAIR AND PAIRED ISO-
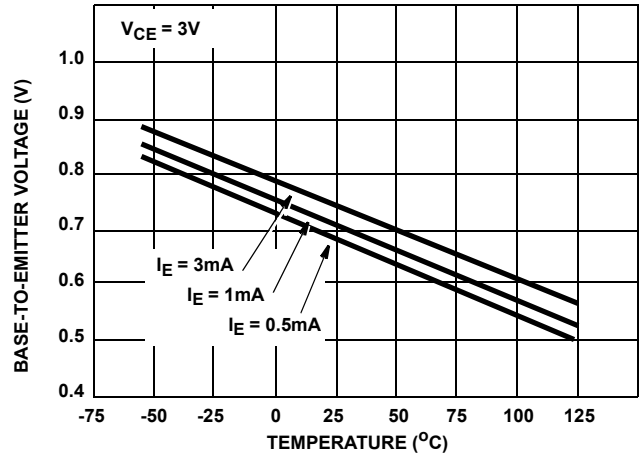LATED TRANSISTORS vs EMITTER CURRENT



FIGURE 6.  TYPICAL BASE-TO-EMITTER VOLTAGE
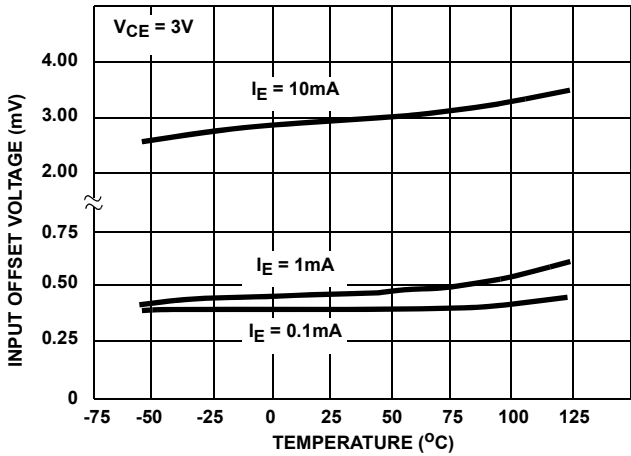CHARACTERISTIC vs TEMPERATURE FOR EACH
TRANSISTOR



FIGURE 7.  TYPICAL INPUT OFFSET VOLTAGE CHARACTERIS-
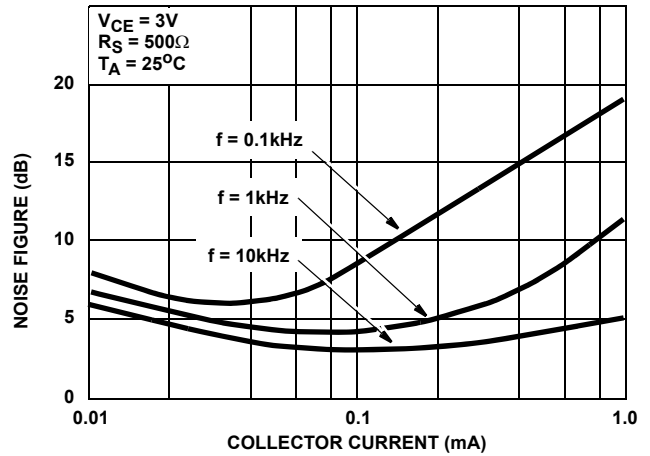TICS FOR DIFFERENTIAL PAIR AND PAIRED
ISOLATED TRANSISTORS vs TEMPERATURE



FIGURE 8.  TYPICAL NOISE FIGURE vs COLLECTOR CURRENT
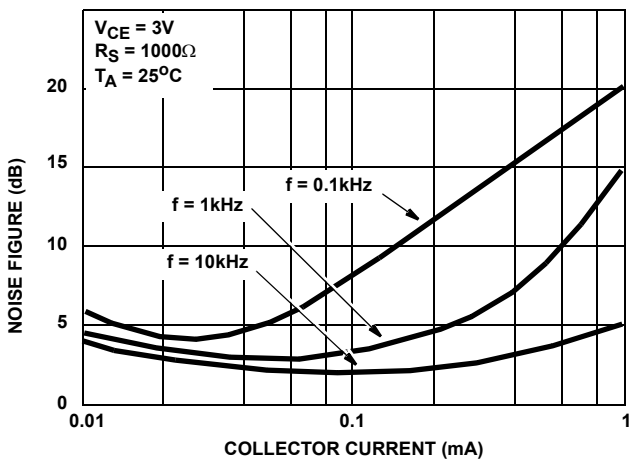


FIGURE 9.  TYPICAL NOISE FIGURE vs COLLECTOR CURRENT
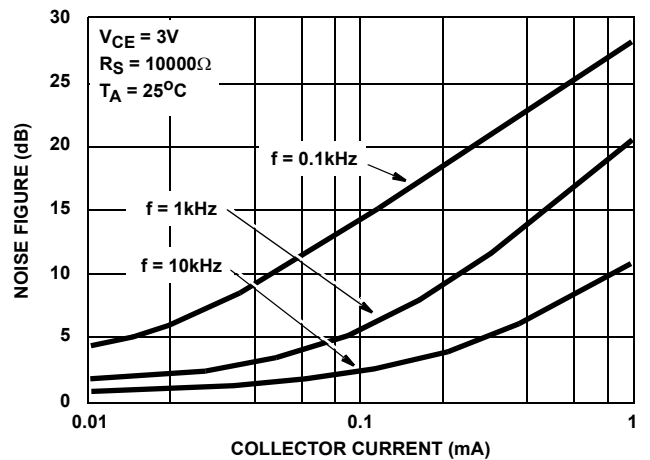


FIGURE 10.  TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

## *Typical Performance Curves* (Continued)
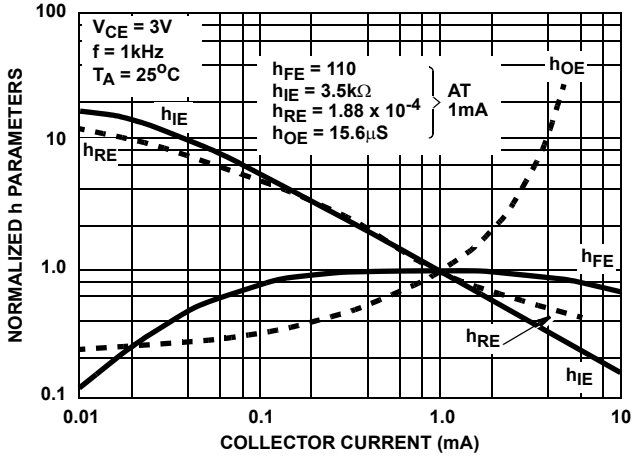


FIGURE 11. TYPICAL NORMALIZED FORWARD CURRENT
TRANSFER RATIO, SHORT CIRCUIT INPUT
IMPEDANCE, OPEN CIRCUIT OUTPUT IMPEDANCE,
AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER
RATIO vs COLLECTOR CURRENT
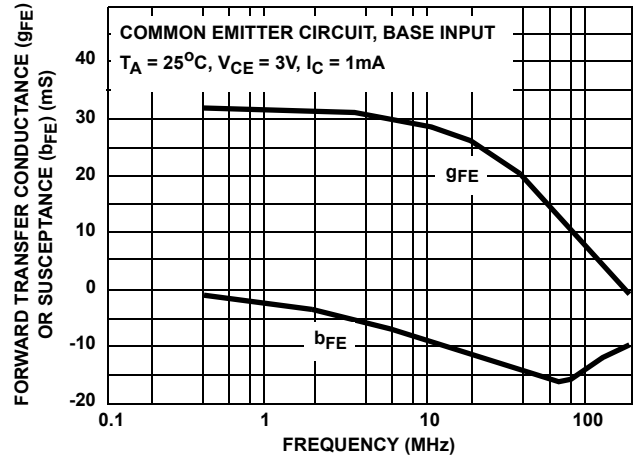


FIGURE 12. TYPICAL FORWARD TRANSFER ADMITTANCE vs
FREQUENCY
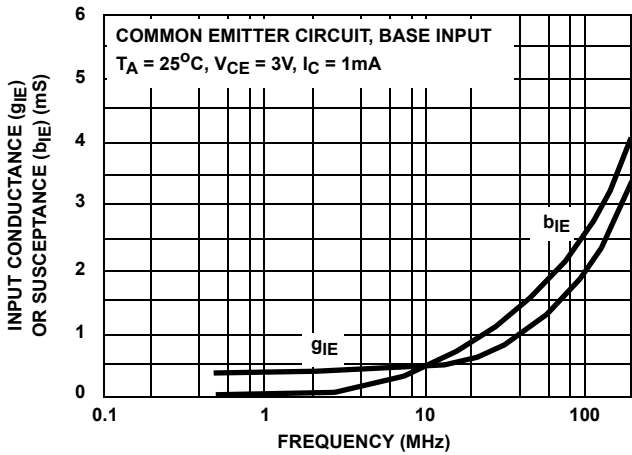


FIGURE 13. TYPICAL INPUT ADMITTANCE vs FREQUENCY
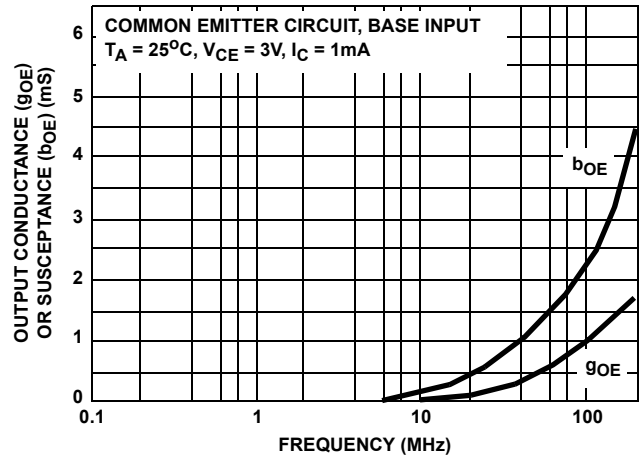


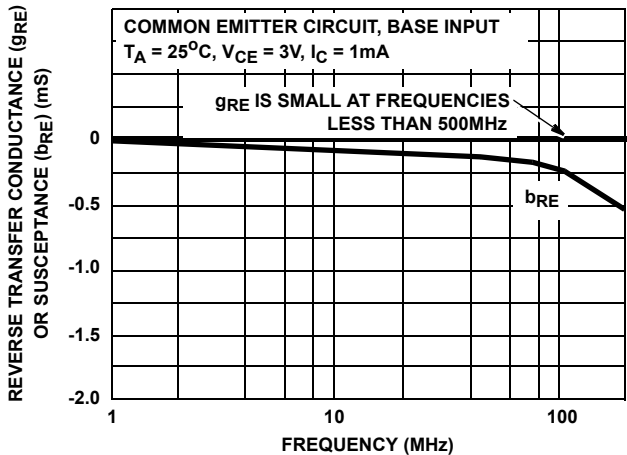FIGURE 14. TYPICAL OUTPUT ADMITTANCE vs FREQUENCY



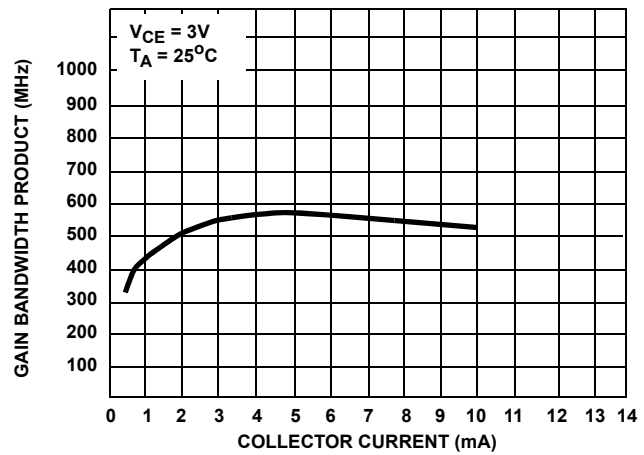FIGURE 15. TYPICAL REVERSE TRANSFER ADMITTANCE vs
FREQUENCY



FIGURE 16. TYPICAL GAIN BANDWIDTH PRODUCT vs
COLLECTOR CURRENT

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