Ultra Low SWaP DaQ for Rockets

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John McWhirter
Robert Brown

Final Report

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Ultra Low SWaP DaQ for Rockets

Andrew Bainbridge
John McWhirter
Robert Brown

Concept of Operations

REVISION – 0.1
3 October 2022

Concept of Operations
FOR
Ultra Low SWaP DaQ for Rockets

Team SWaP JAR

Approved by:

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Prof. Kalafatis Date

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T/A Date

Change Record

Rev.	Date	Originator	Approvals	Description
0.0	09/15/2022	Andrew Bainbridge		Draft Release
0.1	10/03/2022	Andrew Bainbridge		Midterm Report Release
0.2	4/27/2023	John McWhirter		Final Report Release

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1. Executive Summary

The company Sandia has requested for an UL-SWaP DaQ unit, which stands for "Ultra Low Size, Weight, and Power Data Acquisitions" unit. The purpose of the unit is to receive data from multiple sensors during rocket flight and transmit that data. The unit is to operate under rocket test flights, henceforth, the unit will be optimized in its size, weight, and power. In doing so, testing methods become more efficient, utilize less resources, and ultimately shorten the testing process. The implemented technology will lead to faster development and help Sandia fuel their mission of creating national and global security.

2. Introduction

Sandia National Laboratories operates as one of the three National Nuclear Security Administration Research and Development Laboratories in the United States. Science and Technology is being developed to counter threats to our National Security. Through them, the team has been given the opportunity to design a Data Acquisition unit for Rocket Testing. This unit will receive an arbitrary number of signals from sensors built into rockets and convert the analog signals into digital signals. It will also provide more space in the designated area for the technologies creating these signals allowing for a more productive utilization of the overall size, weight, and power.

2.1 Background

The current data acquisition systems are created dependent upon the data providing systems. This introduces a redundancy where the rocket payload has similar data acquisition systems. A new ultra low size, weight, and power data acquisition unit, or ULSWaP DaQ, designed to receive any number of arbitrary analog signals and convert them into digital signals will provide a more effective use of the physical space provided in the Sandia Rocket payload. In effect, this reduces the overall weight of the rocket and provides a consistent method to receiving and transmitting data.

2.2 Overview

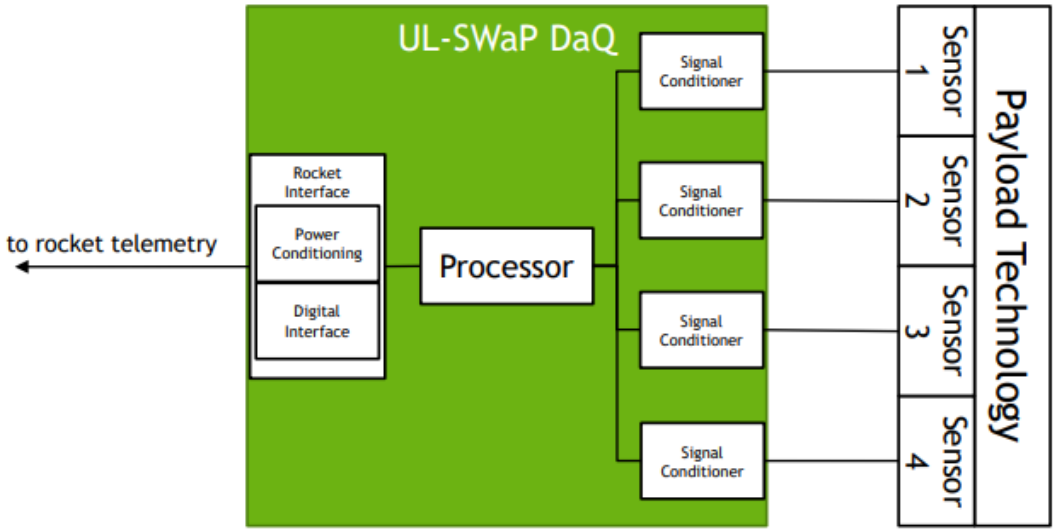

Figure 1: UL-SWaP DaQ Block Diagram

As shown in *Figure 1*, the Payload Technology is unknown to the UL-SWaP DaQ. However, the signals which it receives from the Payload Technology are inferred to meet the conditions of the Data Acquisition (DaQ) unit. The Signal Conditioners will refine each signal into a precise digital signal. The processor then receives each signal and uses an algorithmic method to translate the measured voltage or current driven digital signal into legible values for which the sensor is detecting. Finally, the signal is transmitted into the Rocket Interface which will provide that information to rocket telemetry.

2.3 Referenced Documents and Standards

The following documents were used in reference in this report and in setting the standards of the UL-SWaP DaQ:

- "Ultra Low SWaP DaQ for Rocket Flights"
    - Document: SWaP_DaQ_For_Rockets_SAND2022-10523-O.pdf

3. Operating Concept

3.1 Scope

The UL-SWaP DaQ unit is designed to receive data from a sensor during rocket flight and transmit that data directly to the user. The unit will receive various input signals with amplitudes ranging from 10 mV to 20 V. These signals will be attenuated or amplified by the unit. In addition, our unit will convert these signals into a single digital signal and drive a Low Voltage Differential Signal to be processed by rocket telemetry.

3.2 Operational Description and Constraints

3.2.1 Operational Description

The UL-SWaP DaQ unit will be used to obtain data from various devices tested on rockets and provide that data to the user/experimentalists. In particular, the device will be used specifically to help test devices and instruments created by engineers within the Sandia Company. Sandia's main mission is to develop nuclear weapons and deterrent systems; Therefore, the device will be used to assist in developing new technology and equipment that will help deter foreign forces.

3.2.2 Operational Constraints

The main constraint is that the small design of the data acquisitions unit limits the amount of sensors that can be in use. This means that only a limited amount of equipment can be tested with the unit at one time.

3.3 System Description

Our system is an UL-SWaP DaQ for rocket flights. This stands for "Ultra Low Size, Weight, and Power Data Acquisitions" unit. The main role of our device is to retrieve data from an experimentalist's device and send that data back to the user by communicating with the rocket telemetry system. Our device is made up of a series of signal conditioners that will take in analog signals from the device payload and filter those signals to remove unwanted background noise. These signals are then converted into a digital signal through the processor of the device and are transmitted to the rocket telemetry to be sent back to the user. This device will give the user real time data on how their equipment is performing with the rigorous environment of rocket flight.

3.4 Modes of Operations

The specific modes of operation will be dependent on the sensor of the payload for the equipment in testing. However, the data acquisitions unit will be hooked up manually to a payload with a certain amount of sensors and will then be in "automatic" or "standby" as it waits to read and send information that it gets from the device during flight.

3.5 Users

Our system will be targeted towards Sandian engineering experimentalists who do not have as much experience with electrical systems or who require the assistance of an electrical engineer. Our device will be user friendly and will allow experimenters to easily access the data necessary for their piece of equipment. The device will be accompanied by a user manual and datasheet, so that it can easily be installed by any experimenter regardless of their specific technical background. This will be described in more detail in the "Support" section of this document.

3.6 Support

Support would be provided in the form of a data sheet and a user manual. The datasheet will include the specific design of the device and how the data will get back to the user. It will also include the power requirements and temperature limitations of the DaQ. The user manual will inform the user how to incorporate the DaQ into a system of sensors.

4. Scenario(s)

4.1 General Purpose Accelerometer

A new accelerometer has been created by a mechanical engineer in a department at Sandia. However, their knowledge of computer engineering is limited to the sensor they designed and the analog signal it has created. Designing a DaQ is outside the scope of the mechanical engineer's project and they have requested a method to read the data the new accelerometer is producing. Using the UL-SWaP DaQ, the engineers can easily install their unit into the rocket and wire together the analog signal transmitter to the DaQ without designing a DaQ for their sensor.

5. Analysis

5.1 Summary of Proposed Improvements

Some advantages of this DaQ system will be its superior performance in size, weight, and power within the field of rocketry. Certain design considerations must be made when working in the field of rocketry and this DaQ will be developed to meet those criteria. Our DaQ will consume less energy, be lightweight, and have a smaller size when compared to traditional DaQ systems. Another advantage of this DaQ system will be its modularity. The modularity of this DaQ will allow experimenters to compartmentalize their experiments on the rocket with considerable ease.

5.2 Disadvantages and Limitations

The disadvantages to the UL-SWaP DaQ include:

- The system will have a bandwidth limitation due to the number of analog signals it is going to receive.
- One disadvantage is that our system will have size restrictions and integrating a cooling system for the processor will be challenging. Additionally, the DAQ will be on a rocket and further heating from the engine is likely.

5.3 Alternatives

The alternative, and current solution, does have advantages. Whichever party designs the sensor payload and the DaQ for that payload also has the ability to debug each project and tune it to their desired needs. This could result in a better signal for that payload than what could be provided by our UL-SWaP DaQ.

UL-SWaP DaQ for Rocket Testing

Andrew Bainbridge
John McWhirter
Robert Brown

Functional System Requirements

REVISION – 0.2
27 April 2023

FUNCTIONAL SYSTEM REQUIREMENTS
FOR
UL-SWaP DaQ

PREPARED BY:

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Author Date

APPROVED BY:

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Project Leader Date

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John Lusher, P.E. Date

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T/A Date

Change Record

Rev.	Date	Originator	Approvals	Description
0.1	10/03/22	Andrew Bainbridge		Midterm Report Release
0.2	11/30/22	John McWhirter		Final Report Revisions
0.3	4/27/23	John McWhirter		Updated Final Report

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6. Introduction

6.1. Purpose and Scope

The company Sandia has requested for an Ultra Low Size, Weight, and Power Data Acquisitions unit (UL-SWaP DaQ). The purpose of the unit is to receive and transmit data to rocket telemetry regardless of the type or number of sensors in the payloads. This data will be used to assess the integrity of each payload on the rocket or the rocket itself. In addition, the unit will be optimized in size, weight, and power. The unit will also be designed to be easily integrated with outside electrical systems. Overall, the UL-SWaP will cut down on expenses, reduce rocket payload space and resources, and provide a consistent method for data collection.

6.2. Responsibility and Change Authority

Our project is led by Sandia National Labs, with Dr. Matthew McDonough acting as our head sponsor. Changes made to the project requirements, performance, or implementation will be made by the head sponsor of our project or by the consensus of all of the team members in our team. The team leader, Andrew Bainbridge, is responsible for keeping the team on track with fulfilling all of the project requirements. Team members will provide assistance to each other where needed, however each team member will be responsible with fulfilling the requirements necessary for their respective subsystem which is indicated below:

- Andrew Bainbridge: Signal Conditioning
- John McWhirter: Processor and Interface
- Robert Brown: Power Module

7. Applicable and Reference Documents

7.1. Applicable Documents

The following documents, of the exact issue and revision shown, form a part of this specification to the extent specified herein:

Document Number	Revision/Release Date	Document Title
352A71	Revision D - 15 Jan 2014	**PCB PIEZOTRONICS: ICP Accelerometer - Datasheet**
SLVS493E	March 2004	**TPS6513x Dual, Positive and Negative Output DC-DC Converter**
SLUSEF6C	Nov 2022	**LMR51420 SIMPLE SWITCHER® 4.5-V to 36-V, 2-A, Synchronous Buck Converter in a SOT-23 Package - Datasheet**
TC7660S	07/04/2015	**Super Charge Pump DC-to-DC Voltage Converter**
DS011394	June 1999	**LM2574/LM2574HV SIMPLE SWITCHER 0.5A Step-Down Voltage Regulator**

M9999-072805	July 2005	**LMR2574 52KHz Simple 0.5A Buck Regulator**
DS60001185H	May 14 2019	**32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Audio/Graphics/Touch (HMI), USB, and Advanced Analog**
237316fa	LT 0317 - REV A	**LTC2373-16 16-Bit, 1Msps, 8-Channel SAR ADC with 96dB SNR**
ADN4661	12/08—Revision 0: Initial Version	**Single, 3 V, CMOS, LVDS, High Speed Differential Driver**
SLOS214C	Released Oct 1998 - Revised March 2007 (Rev C)	**70-MHz Programmable-Gain Amplifiers datasheet (Rev. C)**
6362fa	Revision A - 2012	**Precision, Low Power Rail-to-Rail Input/Output Differential Op Amp/SAR ADC Driver**

Table 1: Applicable Documents

7.2. Reference Documents

The following documents are reference documents utilized in the development of this specification. These documents do not form a part of this specification and are not controlled by their reference herein.

Document Number	Revision/Release Date	Document Title
XCEL-100-1	2014	**Kulite: High Temperature Miniature Pressure *Transducer - XCEL-100 Series**
DS902550	2016	**Surface RTD Temperature Probes**
SNLA187	Jan 2008	**LVDS Owner's Manual: Including High-Speed CML and Signal Conditioning 4th Edition**
DS70005283B	November 11 2016	**PIC32MX470 Curiosity Development Board User's Guide**

Table 2: Reference Documents

7.3. Order of Precedence

In the event of a conflict between the text of this specification and an applicable document cited herein, the text of this specification takes precedence without any exceptions.

All specifications, standards, exhibits, drawings or other documents that are invoked as "applicable" in this specification are incorporated as cited. All documents that are referred to within an applicable report are considered to be for guidance and information only, except ICDs that have their relevant documents considered to be incorporated as cited.

8. Requirements

This section defines the minimum requirements that the development item(s) must meet. The requirements and constraints that apply to performance, design, interoperability, reliability, etc., of the system, are covered.

8.1. System Definition

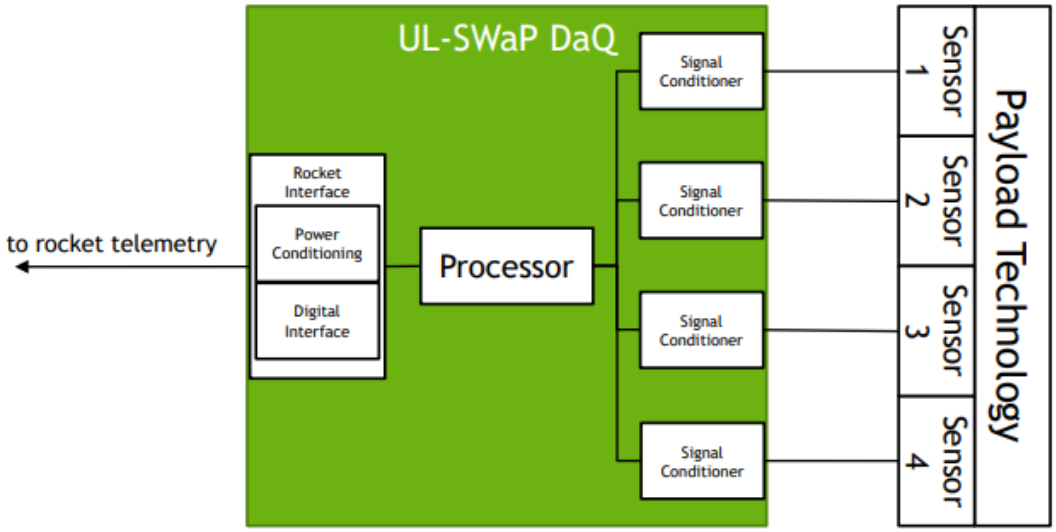

Figure 2: UL-SWaP DaQ Block Diagram

The UL-SWaP DaQ is a data acquisitions unit that is designed to be low in size, weight, and power and usable during rocket flight. The system is divided into three main subsystems: the signal conditioning, the processor and interface unit, and the power module unit. The signal conditioning subsystem is responsible for taking in the analog signals given from the sensor connected to the payload and converting it into clean usable digital signals for the processor. The processor and interface subsystem is responsible for communicating with each signal conditioner in order to control the conditioning and operability of each signal and to transmit the data to the rocket telemetry. The power module subsystem is responsible for supplying adequate power to all components. The system is designed to be hardware compatible with the sensors for experimentalists. In addition, the low power and size design will allow for easy mounting/storage of the device within each payload.

8.2. Characteristics

This section describes all of the functional, physical, and electrical characteristics of the UL-SWaP DaQ.

8.2.1. Functional / Performance Requirements

8.2.1.1. Maximum Power Draw

The power draw of the UL-SWaP DaQ System shall not exceed 3 Watts. The goal of the project is to optimize the power throughout the duration of this project. Required power rails are 3.3V, 5V, 10V, and -10V.

> *Rationale: This power requirement was specified by our sponsor at Sandia to ensure more power is being delivered to the payload sensors.*

8.2.1.2. Variable Signal Conditioning

The UL-SWaP DaQ shall have the necessary electronic components to filter, amplify, and/or attenuate each input signal. In addition, each signal conditioner shall be programmed independently of other signal conditioners allowing for various different configurations for various different signals.

> *Rationale: The goal of this project is to provide a consistent method of data acquisition for the payload sensors defeating the need for clients of Sandia to produce a sensor and a DaQ for that sensor. Ultimately reducing the size, weight, and power of the payload.*

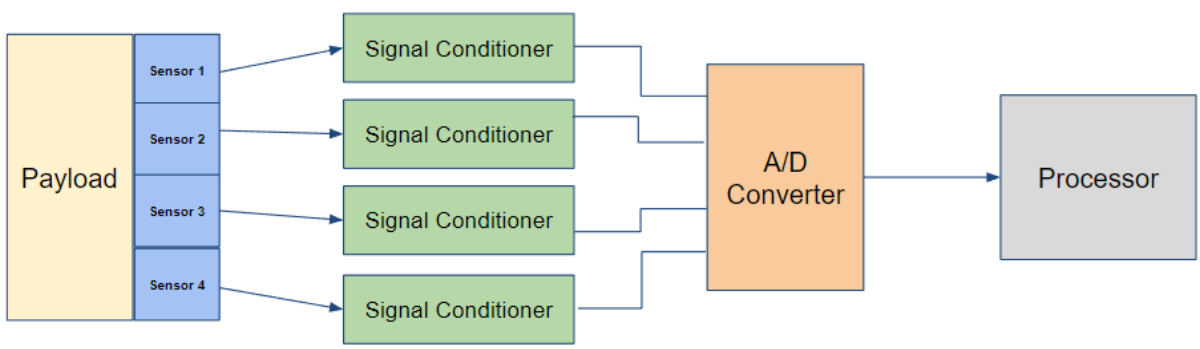

Figure 3: Variable Signal Conditioning Circuit

8.2.1.3. LVDS Data Transmission Protocol

The UL-SWaP DaQ shall transmit the data received from the input signals with LVDS protocol. This will aid in the Higher frequencies of the input signals while maintaining low power.

8.2.1.4. Hardware/Software Selectable Output Voltage

The UL-SWaP DaQ shall have the capability of Hardware and/or Software selectable sensor output voltage using the table below.

Configuration Number	*Gain dB*	*Gain V/V*
0	-22	0.08
1	-16	0.16
2	-10	0.32
3	-4	0.63
4	2	1.26
5	8	2.52
6	14	5.01
7	20	10.0

Table 3: Configuration Table for Programmable Gain Amplifier and main.c

Rationale: This requirement was stated by the sponsor. It is desired to develop a software selectable sensor output voltage after a method through hardware is obtained.

8.2.2. Physical Characteristics

This section describes all of the physical characteristics of the UL-SWaP DaQ unit. More details on this can be found in the ICD section of this report.

8.2.2.1. Mass

The mass of the UL-SWaP DaQ System shall be less than or equal to 500 grams. We will be trying to optimize this weight to be as low as possible throughout the duration of this project.

Rationale: The weight requirement specified by our sponsor was to optimize the DaQ to be as low as possible.

8.2.2.2. Volume Envelope

The volume of the DaQ shall be less than or equal to 3 inches in height, 3 inches in width, and 3 inches in length. It is desired that the volume of the DaQ be 2 inches in height, 2 inches in width, and 2 inches in length.

Rationale: This is a requirement specified by our sponsor due to constraints of their system in which the UL-SWaP DaQ is integrating.

8.2.2.3. Mounting.

The UL-SWaP DaQ will be connected and mounted depending on the user and payload being tested.

Rationale: The UL-SWaP DaQ will be mounted according to the standards and needs of the experimentalist testing their equipment.

8.2.3. Electrical Characteristics

8.2.3.1. Inputs

The DaQ may have the following transducer inputs that will be connected to the unit in order to collect data of the payload: Accelerometer (shock), pressure, RTD (temperature), and output voltage. In addition, there will also be an input connection to the power supply of the DaQ in order to provide power to the unit. The DaQ may have unknown transducer inputs.

8.2.3.1.1. Input Voltage Level

Refer to the "Primary Input Power" section of the ICD for this information.

8.2.3.2. Power Consumption

The maximum peak power of the system shall not exceed 3 watts.

> *Rationale: This is a requirement specified by our sponsor due to constraints of their system in which the UL-SWaP DaQ is integrating.*

8.2.3.4. Outputs

8.2.3.4.1. Data Output

The UL-SWaP DaQ shall include an interface compatible with the data system for testing purposes only. The scope of this project is within the DaQ. Any Data Output created from a testing input shall be collected with existing software.

> *Rationale: The UL-SWaP DaQ is unaware of the type of data being received and transmitted. It only knows how it must condition each signal and convert them into a digital signal.*

8.2.3.4.2. Diagnostic Output

The UL-SWaP shall include a method to debugging signal conditioners using outside Signal Generators and Oscilloscopes.

> *Rationale: Provides the ability to debug the circuit without designing a new set of circuits to debug.*

8.2.3.5. Connectors and Wiring

The UL-Swap DaQ will have signal input Nano Connectors on the board layout. These inputs will be wired by traces that will connect to the PIC-32 processor and the power module. The processor will have a debugging and programmable interface for the ICD4 in order to access the processor.

> *Rationale: This is a requirement specified by our customer due to constraints of their system in which the Search and Rescue System is integrating.*

8.2.4. Environmental Requirements

The UL-SWaP DaQ unit will be enclosed with the payloads in a secure environment inside of a Sandia National Labs based rocket. Therefore, there are no necessary environmental requirements to consider for the scope of this project other than the change in dynamic pressure throughout the duration of the rocket flight except for general housing of the components.

Rationale: This is a requirement specified by our sponsor due to constraints of their system in which the UL-SWaP DaQ is integrating.

8.2.4.1. Pressure

During rocket flight, the increasing altitude causes a decrease in the atmospheric pressure; however, the constant increase in rocket velocity during rocket flight causes an increase in the dynamic pressure of the rocket, and in turn can cause pressure vibrations. Therefore, the UL-SWaP DaQ will be designed so that it is symmetrical both in design and weight so that it will be able to withstand the intense vibrations that occur during rocket flight.

8.2.5. Failure Propagation

The UL-SWaP DaQ will log all results of the input and output signals. In addition, the configurations for each of the signal conditioners will be used in defining faults during flight time which will be accessible in a detailed log.

9. Support Requirements

The experimentalist using the UL-SWaP DaQ will be given two supporting documents in order to use and understand the specifications of the DaQ: a data sheet and a user manual

9.1. Data Sheet

The Data sheet of the UL-SWaP DaQ will not be finalized until the end of this project. However, the data sheet will be include all of the following specifications of the DaQ:

- Voltage input modules (maximum and minimum)
- Frequency ranges for each signal conditioner
- Accepted signal inputs/measurements
- Input hardware
- Schematic of DaQ
- A/D characteristics
- PIC32 Processor Specifications
- Power Module DC-DC Conversion Specifications
- Doxygen Generated Documentation
- Etc.

9.2. User Manual

The experimentalists will also be given a user manual that explains how to set up the UL-SWaP DaQ with their system. Specifically, how to connect their payload sensors to the DaQ and how they will be able to access the data. The payload sensors will be connected to the DaQ with Nano-D Connectors so they can withstand the high-G environment of rocket flight. This will describe which inputs will take in what sensor signal, the range of that signal, and the frequency of the signal. The data will be transferred to the user using an LVDS system. This document will be appended to the data sheet for the user to have so they will be able to connect the DaQ to their device.

9.3. Doxygen Generated Documentation and Github Repository

Doxygen Generated Documentation will be provided allowing for a user-friendly interface to the project coded in C. This will describe the directory structure of the code, provide configuration details for the PGAs, and guidance on general maintenance of the code. A Github Repository will also be used for Revision History and easy code migration.

UL-SWaP DaQ for Rocket Testing

Andrew Bainbridge
John McWhirter
Robert Brown

Interface Control Document

REVISION – 0.2
27 April 2023

INTERFACE CONTROL DOCUMENT
FOR
UL-SWaP DaQ

PREPARED BY:

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Author Date

APPROVED BY:

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Project Leader Date

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John Lusher II, P.E. Date

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T/A Date

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Rev.	Date	Originator	Approvals	Description
0.0	10/03/22	Andrew Bainbridge		Midterm Report Release
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0.2	4/27/23	John McWhirter		Update Final Report Release

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10. Overview

The purpose of this document is to provide a reader with a general understanding of the subsystem designs and physical characteristics within this UL SWaP DaQ. The intent behind designing and building this DaQ is to provide researchers at Sandia National Laboratories an easy way to communicate with any sensors used within their in-flight experiments. The UL SWaP DaQ will comprise three main subsystems: the power module, the signal conditioning units, and the processor and interface. The signals being created by the sensors will be sent through the signal conditioners where they will be filtered, attenuated and/or amplified. That signal is then passed through an ADC converter so that it may be read by the processor. The processor will then pass the data on to an LVDS driver. All the components within this module will receive their power from the main power supply for the payload which is regulated and stepped down by buck converters.

11. References and Definitions

11.1. References

All documents that were used for reference in this report are shown in the table below:

Document Number	Revision/Release Date	Document Title
352A71	Revision D/ 15 Jan 2014	**PCB PIEZOTRONICS: ICP Accelerometer - Datasheet**
SNLA187	Jan 2008	**LVDS Owner's Manual: Including High-Speed CML and Signal Conditioning 4th Edition**
XCEL-100-1	2014	**Kulite: High Temperature Miniature Pressure Transducer - XCEL-100 Series**
SLUSEF6C	Nov 2022	**LMR51420 SIMPLE SWITCHER® 4.5-V to 36-V, 2-A, Synchronous Buck Converter in a SOT-23 Package - Datasheet**
SLVS493E	March 2004	**TPS6513x Dual, Positive and Negative Output DC-DC Converter**
TC7660S	07/04/2015	**Super Charge Pump DC-to-DC Voltage Converter**
DS011394	June 1999	**LM2574/LM2574HV SIMPLE SWITCHER 0.5A Step-Down Voltage Regulator**
M9999-072805	July 2005	**LMR2574 52KHz Simple 0.5A Buck Regulator**
DS902550	2016	**Surface RTD Temperature Probes**
DS70005283B	November 11 2016	**PIC32MX470 Curiosity Development Board User's Guide**

Table 4: Reference Documents

11.2. Definitions

Definitions will be located in "Appendix B" of this document.

12. Physical Interface

12.1 Weight

Due to the goal of making the DaQ as low weight as possible while still being effective, the weight of the unit is subject to change throughout the course of this project. However; the goal weight of the UL-SWaP DaQ is to be under 400 grams without the outer covering, and under 500 grams with the outer protective covering.

12.2 Dimensions

Due to the goal of making the DaQ as small as possible while still being effective, the size of the unit is subject to change throughout the course of this project. However; the UL-SWaP DaQ will have the following dimension specifications:

- Maximum size: $9in^2$
- Stretch/Goal size: $4in^2$

12.3 Mounting Locations

The UL-SWaP DaQ will be stored with the payload in the rocket during the duration of the flight. The mounting locations of the DaQ will be dependent on the needs of the payload and the resources available to the experimentalist. The low size and weight design of the DaQ will give the experimentalists options on how and where they desire to store the DaQ in order to get the best results.

13. Thermal Interface

The UL-SWaP DaQ will be enclosed in a relatively controlled environment inside of a Sandia National Labs rocket, where the thermal interfaces are outside of the scope of this project.

14. Electrical Interface

14.1. Primary Input Power

Primary input power will be considered from two areas: the power input from the sensors into the signal conditioning system and the power delivered into each system component by the power module. The payload power supply is a DC supply that starts up to 32V and lowers down to 24V as the flight of the rocket proceeds. The components of the signal processor and the processor will require lower, more stable voltages. Our team will use a DC-DC buck converter called LMR51420 created by Texas Instruments due to its wide input voltage range, high efficiency, and ease of use. The PIC32 microcontroller will require a 3.3V DC voltage source, the LTC2373 ADC will require a 5V DC voltage source, the PGAs will require a positive and negative 10V DC voltage source, and the differential amplifiers will require a 5V DC voltage source. Three DC-DC converters will be used. These converters require RLC components to be fully operational. Guidelines from the chosen converter data sheet provide more details on chosen RLC components.

14.1.1. Signal Conditioning Input Power

Each of the sensors that are sending signals from the payload to the DaQ will be at different voltage ranges as the input voltage for the signal conditioners:

- Accelerometer: 7-12V input
- RTD Sensor: < 0.5mA input
- Pressure Sensor: 0-200mV input
- Voltage output sensor: 0-32 Volts; depends on the stimulus measured

Note: These are sample inputs. It is possible to have signals outside the range of this. Each will be adjusted accordingly.

14.1.2. Processor Input Power

The processor will require a constant 3.3 voltage input in order to function. This will be supplied by a DC-DC buck converter which receives its input from the main payload supply.

14.2. Polarity Reversal

Differential Signaling is interpreted by detecting which Voltage lead is in the HIGH state. If the positive Voltage Reference is in the HIGH state, the negative Voltage Reference is in the LOW state. This aids in maintaining signal integrity. The distance of our output signal is unknown, hence, Differential Signaling ensure the least data loss during transmission.

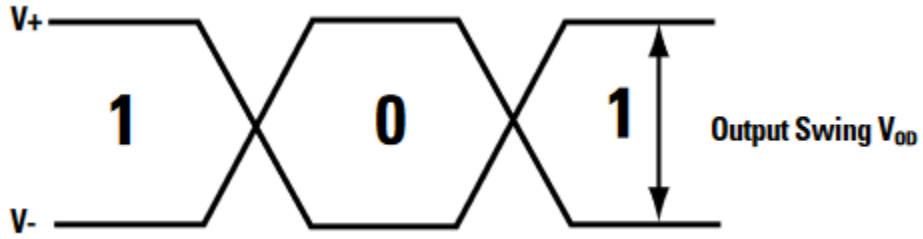

Figure 4: Differential Signaling

14.3. Signal Interfaces

A combination of any of the sensors described in this section can be used with our system. In addition, new sensors could be introduced that are unknown to the team.

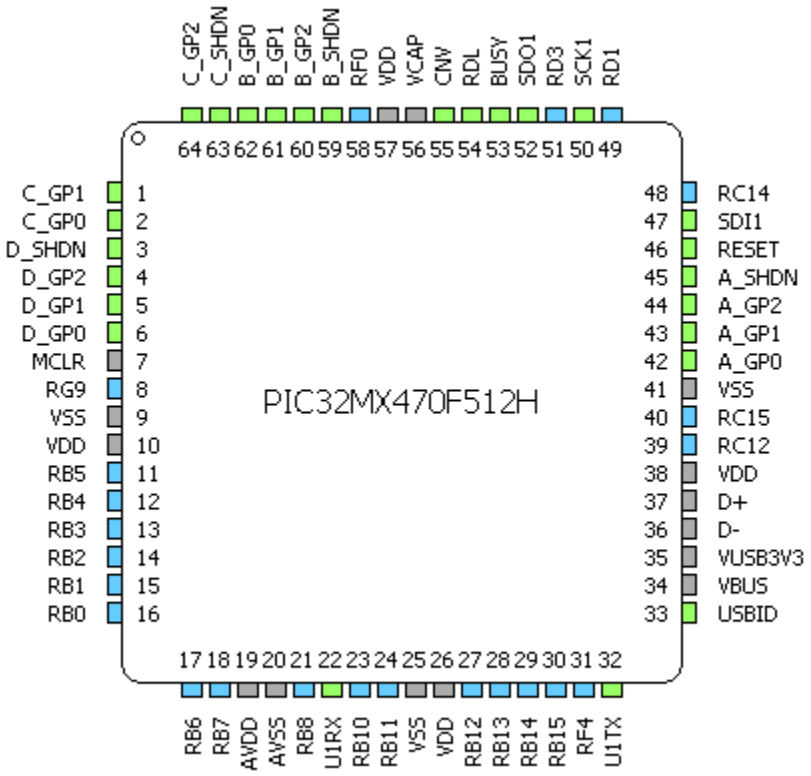

Figure 5: PIC32 with Pin Labels Block Diagram

14.3.1. Accelerometer Sensor

The accelerometer will output a voltage range shown in the table below. The specification sheet for the sensor will be used to program our PIC32 into configuring the necessary signal conditioners. This sensor requires a constant current from 0.2 to 25 mA.

Sensor	Output Bias Voltage	Excitation Voltage	Frequency Range
Model : 352A71	7 to 12 VDC	18 to 30 VDC	0.2 to 25kHz

Table 5: Output Voltage and Frequency Range of Accelerometer

14.3.2. RTD Temperature Gauge

The RTD Temperature Gauge will output a voltage and current range shown in the table below. The specification sheet for the sensor will be used to program our PIC32 into configuring the necessary

signal conditioners. The frequency range of the sensor will depend on the signal path of the conditioner and may range within 10 to 100kHz.

Sensor	Output Bias Voltage	Output Bias Current	Frequency Range
Model : 6568T13	0 to 10 VDC	4 to 20 mA	Dependent on signal path

Table 6: Output Voltage/Current and Frequency Range of RTD Gauge

14.3.3. Pressure Sensor

The pressure sensor will output a voltage range shown in the table below. The specification sheet for the sensor will be used to program our PIC32 into configuring the necessary signal conditioners. There will be a varying output frequency that is proportional to the pressure range of the environment.

Sensor	Full Scale Output	Excitation Voltage	Frequency Range
Model : xcel-100	0-200 mV	10 to 12 VDC	175 kHz to 1 MHz

Table 7: Output Voltage and Frequency Range of Pressure Sensor

14.3.4. Pure Voltage Output Sensor

For testing purposes, this sensor will be an 10 kOhm potentiometer. The details of the circuit are described in the table below.

Sensor	Full Scale Output	Excitation Voltage	Frequency Range
Potentiometer	-32 to 32 VDC	0 to 32 VDC; Depends on the stimulus measured	10 kHz to 100 kHz

Table 8: Output Voltage and Frequency Range of Pure Output Voltage

14.4. User Control Interface

The data will be collected by an external system. For testing purposes, this system will be a combination of oscilloscopes, function generators, and an ICD4 to interface with the PIC32.

15. Communications / Device Interface Protocols

15.1. PIC32 I/O Data Communication

The output signals will meet the TIA/EIA-644, or LVDS, standard. This is due to the bandwidth range of the payload sensors, 10 kHz-100kHz.

15.2. PIC32 I/O to Peripherals

The onboard PIC32 will control the PGAs and ADC Converter. GPIO pins on the PIC32 microcontroller will be dedicated to the PGAs to configure gain and control PGA shutdown. The PIC32 will communicate to the ADC under SPI protocols and output a digital signal under UART protocols to an LVDS Driver. The PIC32 will be programmable via connection of ICD4. The commands will contain configurations for all components on the board.

UL-SWaP DaQ for Rocket Testing

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John McWhirter
Robert Brown

Subsystem Reports

REVISION – 0.2
27 April 2023

SUBSYSTEM REPORTS
FOR
UL-SWaP DaQ

PREPARED BY:

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Author Date

APPROVED BY:

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Project Leader Date

_____
John Lusher II, P.E. Date

_____
T/A Date

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16. Introduction

The Ultra Low Size, Weight, and Power Data Acquisitions unit can be broken down into the following subsystems; power conditioning, signal conditioning, and the processor and interface subsystem. The power conditioning subsystem created and distributed the proper power rating to each section of the device that needs a particular voltage and current in order to function. The signal conditioning takes in the input signals being tested on the aircraft and turns them into differential outputs that are adjusted to be sent to the processor. The processor and interface subsystem is in charge of taking in the adjusted signal and converting it into digital data that will then be sent to the user.

17. Power Subsystem Report

17.1. Subsystem Introduction

This power module was designed with rocket flight in mind. The power source for the rocket was to be a 32V DC battery that would drop down to 25V throughout the flight of the rocket. Thus, it was necessary to consider a wide input voltage when designing the module. Additionally, there were several different loads that were required by the other subsystems. These can be seen in Table 9. Other aspects that had to be considered were the power consumption, size, and weight of the power subsystem.

Part	Voltage (V)	Current (mA)	Power (W)
PIC32	3.3	~100	.33
ADC	5	~11	0.55
PGA	+/-10	~40	0.4
Diff. Amp	5	~4	0.02
LVDS Driver	3.3	~10	0.033

Table 9: Load requirements for power subsystem

17.2. Subsystem Details

In order to provide efficient use of space, only 3 ICs were used in the subsystem design. A DC-DC buck (LMR51420 by TI) converter was used to create the 3.3V and 5V rails. A dual output boost converter/inverter (TPS6513x by TI) was used to create the 10.5V and -10V rails. The 3.3V rail was fed into the dual output IC as well as its necessary loads. The DC-DC converter used for the 3.3V and 5V rails were identical and were rated up to 2A of current. The actual current draw from the loads was well below this figure so feeding the 3.3V system into its designated loads as well as the +/- 10V system did not draw more current than it was rated to produce.

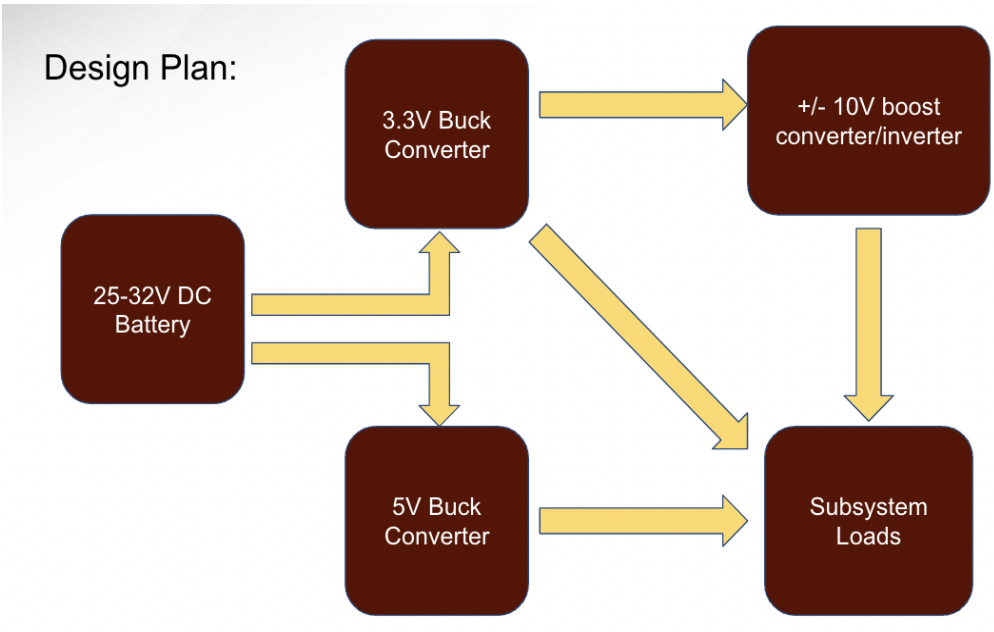


Figure 6: Power system block diagram

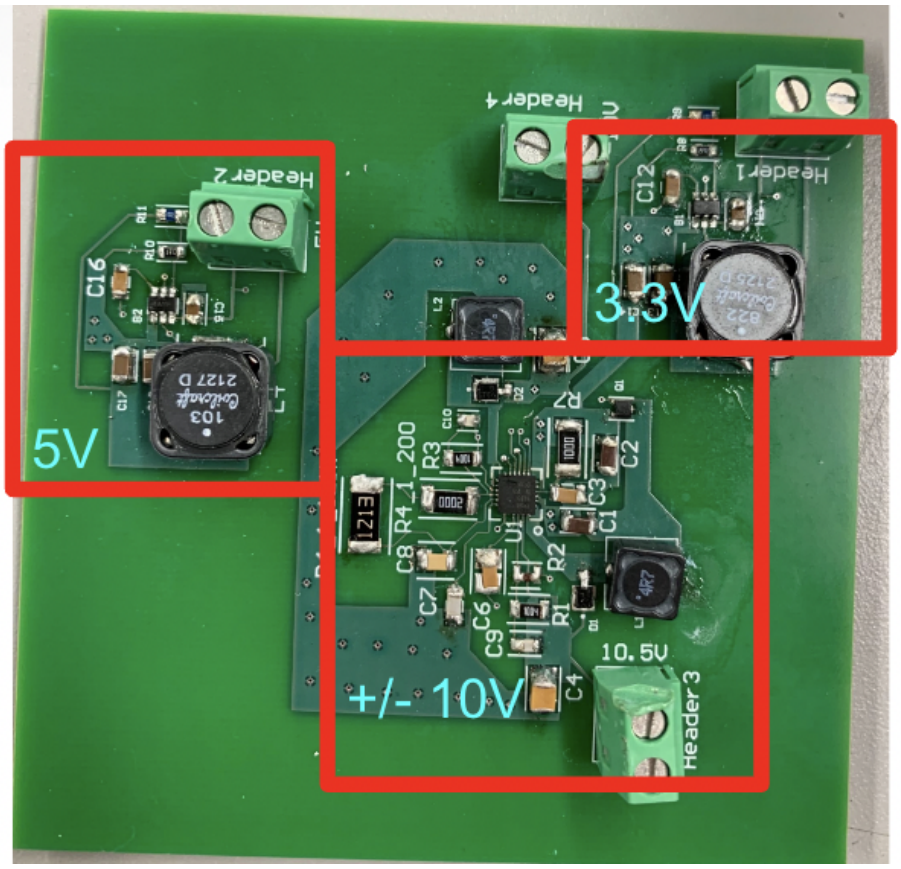
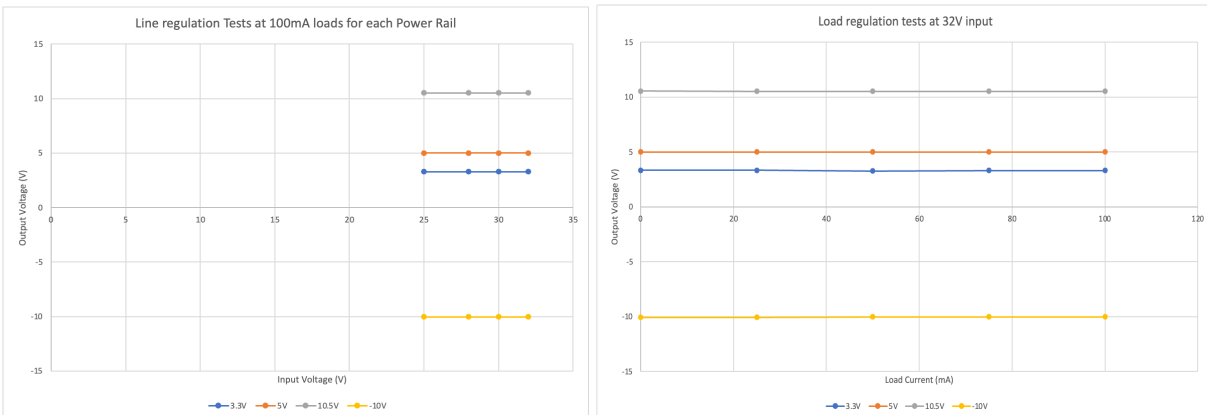


Figure 7: First iteration power PCB

17.3. Subsystem Validation

Validation of the power subsystem was done using an e-load. Line and load tests, power consumption tests, efficiency tests, and waveform readings were conducted.



Figures 8: Line and load regulation results

The total energy consumed by the power sub-system equalled ~1.11Watts. This test was conducted by connecting the multimeter in series with the power supply and then attaching a 0A load to each system individually.

Power Rail Voltage (V)	Power (W)
3.3	0.26
5	0.29
10.5	0.28
-10	0.28

Table 10: Power consumption by power subsystem

These were the efficiency results of the different power rails at different voltages and load currents. Data was based on line and load measurements. The equation used to calculate efficiency was:

$$\text{Efficiency} = \frac{(Vout_load * I_load)}{(Vin_10volt\ module * I_10volt\ module)} * \ 100\%$$

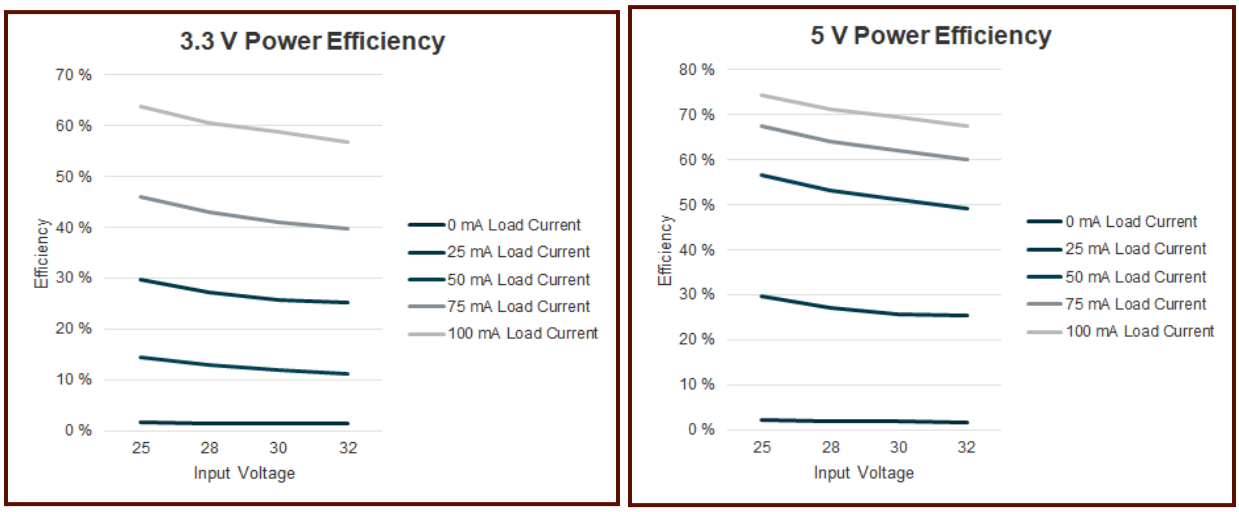


Figure 9: 3.3V and 5V power rail efficiencies

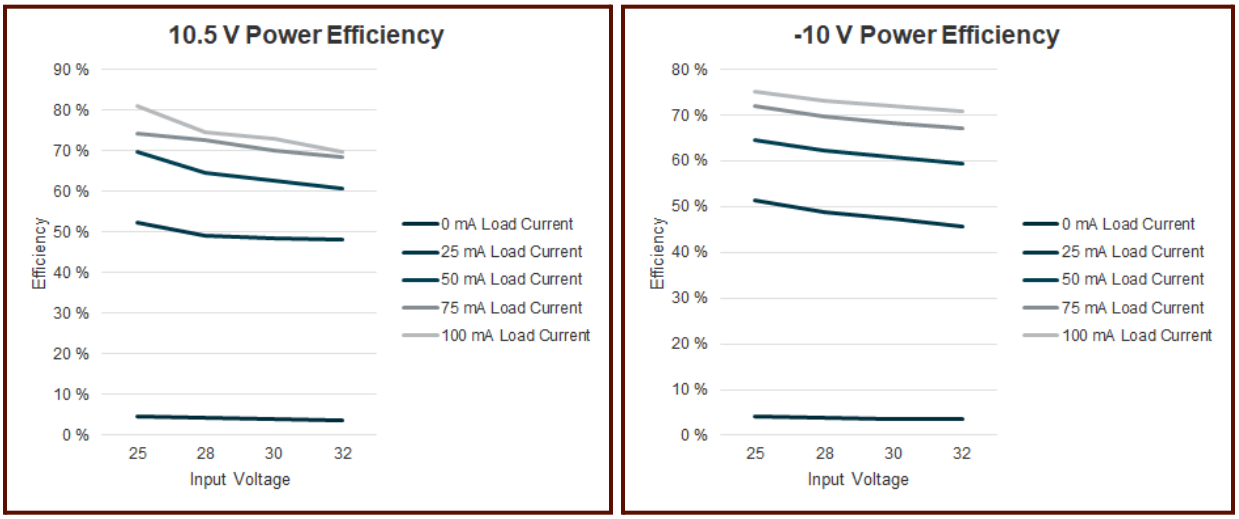


Figure 10: 10.5V and -10V power rail efficiencies

Here are the waveforms of each power rail with 0A load attached:

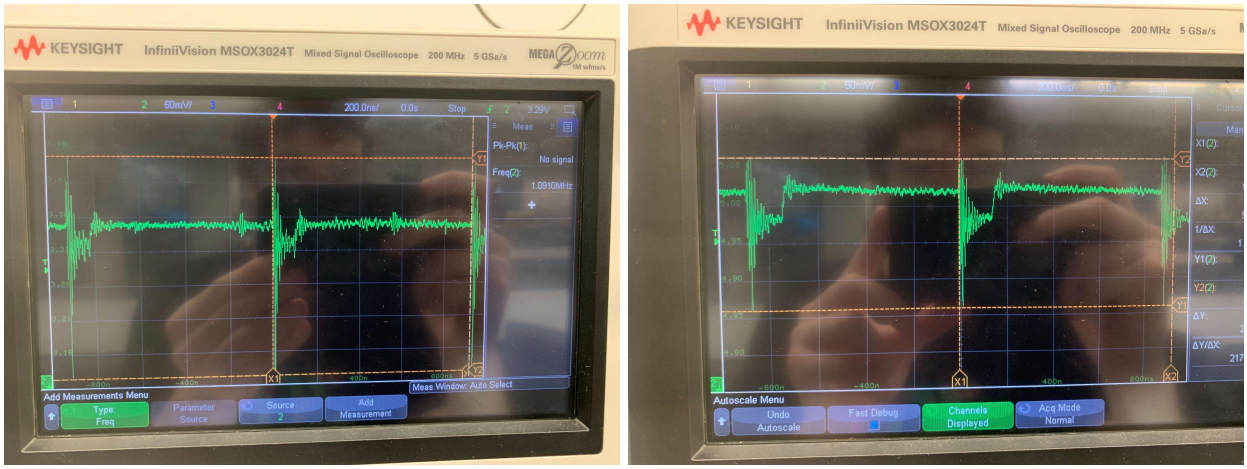


Figure 11: 3.3V and 5V waveforms

Figure 12:10.5V and -10V waveforms

The noise that can be seen in the 10.5V and -10V waveforms was most likely the result of feeding the 3.3V power rail as a source for the boost/inverting IC. All switching frequencies were within expected ranges based on the data sheet. However, the switching frequencies for the 3.3V and 5V rails were above the expected value based on the components chosen. They were supposed to have been about 500kHz but instead switched at about 1.1Mhz. This was an interesting finding given that the other selectable switching frequency that was offered by the data sheet was 1.1MHz.

17.4. Subsystem Conclusion

Overall, the design of the PCB was space-efficient and performed as expected. The line and load regulation tests showed great results. The power consumption by the power subsystem, combined with all the load requirements, remained under the target of 3 Watts total. The efficiency of each power rail was nearly the same as the data sheets indicated. If the other subsystems drew more current, the power rails would have actually performed more efficiently. The majority of noise in the power rails was in the 10.5V and -10V rails. They had seemingly random signals in between the normal ripple voltages. This was most likely due to the 3.3V rail being used as a source for the boost/inverter IC used to create the 10.5V and

-10V rails. One of the biggest challenges while validating the power subsystem was the -10V rail. It would jump to -17V as soon as the load current surpassed 25mA. The solution was an extra 50k ohm resistor in series with the feedback capacitor in the feedback network. Second and third iterations of the project had the power subsystem onboard the same PCB as the other subsystems. It used the exact same design, just with smaller resistors and capacitors. Every other part remained the same.. Overall, the system performed adequately and successfully provided power to the other subsystems.

18. Signal Conditioning Subsystem Report

18.1. Subsystem Introduction

The signal conditioning subsystem is designed to take in 4 different input signals at one time. These signals will be adjusted and filtered in order to meet the acceptable range required by the ADC. The system will be connected to the microcontroller so that it has a software adjustable gain option for the user to select the gain needed for a particular input signal.

18.2. Subsystem Details

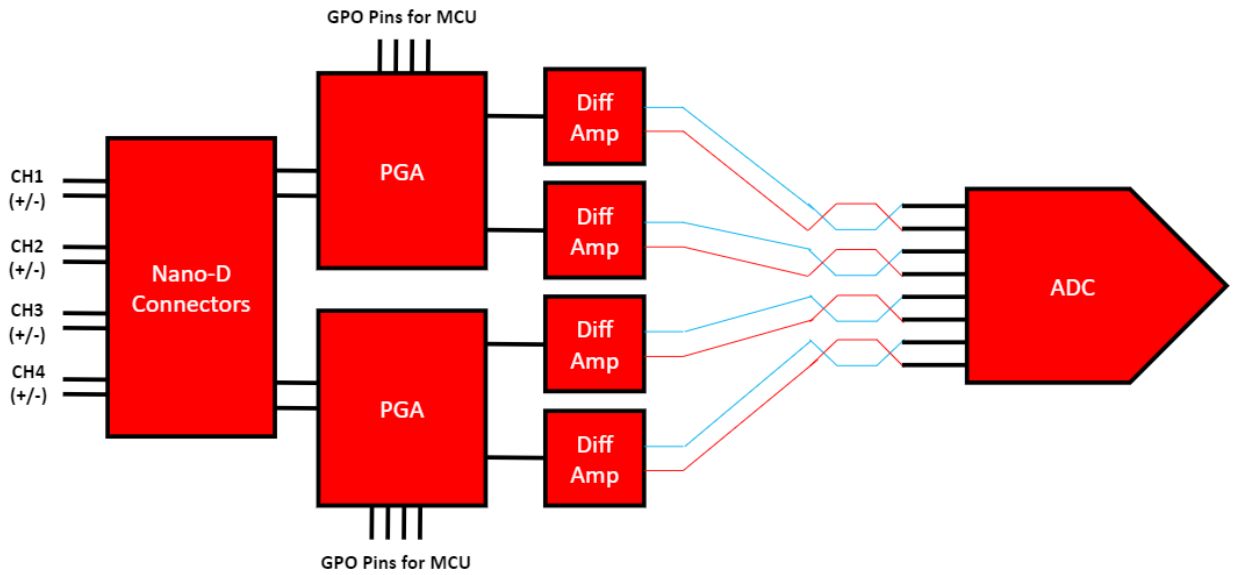


Figure 13: Signal Conditioning Block Diagram

As shown in *Figure 13* above, the DAQ can take in up to 4 input signals at one time at a variety of ranges using Nano-D Connectors. However, the DAQ will be tested using the following sensors: accelerometer, RTD sensor, pressure sensor, and a voltage output sensor. These signals are sent to the PGAs (Programmable Gain Amplifier) in which they will be amplified or attenuated depending on the input signal given. The PGAs will be connected to the processor, which uses GPIO pins in order to select the gain needed for a specific signal. The specified gains that the PGA can provide are shown in *Table 11* below:

G_2	G_1	G_0	PGA GAIN (dB)	PGA GAIN (V/V)
0	0	0	−22	0.08
0	0	1	−16	0.16
0	1	0	−10	0.32
0	1	1	−4	0.63
1	0	0	2	1.26
1	0	1	8	2.52
1	1	0	14	5.01
1	1	1	20	10.0

Table 11: PGA Nominal Gain/Attenuation

The G_2, G_1, and G_0 pins are signals sent from the microcontroller to the PGAs in order to select the required gain for a particular signal. Once the signals have been properly conditioned, they will then be sent to a differential amplifier that will create a positive and negative AC signal that both range from 0 to 4.096 Volts. This is the operational range of a fully differential input to the ADC. Lastly, the completed PCB demo design is shown in *Figure 14* below:

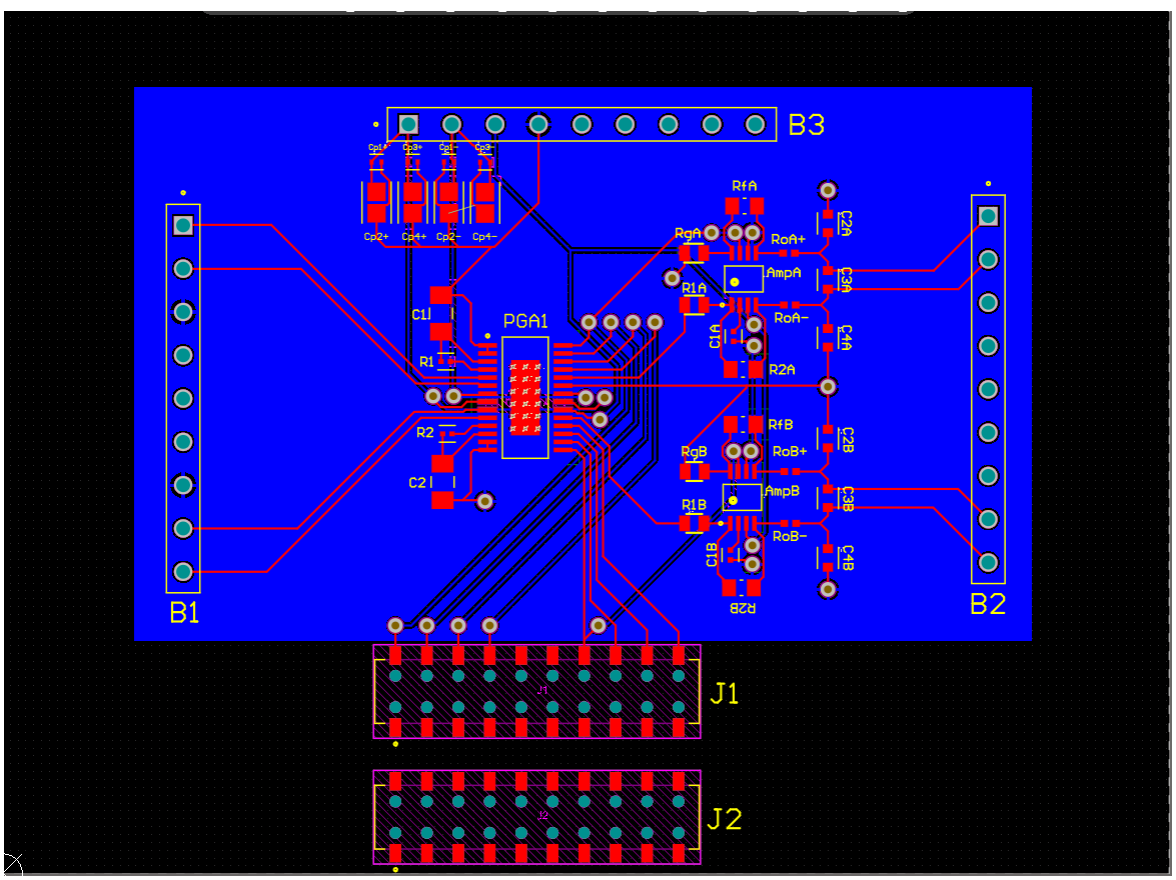


Figure 14: Signal Conditioning PCB Design

This design was then optimized and condensed on an integrated board with the processor on the 1st iteration, with the processor and power conditioning on the 2nd iteration, and then as its own modular board in the 3rd conceptual design. The figures for the first and second iterations are located in *Figure 15* and *Figure 16* below, respectively. The third iteration will be shown in the "System Reports " section of this report.

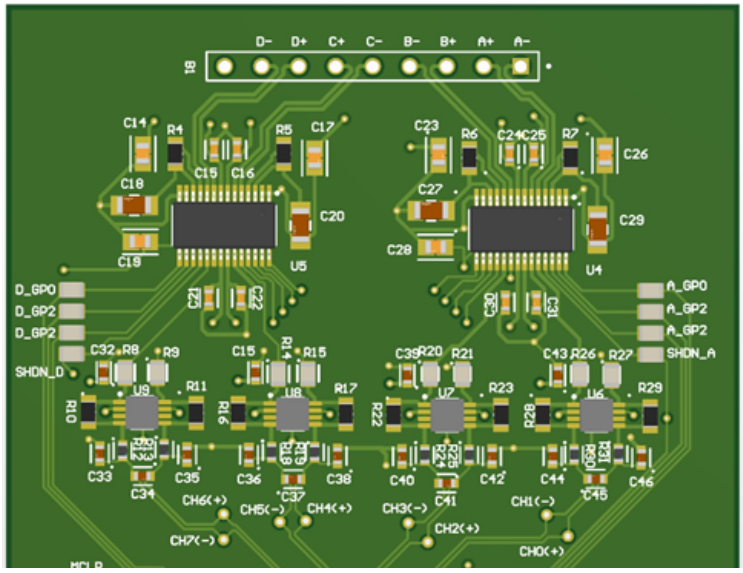


Figure 15: Signal Conditioning PCB - 1st Iteration

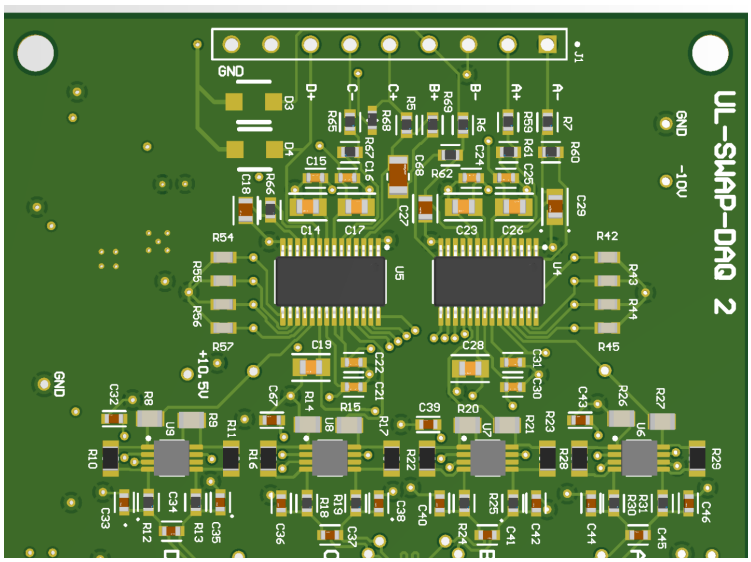


Figure 16: Signal Conditioning PCB Design - 2nd Iteration

18.3. Subsystem Validation

The system was validated by testing different input signals on a test circuit and checking that it produced the proper output differential signal. The table below shows the different input signals that were tested on the circuit:

Test Input Voltage:	Gain Required:	Expected Output:	Passed?
200mV (Switch 1)	10	two 4V to 0V differential signals	Yes
1V (Switch 2)	2	two 4V to 0V differential signals	Yes
2V (Switch 3)	1	two 4V to 0V differential signals	Yes
4V (Switch 4)	0.4	two 4V to 0V differential signals	Yes

Table 12: Signal Conditioning Validation Test Cases

These signals were produced using the AD2 waveform generator and also to measure the output differential signal that was created. The figures below show a screenshot of each test case, with the yellow signal being the input sensor and the blue signal being the positive differential output. The negative differential signal was produced properly, but is not shown in the figures due to only having two sources to measure the signals:

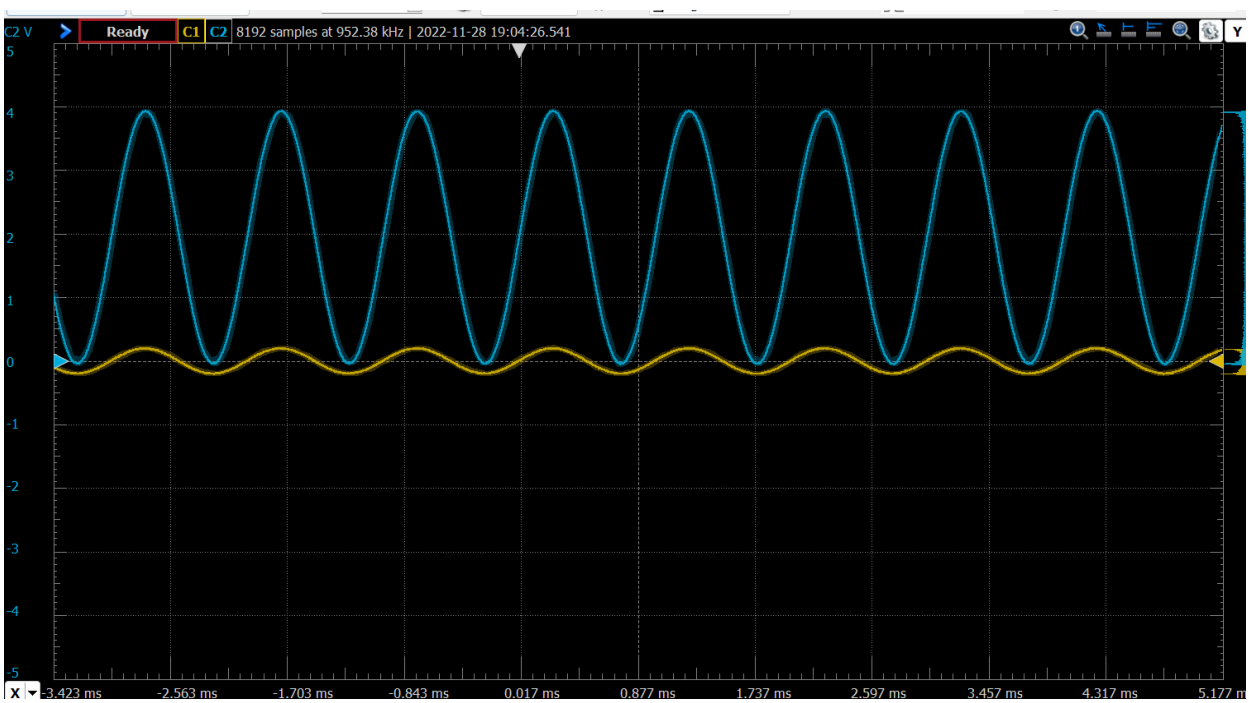


Figure 17: Validation Test - 200mV input

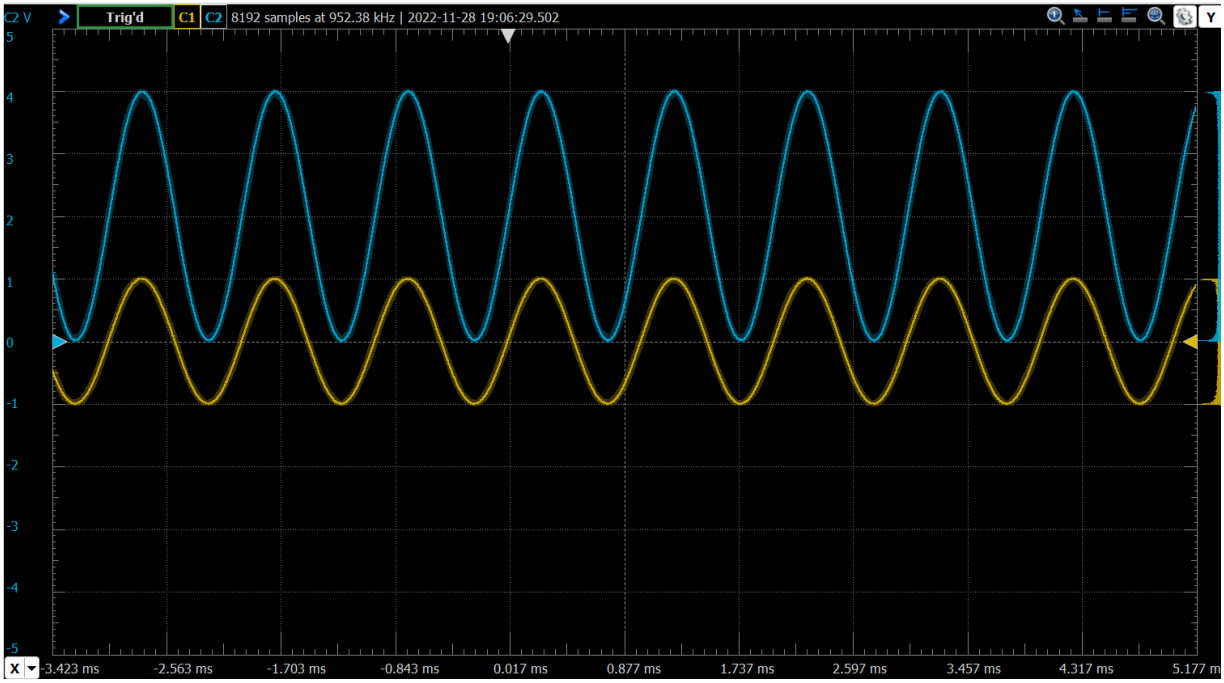


Figure 18: Validation Test - 1V input

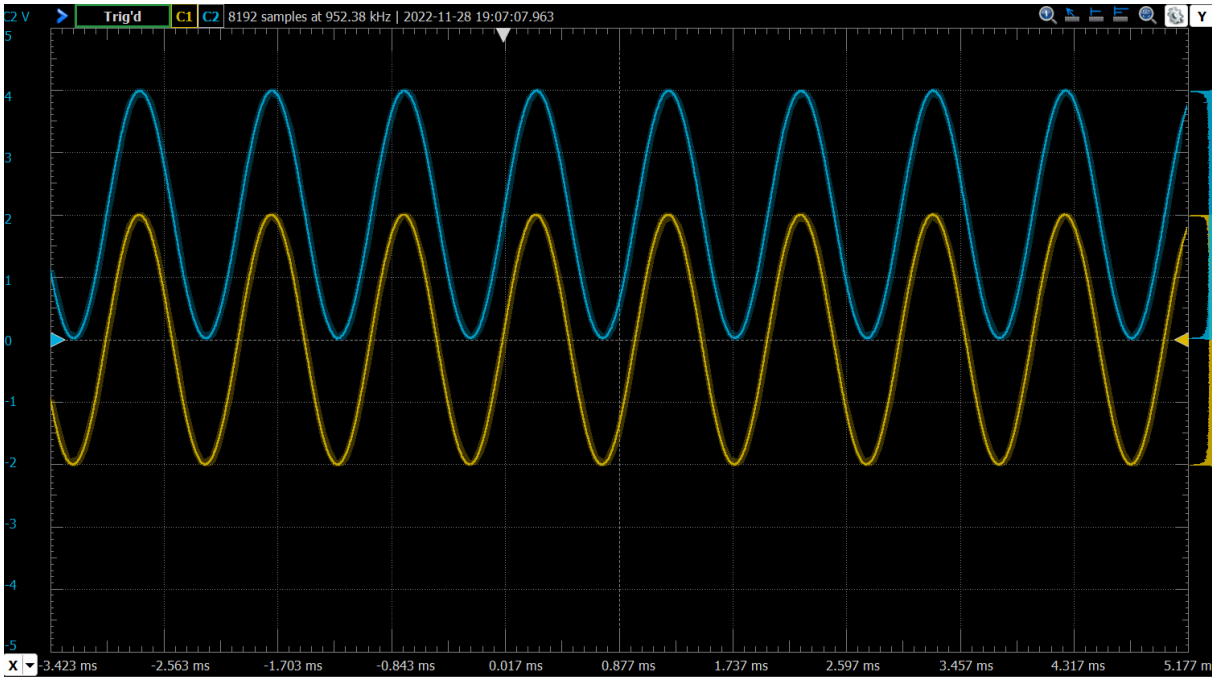


Figure 19: Validation Test - 2V input

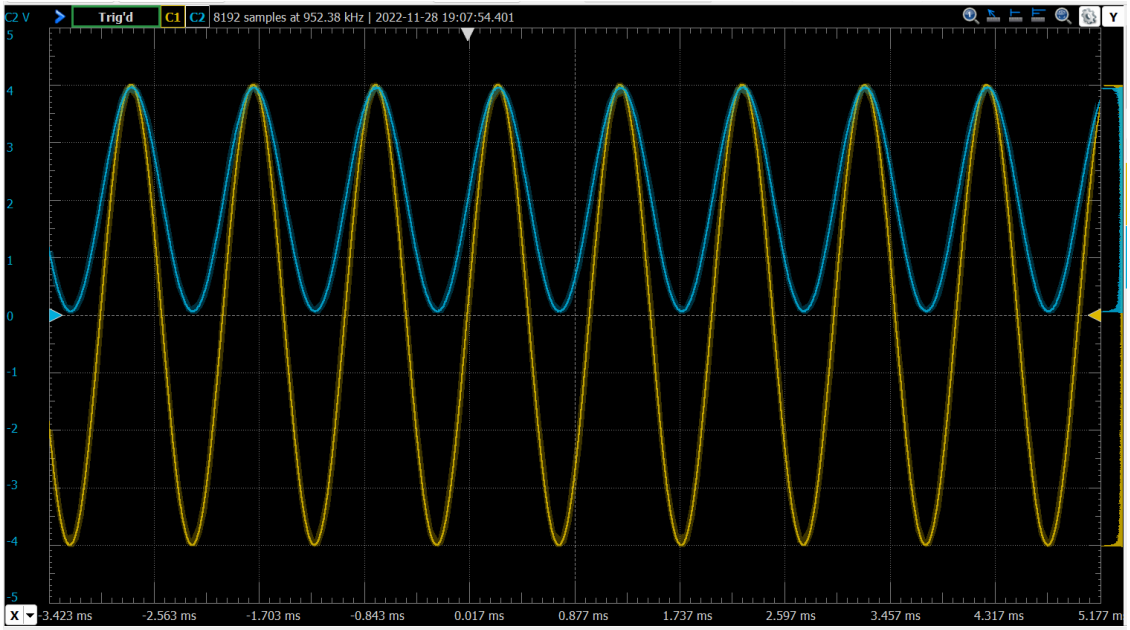


Figure 20: Validation Test - 4V input

This was also validated with the use of the physical sensors required for this project. These sensors included the shock accelerometer, sheer accelerometer, pressure sensor, voltage output sensor, and RTD sensor. The voltage output sensor was tested previously with an input voltage and is therefore not located in the data below. The data and waveforms of each sensor tested at differing gains are shown in the figures and table below:

Input Voltage Sensor	Gain	Expected Output	Actual Output	% Error
Shock Accelerometer	0.08	43.98 mV	48 mV	20%
Shear Accelerometer	0.32	52.15 mV	50 mV	4%
Pressure	1.26	1.47	1.38	6%
RTD	5.01	0.548 V	1.62	19%

Table 13: Sensor Signal Conditioning Data

As you can see, there is a lot of error present in the Shock Accelerometer and RTD sensor. The main reason for this is because the sensors are normally going to be provided with excitation voltage from the rocket, and will therefore create an excitation current for the sensor. However, since that is outside of the scope for this project, it wasn't able to be tested efficiently with the design and materials available.

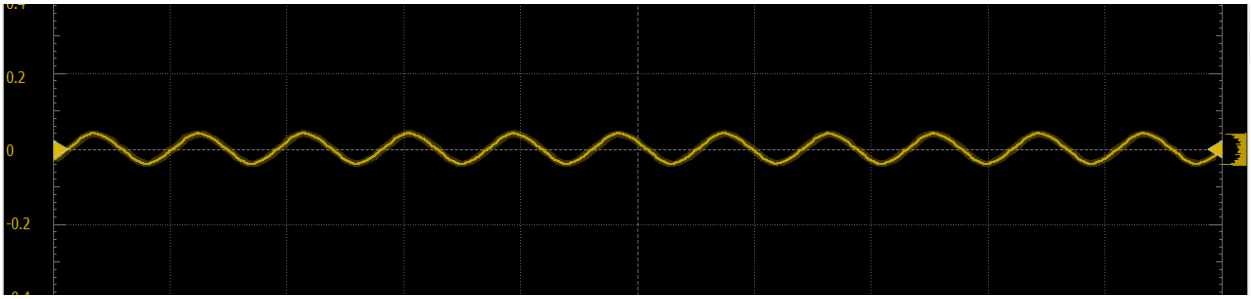


Figure 21: Shock Accelerometer - Gain of 0.08

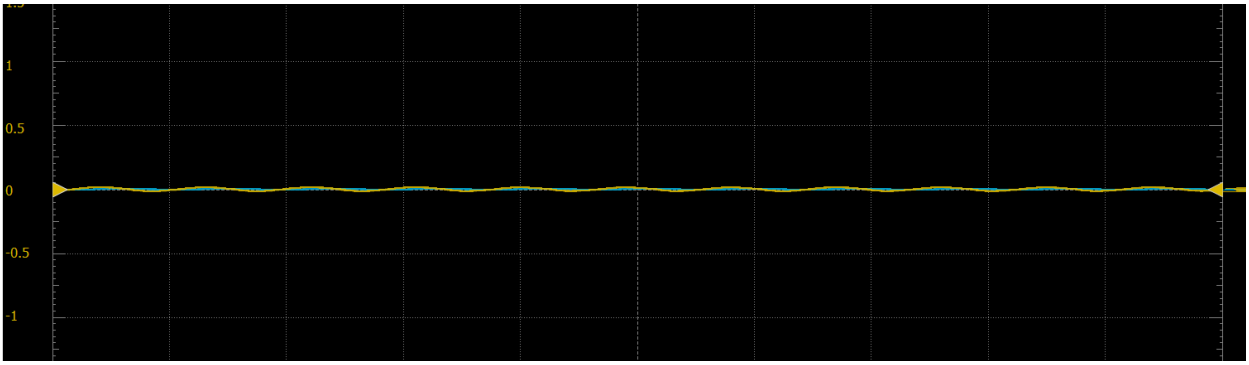


Figure 22: Shear Accelerometer - Gain of 0.32

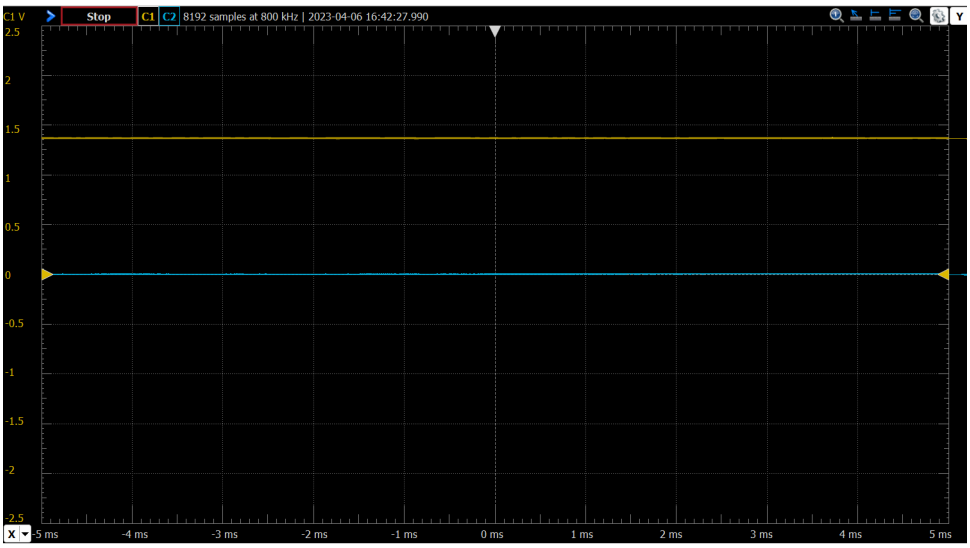


Figure 23: Pressure Sensor - Gain of 1.26

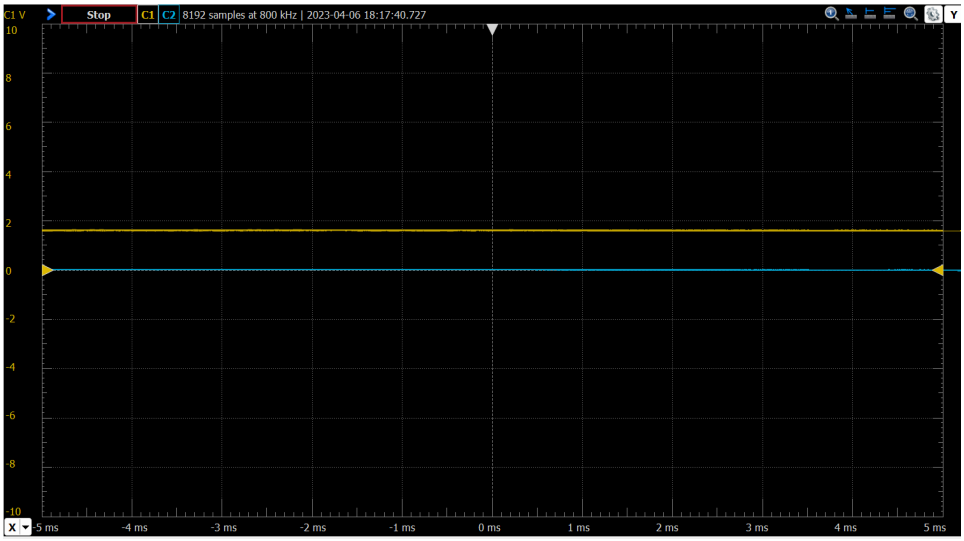


Figure 24: - RTD Sensor (temperature) - Gain of 5.01

18.4. Subsystem Conclusion

Overall, the validation of the subsystem went as expected and supports that the system is ready for integration with the other subsystems. All test cases passed and produced the necessary voltage needed for the ADC's 0V to 4.096V operational range. The actual physical sensors were also able to be tested with the system and produced relatively stable results. There was a large amount of error in some of the physical sensors requiring continuous excitation current; however, it was determined that the power of the sensors was outside of the scope of our project. Therefore, the signal conditioning subsystem worked as expected overall with some error present in the physical sensors.

19. Processor and Interface

19.1. Subsystem Introduction

The Processor and Interface subsystem includes the microcontroller (MCU), analog to digital converter (ADC), programmable gain amplifier (PGA) software configuration, and the Low Voltage Differential Signal (LVDS) driver. The MCU will use Serial Peripheral Interface (SPI) communication protocols with the ADC to obtain the conversion of each input signal. Each SPI message will then be converted to a voltage reading and then output to the LVDS Driver through Universal Asynchronous Receiver Transmitter (UART) communication. The purpose of this subsystem is to sample each channel between 10 kHz and 100 kHz. The method parts described have been validated to do so below.

19.2. Subsystem Details

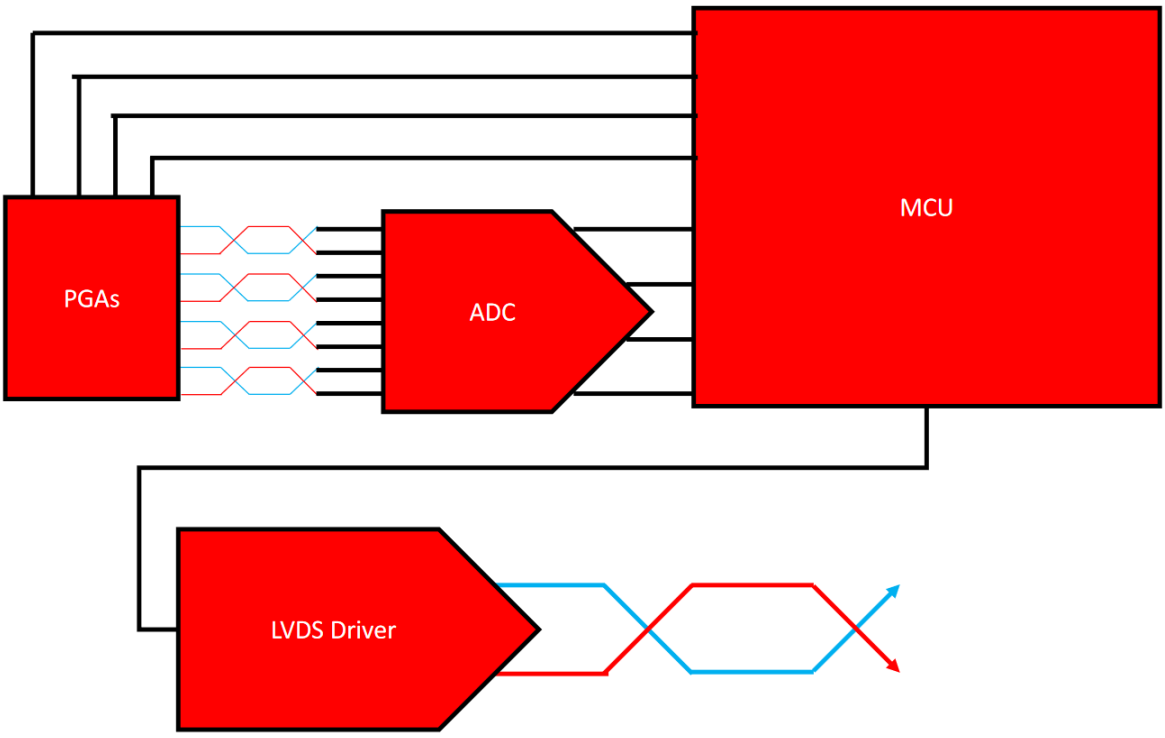


Figure 25: Processor and Interface Block Diagram

Figure 25 indicates a high-level diagram of how the MCU is connected to each of the components. To begin the flow, the MCU will program each of the PGAs with the desired gain determined before the code is compiled. In the code, 2 variables for each PGA have been created: Shutdown and Configuration. If the Shutdown variable is set to high, then the MCU will skip that signal and adjust accordingly. The Configuration variable must be a number between 0 and 7 which is translated to a gain value shown in Table 11. These GPIO pins are static and will not change throughout the

operation. Figure 26 is a snippet of the C Project where the user will configure the PGA GPIOs. They are configured in the function shown in Figure 27.

```
// ****************************************************************************
// ****************************************************************************
// Section: Main Entry Point
// ****************************************************************************
// ****************************************************************************

uint8_t pga1A_shdn = 0;
uint8_t pga1B_shdn = 0;
uint8_t pga2A_shdn = 0;
uint8_t pga2B_shdn = 0;


uint8_t pga1A_config = 0;
uint8_t pga1B_config = 0;
uint8_t pga2A_config = 0;
uint8_t pga2B_config = 0;
```

Figure 26: C snippet of PGA configuration Variables

```
void configurePGA1A(uint8_t config, uint8_t shdn){
    if(shdn){
        PGA1G0A_Clear();
        PGA1G1A_Clear();
        PGA1G2A_Clear();
        PGA1SHDNA_Set();
        return;
    }
    if(config & 0x01){
        PGA1G0A_Set();
    }
    else{
        PGA1G0A_Clear();
    }
    if(config & 0x02){
        PGA1G1A_Set();
    }
    else{
        PGA1G1A_Clear();
    }

    if(config & 0x04){
        PGA1G2A_Set();
    }
    else{
        PGA1G2A_Clear();
    }
    return;
}
```

Figure 27: PGA Configure Function

Then, the MCU will reset and program a sequencer built inside of the ADC. To reset the ADC, first the Reset pin on the ADC will be set to high and then set to low. Then, when the MCU sets the CNV pin on the ADC to high and then low, the ADC will begin a conversion and set its BUSY pin to High. When the BUSY pin is set to low, the MCU will set the RDL pin to Low and read the SPI message.

The message sent from the ADC is a 24-bit word containing 16-bits of the Data Conversion, a separating bit, and the 7-bit configuration word. As the SPI message is being read by the MCU, the next conversion's configuration word is being written into the sequencer memory. On the next cycle, this conversion will be read. Figure 28 is a code snippet to execute the task of resetting the ADC and programming the Sequencer:

```
119    /**
120     * \section Reset the ADC
121     * @return
122     */
123    RESET_Set();
124    for(int i = 0; i < 100; i++);
125    RESET_Clear();
126    RDL_Set();
```

Figure 28: C code snippet of Resetting the ADC

After the MCU Resets the ADC, a Finite State Machine (FSM) is used to begin the next operation. Figure 31 is a diagram of the FSM. To summarize the diagram, the MCU begins in the START state and uses a GPIO pin to initiate a conversion in the ADC. Then, the MCU will wait for the conversion to complete before delivering the next conversion and sampling the conversion on the SPI bus. Each sample is then stored onto a ring buffer which can fit 4 readings, one for each channel, and then write the buffer to UART as voltages separated by commas. This will easily translate the data into a CSV output stream to rocket telemetry.

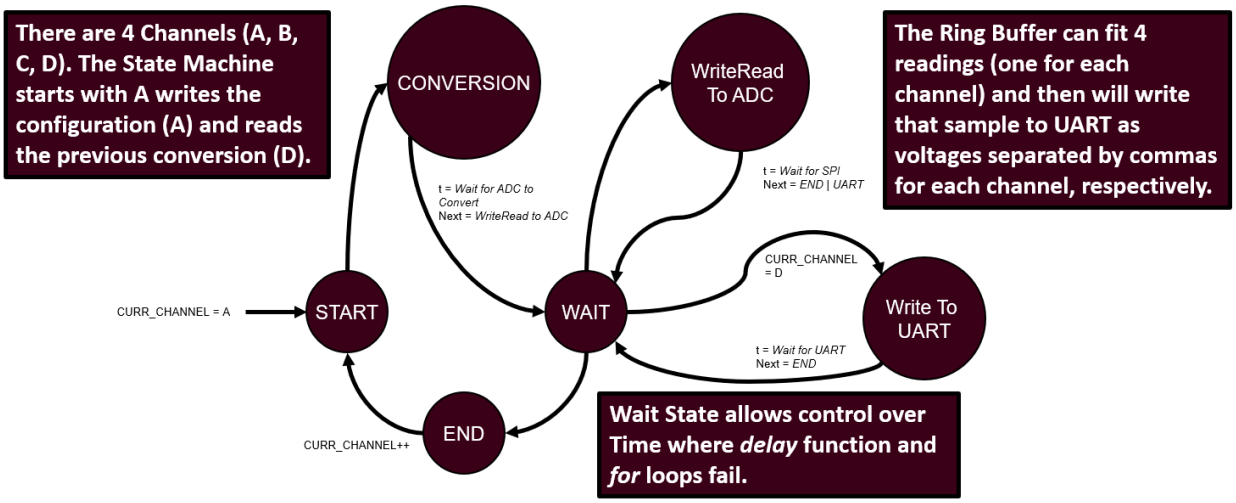


Figure 29: Finite State Machine

Please find Appendix E of the System Report for the final github repository and Doxygen-Generated Documentation.

Figure 30 and 31 are the PCB designs for this subsystem which includes the LTC2373 as the team's ADC, a PIC32MX470 as the team's MCU, an ADN4661BRZ as the team's LVDS Driver, and an interface port for the ICD4.

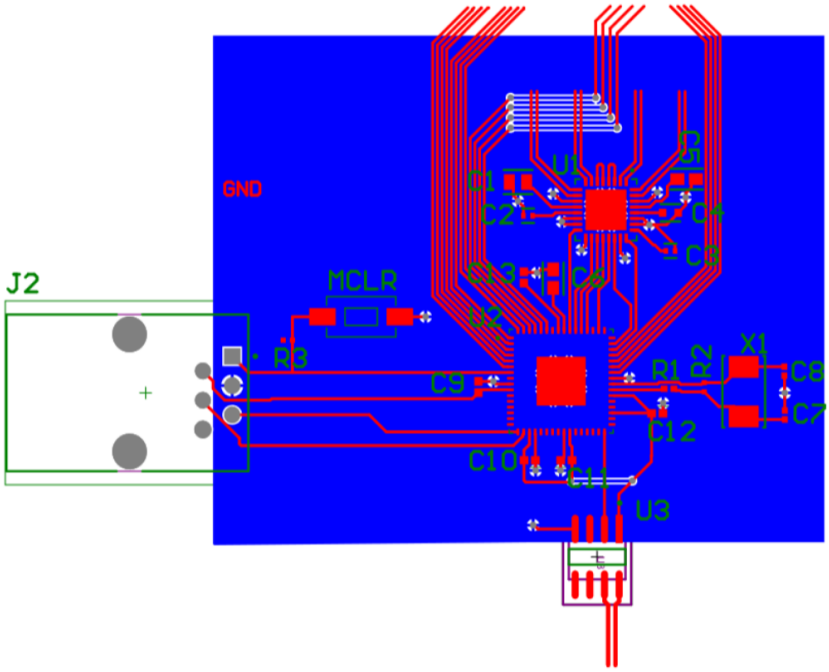


Figure 30: Colored View of Processor and Interface Subsystem

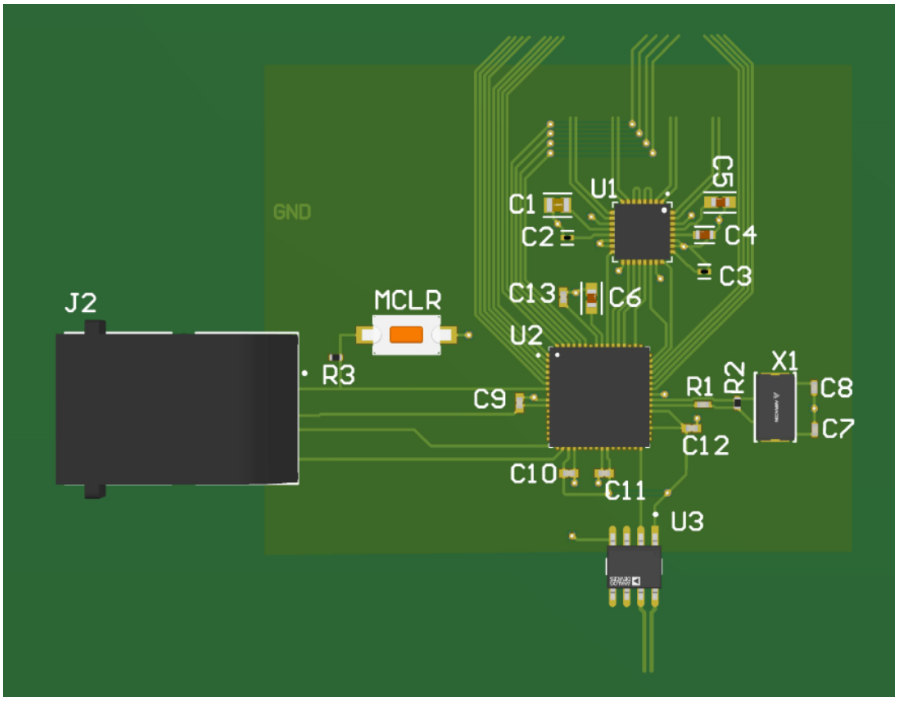


Figure 31: Top level view of Processor and interface Subsystem

19.3. Subsystem Validation

To validate the subsystem, the PIC32MX470 Curiosity Development Board was obtained to act as the MCU. A breakout board for the LTC2373-16 was designed and manufactured to act as the ADC. It has been determined that the PIC32MX470 and LTC2373 will be used in the final development of our design. While beginning the debugging process, the MCU successfully configured the ADC with a control word and a 24-bit data conversion was obtained from the ADC.

Figures 32 and 33 are captures made by the ADC on the second iteration of the design. Unfortunately, due to the testing environment of the subsystem, these captures are extremely noisy and outside the requirement of the data error. The problem was fixed by removing a capacitor and utilizing the oscilloscopes UART Receiver, but a new data capture measurement without the signal conditioners was unable to be retrieved due to a Power Subsystem failure which shorted the MCU and ADC and time constraints.

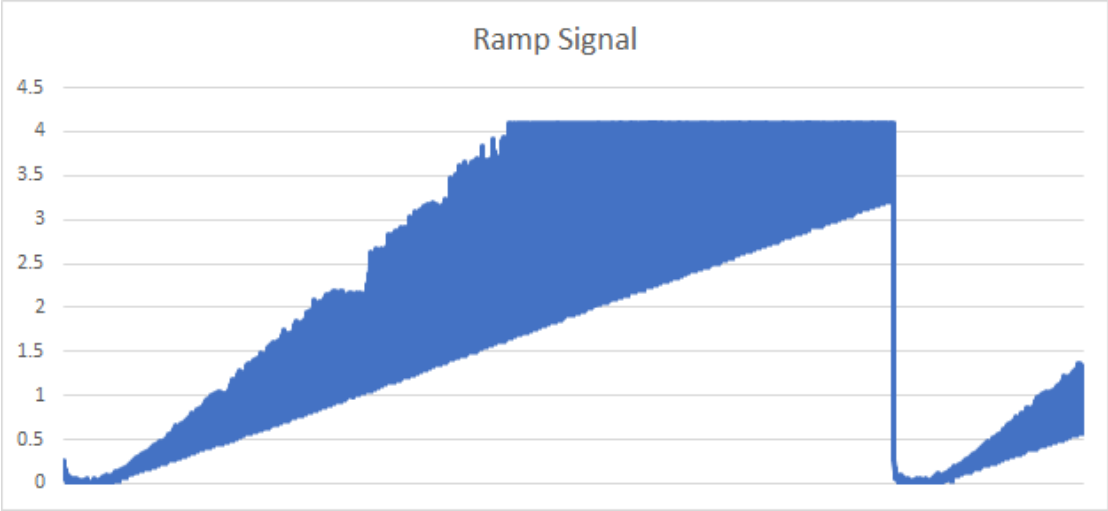


Figure 32: Noisy Ramp Signal Capture

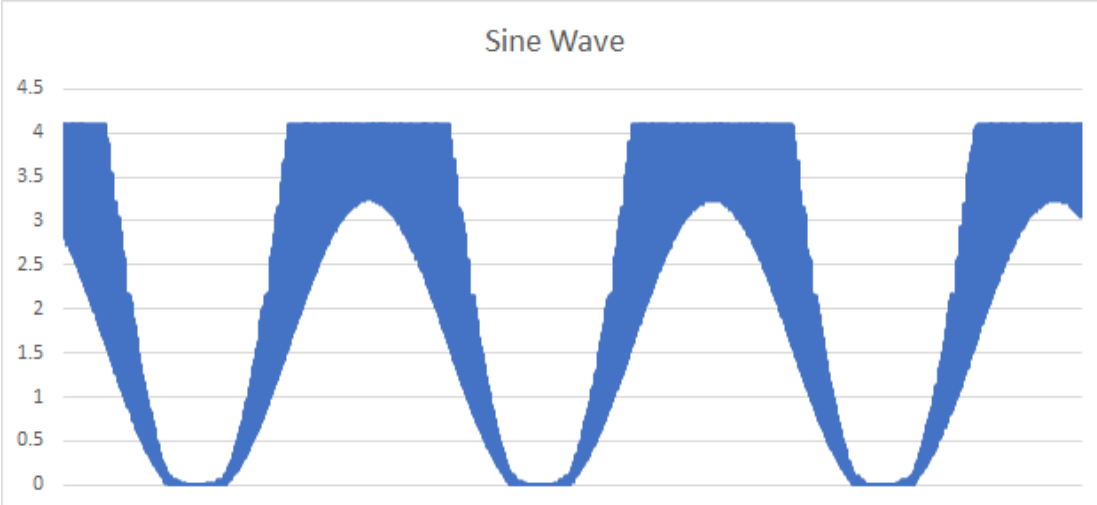


Figure 33: Noisy Sine Signal Capture

19.4. Subsystem Conclusion

The subsystem was partially functional with the ADC breakout board and development board during the fall semester. However, due to price and time constraints, the team moved on to a fully integrated design. After the first iteration was completed, the new Finite State Machine code was developed to control the computations executed in the Microcontroller. The result was a fully functional subsystem with a sampling rate of 160 kHz and data error of approximately 1%. A table of these values are shown in the System Report. None of the parts were changed from the first iteration to the second iteration nor the second iteration to the third iteration as validation results remained the same. It is expected that a higher sampling rate can be achieved with the proper instrumentation for reading a UART message. The baud rate is currently at 500 kHz with a data error of 0.001%. By increasing the UART baud rate and SPI clock rate (2 MHz), one can achieve a much higher sampling rate.

Appendix A: Acronyms and Abbreviations

Below are the defined acronyms and abbreviations used throughout this document:

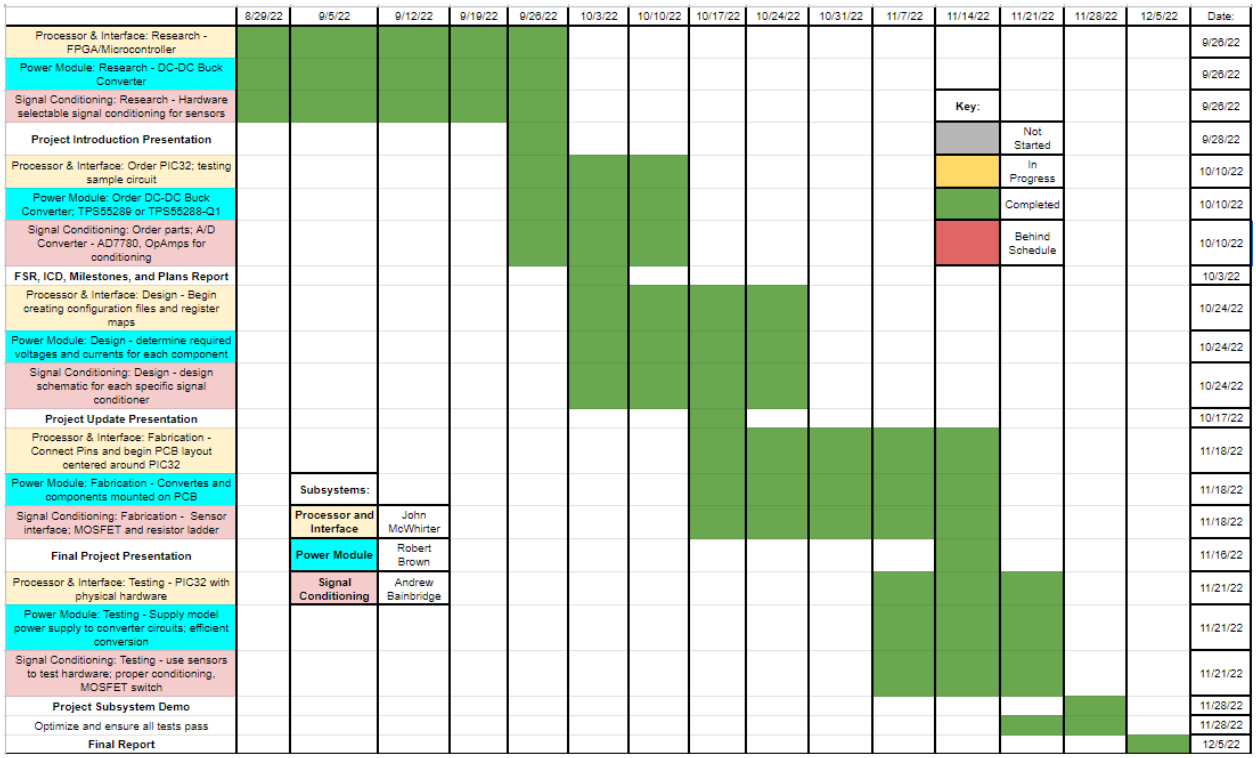
BIT	Built-In Test
DaQ	Data Acquisitions Unit
ETC	Etcetera
GUI	Graphical User Interface
Hz	Hertz
ICD	Interface Control Document
kHz	Kilohertz (1,000 Hz)
kOhm	Kiloohm (1,000 Ω)
LVDS	Low Voltage Differential Signaling
mA	Milliamp
MHz	Megahertz (1,000,000 Hz)
mW	Milliwatt
RTD	Resistance Temperature Detector
UL-SWaP	Ultra Low - Size, Weight, and Power
USB	Universal Serial Bus
ICD4	In-Circuit Debugger 4
ADC	Analog-To-Digital Converter
GPIO	General Purpose Input and Output
PGA	Programmable Gain Amplifier
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
IDE	Integrated Development Environment
MCU	Microcontroller
FSM	Finite State Machine

Appendix B: Definition of Terms

Below are the definitions of certain terms used throughout this document:

Term:	Definition:
Op-Amp	Is an operational amplifier used for amplification, attenuation, or filtering of a signal.
LVDS Protocol	Is a physical protocol defined by a differential signal pair, with bits being defined by either positive or negative 3.5 mA current source passing through a 100 Ohm terminating resistor causing a 350 mV differential signal.
Analog to Digital Converter	A system that converts an analog input signal into a digital output signal
Microcontroller	A small computer designed to control a single operation within an embedded system
CNV	Conversion Pin on LTC2373-16
MPLAB X IDE	A software program provided by Microchip with tools to easily configure their microcontrollers. See https://www.microchip.com/en-us/tools-resources/develop/mplab-x-ide
UL SWaP DaQ Github Repository	Repository for Altium files, C Project, and Doxygen Documentation https://github.com/JohnMcWhirter10/ULSWAP-DAQ
Finite State Machine	A mathematical model used to abstractly define operations. It is most commonly used in devices with smaller computations.

Appendix C: Execution Plan



Appendix D: Validation Plan

Paragraph #:	Test Name:	Success Criteria:	Methodology:	Status:	Responsible Engineers:
8.2.1.1.	Maximum Power Draw	System draws 3mA of less of total power.		UNTESTED	Robert Brown
8.2.1.2.	Variable Signal Conditioning	Proper conditioning is applied based on the signal input given.	Test signal is inputed and tested for same output regardless of hardware input chosen.	TESTED	Andrew Bainbridge
8.2.1.3.	LVDS Data Transmission Protocol	Data from sensors is properly transfered digitally to user.	Test signal is inputed and compared between direct connection and user interface	UNTESTED	John McWhirter
8.2.1.4.	Hardware/Software Selectable Output Voltage	That each signal conditioner performs the correct conditioning.	Each sensor is connected and tested with input signal to see if output voltage matches	TESTED	Andrew Bainbridge
8.2.2.1.	Mass	The total weight of all subsytems is <= 200 grams	Measure each sub system with a digital scale	UNTESTED	Andrew Bainbridge, John McWhirter, Robert Brown
8.2.2.2.	Volume Envelope	The toal volume of the device will be less than 27 inches cubed (3inx3inx3in).	Each subsytem's dimensions and volumes will be calculated and added in order to stay under a total volume of 27 inches cubed.	UNTESTED	Andrew Bainbridge, John McWhirter, Robert Brown
8.2.3.1.1.	Input Voltage Level (Signal conditioners)	ADC coverters: 2.5-5.25V; Op-Amps: 10-30V; Accelerometer: 7-12V; Pressure: 100mV; RTD: 1-100mV	Each path of power module input connection and sensor output will be tested for correct voltage and current values.	UNTESTED	Robert Brown
8.2.3.1.1.	Input Voltage Level (Processor)	PIC32 will require a 3.3V input from the power source.	The output from the power supply will be measured with a voltmeter to ensure it is as close to 3.3V as possible.	UNTESTED	Andrew Bainbridge, Robert Brown
8.2.3.4.1.	Data Output	The output data matches the expected output from a specific input signal	The output will be compared with the expected output that should be received by a specific test signal.	PARTIAL	John McWhirter
8.2.3.4.2.	Diagnostic Output	The tested signal generators and oscilloscopes are able to supply the signal conditioners with test signals for the processor to see as well.	Signal generator and oscilloscope will be provided and the expected data to receive from the test input will be compared to the actual output on the interface.	TESTED	John McWhirter
N/A	Signal Conditioning Demo	The subsystem takes in signals and turns them into usable digital signals for the processor to utilize.	Sensors will be used to test different inputs and will be checked that the proper signal conditioning was applied.	TESTED	Andrew Bainbridge
N/A	Processor and Interface Demo	The processor takes in the digital signal and displays the daya on an interface availiable to the user.	Test digital inputs will be given to the processor and the output will be compared to the expected output on the interface.	PARTIAL	John McWhirter
N/A	Power Module Demo	The subsystem supplies the proper amount of power to each component of the system.	Each output from the power module will be measured to ensure it has the expected voltage and/or current at each node.	TESTED	Robert Brown

UL-SWaP DaQ for Rocket Testing

Andrew Bainbridge
John McWhirter
Robert Brown

System Reports

REVISION – 0.1
27 April 2023

System Reports
for
UL-SWaP DaQ

Prepared by:

_____
Author Date

Approved by:

_____
Project Leader Date

_____
John Lusher II, P.E. Date

_____
T/A Date

Change Record

Rev.	Date	Originator	Approvals	Description
0.0	4/27/2023	John McWhirter		Final Report Release

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20. Introduction

The following documentation describes the full system of the Ultra Low Size, Weight, and Power Data Acquisitions unit. Each subsystem is completely integrated and validated to the specifications requested. In addition, our design's impact on the industry is a more productive use of time and resources and has the potential to decrease the overall number of rocket flights.

21. Details

Our project's methodology is founded on rapid prototyping. There are two productions of our design and a third conceptual design. Each design contains its own technical merits, but meets the specifications of the Function System Requirements document.

21.1. The First Iteration

The first iteration of the design was primarily focused on creating a concept build design that had multiple test points for testing each subsystem after being integrated onto the same board. The only subsystem that wasn't completely integrated on the first iteration was the power conditioning. The design was split into two different boards: one with the signal conditioning and processor unit interfaced and one with the power conditioning. This allowed for each system to be tested simultaneously without the need of the power board in order to test the rest of the system. Allowing for more time efficient testing of the system in a safer fashion. Figures of the signal conditioning/processor board and the power board are located below in *Figure 34* and *Figure 35.* A physical picture of the boards are located in *Figure 36* as well.

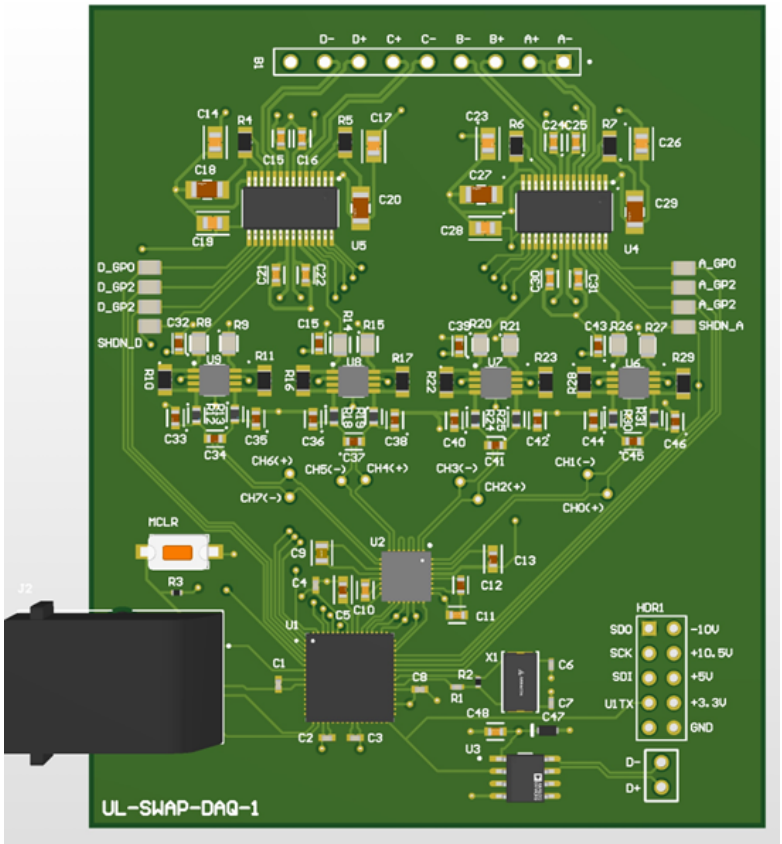


Figure 34: UL-SWaP-DaQ First Iteration Design

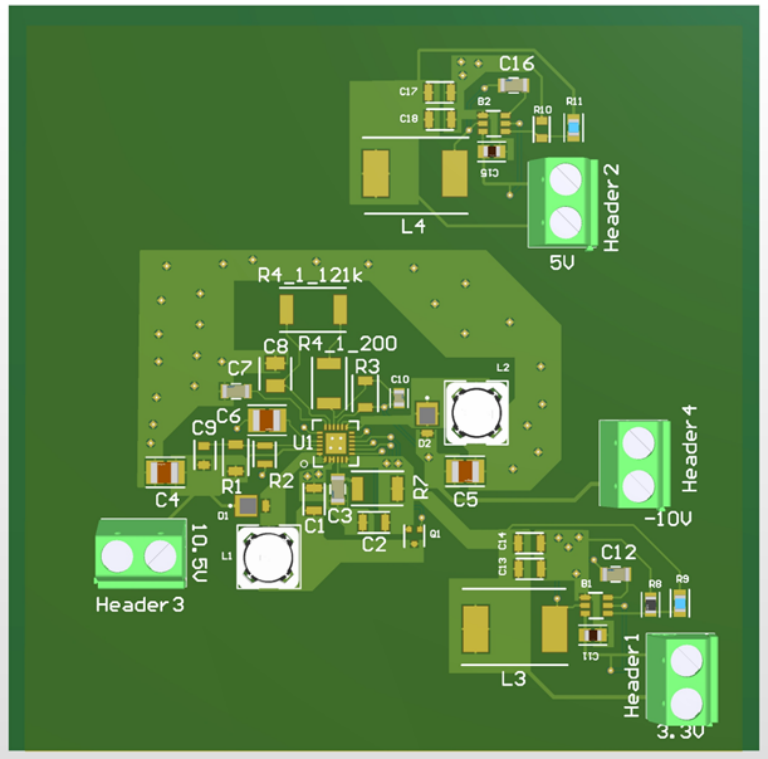


Figure 35: Power PCB Design

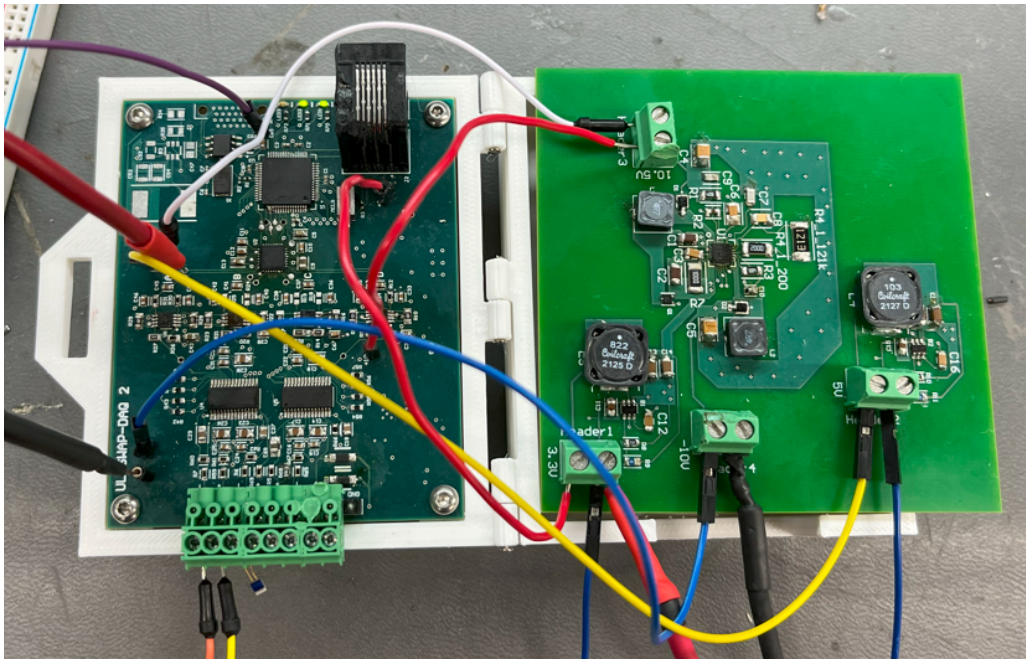


Figure 36: 1st Integrated Full System Design

21.2 The Second Iteration

The second iteration of our design focused on compiling each of the subsystem's components onto a single board. It was desired that the board be within a 3" x 3" surface area and so our team developed this solution. Initially, the voltage rails were not working properly due to a placement of parts in those regions. We believed there to be a short, despite this, the Power PCB from the initial design contains the same part values and connections as this iteration. Thus, the Power PCB can be used to power this design if necessary. Many of the problems with our design were found in the testing procedures we conducted. By manipulating how we were validating the design, we successfully adjusted the input signal to be read by the ADC. Unfortunately, the ADC was faulty and could only read a single-ended input in Channel A, but the functionality of the ADC to switch between channels was validated in the 1st iteration. *Figure 37* shows a top view of the PCB design, *Figure 38* shows a bottom view of the design, and *Figure 38* shows the physically integrated design.

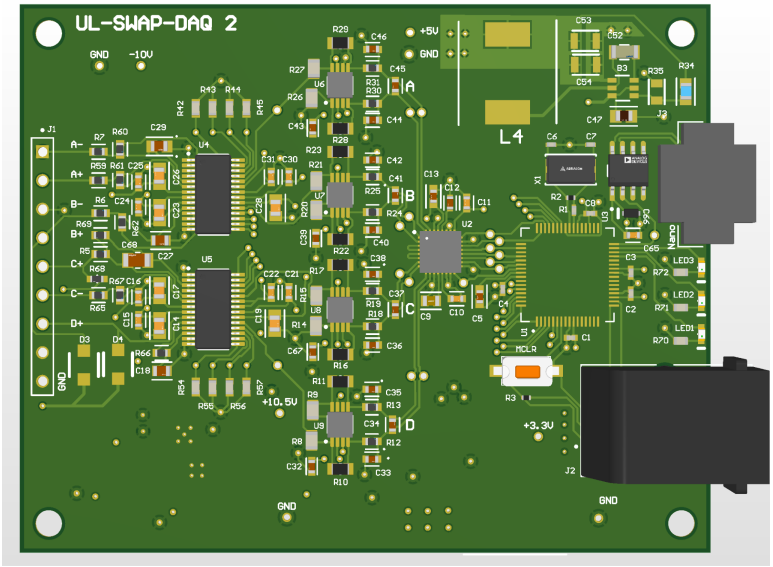


Figure 37: 2nd UL-SWaP-DaQ PCB Design Front

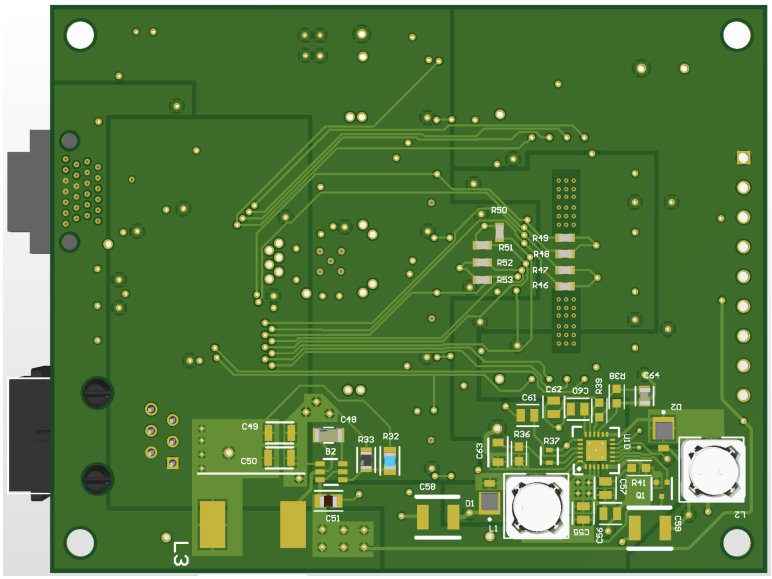


Figure 38: 2nd UL-SWaP-DaQ PCB Design Back

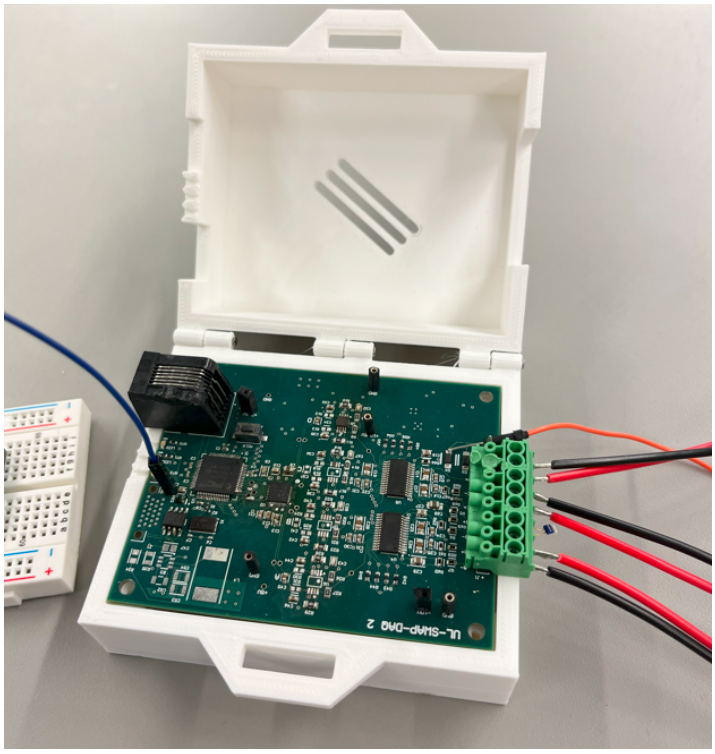


Figure 39: 2nd Integrated Full System Design

21.3 The Third Iteration

The third iteration of our design was mainly focused on compacting the design of the unit as much as possible and creating a modular design that is scalable for the user. These goals were accomplished by switching most of our components to 0402 size components on the board and creating a main board with a modular board for sensors and signal conditioning. The main board is located in *Figure 40* and *Figure 41* and the modular board is located in *Figure 42* and *Figure 43* below:

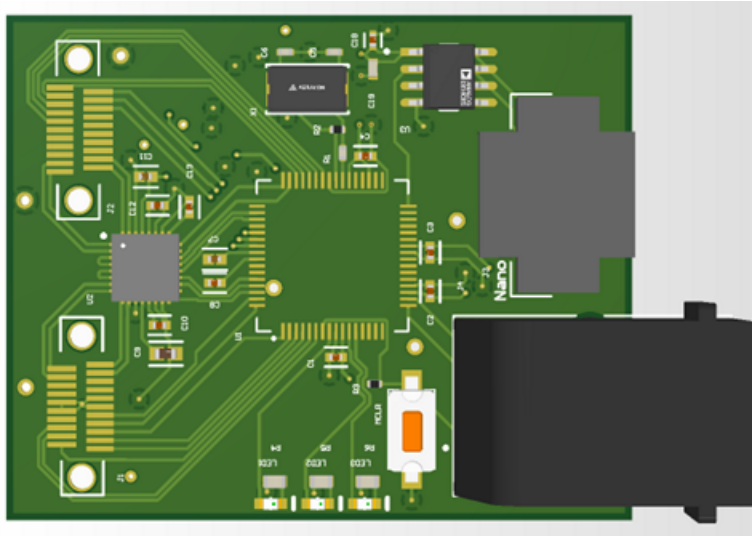


Figure 40: 3rd UL-SWaP-DaQ PCB Design Main Front

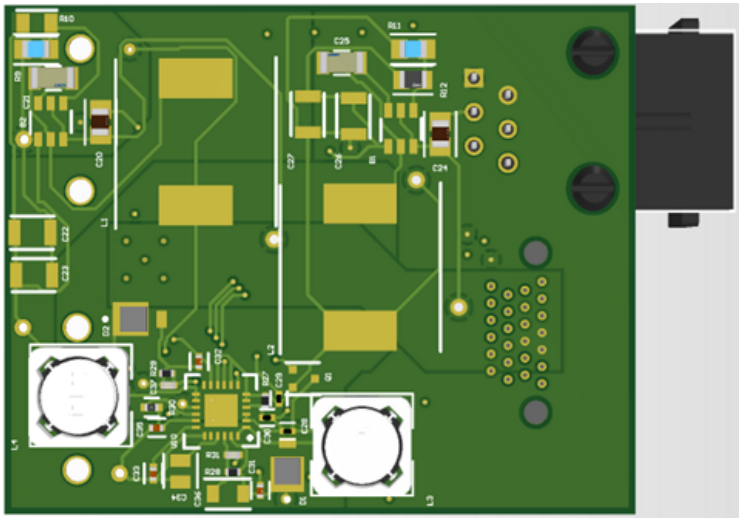


Figure 41: 3rd UL-SWaP-DaQ PCB Design Main Back

The main board contains all of the power conditioning and processing components and accomplishes the same requirements of the first two iterations. However, the board contains two Nano-D connectors that allow for the modular board to connect to the board depending on the number of sensors the user requires for testing, ranging from 0 to 4 sensors. This modular design is shown below:

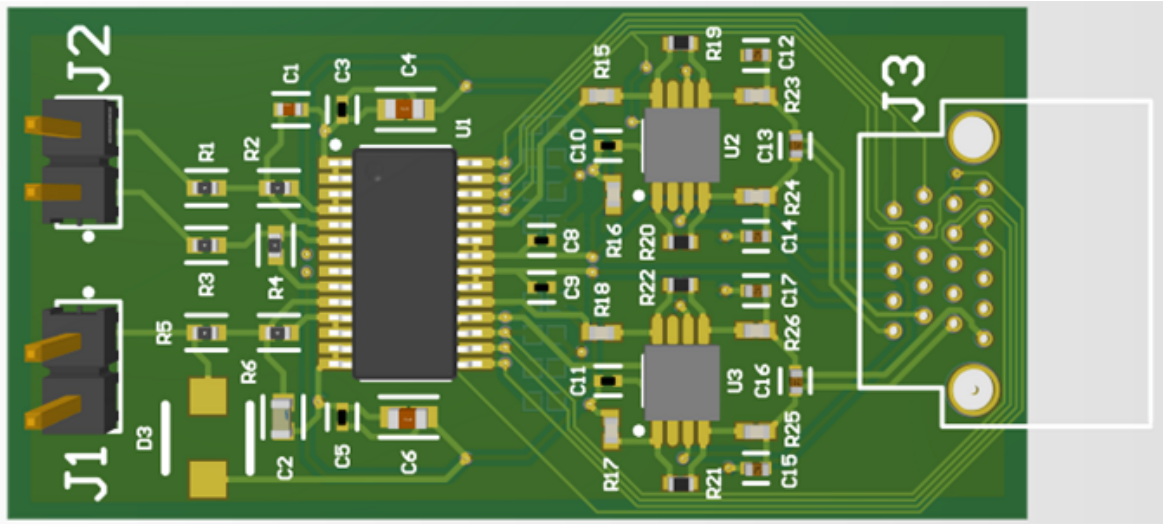


Figure 42: 3rd UL-SWaP-DaQ PCB Design Module Front

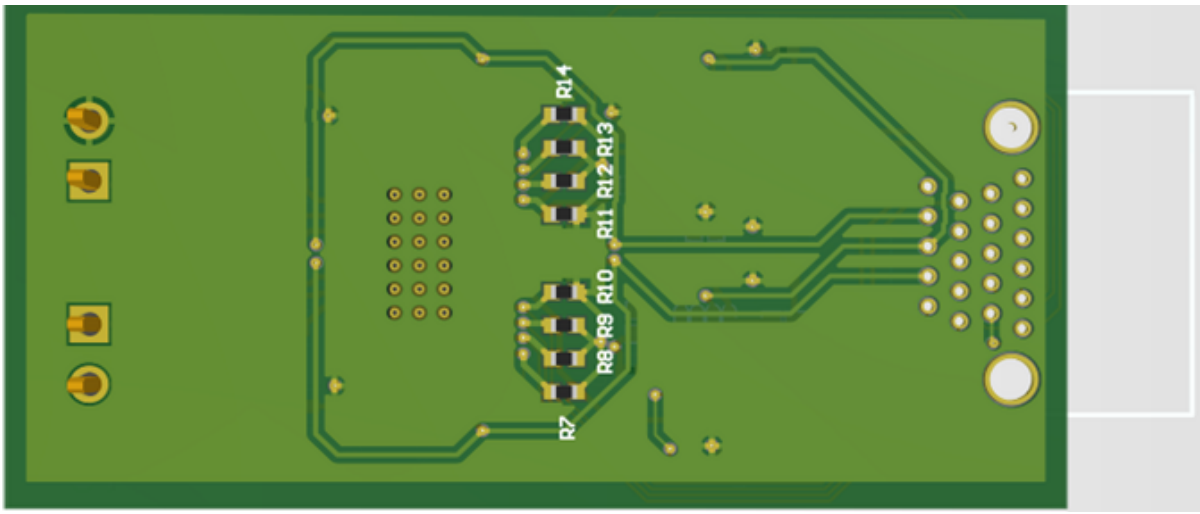


Figure 43: 3rd UL-SWaP-DaQ PCB Design Module Back

The modular design allows for an overall more compact design; however, it also allows for easier scalability of the design. For example, if an experimentalist wanted to use a very specific sensor that required a specific signal conditioning circuit, they would only have to change the modular design of the unit instead of changing the whole board. This allows the unit to still be operational even in the middle of the design process.

22. Validation

Item	Theory	Target	Stretch	Measured
Sampling Frequency	1 Msps	10 kHz	100 kHz	154-170 kHz
Data Output Error	+-3%	3%	1%	~1.0254%

Table 14: Processor & Interface Validation

Table 14 contains the measured Sampling Frequency of the Functioning system. As noted, the target goal was a minimum of 10 kHz. Our team first found that the system was operating at 6 kHz per channel. With relatively few adjustments to the UART output baud rate and SPI clock rate, we were able to maintain a data output error of 1 % and sample at 160 kHz maximum. It is recommended that the system be operated under 80 kHz sampling frequency if negligible data output error is desired.

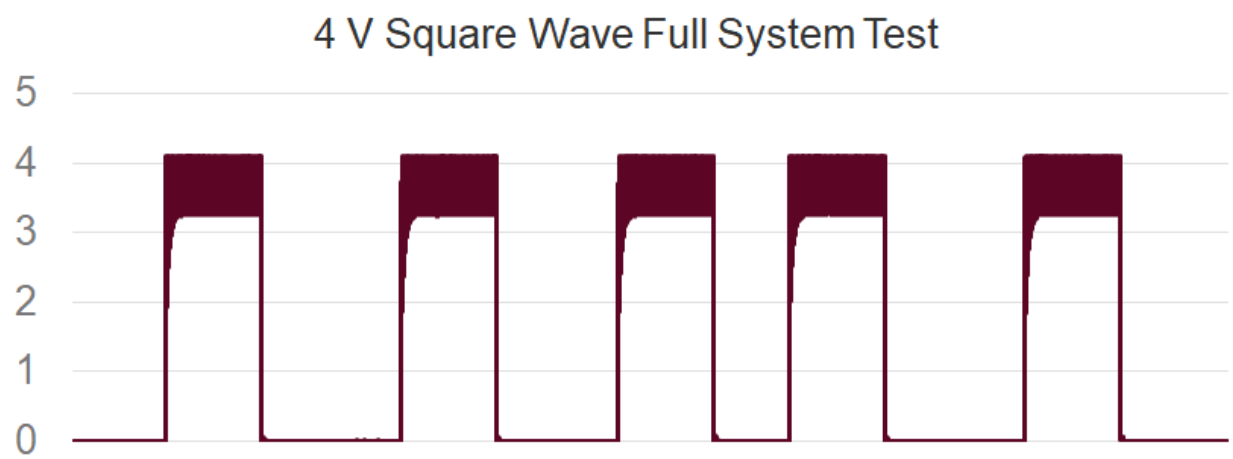


Figure 44: Processor & Interface 4 V Square Wave Data Capture

Figure 44 is a sample capture of a 4 Volt Square wave to the input of the ADC. This wave was initially a 2 Volt square wave before the signal conditioners and is provided with a gain of 2 to produce a 4 volt square wave.

Input Voltage Sensor	Gain	Expected Output	Actual Output	% Error

1 V	0.16	0.16 V	0.155 V	3%
1 V	0.32	0.32 V	0.321 V	~0%
1 V	1.26	1.26 V	1.262 V	~0%
200 mV	10	2 V	2.01 V	~0.50%
Shock Accelerometer	0.08	43.98 mV	48 mV	20%
Shear Accelerometer	0.32	52.15 mV	50 mV	4%
Pressure	1.26	1.47	1.38	6%
RTD	5.01	0.548 V	1.62	19%

Table 15: Signal Conditioning Validation - Gain Error

Table 15 contains the data found when testing the integrated design with both input voltages and the physical sensors required for the design. The table shows what input signal/sensor is being inputted/tested, the gain used to alter the signal, the expected and actual output, and then the error between those results. As stated earlier in this report, there is a lot of error present in the Shock Accelerometer and RTD sensor. The main reason for this is because the sensors are normally going to be provided with excitation voltage from the rocket, and will therefore create an excitation current for the sensor. However, since that is outside of the scope for this project, it wasn't able to be tested efficiently with the design and materials available.

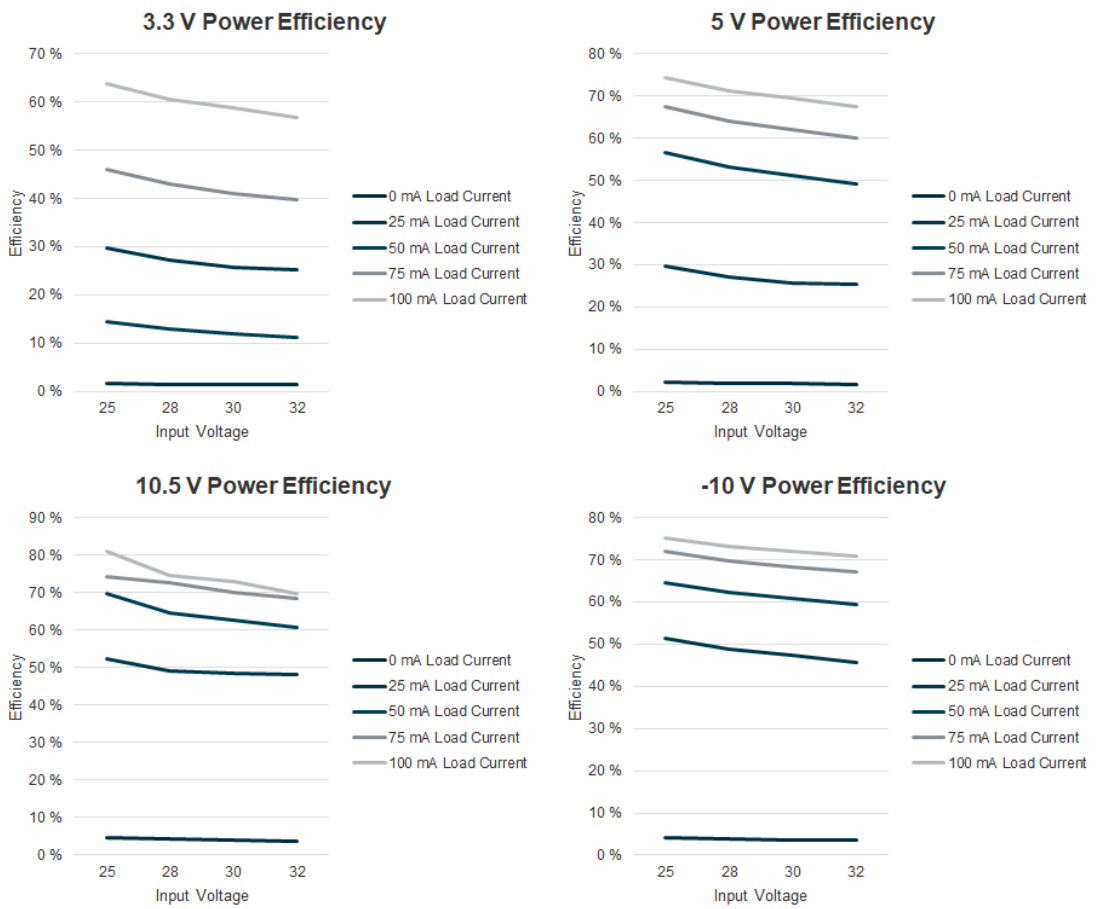


Figure 45: Power Efficiency Graphs

Efficiency results of the power system were measured using a multimeter in series with the power supply as well as the different loads. The different load currents represented the variable loads that were put on the different power rails. Different input voltages also represented how the rocket power source would behave throughout the flight, dropping from 32V to 25V. Efficiency results were nearly the same as the data sheet, indicating an efficient system. Efficiency increased as load current increased, and it increased as input voltage decreased. There were no apparent problems with powering the other subsystems.

23. Outcome

In this section, we will go over the overall outcomes achieved by each iteration of the UL-SWaP DaQ and what adjustments were made throughout the design and prototyping process.

23.1 The First Iteration

The first iteration design proved the concept that we were trying to achieve in our initial design of the unit and allowed for the system to operate with multiple points for testing the design in an effort to optimize for future iterations. The first iteration included two boards: one board populated with the signal conditioning and processor/interface components and one board populated with the power conditioning components. This modular design allowed for simultaneous testing of the power and signal/processor subsystems in an effort to make edits for a second iteration. For the power board, the +10.5V, +5V, and +3.3V rails were tested and validated to power the UL-SWaP DaQ properly and with enough power. For the signal/processor board, the PGAs produced a proper amplified/attenuated signal that could be received by the differential amplifiers. The processor unit was also able to produce a software selectable gain for the PGAs and be properly programmed by the user.

Some of the problems found from the first board were LVDS Driver placement, -10V rail part selection, proper level up of differential signal, physical sensor integration, and communication between the MCU and ADC. The LVDS driver was being tested and was accidentally stripped from the board along with the surface mount pads connected to it. The -10V rail would not produce a reliable constant voltage output and the differential amplifiers would not level up the differential signal to the proper range needed for the ADC (0V to 4.096V). In addition, the physical sensors were not all working properly due to improper signal conditioning for the RTD and pressure sensors. Finally, the communication between the ADC and MCU was problematic due to the use of a delay function and sequential programming. All of these problems were identified and fixed for the second iteration of the board.

23.2 The Second Iteration

The main adjustments made to the second iteration of the board was the integration of the power conditioning, adjusting the signal conditioning for the RTD and pressure sensors, and compacting the design in order to keep it within an area of 9 square inches. The second iteration achieved a full functioning and integrated system by having a complete and functioning power system as well as a processed signal through the Signal Conditioners and digital system. The communication between the MCU and ADC was addressed with new firmware based on the concept of a Finite State Machine implemented with a switch-case block and timer interrupts built into the MCU. Lastly, the output signal was a nominal LVDS UART signal.

The second iteration identified new problems with the design. The power component footprints were not adjusted properly and resulted in a problematic part placement. Despite this, parts were placed onto a power board and system validation was met.

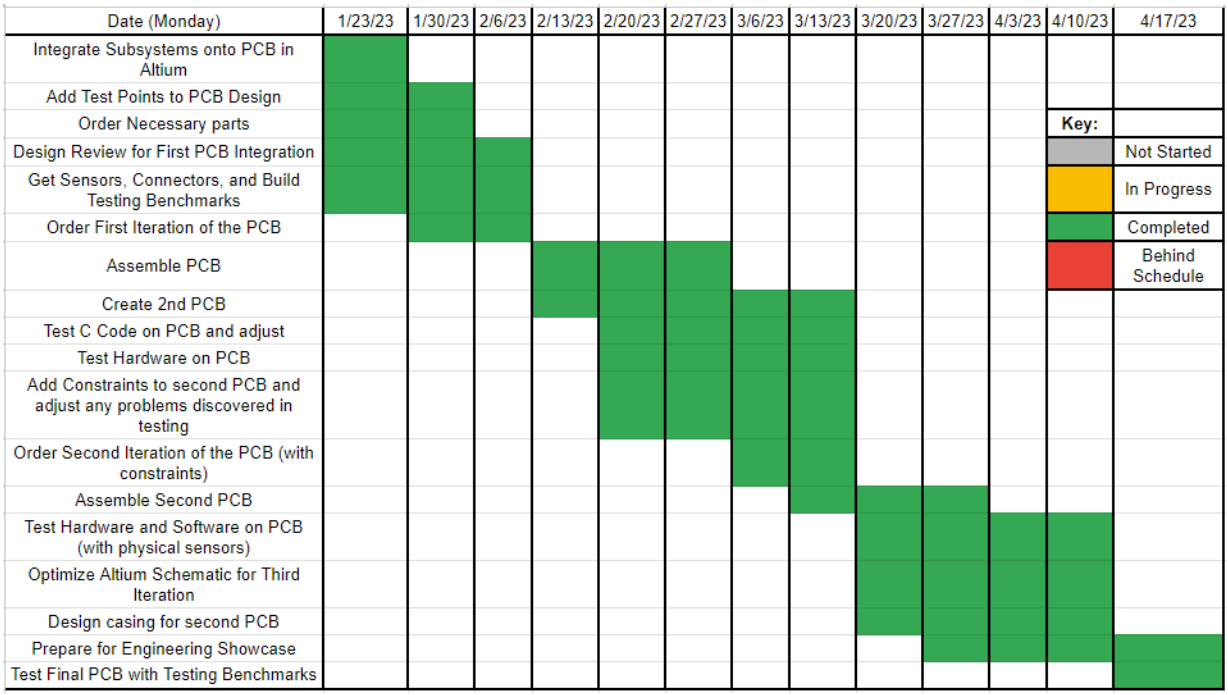
23.3 The Third Iteration

The final iteration of our design was not produced, but it was designed with focus on compactness and scalability. The second iteration was broken down into a Main board, consisting of power and the processor, and a Module board, consisting of signal conditioners. The overall volume was reduced substantially to less than 8 cubic inches with housing. In addition, the user has the ability to produce their own Module focused on the optimization of their sensors while still allowing two signals to be digitized. All of the parts were rechosen to be smaller and still be within the parameters of their functions.

24. Conclusion

The project concluded with successful operation. The signals are properly amplified or attenuated based on the firmware programmed into the microcontroller. The ADC can operate at higher than the stretch goal of our project for each channel. Due to the time constraint of this project, we were unable to test the operation of our data acquisition unit on a rocket flight. But, considering the success of our validation, we assume it will successfully function. In addition, our product has the potential to reduce the number of rocket flights which will save Sandia and their customers time and resources.

Appendix A: Execution Plan



Appendix B: Validation Plan

Paragraph #:	Test Name:	Success Criteria:	Methodology:	Status:	Responsible Engineers:
8.2.1.1.	Maximum Power Draw	System draws 3 Watts or less Power	Use Electronic Load to test Power Draw; will test with all PGAs on and with sensor connected.	TESTED	Robert Brown
8.2.1.2.	PGA Amplified Output	PGA alters the input signal to be within a +/- 2V signal	Test input signal of 1Vpp was properly attenuated to 0.32V with a gain of 0.32.	TESTED	Andrew Bainbridge
8.2.1.2.	Variable Signal Conditioning	Gain placed on Input Signal is measured within a 5% error on Output Signal	Signal Generator will provide a voltage signal which will be adjusted through Signal Conditioners and measured before ADC.	TESTED	Andrew Bainbridge
8.2.1.3.	LVDS Signal creation	The LVDS Driver successfully creates an LVDS signal out of the UART protocol	Use an oscilliscope with differential capabilities to verify LVDS generation and Decomposition into UART message.	TESTED	John McWhirter
8.2.1.3.	Transmission Efficiency Test	The amount of samples transmitted from the DAQ to the user is < 5% error	System will be ran for X amount of minutes and the expected number of samples will be compared with the experimental number	TESTED	John McWhirter
8.2.1.4	Hardware Selectable Gain	The PGA GPIO pins are able to be set to a high or low voltage in order to control the gain of the PGA	Measured 1.6 Volts when set to High and 0.2 Volts when set to low.	TESTED	Andrew Bainbridge
8.2.1.4.	Software Selectable Gain	The PGA GPIO pins are set to either High or Low dependent on Firmware and GPIO pins connected to the MCU	Measured >1 voltage at the GPIO pin to check for set to High and <1 for set to low.	TESTED	John McWhirter
8.2.2.1.	Mass	The total weight of all subsytems is less than 500 grams	The Final PCB will be measured at each Iteration on a digital scale.	TESTED	ALL
8.2.2.2.	Volume Envelope	The total volume of the device will be less than 27 inches cubed (3inx3inx3in).	The system dimensions and volume will be measured both before and after integration to ensure the system is within the range specified.	TESTED	ALL
8.2.3.1.1.	Input Voltage Level (Signal conditioners)	PGAs will require a +10.5V, -10V, and +5V input and the differential amplifiers will require a +5V input from the power source.	Each path of power module input connection and sensor output will be tested for correct voltage and current values.	TESTED	Robert Brown
8.2.3.1.1.	Input Voltage Level (Processor)	PIC32 will require a 3.3V input from the power source.	Load and Line Test Converter and monitor voltage on MCU at worst and best case scenarios (Worst: all 4 input channels used at variable gain, Best: 1 input channel used at 0 gain.)	TESTED	Robert Brown
8.2.3.4.1.	Data Output	4 conditioned signals are properly measured by the ADC and displayed on a console	An AC and DC signal will be tested separately and then together on 1 or more channels of the DaQ. The measurement will be taken using an Analog Discovery Unit and then displayed on graphs.	TESTED	John McWhirter
N/A	Signal Conditioning Demo	Test input signals (physical sensors) to create into 2 differential signals between 0 to 4.096V: 100mV, 1V, 2V, 4V, 7V, 10V	Will measure test points between differential amplifiers and ADC to ensure conditioned signal is within 0 to 4.096V.	PARTIAL	Andrew Bainbridge
N/A	Processor and Interface Demo	The PIC32 can read SPI messages from the ADC and transmit a UART message to the LVDS Driver.	Test digital inputs will be given to the processor and the output will be compared to the expected output on the interface.	TESTED	John McWhirter
N/A	Power Module Demo	The subsystem supplies the proper amount of power to each component of the system.	Each output from the power module will be measured to ensure it has the expected voltage and/or current at each node.	TESTED	Robert Brown

*The signal conditioning demo is marked as “partial” due to some of the physical sensors having too much gain error during testing and validation.

Appendix C: Doxygen

The Doxygen HTML output is attached to this online document as a Zip file. Open the 'index.html' file in a browser. In addition, the Doxygen HTML is provided in the github repository. See Appendix E.

Appendix D: System Operation Manual

The system operates using the MPLAB X IDE v6.00 software. To program the MCU, one may adjust the C code provided in the github link under Appendix E. Please note that code was automatically generated by Harmony v3 and the configuration files are located in the github directory with the extension *.mhc. See Appendix E.

Appendix E: Github Repository Link

The following link is a github repository containing the PCB Libraries, schematics, and Each of the Altium Projects used to design our board. In addition, the firmware is found in the directory under the UL-SWAP-DAQ-firmware directory. Finally, the doxygen Output is found under the doxygen directory.

https://github.com/jmcwhirter1608/ULSWAPDAQ