Chapter 1
Introduction

Since the beginning of the new millennium, the world of digital system design has witnessed an unprecedented phenomenon: a rapid and persistent reduction in feature sizes well into the nanoscale realm. Advancements in device technology and fabrication techniques have enabled designers to tread into previously uncharted territories; integration of billions of transistors on-die is now a reality. At such integration levels, it is imperative to employ parallelism to effectively utilize the transistors [1].

1.1 The Diminishing Returns of Instruction-Level Parallelism

In order to extract as much parallelism out of the processing engine as possible, today's microprocessors incorporate a multitude of sophisticated micro-architectural features, such as multiple instruction issue, dynamic scheduling, out-of-order execution, speculative execution and dynamic branch prediction. However, in order to sustain performance growth, future superscalar microprocessors must rely on even more complex architectural innovations. Olukotun et al. [2] have showed that circuit limitations and limited instruction level parallelism will diminish the benefits afforded to the superscalar model by increased architectural complexity. Increased issue widths cause a quadratic increase in the size of issue queues and the complexity of register files. Furthermore, as the number of execution units increases, wiring and interconnection logic complexity begin to adversely affect performance. This newly-developed ability to integrate previously unimaginable amounts of logic on a single die has naturally led to a paradigm shift in computer architecture. Instead of concentrating on exploiting the saturating Instruction-Level Parallelism (ILP) through complex, super-scalar cores, architects are now starting to target Thread-Level Parallelism (TLP) by using multiple simple Central Processing Units (CPU) cores. The embodiment of this transition is the advent of Chip Multiprocessors (CMP) as a viable alternative to the complex superscalar architecture. CMPs are simple, compact processing cores forming a decentralized micro-architecture which scales more efficiently with increased integration densities

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[2]. The Cell Processor from Sony, Toshiba and IBM (STI) [3], and the Sun UltraSPARC T1 (formerly codenamed Niagara) [4] signal the growing popularity of such systems. Furthermore, Intel's very recently announced 80-core TeraFLOP chip [5] exemplifies the irreversible march toward many-core systems with tens or even hundreds of processing elements.

1.2 The Dawn of the Communication-Centric Revolution

The multi-core thrust has ushered the gradual displacement of the computation-centric design model by a more communication-centric approach [6]. The large, sophisticated monolithic modules are giving way to several smaller, simpler processing elements working in tandem. This trend has led to a surge in the popularity of multi-core systems, which typically manifest themselves in two distinct incarnations: heterogeneous Multi-Processor Systems-on-Chip (MPSoC) and homogeneous Chip Multi-Processors (CMP). The SoC philosophy revolves around the technique of Platform-Based Design (PBD) [7], which advocates the reuse of Intellectual Property (IP) cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations. The appeal of such a modular approach lies in the substantially reduced Time-To-Market (TTM) incubation period, which is a direct outcome of lower circuit complexity and reduced design effort. The whole system can now be viewed as a diverse collection of pre-existing IP components integrated on a single die. Naturally, the correctness and efficiency of operation rely heavily on inter-module communication. In fact, this new design paradigm has inflicted enormous strain on the interconnection backbone, which now needs to undertake a more prominent and sophisticated role.

1.3 The Global Wiring Challenge

The surge in popularity of SoC architectures has, therefore, highlighted the importance of the on-chip interconnection fabric and has drawn attention to the intricacies surrounding the wiring aspects of complex chip design.

Modern Application Specific Integrated Circuits (ASIC) consist of a number of metal layers (around eleven, as of 2006 [8]) situated on top of the active silicon layer. A typical layout is illustrated in Fig. 1.1 [8]. These layers are used to interconnect the various components of the chip. Bottom metal layers tend to be thin and narrow, while top layers are thicker and wider. As shown in Fig. 1.1, metal layers are divided into four distinct groups, based on the length of the respective interconnects: (1) Metal 1 (also referred to as Local), (2) Intermediate, (3) Semi-Global, and (4) Global. The top metal layers (i.e., Global) are used – as their name suggests – for

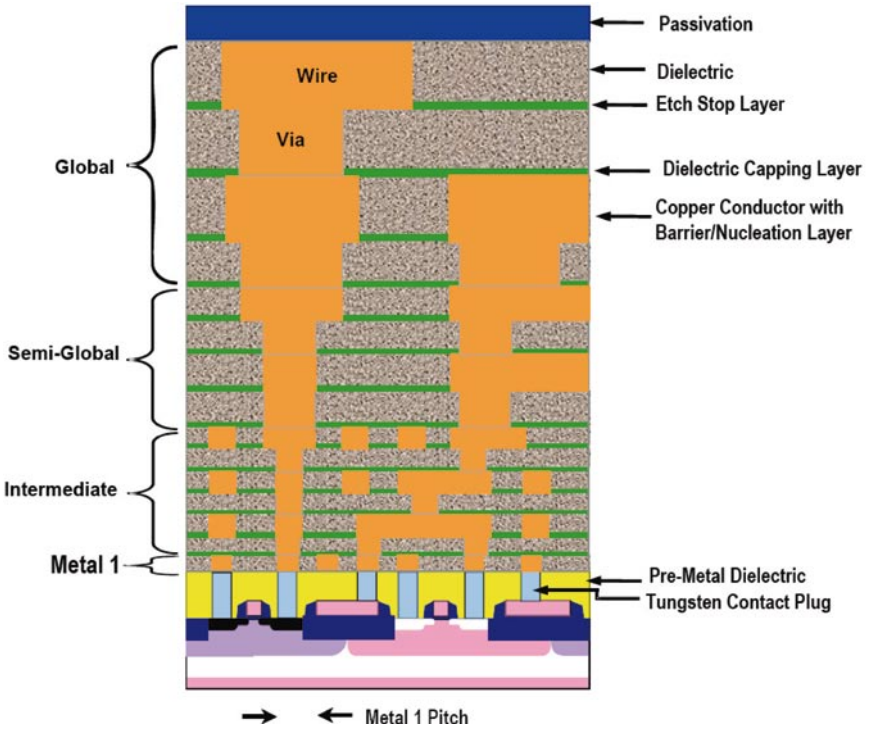

Fig. 1.1 Metal layers in modern ASIC devices [8]

long interconnects between distant components on the chip. The larger cross-section of these wires (a corollary of their larger width and thickness) ensures lower resistance and, therefore, increased propagation speed.

While gate (i.e., logic) delays have been scaling down dramatically over the last few years, global wiring delays are, instead, increasing [8]; as wire cross-sections decrease, resistance increases. This troublesome development is illustrated in Fig. 1.2 [8], which plots relative delay against process technology size. The top two curves on the graph highlight the alarming increase in global wiring delays, relative to gate delays, as technology feature sizes diminish into the nanoscale regime. Global wire delays increase exponentially with feature size, or at best linearly after repeater insertion [9]. Hence, this conundrum is transforming the interconnect backbone into the major performance bottleneck in modern, many-core systems, which require communication over substantial distances across the chip. The long communication distances are further compounded by increasing clock frequencies; the latter imply that signal traversal across the chip die will require many clock cycles [10], adversely affecting overall system performance. Alarmingly, it has been projected that in forthcoming technology nodes, up to 77% of the delay will be attributed to the interconnect [11].

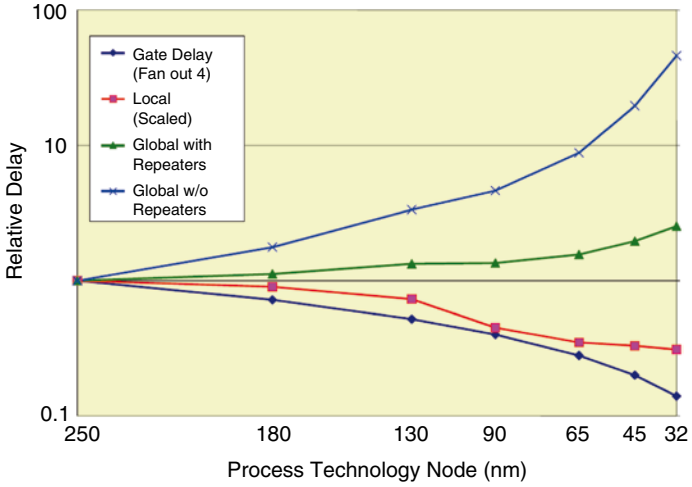

Fig. 1.2 Relative wire delays in ASIC implementations [8]

1.4 The Network-on-Chip (NoC) Solution

A variety of interconnection schemes are currently in use, including crossbars, rings, buses, and NoCs [12]. Of these, the latter two have been dominant in the research community [13,14]. However, buses suffer from poor scalability; as the number of processing elements increases, performance degrades dramatically. Hence, they are not considered appropriate for systems of more than about 10 nodes [13,15]. To overcome this limitation, attention has shifted to packet-based on-chip communication networks, known as Networks-on-Chip (NoC) [13,14,16,17]. Much like their macro-network brethrens, NoCs scale very efficiently as the number of nodes (e.g., processing elements) increases. Due to their scalability, NoCs are considered the most viable solution for many-core chips of the future. Intel's TeraFLOP chip is a prime example of this assertion [5].

NoCs, however, pose several design challenges emanating from their inherently stringent resource constraints; namely, area and power limitations. Recent research results have indicated some worrisome trends pertaining to the NoC's consumption of overall system resources; the chip area and power budgets are increasingly being dominated by the interconnection network [6,18,19]. As the architectural focus shifts from centralized, monolithic designs to distributed, multi-core systems, communication power has become comparable to logic and memory power, and is expected to eventually surpass them [6]. In fact, on-chip communication already consumes a significant portion of the chip's power budget (about 40%) [20,21]. This ominous trend has been observed by several researchers [13,18,22,23] and the realization of its ramifications has fueled momentum in investigating NoC architectures. The on-chip network's significant consumption of valuable resources is a stark reminder of its criticality in digital system design.

Thus, all three critical objective functions in any chip design (namely area, power and performance) are ominously being dominated by the underlying interconnect. This realization is very significant, since its impact could shake the foundations of all future many-core designs. Ideally, the interconnect should not stand out as the prime consumer of on-chip resources. Instead, it should blend as seamlessly as possible within the system, and contribute its services without being the sticking thorn in the design space.

Furthermore, aggressive technology scaling has accentuated the issue of reliability due to a rapid increase in the prominence of permanent faults; these are mostly caused from accelerated aging effects such as Time Dependant Dielectric Breakdown (TDDB) [24–26], Electromigration (EM) [27], Negative Bias Temperature Instability (NBTI) and Hot Carrier Effects (HCE) [28–30]. Moreover, soft upsets caused by cross-talk, coupling noise, power supply noise, and transient faults are also a concern to overall reliability [31–33]. Finally, thermal stressing due to hot spots has a direct bearing on both performance and power consumption and brings another complexity to the design space. In particular, this will play an important role in future 3D chip architectures, where elevated power densities are fairly common [34]. The growing concern about reliability in the interconnection network has prompted extensive research in this area [35–37].

A new serious impediment is also emerging as a force to be reckoned with: Process Variation (PV) resulting from manufacturing imperfections. PV is observed due to random effects, like Random Dopant Fluctuations (RDF) and systematic spatially-correlated effects like dose, focus and overlay variations [38]. These uncertainties impact various device characteristics, such as effective gate length, oxide thickness and transistor threshold voltages. Altered device characteristics may lead to significant variations in power consumption and to timing violations. While PV has been addressed extensively in the circuit and architecture communities, its impact in NoC architectures remains largely unexplored despite the menacing signs.

Given the looming prominence of both reliability and variability artifacts in deep sub-micron circuits, it is no longer sufficient to concentrate solely on the triptych of ***Performance/Area/Power***. Fourth and fifth pillars – comprising ***Reliability/Variability*** issues – should be added to the above trio of evaluation metrics to create a quintet of fundamental design drivers. This penta-faceted approach to evaluating NoC architectures forms the premise of the research presented in this volume.

The work described hereafter aims at developing *a comprehensive framework for designing high-performance, area- and energy-efficient, reliable, thermal-aware, and PV-resilient on-chip networks*, considering a multi-dimensional design space and the underlying technology constraints. Toward that extent, the said research takes a *holistic* approach encompassing the interplay of the previously mentioned evaluation metrics and their synergistic and symbiotic effects. The primary intellectual focus of this endeavor is to *understand the tradeoffs and corresponding ramifications of designing mission-critical components destined for severely constrained environments*, while still satisfying all the prescribed requirements.

1.5 Overview of Research

The previous section outlined the significance of reliability and variability in the design and evaluation of on-chip networks. The research presented in this volume will, therefore, give equal weighting to all five design metrics, and attempt to provide a detailed design space exploration of NoC architectures encompassing all primary design drivers. The aim is to develop architectural solutions to tackle all issues involved in a modern interconnection fabric connecting multiple cores. The problem will be attacked through a *two-pronged process*: (1) ***MICRO-Aarchitectural Innovations*** at the granularity of individual hardware components, and (2) ***MACRO-Architectural Solutions*** at a higher abstraction level; i.e., looking at the interconnection system as a whole. These two threads are highly interdependent and cannot be viewed in isolation; they complement each other and are entangled in an elaborate interplay which encircles the entire design. Efficient NoC implementations should address both facets and ensure seamless integration of the two. The proposed approach is illustrated abstractly in Fig. 1.3. As indicated in the figure, the micro-architectural investigation will concentrate on (a) the on-chip ***Router*** and (b) the ***Network Interface Controller (NIC)***, which constitute the main components within a network node. The bulk of the exploration will focus on the router, which offers a lot more flexibility in design choices. The macro-architectural

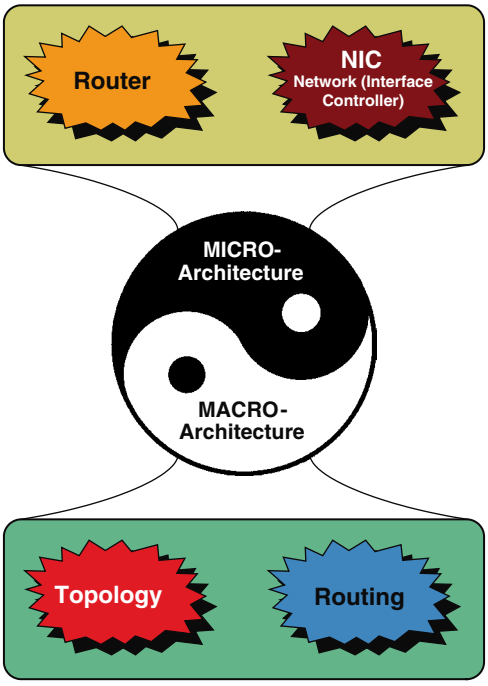

Fig. 1.3 High-level overview of the proposed research exploration

investigation will address (a) the network ***Topology*** and (b) the ***Routing*** process and associated algorithms.

Figures 1.4 and 1.5 expand on Fig. 1.3, and provide a more detailed overview for each of the two proposed paths (the micro- and macro-architectural approaches). The figures summarize the work completed by the author in the major design categories of the two core themes. Individual research projects are identified by a design keyword and the conference at which they appeared (see legend on page 9). The grid at the bottom of both figures classifies the projects based on their contribution to the previously mentioned quintet of fundamental evaluation metrics: (1) Performance, (2) Power, (3) Area, (4) Reliability, and (5) Variability.

Figure 1.4 (MICRO) divides the Router theme into its main components (***Buffers, Arbiters,*** and ***Crossbar***), while the NIC is investigated in terms of its main characteristic, i.e., the architectural ***Structure***. Similarly, Fig. 1.5 (MACRO) divides the Topology theme into ***Hybridization*** and ***Links***, and the Routing theme into ***Deterministic*** and ***Adaptive***. All these sub-categories combine to provide a complete picture of the NoC architecture, ranging from fine-grained (MICRO) to coarser-grained (MACRO) granularities.

1.5.1 Legend for Figs. 1.4 and 1.5

ViChaR: **"ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers,"** presented at the 39th Annual International Symposium on Microarchitecture (MICRO), December 2006 [39].

RoCo: **"A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks,"** presented at the 33rd Annual International Symposium on Computer Architecture (ISCA), June 2006 [40].

[AC,
PA,
TPA,
SON,

HBH Scheme]: **"Exploring Fault-Tolerant Network-on-Chip Architectures,"** presented at the International Conference on Dependable Systems and Networks (DSN), June 2006 [37].

ANCS-05: **"Design and analysis of an NoC architecture from performance, reliability and energy perspective,"** presented at the Symposium on Architecture for Networking and Communications Systems (ANCS), October 2005 [41].

MEP: **"A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects,"** presented at the International Conference on Nano-Networks (Nano-Net), September 2006 [42].

3D NetInMem: **"Design and Management of 3D Chip Multiprocessors Using Network-in-Memory,"** presented at the 33rd Annual International Symposium on Computer Architecture (ISCA), June 2006 [43].

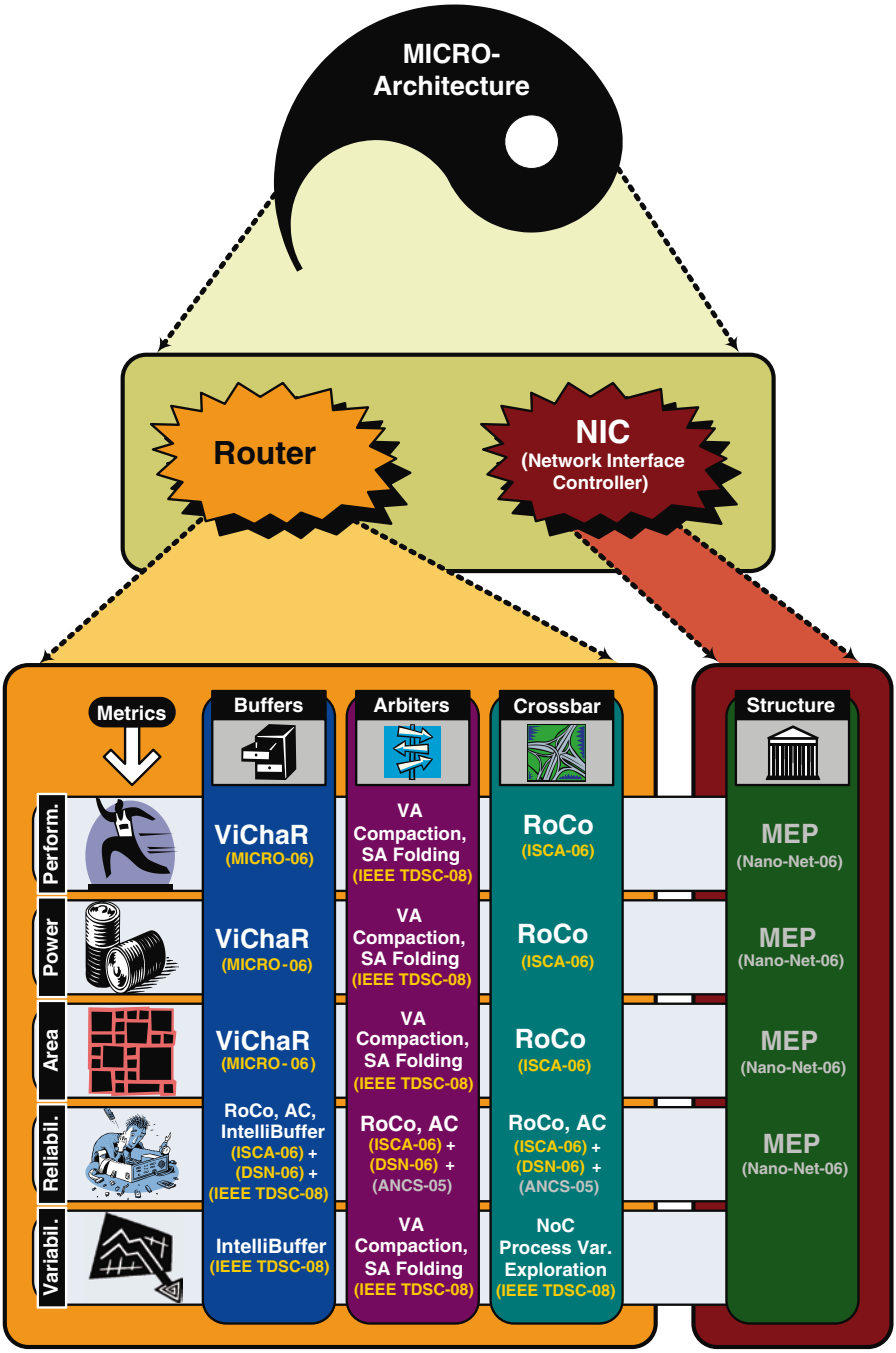

Fig. 1.4 Overview of MICRO-architectural research (see Section 1.5.1 for legend)

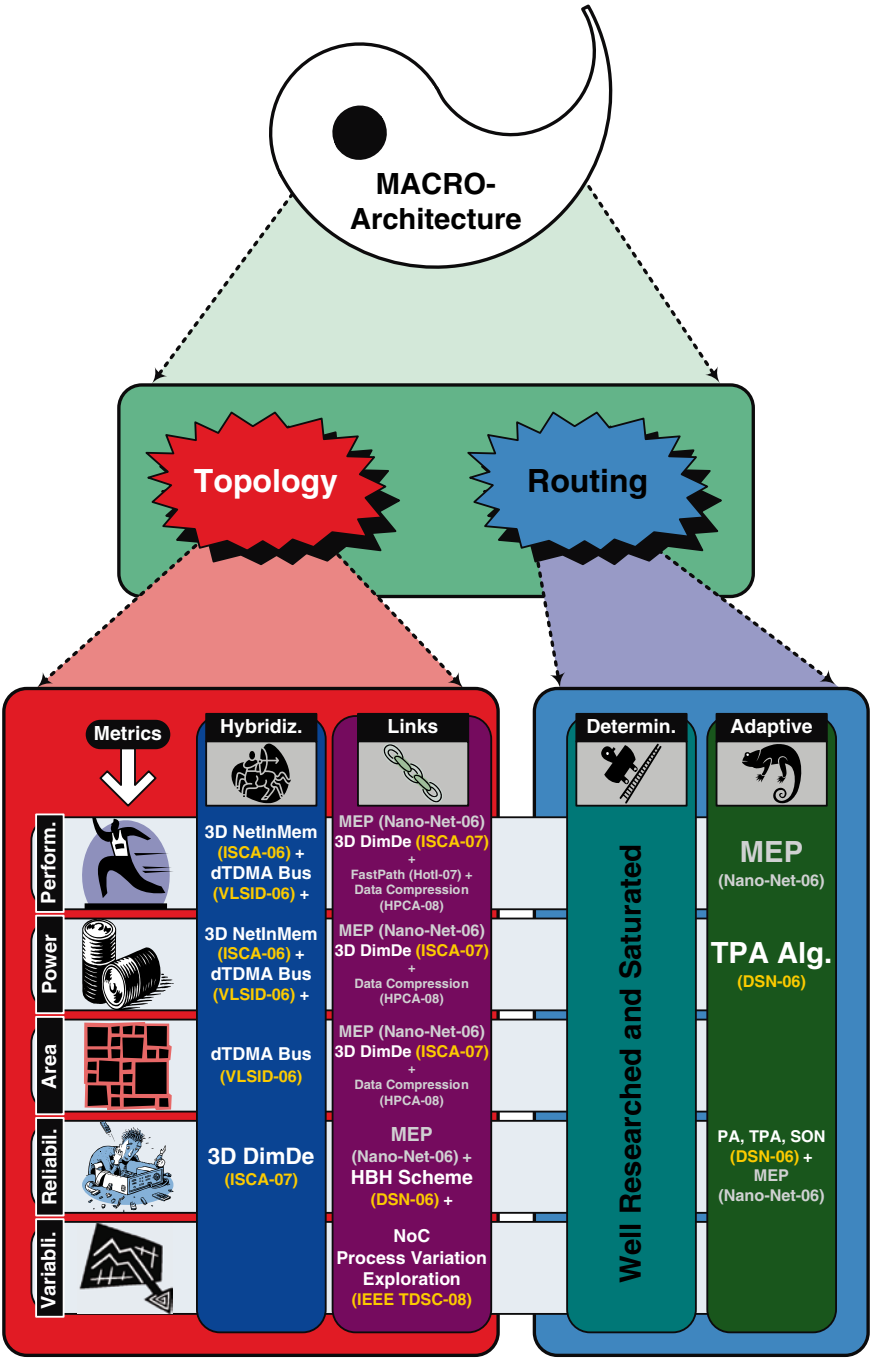

Fig. 1.5 Overview of MACRO-architectural research (see Section 1.5.1 for legend)

3D DimDe: **"A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures,"** presented at the 34th Annual International Symposium on Computer Architecture (ISCA), June 2007 [44].

dTDMA Bus: "**A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks,"** presented at the 19th International Conference on VLSI Design, January 2006 [15].

[IntelliBuffer,
VA Compaction,
SA Folding,
NoC Process Variation
Exploration]: **"On the Effects of Process Variation in Network-on-Chip Architectures,"** in the IEEE Transactions on Dependable and Secure Computing (TDSC), to appear in print; published online in 10.2008 [45].

FastPath: **"Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects,"** presented at the 15th Annual Symposium on High-Performance Interconnects (IEEE Hot Interconnects), August 2007 [46].

Data Compression: **"Performance and Power Optimization through Data Compression in Network-on-Chip Architectures,"** presented at the 14th International Symposium on High-Performance Computer Architecture (HPCA), February 2008 [47].

Keywords that are grayed-out in Figs. 1.4 and 1.5 indicate projects that do not form an integral part of this volume; however, they are included because of their peripheral significance and complementary role to the underlying concepts. These projects are briefly discussed in Chapter 10, which constitutes a digest of additional research conducted by the author in the area of on-chip interconnects.

The complementary nature of the two core thematic strands (MICRO and MACRO) implies that several of the projects contained within this volume fall under both categories. This attribute is further testament to the intertwined ramifications of NoC architectural exploration. The apparent overlap between MICRO- and MACRO- architecture in various pieces of work presented in this volume is illustrated diagrammatically in Fig. 1.6. In this figure, keywords shown in white represent work of peripheral significance to this volume.

Building upon the premise of exploring two research streams (MICRO and MACRO) this volume comprises *two distinct sections, each spanning four chapters*. The overall thematic structure of the volume is illustrated abstractly in Fig. 1.7.

The *first section* of the volume (Chapters 3 through 6) delves into the MICRO-architectural world of Networks-on-Chip; it contains detailed work on most of the major components found inside an on-chip router, as well as several novel concepts enhancing the overall operation of the network. Specifically, Chapter 3 presents a novel dynamic buffer manager, which optimizes the size and performance of the NoC buffers. Chapter 4 describes a decoupled router architecture that decomposes incoming traffic into two independent flows based on the direction of travel. The two flows are subsequently served by two smaller, leaner, and faster modules that are independently operated; this allows for partial router operation and graceful degradation. Chapter 5 develops several new ideas on fault-tolerance and reliability

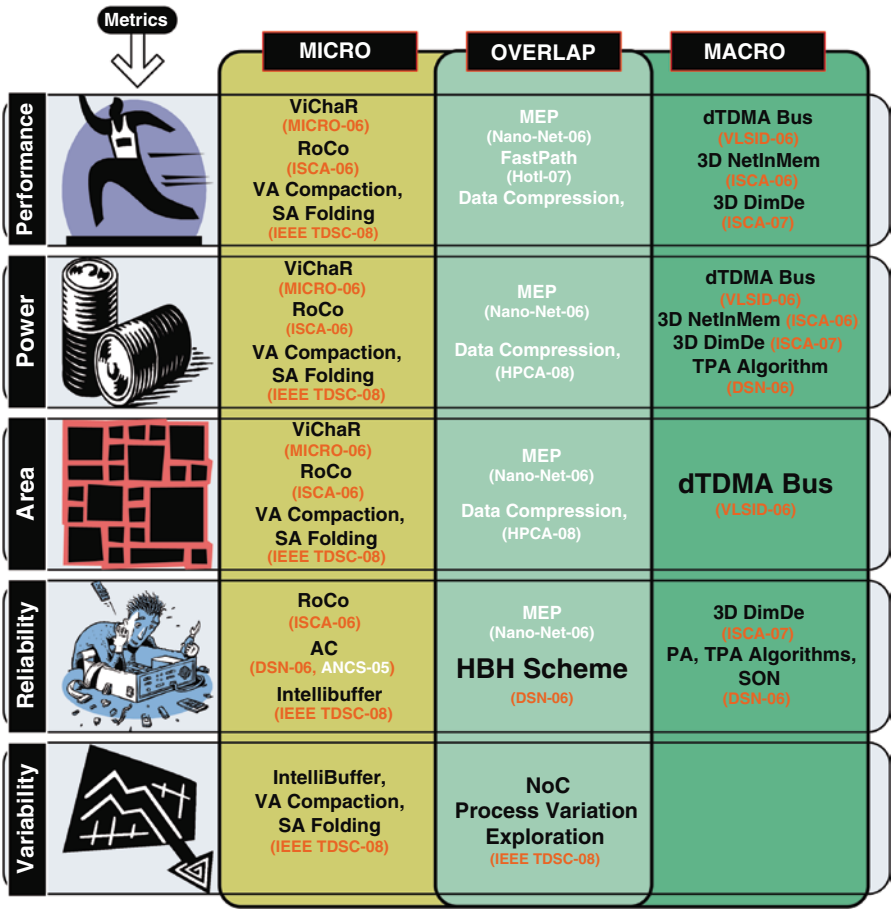

Fig. 1.6 Overlap between MICRO- and MACRO-architectural NoC research

in the presence of both soft (i.e., transient) and hard (i.e., permanent) failures in either the inter-router links or within the routers themselves. Finally, Chapter 6 tackles the relatively new and rapidly emerging threat of Process Variation. Several architectural solutions are proposed to account for process variability and counter its adverse effects.

The *second section* of this volume (Chapters 7 through 10) shifts focus to the MACRO-architecture of the NoC. Attention now is turned to higher abstraction layers that view the network as a whole system and try to investigate the behavior of both the network and the processing elements as a single entity working in unison. Chapter 7 starts this exploration by investigating the notion of interconnect hybridization; a newly developed bus structure is fused with an underlying NoC to reap benefits from both architectures in a unified environment. Chapter 8 extends the notion of hybridization to the third dimension. A new three-dimensional network

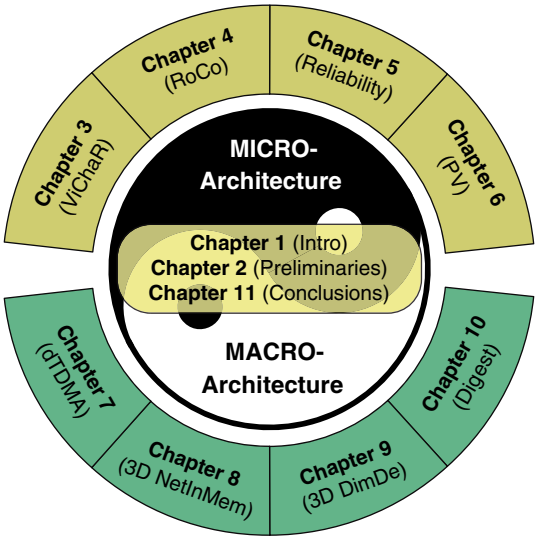

Fig. 1.7 Thematic structure of volume

topology is presented, which leverages the advantages of the emerging 3D stacking technology. In this implementation, the bus architecture is employed for transfers in the vertical (i.e., inter-layer) direction. The new design dramatically improves the L2 cache performance of a large CMP implementation. Chapter 9 continues the author's investigation into the fascinating world of 3D chips. Several new interconnect structures are investigated within the context of 3D integration, and a new dimensionally decomposed router architecture is presented, which leverages a true, physical 3D crossbar design. This new architecture constitutes a natural extension of the 2D decoupled router of Chapter 4. Finally, Chapter 10 presents a digest of additional research conducted by the author in the field of NoCs. This work is presented in summary, because it was not deemed to be of integral value to this volume. However, the salient features of these projects are certainly complementary and of significant peripheral value to the overall volume.

The work presented in this volume address the issues under investigation through the aforementioned penta-faceted evaluation prism, which encompasses the five key metrics of (1) **performance**, (2) **silicon area consumption**, (3) **power/energy efficiency**, (4) **reliability**, and (5) **variability**.