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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

A Dynamic Hardware Architecture for Future Networks

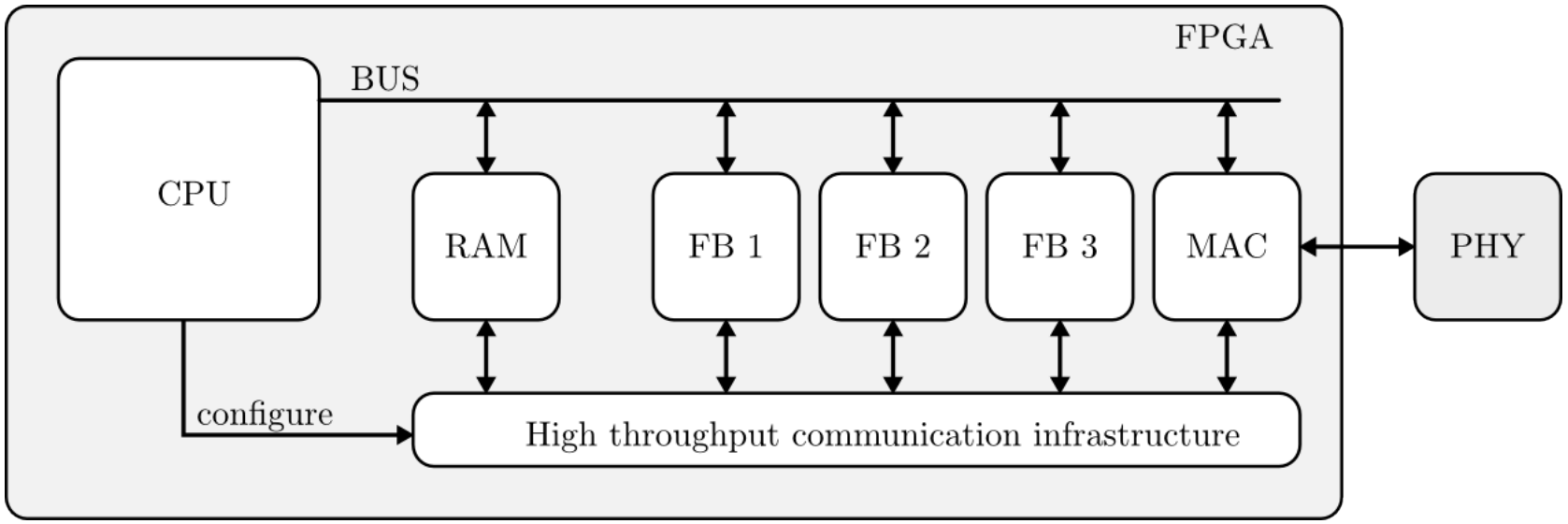
Master Thesis by Richard Huber

2nd Intermediate Presentation

Advisor: Ariane Keller
Co-Advisors: Dr. Stephan Neuhaus, Daniel Borkmann
Professor: Prof. Dr. Bernhard Plattner

Summary of 1st presentation

- ReconOS: Hardware acceleration with OS ressources
- ANA: Autonomous network architecture
- Problem: Shared bus is bottleneck



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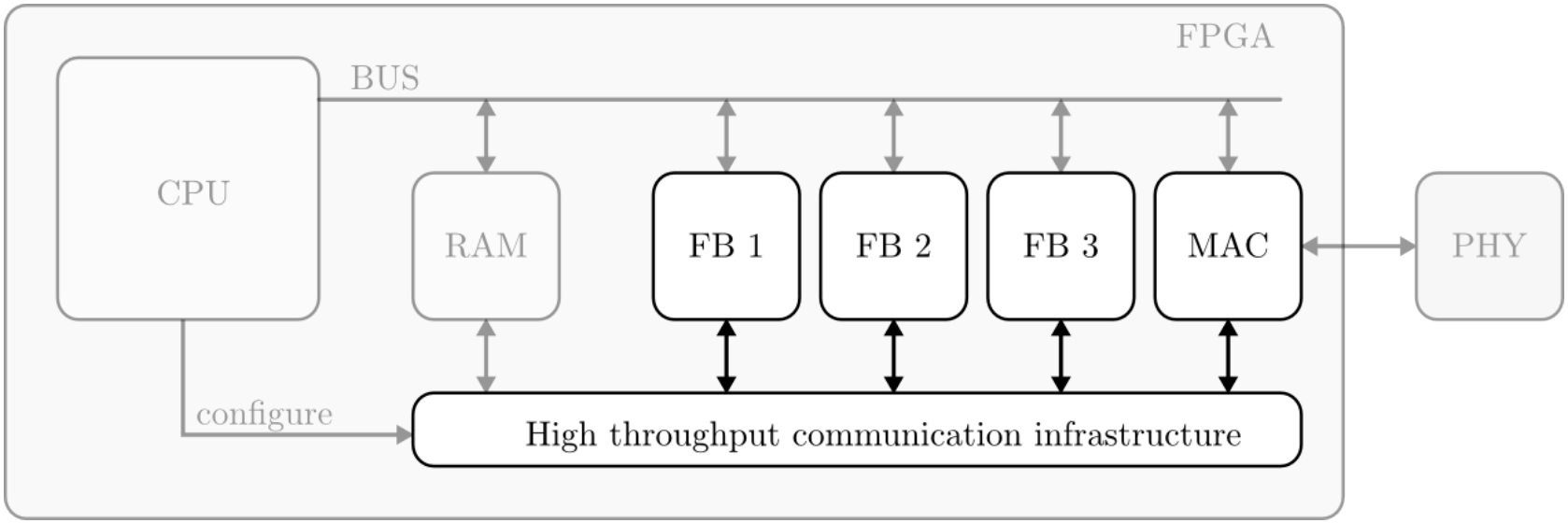
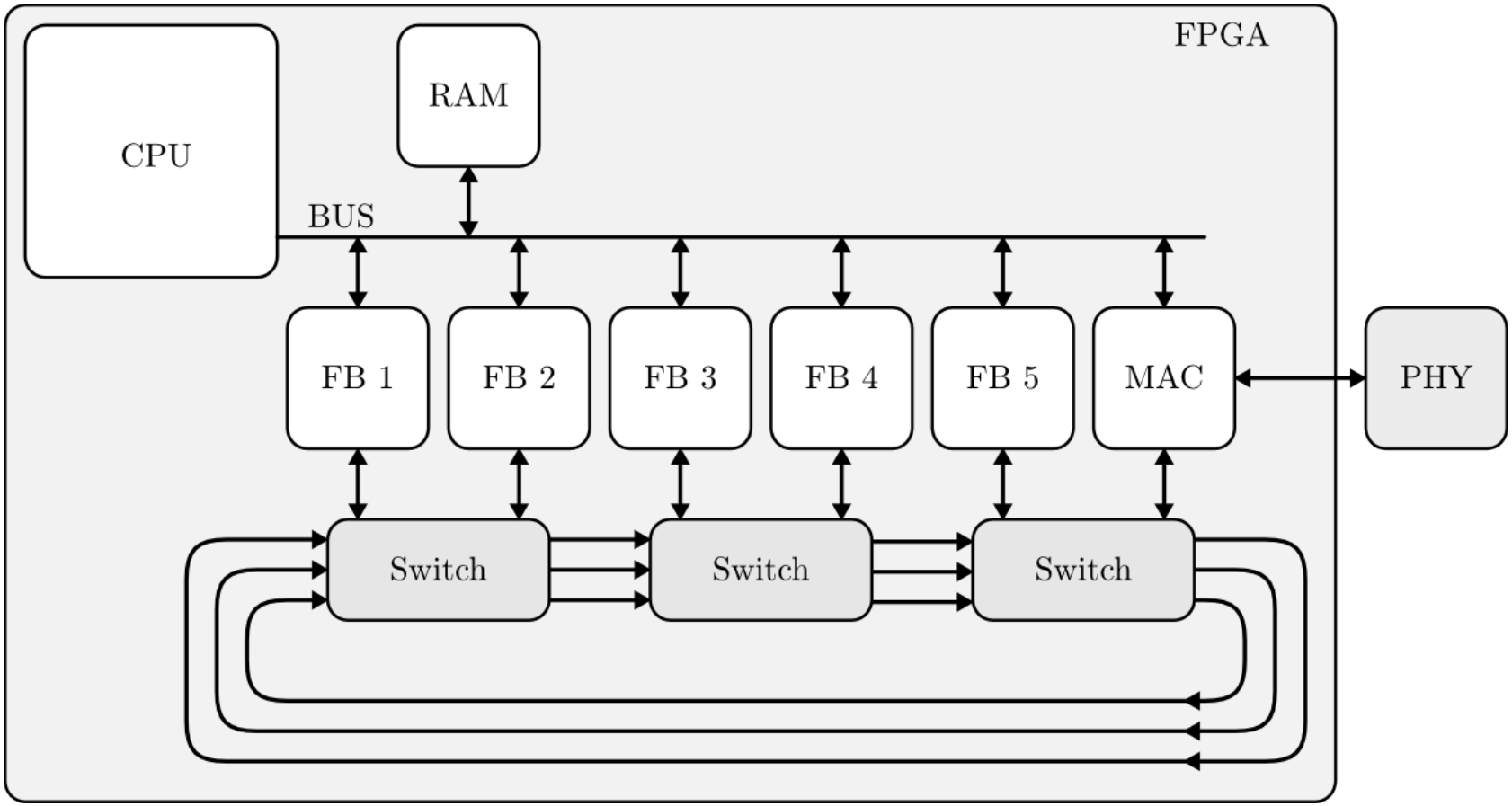


Network on Chip (NoC) Architecture



Hardware – Software Data Transfer

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  - a) All FB read/write data to RAM
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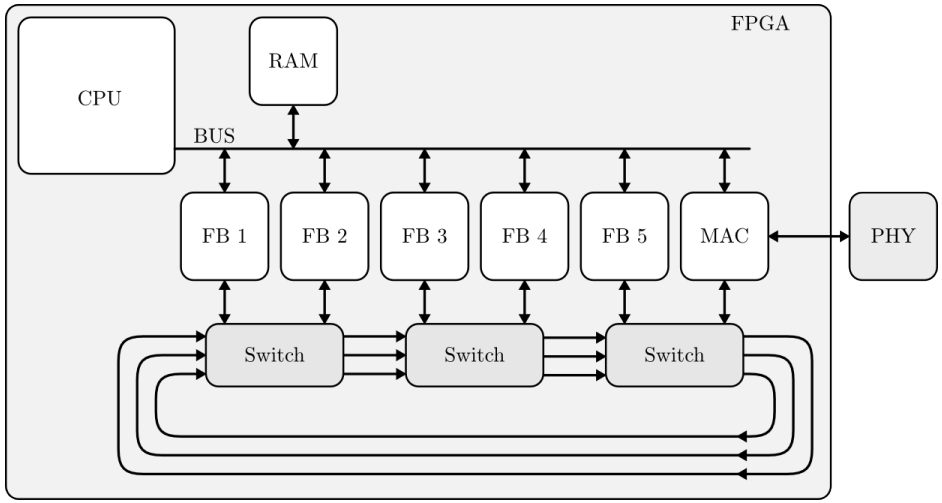

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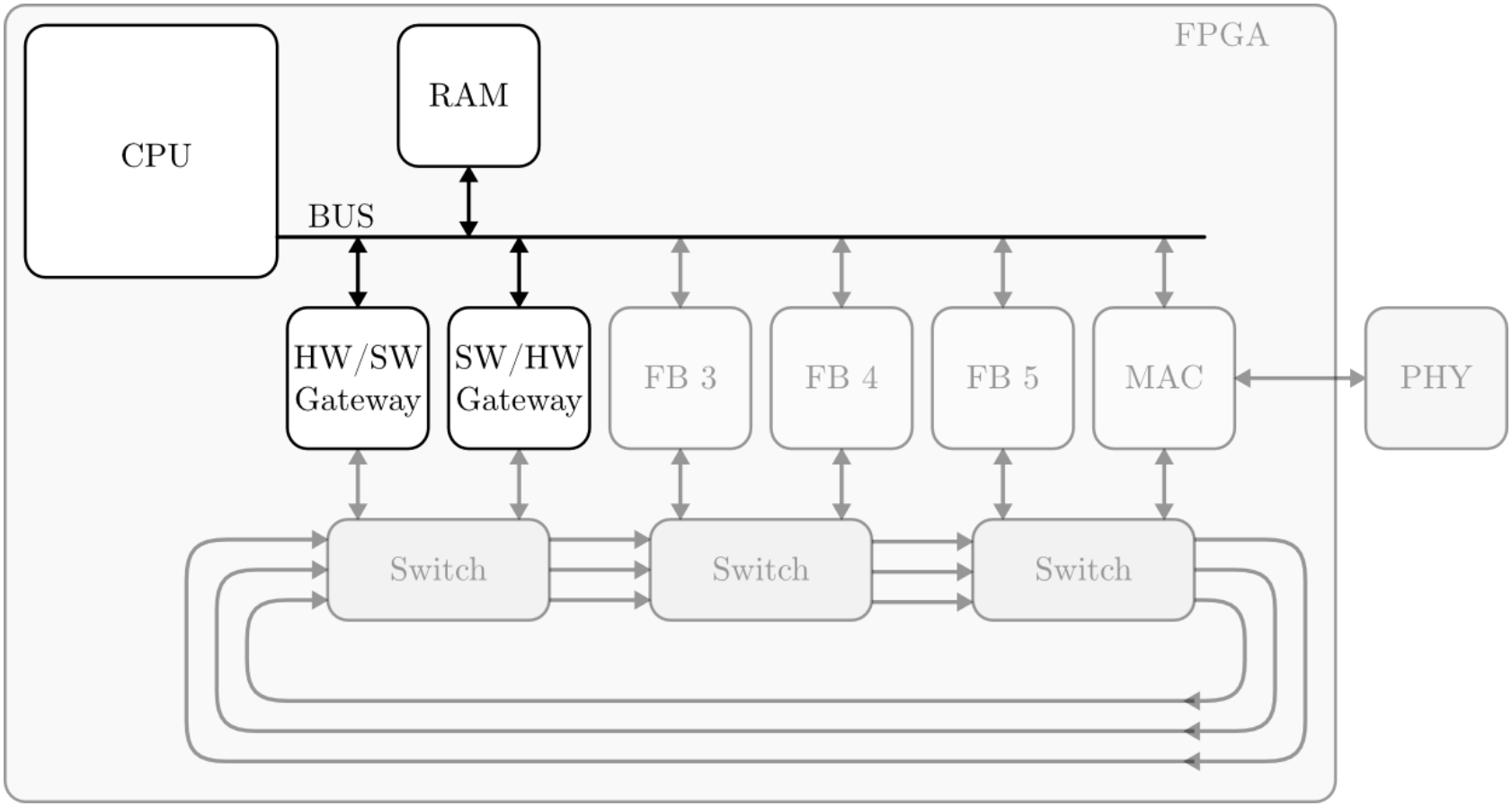
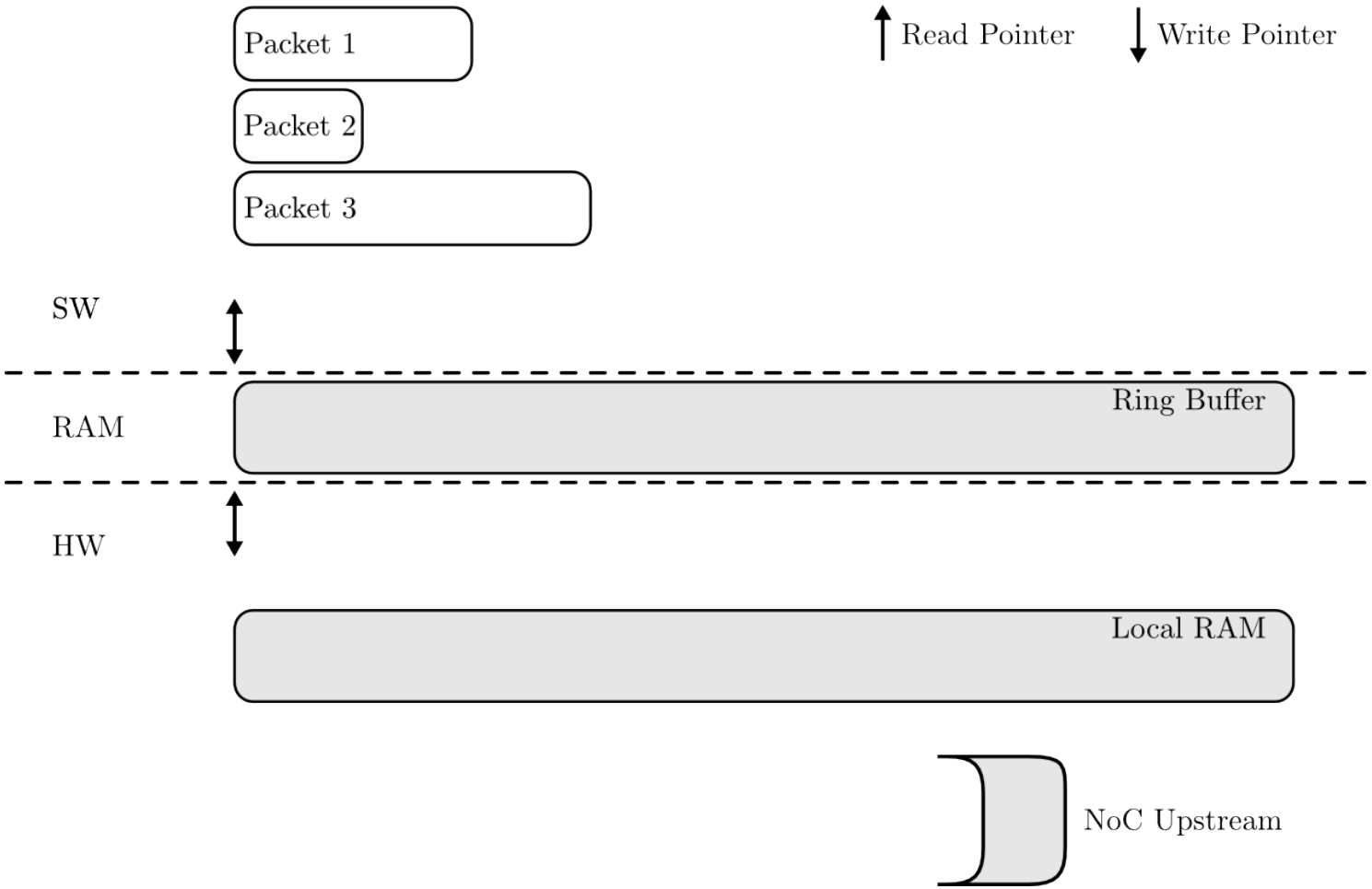


Principle of SW to HW gateway

- Use RAM area as ring buffer
- HW to SW gateway similar, just the other way around

Software to Hardware Gateway



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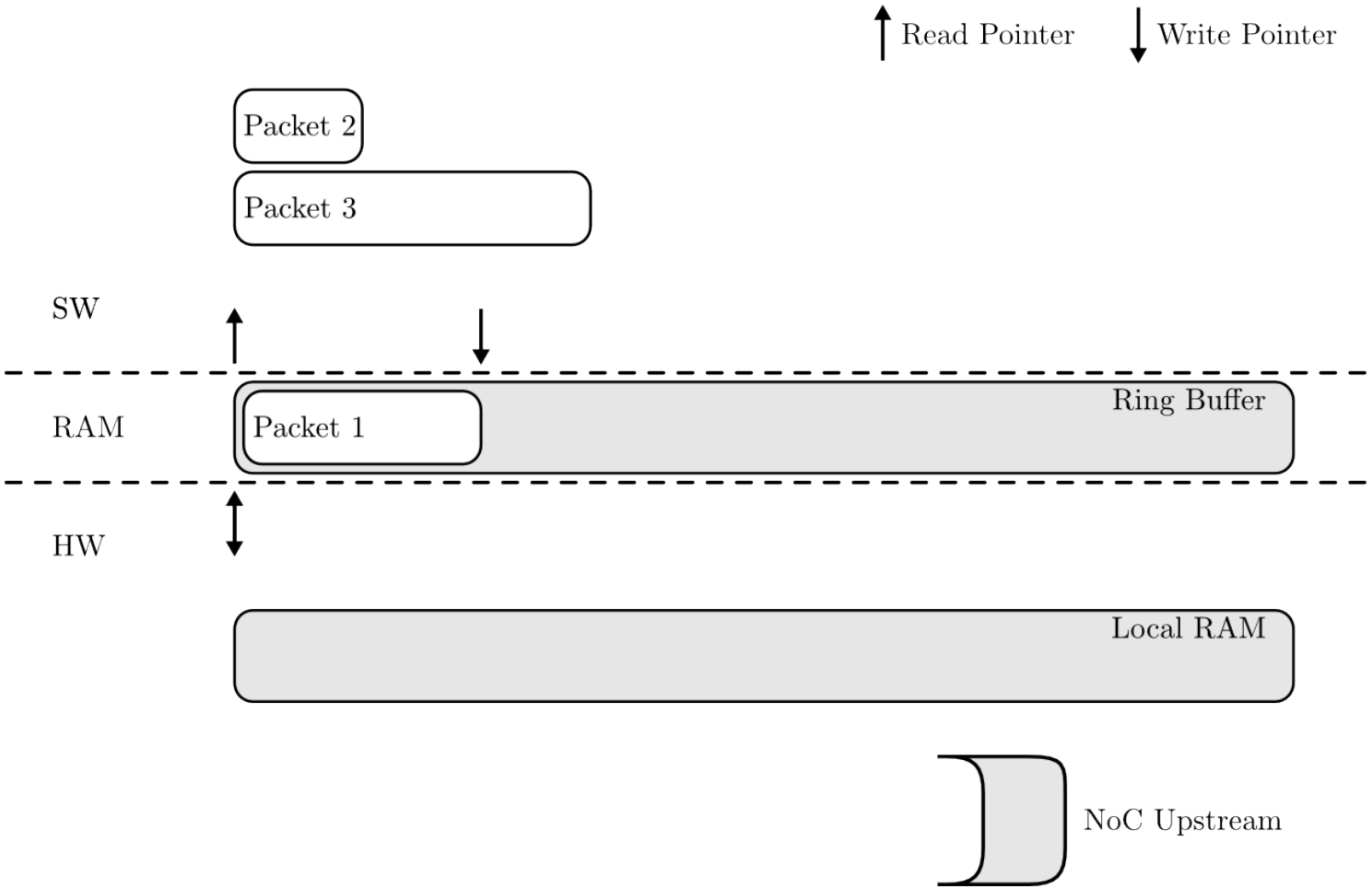

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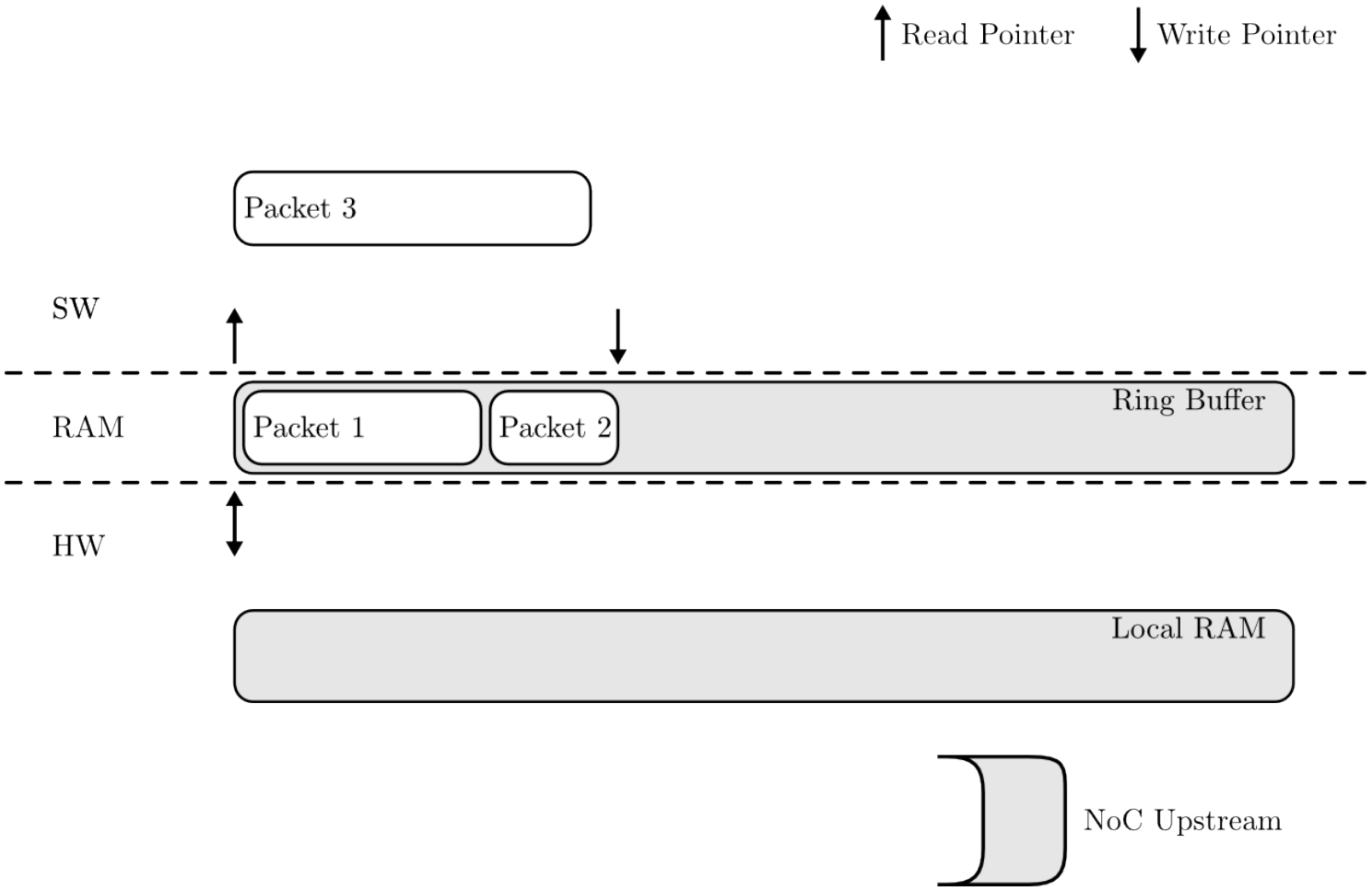

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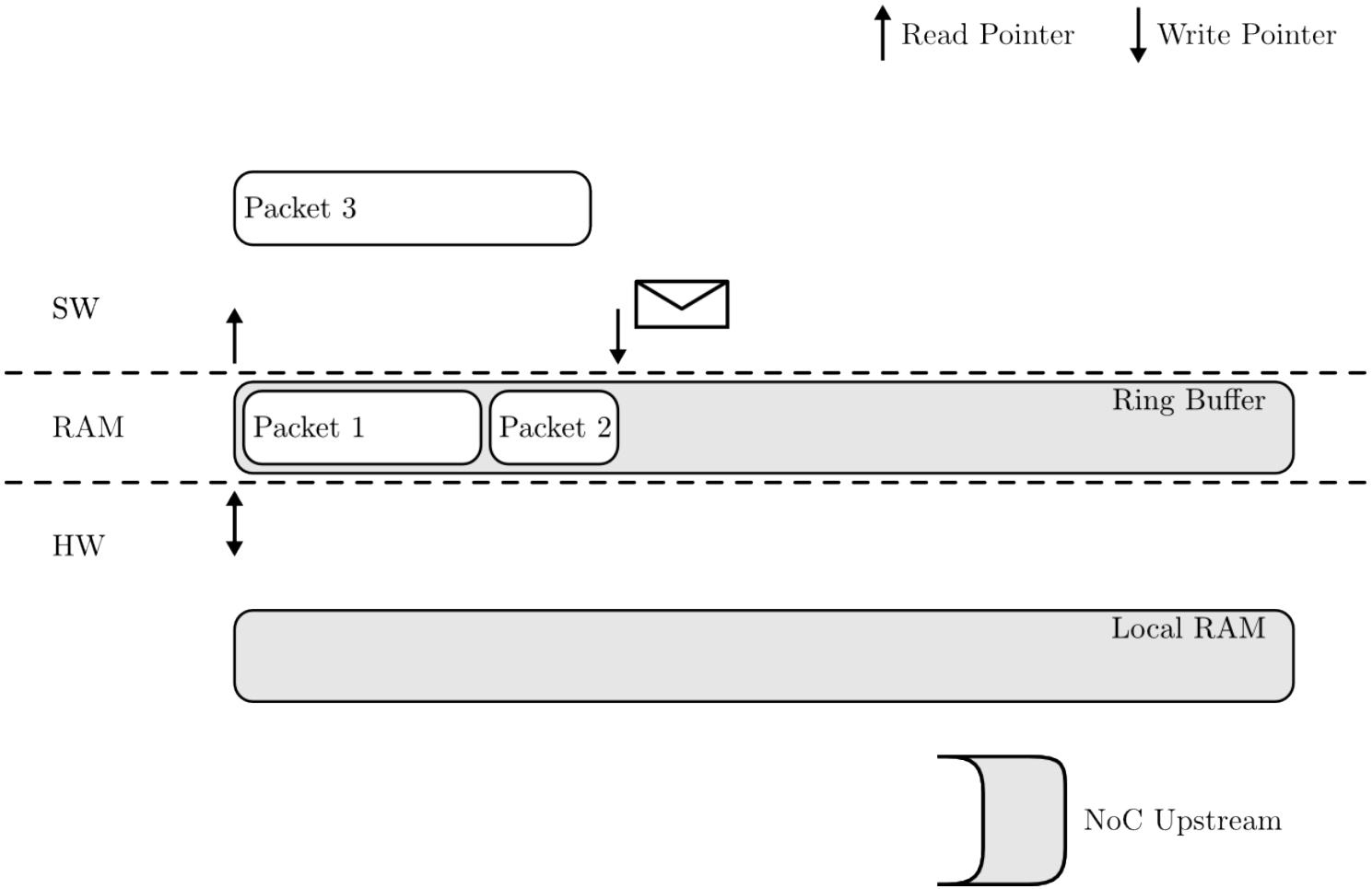
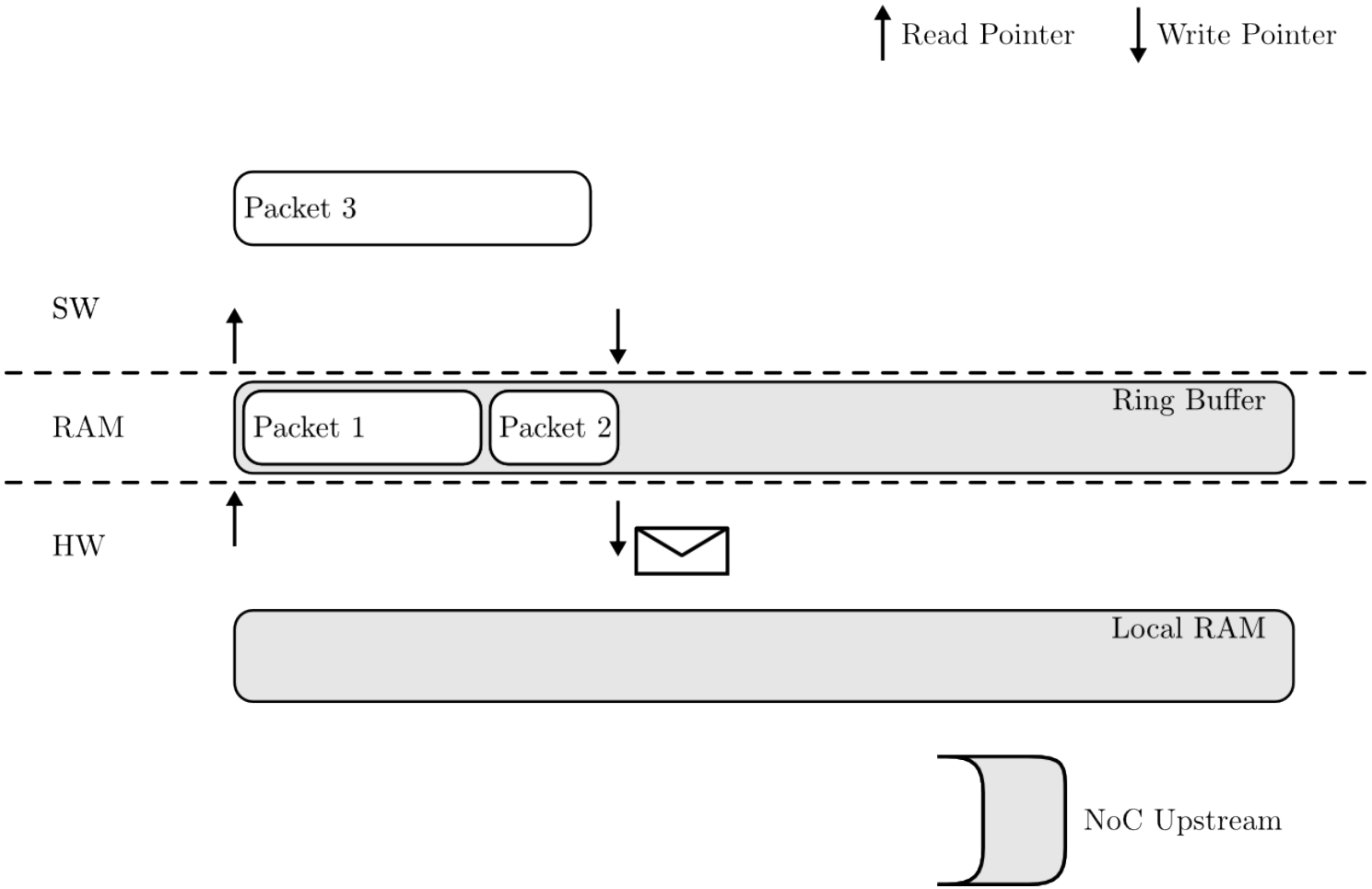
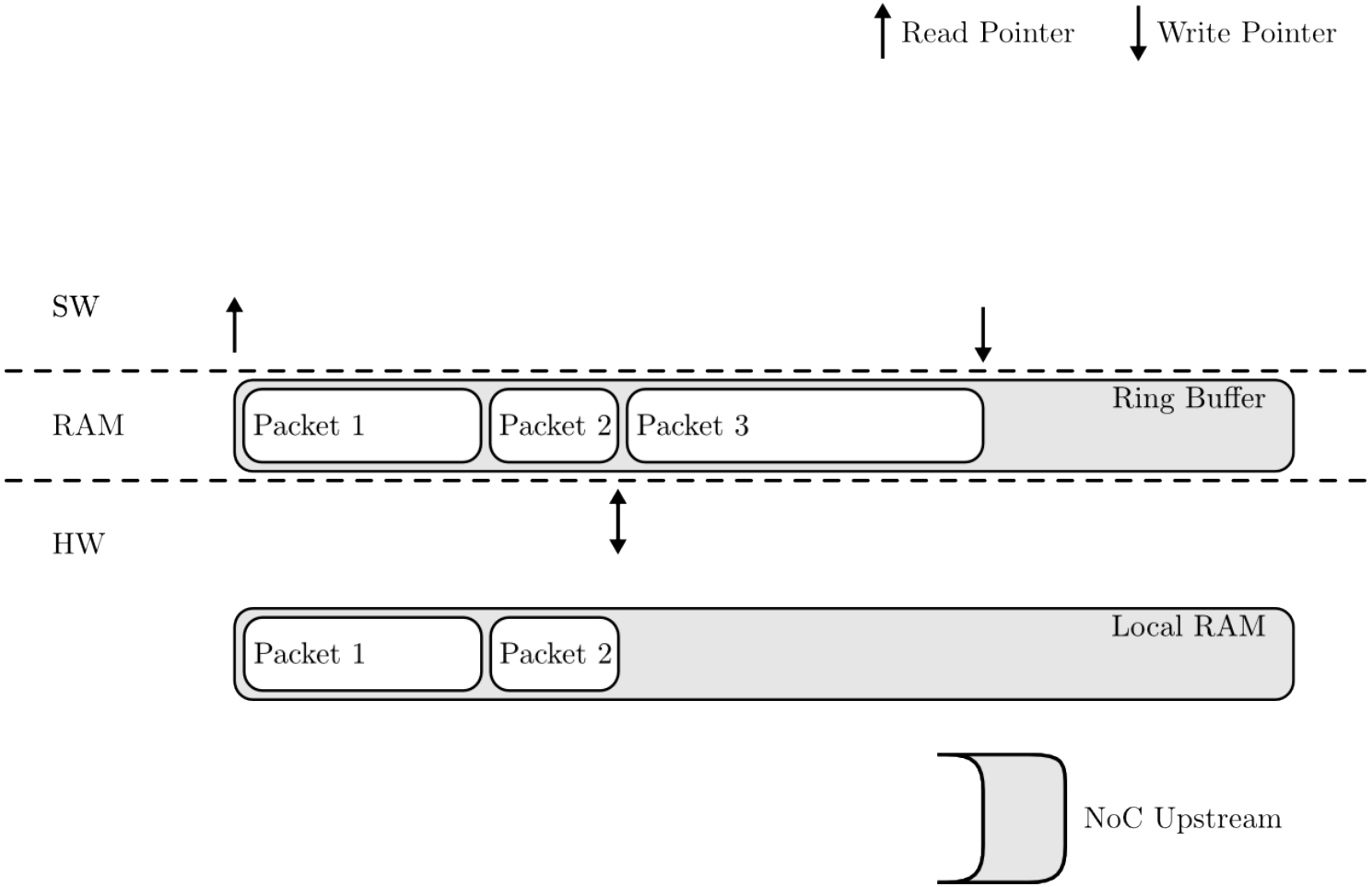



Read Pointer
Write Pointer
Packet 3
SW
RAM
Packet 1
Packet 2
Ring Buffer
HW
Local RAM
NoC Upstream

Software to Hardware Gateway



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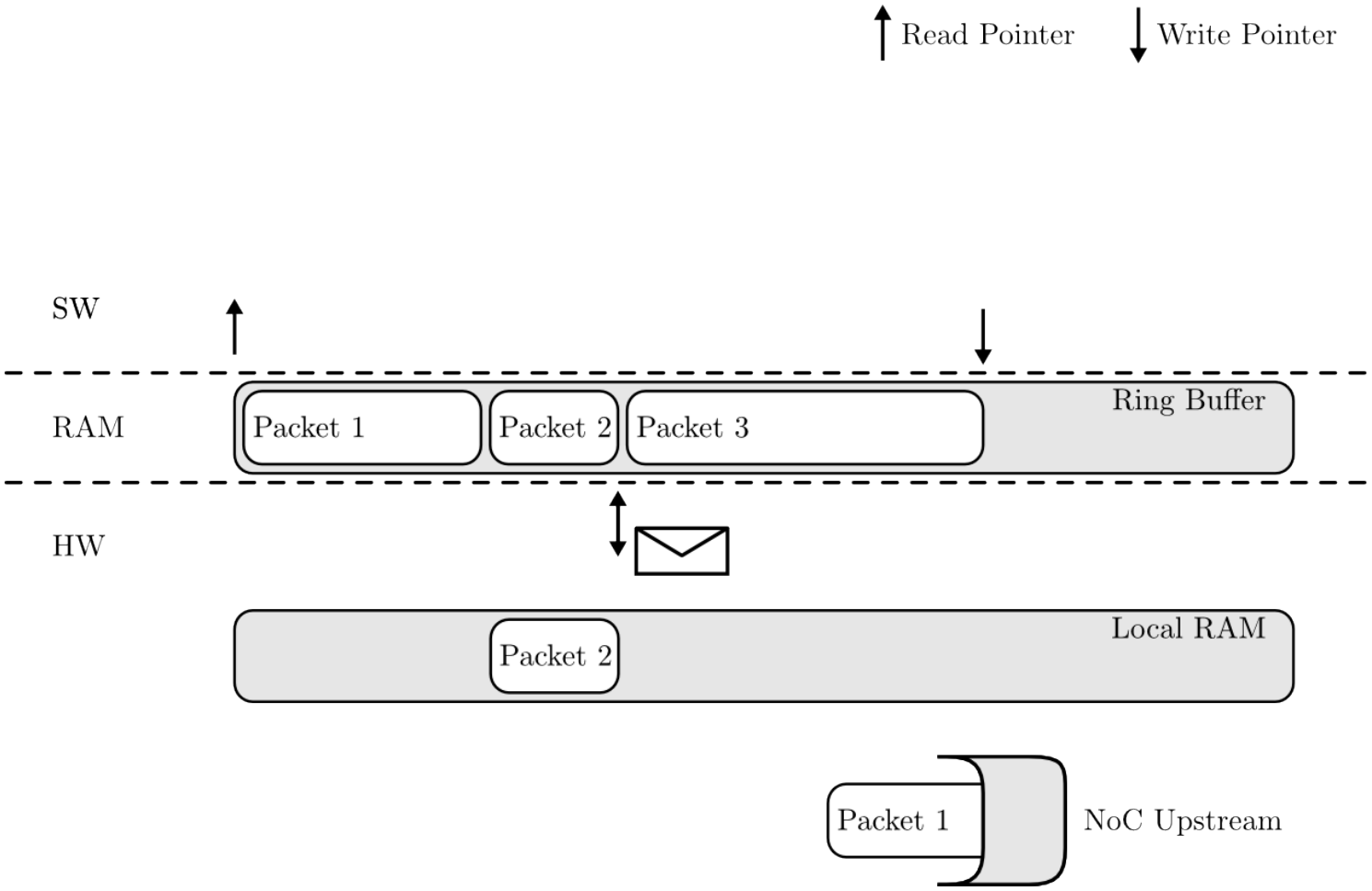

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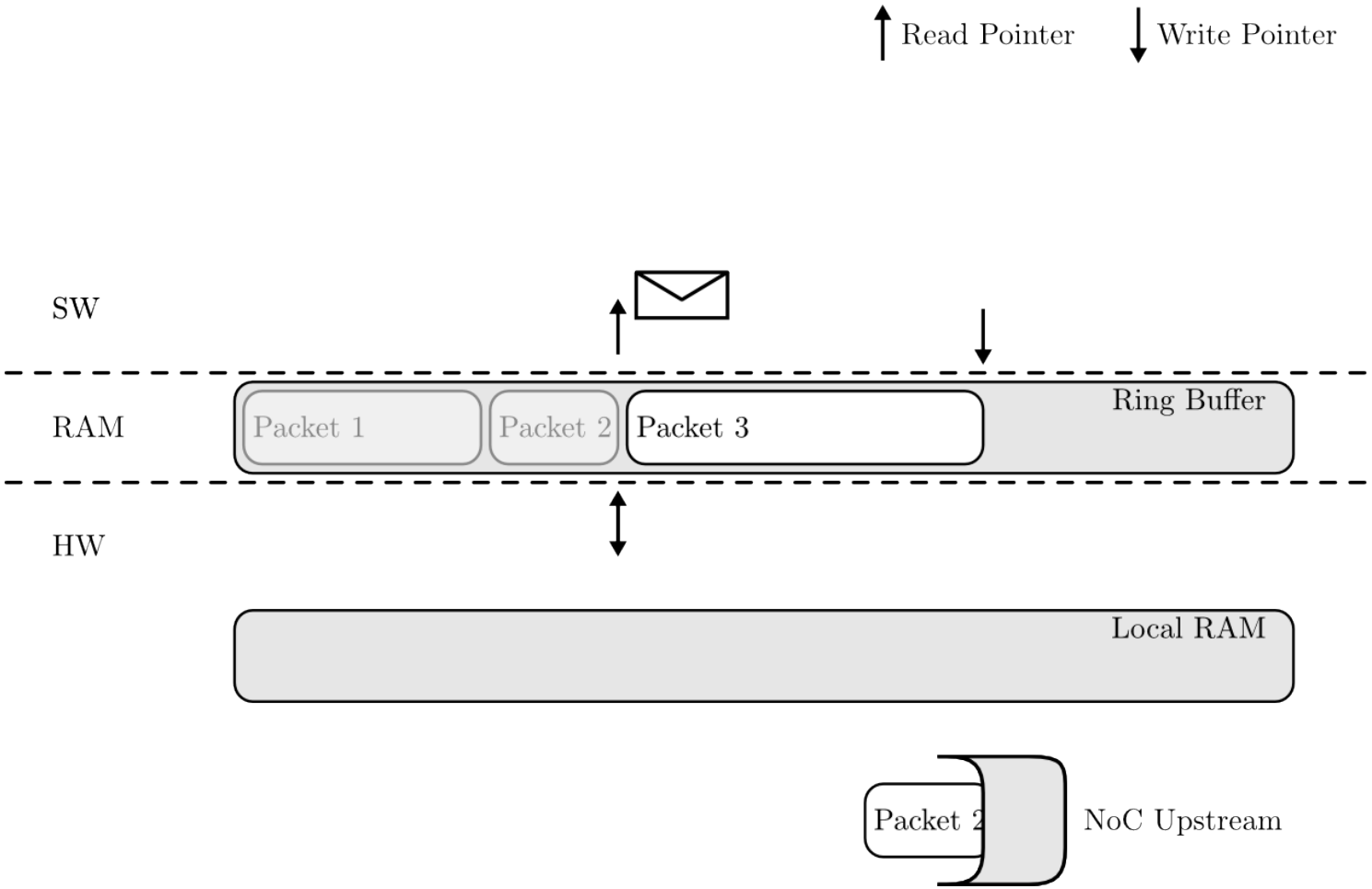

When to send write pointer to HW

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  - Packets have urgent flag
  - When flag set, transmit write pointer immediately

Task List

- ✔ Familiarization
- ✔ Evaluation of possible architectures
- ✔ Communication between HW blocks
- ➔ Conf guration interface
- ✔ Communication between HW blocks and SW
- ➔ Performance evaluation
- ➔ Final report

Challenges

- Diff cult to simulate hardware threads
- Endianness of target platform
- Take care of race conditions

Summary

- Network on Chip implemented for data transfer between HW threads
- Using ring buffers to transfer data from SW to HW and vice versa
- Dedicated HW and SW threads implemented for this purpose

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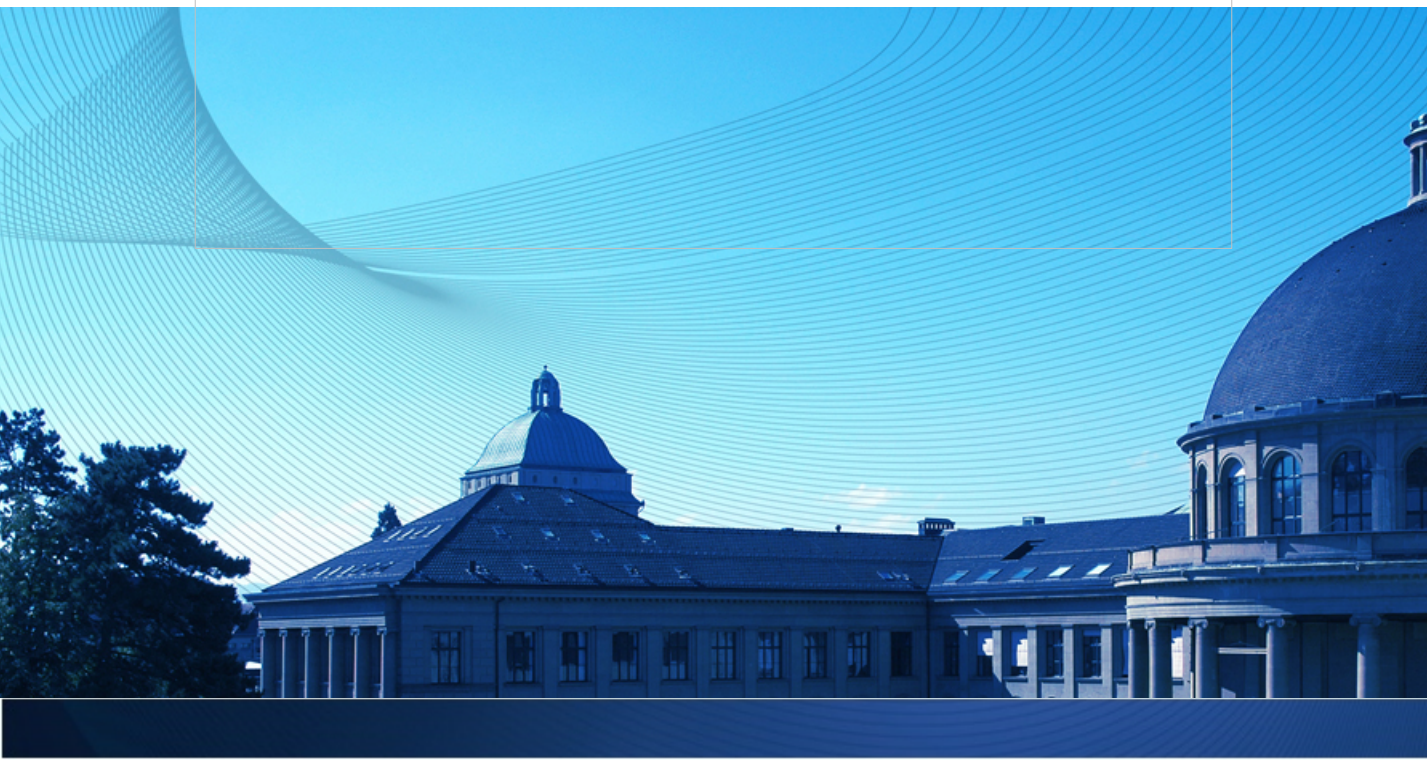

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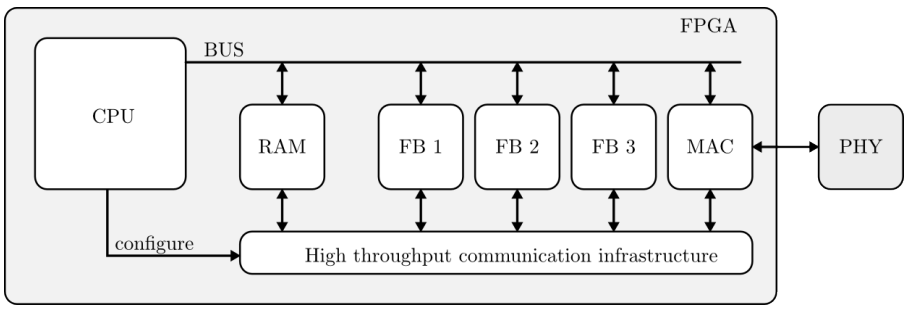

Ausgangslage

Motivation warum wir überhaupt etwas machen

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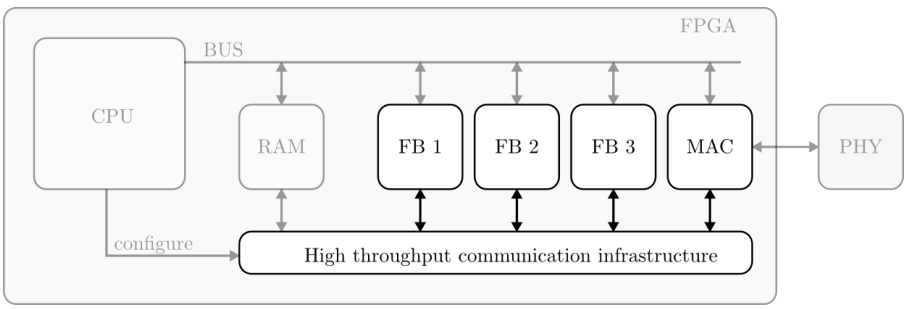

Im ersten Teil fokusierten wir auf den Datenaustausch zwischen den Hardware threads

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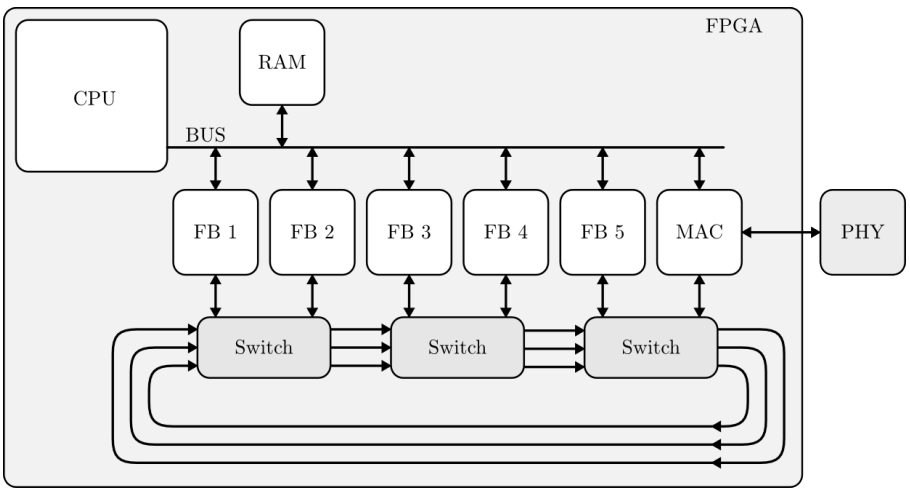
Network on Chip (NoC) Architecture



Stand bei letzter Präsentation

Bemerke: die Hardwarethreads sind immer noch am BUS angehängt, benuzten ihn aber nur für die Konfiguration, nicht zum Datentransfer.

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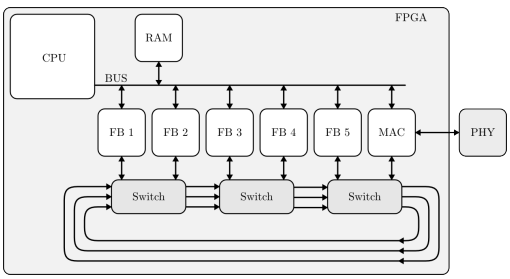

Die beiden Möglichkeiten, die wir diskutiert haben:

a) Alle FB senden ihre Daten unabhängig in die SW

vs.

b) FB senden alle Daten über NoC zu einem Gateway

Ausgelöste Interrupts:

a) mehr, b) weniger

Latenz

a) geringer

b) grösser

Wobei das bei starker Last durch die geringere Anzahl Interrupts aufgehoben wird.

Darum: Entscheid für b)

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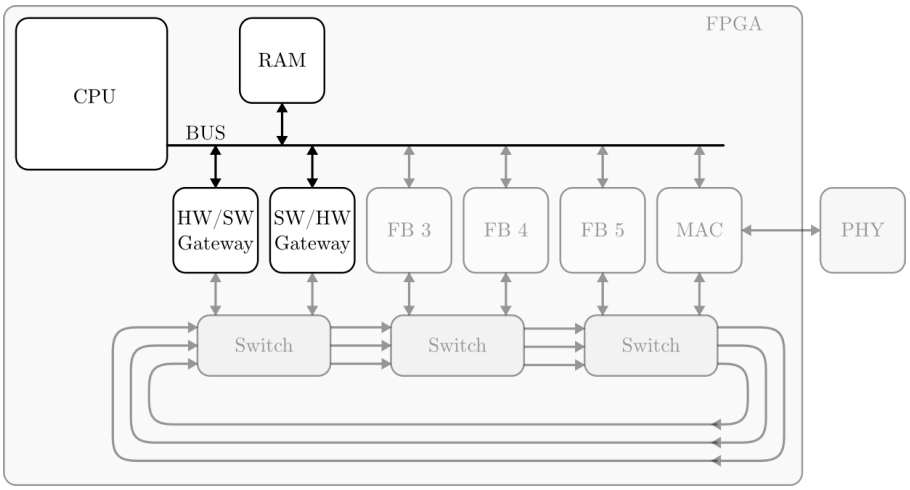

Im zweiten Teil fokusieren wir auf den Datenaustausch zwischen Software, die in der CPU läuft, und den Hardwarethreads

Ein Hardwarethread ist zuständig für den Transfer von Daten von HW nach SW und ein anderer für den Transfer von SW nach HW.

Principle of SW to HW gateway

- Use RAM area as ring buffer
- HW to SW gateway similar, just the other way around

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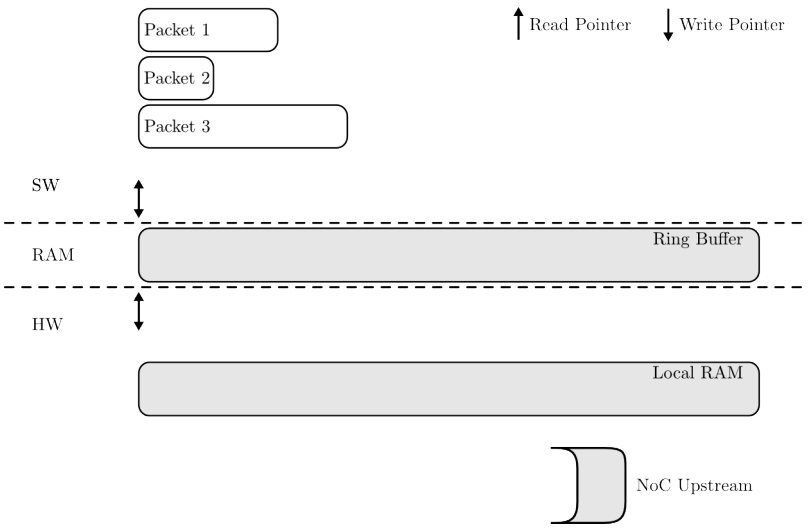
Software to Hardware Gateway



Demonstration des SW to HW gateways

SW hat 3 Pakete zu senden

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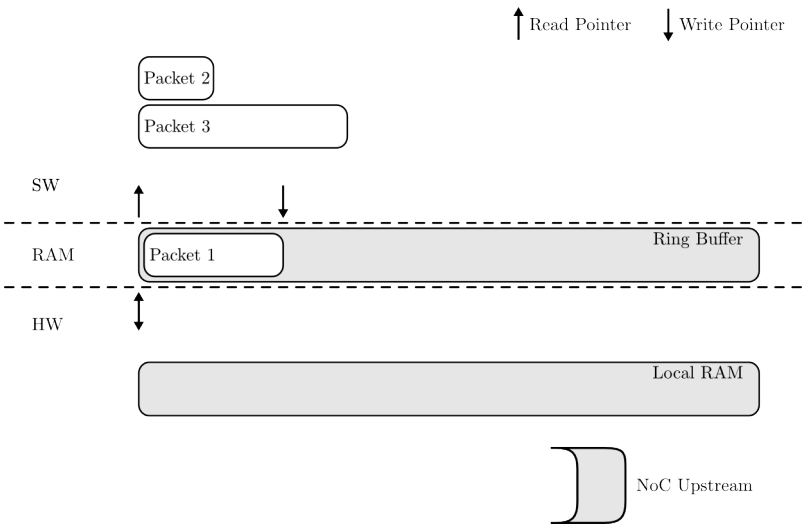

Packet 1 in Ring Buffer geschrieben

Write Pointer erhöht

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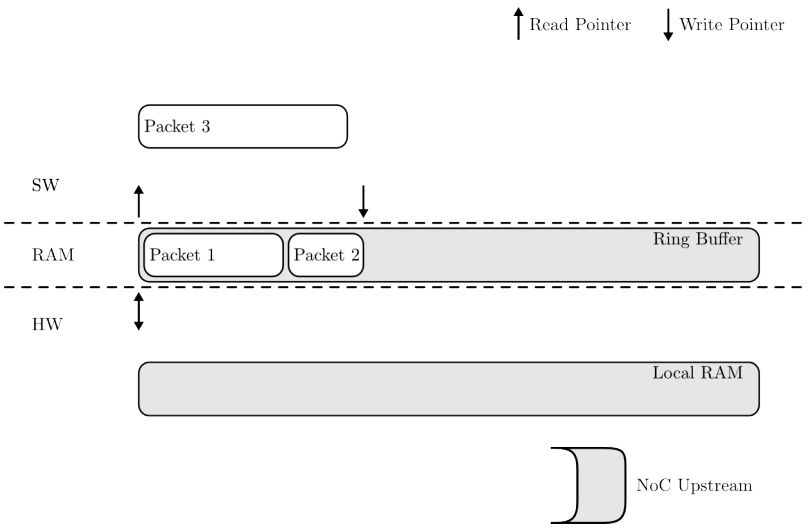

Packet 2 in Ring Buffer geschrieben

Write Pointer erhöht

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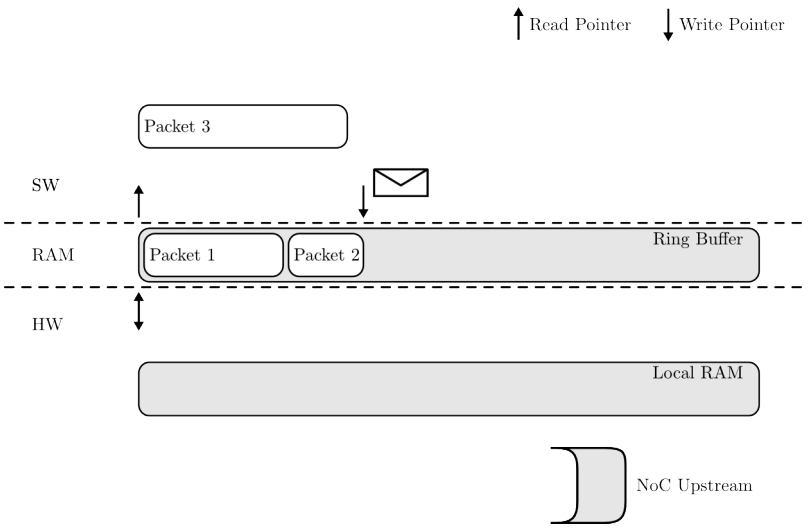
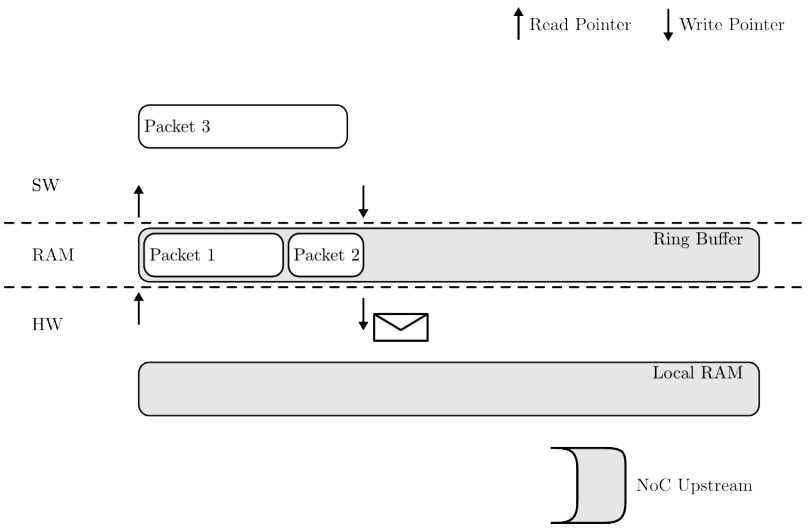


Entschieden (aus irgendeinem Grund, dazu später mehr) dass der Write Pointer an die HW geschickt werden soll



Nachricht mit write pointer bei HW angekommen

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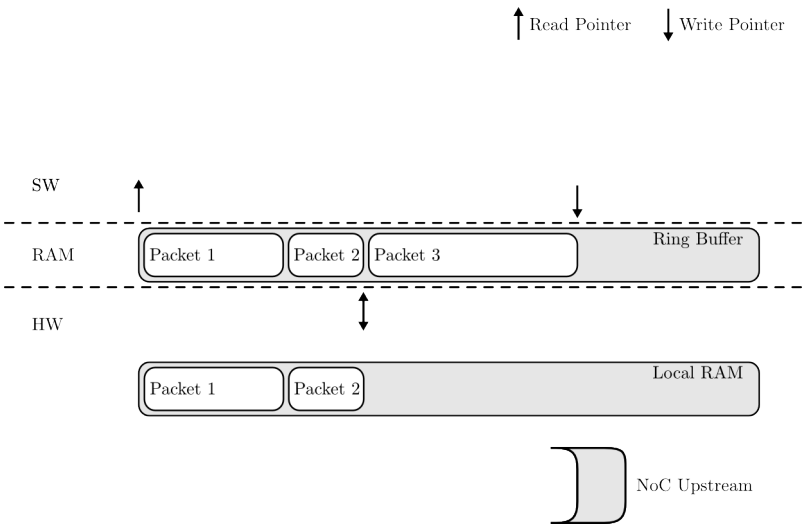

HW kopiert gültige Daten ins lokale RAM

SW schreibt Packet 3 in Ring Buffer

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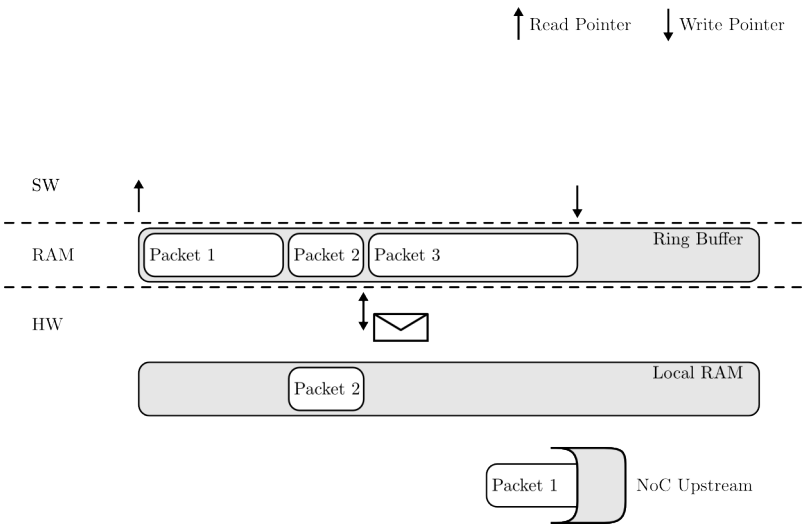

HW ist fertig mit kopieren und schickt read pointer an SW

HW liest Packet 1 vom lokalen RAM und schreibt es ins NoC Interface

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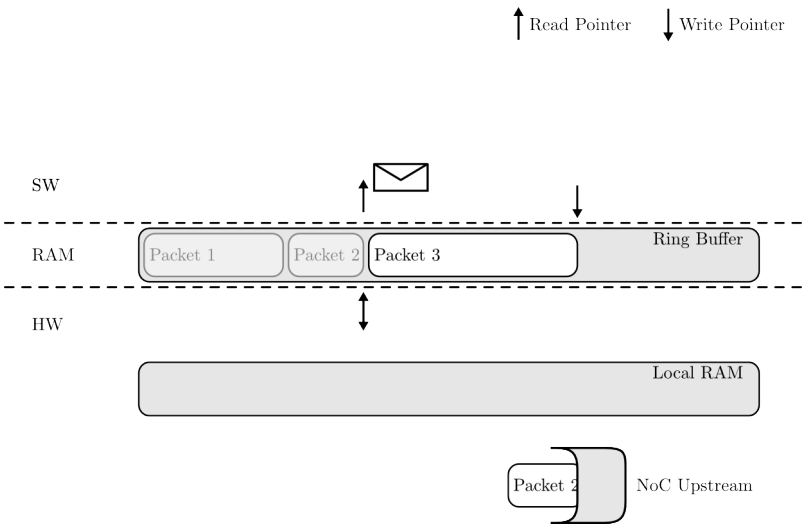

Nachricht mit read pointer kommt bei SW an → Pakete vor read pointer werden ungültig

HW schreibt Packet 2 ins NoC Interface

usw....

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