Xilinx VU9P FPGA, 240 MHz clock cycle, initial interval = 1, 10 bit precision (5 bits for int part)

Model	Python AUC	HLS AUC	Latency (clk)	LUT %	FF %	DSP %
NN	0.985	0.982	8	0.104	0.029	0.292
GBDT	0.986	0.981	3	0.140	0.027	0.0