ECE 3056
Lab 2 – Cache Simulator
Extra Credit – Implementation of I cache, D cache, and L2 cache.
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In order to implement the desired behavior, I expand the previous cache simulator in order to add an extra layer of memory. The base code of the data structure cache_struct with associated arrays for tags, valid bits, dirty bits, and LRU counter now represents the layer L2. The Firs Layer is implemented also using dynamically allocated array of structures, but with being a direct map if doesn't need to have arrays instantiated inside of the structure. Moreover, the field LRU is now irrelevant, yielding in a structure of booleans and integers: tag (int), validBit (boolean), dirtyBit (boolean).

The application outputs Local and Global miss rates, as well as hits and misses for the individual pieces of hardware. In order to check for correct implementation the following equation was used:

$$D_{miss} + I_{miss} = L2_{miss} + L2_{hit}$$

The formula is derived bellow.