ARQUITECTURAS DE ALTO DESEMPENHO

Ano lectivo de 2022/2023

1. GENERAL INFO

Semester: 1
Weekly load: 1H (lecture) + 2H (lab)
Credit units: 6 *ECTS*
Audience: Mestrado em Engenharia de Computadores e Telemática (*MECT*)
Scientific area / sub-area: Informática / Arquitectura dos Sistemas Computacionais
Course coordination: António Rui Borges (*ARB*) – ruib@det.ua.pt

2. TEACHING STAFF

António Rui Borges (*ARB*) – ruib@det.ua.pt
L 2.ª feira: 10h – 11h (Anf. V)
LC1 2.ª feira: 14h – 16h (Room 101)
LC2 2.ª feira: 16h – 18h (Room 101)
LC3 3.ª feira: 9h – 11h (Room 101)
LC4 3.ª feira: 11h – 13h (Room 101)
Tutorial 2.ª feira: 18h – 19h (Anf. V)
Further student assistance is available by appointment (IEETA)

3. OBJECTIVES

- to introduce the most relevant design concepts present in recent generations of processors and how they affect the performance of a computer system
- to describe the organization of the memory hierarchy, in particular cache and virtual memory
- to get acquainted with computer architecture simulation tools and how they can be used to assess performance.

4. LEARNING OUTCOMES

- to understand the architecture and the most important decisions taken on the design of modern processors and how they affect program execution
- to be able to plan and carry out a set of simulations for testing different processor configurations.

5. PREREQUISITES

- good operating knowledge on digital circuit design
- basic notions on computer architecture and on communication protocols with input-output devices (pooled I/O, interrupt driven I/O and DMA based I/O)
- programming skills in C Language and VHDL at a fair to good level.

6. SYLLABUS

1. Fundamentals of quantitative design and analysis of processors.
2. Pipelined processors organization and limitations to their operation.
3. Memory hierarchy: cache memory and virtual memory.
4. Exploitation of parallelism at the instruction level: advanced techniques for branch prediction, static and dynamic scheduling, speculative processing, multi-instruction issue.
5. Exploitation of parallelism at the task level: multithreading and multiprocessors.
6. Exploitation of parallelism at the data level: vector and graphic (GPUs) processors.

7. MAIN BIBLIOGRAPHY

- J. Hennessy, D. A. Patterson, “Computer Architecture – a Quantitative Approach”, 6th Edition, Morgan Kaufmann, 2017
- W. Stallings, “Computer Organization and Architecture – Designing for Performance”, 10th Edition, Pearson Education, 2016
- D. B. Kirk, W. W. Hwu, “Programming Massively Parallel Processors: A Hands-on Approach”, Morgan Kaufmann, 2017

8. TEACHING / LEARNING MODEL

The course is organized in lectures, lab classes and tutorials.

Lectures present specific topics of the syllabus. The adopted approach tries to entice the students to participate actively in the discussion and to help them to develop skills of critical reasoning and to learn general techniques of problem solving. A challenge is placed to the students in the form of an open problem and its solution by individuals is supported (whoever does it, will get a bonus on the grade of the theoretical component).

Lab classes follow the motto "you learn by doing" and aim the completion of small tasks to prepare the students for the work assignments.

***Work assignment* 1 – Digital circuitry simulation**
Implementing and evaluating specific features in a pipelined architecture.

***Work assignment* 2 – CUDA / OpenCl programming**
Solving a computer intensive task on a GPU architecture.

Students are organized in working groups composed of two elements. Each group must present and defend its own solution to the proposed problems.

Tutorials have for the most part an expositive character and aim to help some of the students to overcome deficiencies in background knowledge as well as to provide a space for the discussion of specific aspects of the course.

Themes to be treated include

Digital circuitry modelling

CUDA programming.

9. GRADING

1. Course grade is determined by the formula

$$course\ grade \;=\; \frac{5 \text{ x } theoretical\ mark \;+\; 5 \text{ x } lab\ mark}{10}\ ,$$

rounding is always carried out *half up* to unities, except when the lab mark is higher than the theoretical mark by more than three units; in this case, rounding is carried out *half down*

2. Theoretical mark is obtained by seating to a written examination which takes place at *época normal* or at *época de recurso* and, optionally, by giving a good answer to the challenge placed during the lectures.

3. Lab mark is obtained by the evaluation of the two work assignments. Each has an equal weight. The lab mark is limited to 17 units: a higher grade requires an additional assignment.

4. The student *passes* the course if the course grade is higher or equal to 10 units.

5. The student *fails* the course if the course grade is lower than 10 units.

10. SPECIAL DATES

deadline for delivering work assignment 1: November 13, 2022

deadline for delivering work assignment 2: January 2, 2023