# 12.2 Control Registers

PORTA REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, TABLE 12-1: PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

ess										Ві	ts								
Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	TDIOA	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6000	TRISA	15:0	TRISA15	TRISA14	_	_	_	TRISA10	TRISA9	_	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
6010	PORTA	31:16	-	_	-	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
6010	FURIA	15:0	RA15	RA14	1	-	ı	RA10	RA9	_	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6020	LATA	31:16		_		_	_	-	_	_	1	_	_	_	_	_	_	_	0000
6020	LAIA	15:0	LATA15	LATA14		_	_	LATA10	LATA9	_	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6030	ODCA	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0030	ODCA	15:0	ODCA15	ODCA14	_	_	_	ODCA10	ODCA9	_	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

### TABLE 12-2: PORTB REGISTER MAP

SS										В	its								S I
Virtual Addres (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0040	TDICD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6040	TRISB	15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6050	PORTB	31:16	_	ı	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0030	FORIB	15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
6060	LATB	31:16	_	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	LAID	15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
6070	ODCB	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6070	ODCB	15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

PIC32MX5XX/6XX/7XX

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information. Note 1:

PORTC REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, **TABLE 12-3**: PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

ess		•								Bi	ts								
Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	TRISC	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6080	TRISC	15:0	TRISC15	TRISC14	TRISC13	TRISC12	_	_	_	_	_	_	_	-	_	_	_	_	F000
6090	PORTC	31:16	_	_	_	-	_	_	_	_	_	_	_	-	_	_	_	_	0000
6090	PURIC	15:0	RC15	RC14	RC13	RC12	ı	ı	I	1	_	I	_	_	1	_	_	_	xxxx
60A0	LATC	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
60A0	LAIC	15:0	LATC15	LATC14	LATC13	LATC12	_	_	_	_	_	_	_	-	_	_	_	_	xxxx
60B0	ODCC	31:16	_	ı	_	_	ı	ı	I	1	_	I	_	_	1	_	_	_	0000
0000	ODCC	15:0	ODCC15	ODCC14	ODCC13	ODCC12	_	_	_	_	_	_	_	_	_	_	_	_	0000

PIC32MX5XX/6XX/7XX

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

**TABLE 12-4**: PORTC REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

SSe										Ві	ts								
Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000	TDIOO	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6080	TRISC	15:0	TRISC15	TRISC14	TRISC13	TRISC12	_	_	_	_	_	_	_	TRISC4	TRISC3	TRISC2	TRISC1	_	FOOF
6000	PORTC	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	-	_	0000
0090	FURIC	15:0	RC15	RC14	RC13	RC12	1	-	_	1	_	_	1	RC4	RC3	RC2	RC1	_	xxxx
0040	LATO	31:16		_	_	_	_	_	_	_	_	_	-	_	_	_		_	0000
60A0	LATC	15:0	LATC15	LATC14	LATC13	LATC12	_	_	_	_	_	_	-	LATC4	LATC3	LATC2	LATC1	_	xxxx
CODO	0000	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
60B0	ODCC	15:0	ODCC15	ODCC14	ODCC13	ODCC12	-	-	_	-	_	_	-	ODCC4	ODCC3	ODCC2	ODCC1	_	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

#### PORTD REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

ess										В	its								S.
Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
	TRIOR	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
60C0	TRISD	15:0	_	_	_	_	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	OFFF
CODO	PORTD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6000	PORID	15:0	_	_	_	_	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
OUEU	LAID	15:0	_	_	_	_	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	_	_	_	_	_	ı	_	ı	_	_	_	_	_	ı	1	_	0000
OUFU	ODCD	15:0	_	_	_	_	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

= unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information. Note 1:

TABLE 12-6: PORTD REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

ess		•								Bi	ts								
Virtual Address (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	TRISD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
60C0	IKISD	15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
6000	PORTD	31:16	_	_	ı	_	ı	_	ı	_	ı	ı	ı	ı	ı	_	_	1	0000
6000	FORID	15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	_	_	-	_	-	_	1	_	1	-	-	1	1	_	_	-	0000
OUEU	LAID	15:0	LAT15	LAT14	LAT13	LAT12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	ODCD	15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

PIC32MX5XX/6XX/7XX

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information. Note 1:

### PORTE REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, **TABLE 12-7:** PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX775F512H AND PIC32MX795F512H DEVICES

ess										В	its								
Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6100	TRISE	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6100	IRISE	15:0	ı	ı	_	_	_	_	_	_	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	OOFF
6110	PORTE	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0110	PORTE	15:0	_	_	_	_	_	_	_	_	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0120	LAIE	15:0	_	_	_	_	_	_	_	_	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	ı	ı	_	_	_	_	_	_	_	ı	_	1	_	_	_	ı	0000
0130	ODCE	15:0	_	_	_	_	_	_	_	_	ODCE7	0DCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

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Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

## **TABLE 12-8:** PORTE REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX775F512L AND PIC32MX795F512L DEVICES

ess		ø.								Ві	ts								"
Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	TRIOF	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6100	TRISE	15:0	_	_	_	_	_	_	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0440	PORTE	31:16			_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6110	PURIE	15:0	_	_	_	_	-	-	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0400	LATE	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6120	LAIE	15:0			_	_	_	_	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
C420	ODGE	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6130	ODCE	15:0	_	_	_	_	-	-	ODCE9	ODCE8	ODCE7	0DCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.