*Arquitecturas de Alto Desempenho*
*Teste 1*

*20 de Janeiro de 2023*

## *Part 1* (4 *points*)

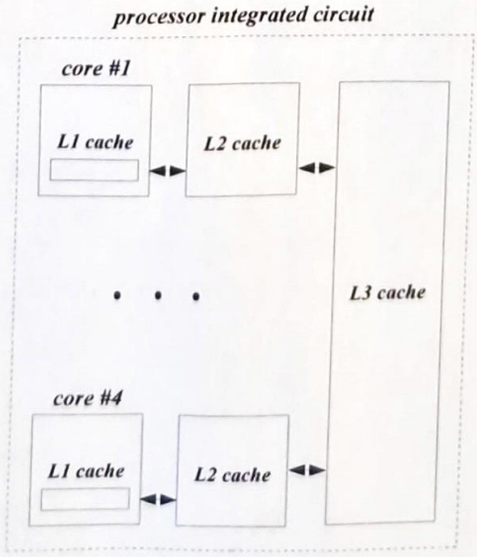
1. Assume a memory subsystem with 30 address lines. (2 points)
   i. How many bytes and double-words can be stored in it? Justify your claims in detail.
   ii. Give two examples of valid addresses (in hexadecimal form) for bytes and double-words stored in the second quarter of its addressing space. Justify your claims in detail.
2. State the law of Amdhal. What is the maximum speed up that can be achieved in running a given application in a 4-core processor if 80% of it may be parallelized? Justify your claims in detail. (2 points)

## *Part 2* (4 *points*)

3. *Pipelining* is a technique universally used nowadays to speed up program execution in a processor. However, if one looks carefully, single instructions are not executed faster, so how the speed up of program execution is actually achieved? Justify your claims in detail. (2 points)
4. For pipelining to be really effective, that is, approaching as much as possible the nominal throughput in normal operation, one has to deal with hazard resolution. Explain in detail what kind of hazards may arise and how they are dealt with for a processor implementing a 5-stage classical pipeline with multiple execution units. (2 points)

## *Part 3* (4 *points*)

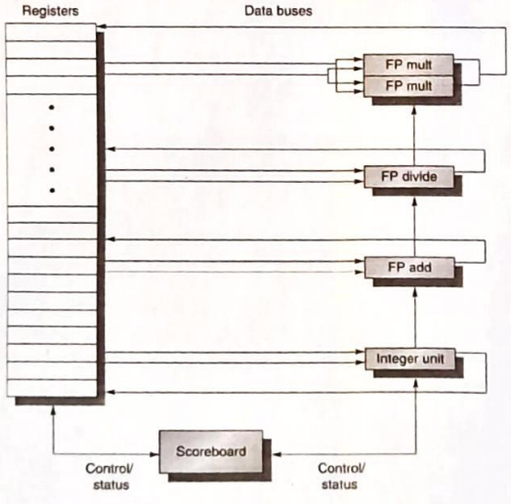
5. The diagram below depicts the cache hierarchy for a 4-core processor. (2 points)




   i. Why three cache levels are typically used?
   ii. Why level 1 is usually divided in an instruction and a data cache?
   iii. What kind of *write policy* is usually applied to them?
6. A cache is typically organized in lines, each capable of storing the contents of a given memory block. A *line*, however, does not store only the contents of the memory block. Other information must be present. Which is it? Justify your claims in detail. (2 points)

## *Part 4* (4 *points*)

7. One basic compiler technique to expose instruction level parallelism is *loop unrolling*. Give an example that illustrates its application. (2 points)
8. The diagram bellow depicts the basic organization of a MIPS processor with a *scoreboard*.




Explain in detail how the different types data hazards are dealt with in this organization and why *scoreboarding* is considered a dynamic scheduling technique. Justify your claims in detail. (2 points)

## *Part 5* (4 *points*)

9. What are the main features of a SIMD architecture? Explain why a *vector* architecture fits in this classification. (1,5 points)
10. What is a *heterogeneous* computer architecture? Describe it in detail. Why is it becoming so popular? (1 point)
11. What is CUDA C? What kind of programming model does it present? (1,5 points)