











SCDS188G - JANUARY 2005 - REVISED JANUARY 2019

TS3A5017

# TS3A5017 Dual SP4T Analog Switch / Multiplexer / Demultiplexer

#### **Features**

- Isolation in the Powered-Down Mode,  $V_{+} = 0$
- Low ON-State Resistance
- Low Charge Injection
- **Excellent ON-State Resistance Matching**
- Low Total Harmonic Distortion (THD)
- 2.3-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 1500-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### **Applications**

- Sample-and-Hold Circuits
- **Battery-Powered Equipment**
- Audio and Video Signal Routing
- Communication Circuits

### **Description**

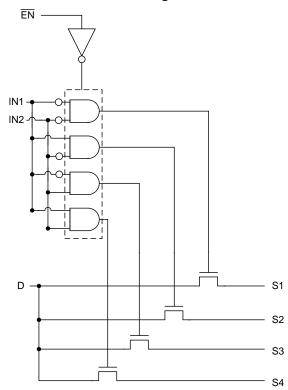
TS3A5017 device is a dual single-pole quadruple-throw (4:1) analog switch that is designed to operate from 2.3 V to 3.6 V. This device can handle both digital and analog signals, and signals up to V<sub>+</sub> can be transmitted in either direction.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	SOIC (16)	9.90 mm × 3.90 mm
	SSOP (16)	4.90 mm × 3.90 mm
T0045047	TSSOP (16)	5.00 mm × 4.40 mm
TS3A5017	TVSOP (16)	4.40 mm × 3.60 mm
	UQFN (16)	2.50 mm × 1.80 mm
	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **Block Diagram**





Ta	h	۵۱	Ωf	$C \cap$	nte	nte
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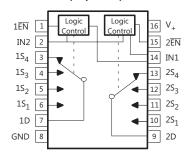
# 4 Revision History

Ch	anges from Revision F (October 2018) to Revision G	Page
•	Changed Feature From: 2000-V Human-Body Model To: 1500-V Human-Body Model	1
•	Changed the HBM value From: ±2000 V To: ±1500 V in the ESD Ratings	4
Ch	nanges from Revision E (April 2015) to Revision F	Page
•	Changed the X <sub>TALK</sub> MAX value From:–49 dB To – 69 dB in the <i>Electrical Characteristics for 3.3-V Supply</i>	6
Ch	nanges from Revision D (December 2008) to Revision E	Page
•	Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	
•	Deleted Ordering Information table	1

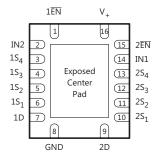


# 5 Pin Configuration and Functions

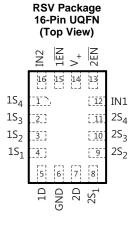
D, DBQ, DGV, and PW Package 16-Pin SOIC, SSOP, TVSOP and TSSOP (Top View)



#### RGY Package 16-Pin VQFN (Top View)



If exposed center pad is used, it must be connected as a secondary ground or left electrically open.



#### **Pin Functions**

	PIN			
NAME	SOIC, SSOP, TVSOP, TSSOP, VQFN NO.	UQFN NO.	TYPE	DESCRIPTION
1D	7	5	I/O	Common path for switch 1
1 <del>EN</del>	1	15	I	Active-low enable for switch 1
1S1	6	4	I/O	Switch 1 channel 1
1S2	5	3	I/O	Switch 1 channel 2
1S3	4	2	I/O	Switch 1 channel 3
1S4	3	1	I/O	Switch 1 channel 4
2D	9	7	I/O	Common path for switch 2
2 <del>EN</del>	15	13	I	Active-low enable for switch 2
2S1	10	8	I/O	Switch 2 channel 1
2S2	11	9	I/O	Switch 2 channel 2
2S3	12	10	I/O	Switch 2 channel 3
2S4	13	11	I/O	Switch 2 channel 4
GND	8	6	_	Ground
IN1	14	12	I	Switch 1 input select
IN2	2	16	I	Switch 2 input select
V+	16	14	_	Supply voltage



### 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage <sup>(3)</sup>		-0.5	4.6	V
V <sub>S</sub> , V <sub>D</sub>	Analog voltage <sup>(3)(4)</sup>		-0.5	4.6	V
I <sub>SK</sub> , I <sub>DK</sub>	Analog port clamp current	V <sub>S</sub> , V <sub>D</sub> < 0	-50		mA
I <sub>S</sub> , I <sub>D</sub>	ON-state switch current	$V_S$ , $V_D = 0$ to 7 V	-128	128	mA
$V_{I}$	Digital input voltage		-0.5	4.6	V
I <sub>IK</sub>	Digital input clamp current <sup>(3)(4)</sup>	V <sub>I</sub> < 0	-50		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>			100	mA
$I_{\text{GND}}$	Continuous current through GND	·	-100		mA
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### 6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage range	0	3.6	V
V+	Supply voltage range	2.3	3.6	V
VI	Control input voltage range	0	3.6	V
T <sub>A</sub>	Operating Temperature Range	-40	85	°C

#### 6.4 Thermal Information

			TS3A5018					
THERMAL METRIC $^{(1)}$ $R_{\theta JA}$ Junction-to-ambient thermal resistance		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	RSV (UQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
		73	82	120	108	91.6	184	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



### 6.5 Electrical Characteristics for 3.3-V Supply

 $V_{\rm c} = 2.7 \text{ V}$  to 3.6 V.  $T_{\rm c} = -40 \,^{\circ}\text{C}$  to 85°C (unless otherwise noted)<sup>(1)</sup>

PAR	AMETER	TEST COI	NDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Swit	tch								
V <sub>D</sub> , V <sub>S</sub>	Analog signal range					0		V <sub>+</sub>	V
r <sub>on</sub>	ON-state resistance	$0 \le V_S \le V_+,$ $I_D = -32 \text{ mA},$	Switch ON, see Figure 12	25°C Full	3 V		11	12 14	Ω
	ON-state			25°C			1	2	
$\Delta r_{\sf on}$	resistance match between channels	$V_S = 2.1 \text{ V},$ $I_D = -32 \text{ mA},$	Switch ON, see Figure 12	Full	3 V			3	Ω
	ON-state	$0 \le V_S \le V_+$	Switch ON,	25°C			7	9	
r <sub>on(flat)</sub>	resistance flatness	$I_D = -32 \text{ mA},$	see Figure 12	Full	3 V			10	Ω
		$V_S = 1 \ V, \ V_D = 3 \ V,$		25°C		-0.1	0.05	0.1	
I <sub>S(OFF)</sub>	S OFF leakage	or $V_S = 3 \text{ V}, V_D = 1 \text{ V},$	Switch OFF,	Full	3.6 V	-0.2		0.2	μΑ
	current	$V_S = 0 \text{ to } 3.6 \text{ V},$	see Figure 13	25°C	0.17	-1	0.5	1	μι
I <sub>SPWR(OFF)</sub>		$V_D = 3.6 \text{ V to } 0,$		Full	0 V	-5		5	
		$V_S = 1 \text{ V}, V_D = 3 \text{ V},$		25°C		-0.1	0.05	0.1	
$I_{D(OFF)}$	D OFF leakage	or $V_S = 3 \text{ V}, V_D = 1 \text{ V},$	Switch OFF,	Full	3.6 V	-0.2		0.2	^
	current	$V_D = 0 \text{ to } 3.6 \text{ V},$	see Figure 13	25°C	0.17	-1	0.5	1	μΑ
I <sub>DPWR(OFF)</sub>		$V_S = 3.6 \text{ V to } 0,$		Full	0 V	-5	;	5	
	S	$V_S = 1 V$ , $V_D = Open$ ,	Switch ON	25°C		-0.1	0.05	0.1	
I <sub>S(ON)</sub>	ON leakage current	or $V_S = 3 \text{ V}, V_D = \text{Open},$	Switch ON, see Figure 14	Full	3.6 V	-0.2		0.2	μΑ
	D	$V_D = 1 \text{ V}, V_S = \text{Open},$	Conitate ON	25°C		-0.1	0.05	0.1	
$I_{D(ON)}$	ON leakage current	or $V_D = 3 V$ , $V_S = Open$ ,	Switch ON, see Figure 14	Full	3.6 V	-0.2		0.2	μΑ
Digital Cont	rol Inputs (IN1, IN								
$V_{IH}$	Input logic high			Full		2		V <sub>+</sub>	V
$V_{IL}$	Input logic low			Full		0		0.8	V
	Input leakage	., ., .		25°C	0.014	-1	0.05	1	
$I_{IH}$ , $I_{IL}$	current	$V_I = V_+ \text{ or } 0$		Full	3.6 V	-1		1	μΑ
$Q_{C}$	Charge injection	$\begin{aligned} &V_{GEN}=0,R_{GEN}=0,\\ &C_L=0.1\;nF, \end{aligned}$	See Figure 21	25°C	3.3 V		5		рС
C <sub>S(OFF)</sub>	S OFF capacitance	V <sub>S</sub> = V <sub>+</sub> or GND, Switch OFF,	See Figure 15	25°C	3.3 V		4.5		pF
$C_{D(OFF)}$	D OFF capacitance	V <sub>D</sub> = V <sub>+</sub> or GND, Switch OFF,	See Figure 15	25°C	3.3 V		19		pF
C <sub>S(ON)</sub>	S ON capacitance	V <sub>S</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 15	25°C	3.3 V		25		pF
C <sub>D(ON)</sub>	D ON capacitance	V <sub>D</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 15	25°C	3.3 V		25		pF
Cı	Digital input capacitance	$V_I = V_+ \text{ or GND},$	See Figure 15	25°C	3.3 V		2		pF
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON,	See Figure 17	25°C	3.3 V		165		MHz
O <sub>ISO</sub>	OFF isolation	$R_L = 50 \Omega$ , $f = 1 MHz$ ,	See Figure 18	25°C	3.3 V		-69		dB

 <sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



### **Electrical Characteristics for 3.3-V Supply (continued)**

 $V_{+}$  = 2.7 V to 3.6 V,  $T_{A}$  = -40°C to 85°C (unless otherwise noted)<sup>(1)</sup>

PAR	AMETER	TEST C	CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN TYP N	IAX	UNIT
X <sub>TALK</sub>	Crosstalk	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 19	25°C	3.3 V	69		dB
X <sub>TALK(ADJ)</sub>	Crosstalk adjacent	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 20	25°C	3.3 V	-74		dB
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, see Figure 22	25°C	3.3 V	0.21%		
Supply								
	Positive supply	$V_1 = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	2.5	7	^
1+	current	$V_1 = V_+ \text{ OI GIND},$	SWILCH ON OF OFF	Full	3.0 V		10	μΑ

### 6.6 Electrical Characteristics for 2.5-V Supply

 $V_{+} = 2.3 \text{ V}$  to 2.7 V,  $T_{\Delta} = -40 ^{\circ}\text{C}$  to 85  $^{\circ}\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PA	RAMETER	TEST CO	NDITIONS	TA	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Swit	ch			_					
V <sub>D</sub> , V <sub>S</sub>	Analog signal range					0		V <sub>+</sub>	V
r <sub>on</sub>	ON-state resistance	$0 \le V_S \le V_+,$ $I_D = -24 \text{ mA},$	Switch ON, see Figure 12	25°C Full	2.3 V		20.5	22 24	Ω
$\Delta r_{\sf on}$	ON-state resistance match	$V_S = 1.6 \text{ V},$ $I_D = -24 \text{ mA},$	Switch ON, see Figure 12	25°C Full	2.3 V		1	2	Ω
r <sub>on(flat)</sub>	ON-state resistance flatness	$0 \le V_S \le V_+,$ $I_D = -24 \text{ mA},$	Switch ON, see Figure 12	25°C	2.3 V		16	18	Ω
		$V_S = 0.5 \text{ V}, V_D = 2.2 \text{ V},$	000 1 19410 12	Full 25°C		-0.1	0.05	0.1	
I <sub>S(OFF)</sub>	S OFF leakage	or $V_S = 2.2 \text{ V}, V_D = 0.5 \text{ V},$	Switch OFF, see Figure 13	Full	2.7 V	-0.2		0.2	μΑ
I <sub>SPWR(OFF)</sub>	current	$V_S = 0 \text{ to } 2.7 \text{ V},$ $V_D = 2.7 \text{ V to } 0,$	see Figure 13	25°C Full	0 V	-1 -5	0.5	1 5	·
		$V_S = 0.5 \text{ V}, V_D = 2.2 \text{ V},$		25°C		-0.1	0.05	0.1	μА
I <sub>D(OFF)</sub>	D OFF leakage	$V_S = 2.2 \text{ V}, V_D = 0.5 \text{V},$	Switch OFF, see Figure 13	Full	2.7 V	-0.2		0.2	
I <sub>DPWR(OFF)</sub>	current	$V_D = 0 \text{ to } 2.7 \text{ V},$ $V_S = 2.7 \text{ V to } 0,$	see rigure 13	25°C Full	0 V	-1 -5	0.5	1 5	
I <sub>S(ON)</sub>	S ON leakage	$V_S = 0.5 \text{ V}, V_D = \text{Open},$ or	Switch ON, see Figure 14	25°C Full	2.7 V	-0.1 -0.2	0.05	0.1	μА
	current D	$V_S = 2.2 \text{ V}, V_D = \text{Open},$ $V_D = 0.5 \text{ V}, V_S = \text{Open},$	Switch ON,	25°C		-0.1	0.05	0.2	
$I_{D(ON)}$	ON leakage current	or $V_D = 2.2 \text{ V}, V_S = \text{Open},$	see Figure 14	Full	2.7 V	-0.2		0.2	μΑ
Digital Cont	rol Inputs (IN1, IN2,	EN) <sup>(2)</sup>							
$V_{IH}$	Input logic high			Full		1.7		$V_{+}$	V
$V_{IL}$	Input logic low			Full		0		0.7	V
$I_{IH},\ I_{IL}$	Input leakage current	$V_I = V_+ \text{ or } 0$		25°C Full	2.7 V	-1 -1	0.05	1	μΑ
Q <sub>C</sub>	Charge injection	$V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,$	See Figure 21	25°C	2.5 V			•	рС
C <sub>S(OFF)</sub>	S OFF capacitance	V <sub>S</sub> = V <sub>+</sub> or GND, Switch OFF,	See Figure 15	25°C	2.5 V		4.5		pF

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

<sup>(2)</sup> All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



### **Electrical Characteristics for 2.5-V Supply (continued)**

 $V_{+} = 2.3 \text{ V to } 2.7 \text{ V}, T_{A} = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C} \text{ (unless otherwise noted)}^{(1)}$ 

PARAMETER		TEST	T CONDITIONS	TA	V <sub>+</sub>	MIN TYP N	MAX	UNIT	
C <sub>D(OFF)</sub>	D OFF capacitance	$V_D = V_+ \text{ or GND},$ Switch OFF,	See Figure 15	25°C	2.5 V	18.5		pF	
C <sub>S(ON)</sub>	S ON capacitance	$V_S = V_+ \text{ or GND},$ Switch ON,	See Figure 15	25°C	2.5 V	24		pF	
C <sub>D(ON)</sub>	D ON capacitance	$V_D = V_+ \text{ or GND},$ Switch ON,	See Figure 15	25°C	2.5 V	24		pF	
C <sub>I</sub>	Digital input capacitance	$V_I = V_+ \text{ or GND},$	See Figure 15	25°C	2.5 V	2		pF	
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON,	See Figure 17	25°C	2.5 V	165		MHz	
O <sub>ISO</sub>	OFF isolation	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 18	25°C	2.5 V	-69		dB	
X <sub>TALK</sub>	Crosstalk	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 19	25°C	2.5 V	-69		dB	
X <sub>TALK(ADJ)</sub>	Crosstalk adjacent	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 20	25°C	2.5 V	-74		dB	
THD	Total harmonic distortion	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, see Figure 22	25°C	2.5 V	0.29%			
Supply									
	Positive supply	$V_1 = V_+ \text{ or GND},$	Switch ON or OFF	25°C	2.7 V	2.5	7	μА	
I <sub>+</sub>	current	VI = V+ OI GND,	Switch ON OF OFF	Full	2.7 V		10		

### 6.7 Switching Characteristics for 3.3-V supply

over operating free-air temperature range (unless otherwise noted)

	<u> </u>	<u>U</u>							
PAR	RAMETER	TEST CONDITIONS			V <sub>+</sub>	MIN	TYP	MAX	UNIT
		V 2.V	C <sub>L</sub> = 35 pF, see Figure 16		3.3 V	1	5	9.5	
t <sub>ON</sub>	Turnon time	$V_D = 2 V,$ $R_L = 300 \Omega,$			3 V to 3.6 V	1		10.5	ns
	$t_{OFF}$ Turnoff time $V_D = X_L =$	V 2.V	C 25 pF	25°C	3.3 V	0.5	1.5	3.5	
t <sub>OFF</sub>		$V_D = 2 V,$ $R_L = 300 \Omega,$	C <sub>L</sub> = 35 pF, see Figure 16	Full	3 V to 3.6 V	0.5		4.5	ns

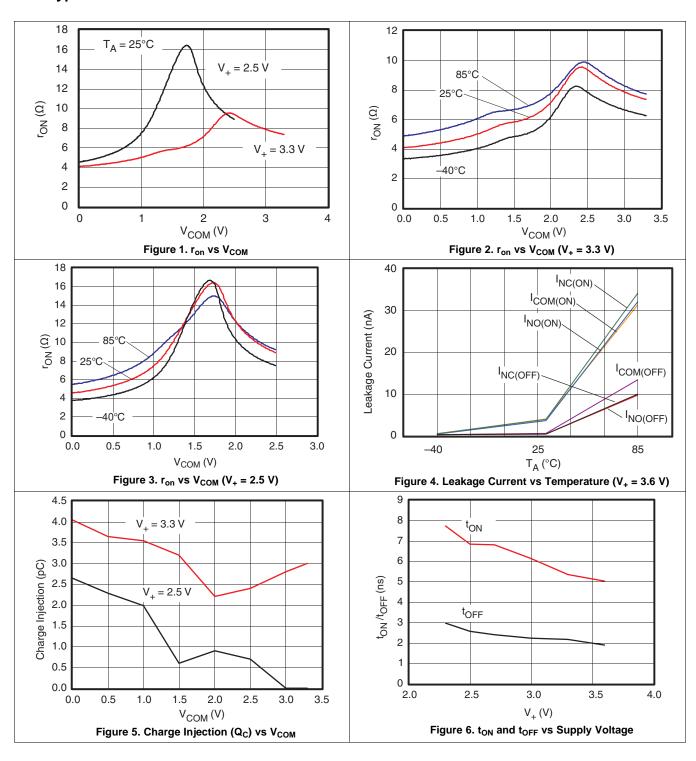
### 6.8 Switching Characteristics for 2.5-V supply

over operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS			V <sub>+</sub>	MIN	TYP	MAX	UNIT
		V 2.V	C 25 pF	25°C	2.5 V	1.5	5	8	
t <sub>ON</sub>	Turnon time	$V_{COM} = 2 V$ , $R_L = 300 \Omega$ ,	C <sub>L</sub> = 35 pF, see Figure 16	Full	2.3 V to 2.7 V	1		10	ns
		V 2V	C 25 pF	25°C	2.5 V	0.3	2	4.5	
t <sub>OFF</sub>	Turnoff time	$V_{COM} = 2 V$ , $R_L = 300 \Omega$ ,	C <sub>L</sub> = 35 pF, see Figure 16	Full	2.3 V to 2.7 V	0.3		6	ns

# TEXAS INSTRUMENTS

#### 6.9 Typical Characteristics

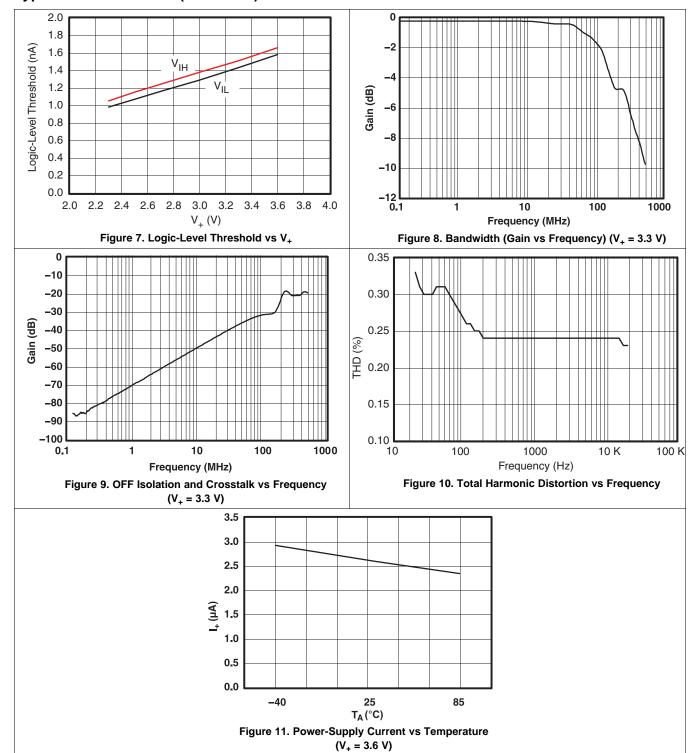


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### **Typical Characteristics (continued)**



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#### 7 Parameter Measurement Information

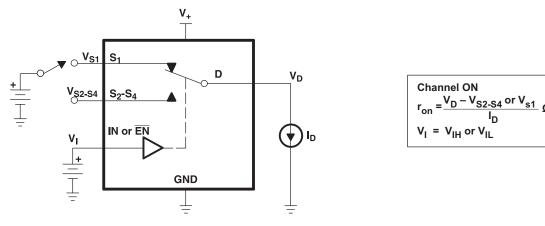


Figure 12. ON-State Resistance (ron)

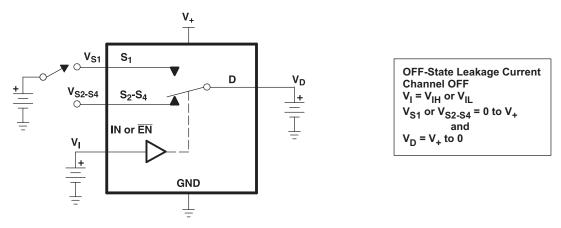


Figure 13. OFF-State Leakage Current ( $I_{D(OFF)}$ ,  $I_{S(OFF)}$ )

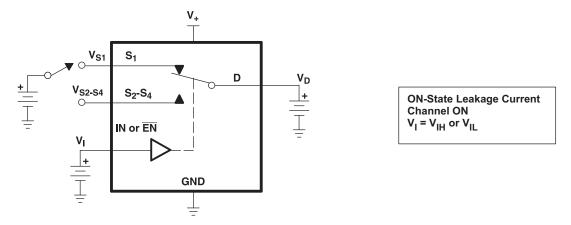
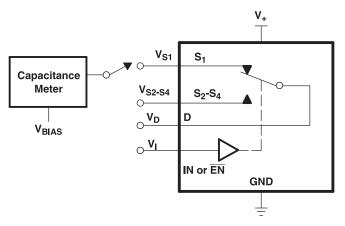


Figure 14. ON-State Leakage Current (I<sub>D(ON)</sub>, I<sub>S(ON)</sub>)



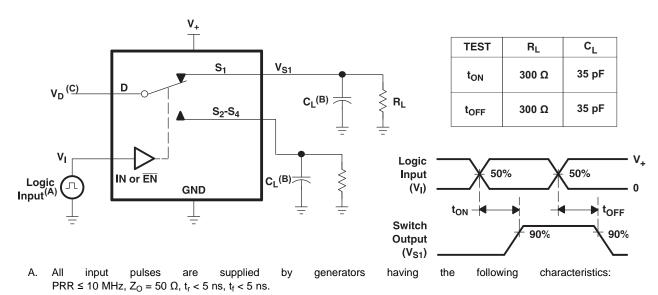
#### **Parameter Measurement Information (continued)**



$$V_{BIAS} = V_{+}$$
 to GND  $V_{I} = V_{IH}$  or  $V_{IL}$ 

Capacitance is measured at S1, S2-S4, D, and IN inputs during ON and OFF conditions.

Figure 15. Capacitance (C<sub>I</sub>,  $C_{D(OFF)}$ ,  $C_{D(ON)}$ ,  $C_{S(OFF)}$ ,  $C_{S(ON)}$ )



- B. C<sub>L</sub> includes probe and jig capacitance.
- C. See Electrical Characteristics for V<sub>D</sub>.

Figure 16. Turnon (ton) and Turnoff Time (toff)

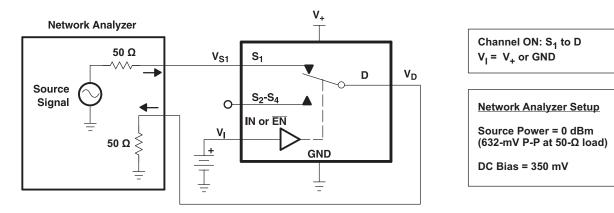
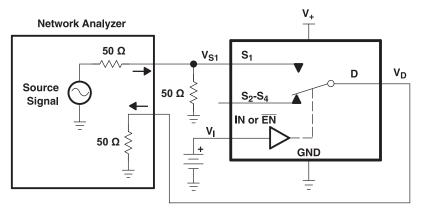


Figure 17. Bandwidth (BW)



### **Parameter Measurement Information (continued)**



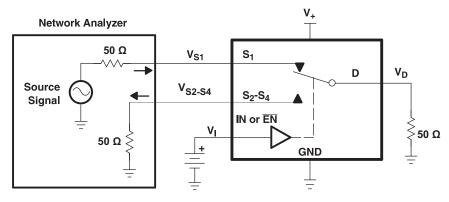
Channel OFF: S to D V<sub>I</sub> = V<sub>+</sub> or GND

**Network Analyzer Setup** 

Source Power = 0 dBm(632-mV P-P at  $50-\Omega$  load)

DC Bias = 350 mV

Figure 18. OFF Isolation (O<sub>ISO</sub>)



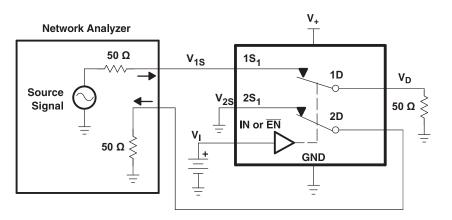
Channel ON:  $S_1$  to D Channel OFF:  $S_2$ - $S_4$  to D  $V_1 = V_+$  or GND

**Network Analyzer Setup** 

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 19. Crosstalk (X<sub>TALK</sub>)



Channel ON: S<sub>1</sub> to D

Network Analyzer Setup

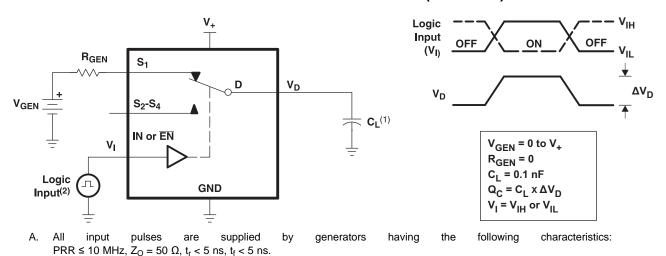
Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 20. Adjacent Crosstalk (X<sub>TALK</sub>)

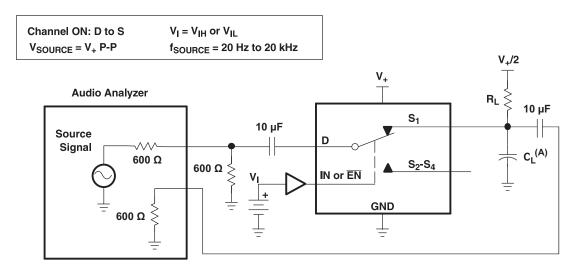


### **Parameter Measurement Information (continued)**



B. C<sub>L</sub> includes probe and jig capacitance.

Figure 21. Charge Injection (Q<sub>C</sub>)



A. C<sub>L</sub> includes probe and jig capacitance.

Figure 22. Total Harmonic Distortion (THD)

### 8 Detailed Description

#### 8.1 Overview

The TS3A5017 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of EN, IN2, and IN1. See Table 1 for the switch configuration truth table.

#### 8.2 Functional Block Diagram

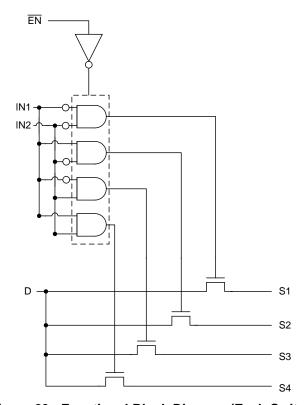


Figure 23. Functional Block Diagram (Each Switch)

#### 8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017 better performance at higher speeds.



### 8.4 Device Functional Modes

**Table 1. Function Table** 

ĒN	IN2	IN1	D TO S, S TO D
L	L	L	$D = S_1$
L	L	Н	D = S <sub>2</sub>
L	Н	L	$D = S_3$
L	Н	Н	D = S <sub>4</sub>
Н	X	X	OFF



#### 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS3A5018 can be used in a variety of customer systems. The TS3A5018 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

### 9.2 Typical Application

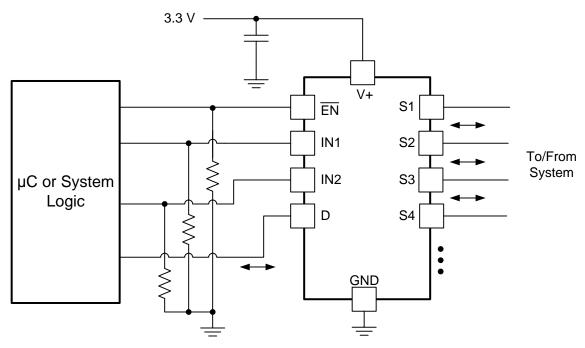


Figure 24. System Schematic for TS3A5017

#### 9.2.1 Design Requirements

In this particular application, V+ was 3.3 V, although V+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

#### 9.2.2 Detailed Design Procedure

In this application,  $\overline{\text{EN}}$ , IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.



#### **Typical Application (continued)**

#### 9.2.3 Application Curve

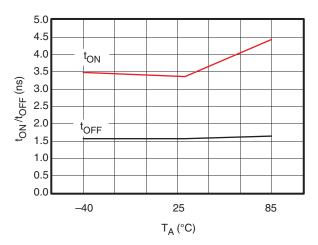


Figure 25.  $t_{ON}$  and  $t_{OFF}$  vs Temperature (V<sub>+</sub> = 3.3 V)

### 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu F$  bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01- $\mu F$  or 0.022- $\mu F$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu F$  bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu F$  and 1- $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 11 Layout

#### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

<u>Un</u>used switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and  $\overline{\text{EN}}$  pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I<sub>CC</sub> or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs*, SCBA004 for more details.



# 11.2 Layout Example

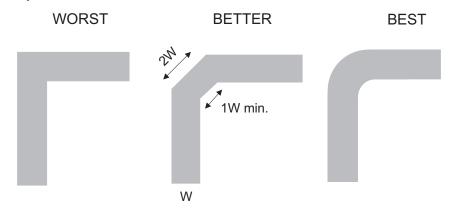


Figure 26. Trace Example



# 12 Device and Documentation Support

# 12.1 Device Support

#### 12.1.1 Device Nomenclature

**Table 2. Parameter Description** 

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NC</sub>	Voltage at NC
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NC or NO ports when the channel is ON
$\Delta r_{on}$	Difference of r <sub>on</sub> between channels in a specific device
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions
I <sub>NC(OFF)</sub>	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
I <sub>NC(ON)</sub>	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN, EN)
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN, EN)
$V_{I}$	Voltage at the control input (IN, $\overline{\text{EN}}$ )
$I_{\rm IH},~I_{\rm IL}$	Leakage current measured at the control input (IN, EN)
t <sub>ON</sub>	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output NC or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
$Q_{\mathbb{C}}$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
C <sub>NC(OFF)</sub>	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C <sub>NC(ON)</sub>	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C <sub>NO(OFF)</sub>	Capacitance at the NC port when the corresponding channel (NO to COM) is OFF
C <sub>NO(ON)</sub>	Capacitance at the NC port when the corresponding channel (NO to COM) is ON
C <sub>COM(OFF)</sub>	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C <sub>I</sub>	Capacitance of control input (IN, EN)
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X <sub>TALK</sub>	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2) .This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.



#### 12.2 Documentation Support

#### 12.2.1 Related Documentation

Implications of Slow or Floating CMOS Inputs, SCBA004

#### 12.3 Trademarks

All trademarks are the property of their respective owners.

#### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





10-Dec-2020

#### PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5017D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5017	Samples
TS3A5017DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	Samples
TS3A5017DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5017	Samples
TS3A5017PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	Samples
TS3A5017RGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	Samples
TS3A5017RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVL	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



#### PACKAGE OPTION ADDENDUM

10-Dec-2020

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF TS3A5017:

Automotive: TS3A5017-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

### PACKAGE MATERIALS INFORMATION

www.ti.com 5-Jan-2021

### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5017DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3A5017DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3A5017DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3A5017PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A5017RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TS3A5017RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

www.ti.com 5-Jan-2021

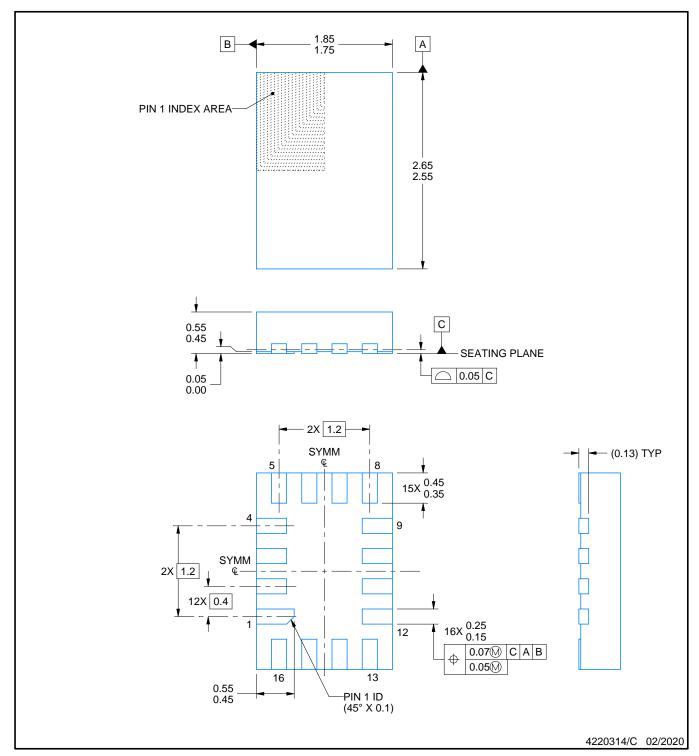


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5017DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TS3A5017DGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
TS3A5017DR	SOIC	D	16	2500	333.2	345.9	28.6
TS3A5017PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
TS3A5017RGYR	VQFN	RGY	16	3000	853.0	449.0	35.0
TS3A5017RSVR	UQFN	RSV	16	3000	200.0	183.0	25.0



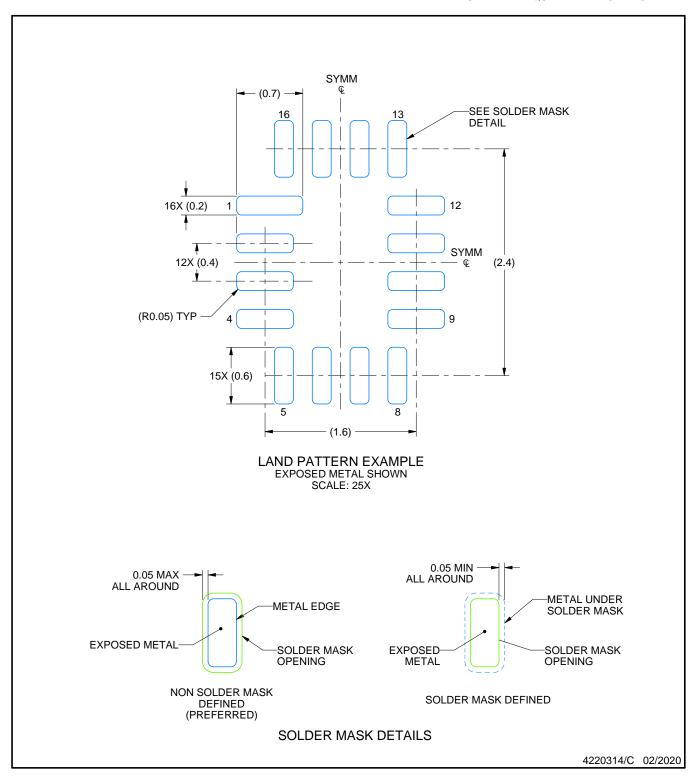
ULTRA THIN QUAD FLATPACK - NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.



ULTRA THIN QUAD FLATPACK - NO LEAD

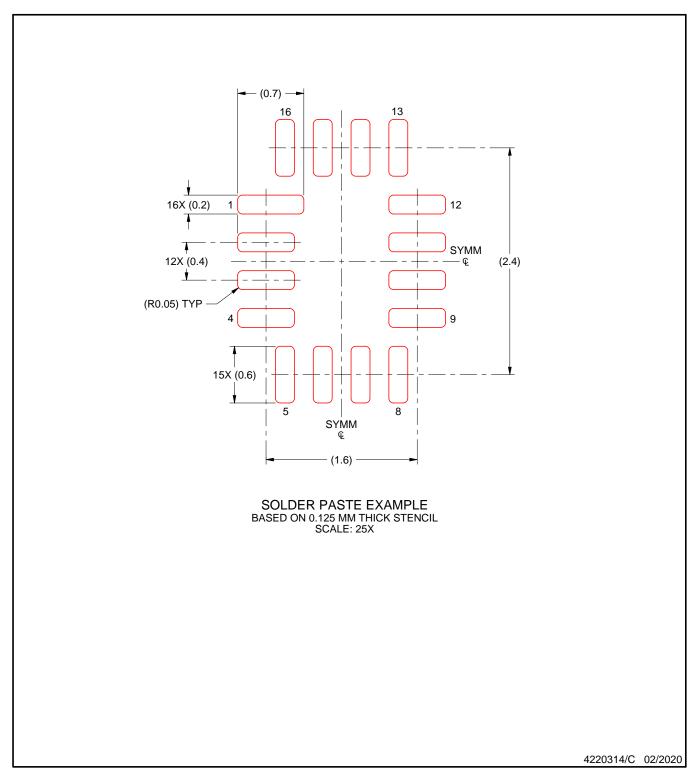


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



ULTRA THIN QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



### DGV (R-PDSO-G\*\*)

#### 24 PINS SHOWN

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



# RGY (R-PVQFN-N16)

#### PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



# RGY (R-PVQFN-N16)

# PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.





SHRINK SMALL-OUTLINE PACKAGE



- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- 4. This dimension does not include interlead flash.5. Reference JEDEC registration MO-137, variation AB.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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