

IO configurations(Min7) – stm32 High Density Device LQFP64

| Compulsory and fixed pin assignments | | | |
|--|-----|--|--|
| Pin name | Pin | Description | Usage |
| V _{SS_1} | 31 | V _{DD} = 2.0 to 3.6V(nominal 3.3V); V _{SS} = 0V Each pair 0.1uF decoupled Overall 1 uF decoupled | These pins are fixed and must be connected as shown. |
| V _{DD_1} | 32 | | |
| V _{SS_2} | 47 | | |
| V _{DD_2} | 48 | | |
| V _{SS_3} | 63 | | |
| V _{DD_3} | 64 | | |
| V _{SS_4} | 18 | | |
| V _{DD_4} | 19 | | |
| V _{SSA} | 12 | V _{DDA} = 2.4 - 3.6V; Must be within ±0.3V of V _{DD} ; ADC supply 0.1uF & 1uF decoupling | |
| V _{DDA} | 13 | | |
| NRST | 7 | Reset input | |
| Boot0 | 60 | Flash/Program select | |
| Boot1/PB2 | 28 | Gnd (necessary???) | |
| PA9/UART1_TX /TIM1_CH2 | 42 | For serial flash & debug printf(); Do not use for other purpose. | |
| PA10/UART1_RX/ TIM1_CH3 | 43 | | |
| V _{BAT} | 1 | Battery backup or V _{DD} (if not used) | |
| PD0/OSC_IN | 5 | Input only | |
| PD1/OSC_OUT | 6 | Output only | |
| Recommended pin assignments (Analog inputs) | | | |
| PC0/ADC123_IN10 | 8 | Preferred analog input pins | gyro |
| PC1/ADC123_IN11 | 9 | | |
| PC2/ADC123_IN12 | 10 | | Sen_LF |
| PC3/ADC123_IN13 | 11 | | Sen_RF |
| PA0/TIM5_CH1/ADC123_IN0 | 14* | Next preferred analog input pins | Sen_LD |
| PA1/TIM5_CH2/ADC123_IN1 | 15* | | Sen_RD |
| PA2/TIM5_CH3/ADC123_IN2 | 16* | | Sen_Flash |
| PA3/TIM5_CH4/ADC123_IN3 | 17* | | BatteryVolt |
| PA4/ADC12_IN4 | 20 | Other analog inputs | |
| PA5/ADC12_IN5/SPI1_CK | 21 | | |
| PA6/TIM3_CH1/ADC123_IN6/SPI1_MISO | 22* | | |
| PA7/TIM3_CH2/ADC123_IN7/SPI1_MOSI | 23* | | |
| Recommended pin assignments (Encoder inputs) | | | |
| PC6/TIM8_CH1 | 37 | Quadrature i/p | |
| PC7/TIM8_CH2 | 38 | | |
| PB4 | 56 | Quadrature i/p. Remap TIM3 here. | |
| PB5 | 57 | | |
| PB6/TIM4_CH1 | 58 | Quadrature i/p | Right_chA |
| PB7/TIM4_CH2 | 59 | | Right_chB |
| PA15 | 50 | Quadrature i/p. Partial remap TIM2 here | Left_chA |
| PB3 | 55 | | Left_chB |
| Recommended pin assignments (Serial comms) | | | |
| PB10/i2c2_SCL/USART3_TX | 29 | I2C2 or USART | |
| PB11/i2c2_SDA/USART3_RX | 30 | | |
| PC10/UART4_TX | 51 | RS232 | |
| PC11/UART4_RX | 52 | | |
| PC12/UART5_TX | 53 | RS232 | |
| PD2/UART5_RX | 54 | | |

| Recommended pin assignments (PWM) | | | |
|-----------------------------------|-----|---|------------|
| PC8/TIM8_CH3 | 39 | Remap TIM3 here for PWM o/p. If TIM3 is already assigned for quadrature i/p, do not use these pins. | |
| PC9/TIM8_CH4 | 40 | | |
| PA8/TIM1_CH1 | 41 | PWM output | Rmotor_pwm |
| PA11/TIM1_CH4 | 44 | | Lmotor_pwm |
| PA0/TIM5_CH1/ADC123_IN0 | 14* | Can be used for PWMs or Analog inputs. TIM3_CH1 & TIM3_CH2 can be used for encoder inputs Pins marked with '*' are also listed before in other entries. They are repeated here for convenience. Do not use the same pins twice. | |
| PA1/TIM5_CH2/ADC123_IN1 | 15* | | |
| PA2/TIM5_CH3/ADC123_IN2 | 16* | | |
| PA3/TIM5_CH4/ADC123_IN3 | 17* | | |
| PA6/TIM3_CH1/ADC123_IN6 | 22* | | |
| PA7/TIM3_CH2/ADC123_IN7 | 23* | | |
| PB0/TIM3_CH3/ADC12_IN8 | 26 | | |
| PB1/TIM3_CH4/ADC12_IN9 | 27 | | |
| General IOs and misc. | | | |
| PC4/ADC12_14 | 24 | Analog input or general IO | Rmotor_dir |
| PC5/ADC12_15 | 25 | | Lmotor_dir |
| PB12/USART3_CK | 33 | Use these pins for HCMS2905 alphanumeric display SPI interface or general IOs. | Disp_CE |
| PB13/SPI2_CK | 34 | | Disp_Clk |
| PB14/SPI2_MISO | 35 | | Disp_RS |
| PB15/SPI2_MOSI | 36 | | Disp_Data |
| PA12 | 45 | Preferred general IOs (these pins have no special alternate functions that is useful) | Led0 |
| PA13 | 46 | | Led1 |
| PA14 | 49 | | Led2 |
| PB8/TIM4_CH3 | 61 | If TIM4 is used for encoder, these pins can be used for general IOs. | TX_Diag |
| PB9/TIM4_CH4 | 62 | | TX_Diag_H |
| PC13 | 2 | Preferred general IO. These 3 pins have low current drive (3mA). Cannot drive LEDs. | Tx_Left |
| PC14 | 3 | | Tx_Right |
| PC15 | 4 | | User-SW |

Notes:

- 2 advance control timers (TIM1, TIM8), PWM, i/p capture, output compare, & quadrature encoder
- 4 general timers TIM2, TIM3, TIM4, TIM5 – i/p capture, output compare, one pulse mode o/p, PWM, quadrature encoder
- 2 basic timers, TIM6, TIM7 for interrupts.
- Total $I_{VDD} < 150\text{mA}$. Individual IO pin can sink or source $\pm 8\text{mA}$, and sink 20mA (with a relaxed V_{OL})
- Individual output pins can be configured as push-pull or open-drain.
- Some alternate function pins can be remapped through AFIO_MAPR register. Refer to section-8 of stm32F10xxx reference manual.
- Maximum of 16 interrupt pins, EXTI0-EXTI15. Can be mapped to any corresponding port pin. E.g. EXTI0 to (PA0/PB0/PC0/...). See section-9 of stm32F10xxx reference manual.
- The IO subsystems pins available are limited by the 64 pin package. The 100-pin or 144 pin package allows more of the pins to be available.
- Most pins are 5V tolerant, except ADC input pins, PB5 & PC13-PC15, OSC_IN
- OSC_IN & OSC_OUT can be connected to a crystal to generate a more accurate clock for CPU