Project Proposal
Joel Meine

Project: Sequential Multiplier, Shift-and-Add (4-bit)

Description:
A digital arithmetic component that will execute the multiplication of two 4-bit binary values; thus the component is limited to the product range of 0 - 225 (15 * 15 = 225).
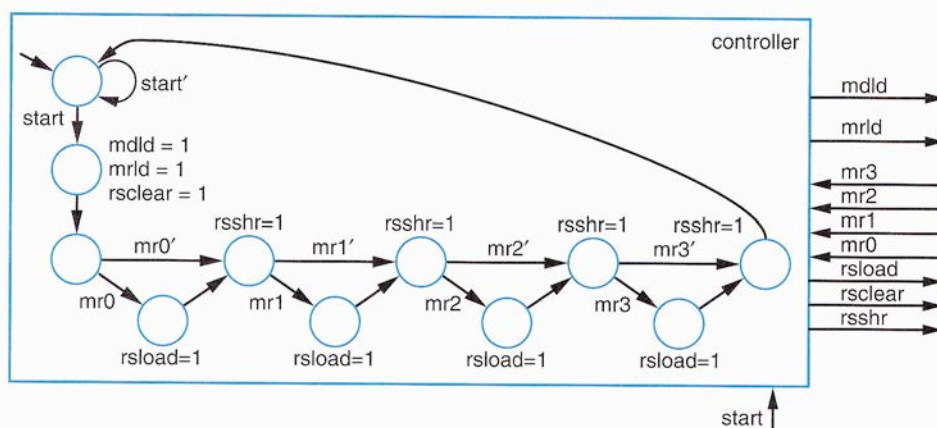
Application:
The function of multiplication is a fundamental and essential operation of mathematics that is widely used within an infinite number of practical, real-world applications. Compared to the array-style multiplier, we see that a trade-off is evident. While the array-style multiplier is much faster than the sequential multiplier, it is also much larger in architecture than the sequential multiplier. Thus we see that if processing speed is a greater priority than physical size of the digital device, the device would incorporate an array-style multiplier(s) resulting in a device that might be considerably large but comparatively fast at computational operations (e.g. a dedicated server). If physical size is a greater priority than the processing speed of the digital device, the device would incorporate a sequential multiplier(s) resulting in a device that might be considerably small but comparatively slow at computational operations (e.g. a smartphone).

HL Diagram:
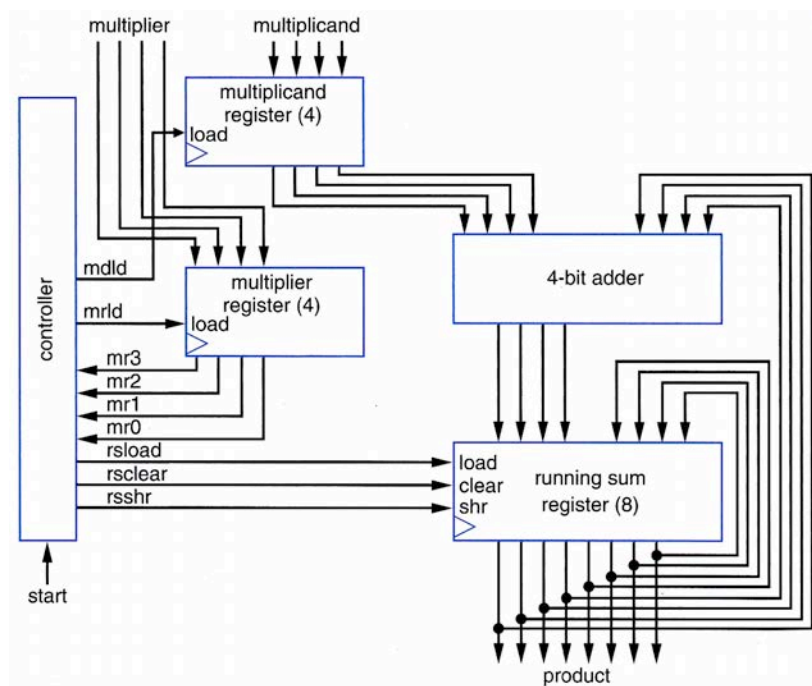
- Inputs: multiplicand (x), multiplier (y)
- Outputs: product (z)

FSM Diagram:

Note: FSM diagrams for the register and adder components not included to avoid redundancy. Only the FSM for the controller above is necessary for this project.

FPGA Specifications:
- SW[7:4] = Multiplicand, Binary (4-bit)
- SW[3:0] = Multiplier, Binary (4-bit)
- LD[7:0] = Product, Binary (8-bit)
- AN[3:0] = Product, Decimal*

* = Denotes that implementing this function is optional.

Schedule:

Task	Deadline
Adder / Registers / Controller	April 18
Structural & Implementation	April 25