

Lab 5 – MOSFET Active Balun Circuit

Objectives

- To execute the instructions of Lab 5 as provided for ECE 3410 from Canvas (<https://usu.instructure.com/>).
 - To use knowledge of common-source, source-follower and common-gate amplifier configurations to design a practical active balun circuit.
 - To confirm design predictions using hand analysis and simulation tools.
 - To build and test the designed balun circuit; to practice systematic laboratory troubleshooting skills.

Introduction

A *balun* is a circuit that converts a single-ended signal to a differential one. The single-ended signal could be generated by a sensor or antenna. Differential signals are often better for transmitting across long wires because they cancel out environmental interference and noise. Differential signals are also required for signal processing with differential circuits like modulators.

Most baluns are made using passive devices – transformers, resistors, inductors, etc. An *active balun* uses an amplifying device like a MOSFET or BJT. A standard MOSFET active balun circuit is shown in Fig. 1. The MOSFET device in this circuit is biased in **saturation**, and **works both as a common-source (CS) amplifier and as a source-follower (SF)**. When considering the signal transferred from v_g to v_{o1} , we have a CS circuit. When considering the signal transferred from v_g to v_{o2} , we have a SF circuit. **To make a good balun, we want the CS and SF circuits to have equal gain, so that the differential output is balanced.**

Source: ECE 3410 >> Lab5.pdf (<https://usu.instructure.com/>)

Preparation

Component and Materials

- CD4007 MOSFET (2) – $M1, M2$
- $20\mu F$ capacitor (1) – C_{G1}
- $1\mu F$ capacitor (3) – C_{S2}, C_{D1}, C_S1
- $100k\Omega$ resistor (1) – R_{G1}
- 510Ω resistor (1), 36Ω resistor (1) – R_{S21}, R_{S22}
- 820Ω resistor (1), 39Ω resistor (1) – R_{D21}, R_{D22}
- 300Ω resistor (1) – R_{IN}
- $2k\Omega$ resistor (4) – $R_{D1}, R_{S1}, R_{DL}, R_{SL}$
- Datasheet for the CD4007 MOSFETs

Equipment

- Power Supply, Dual – V_{DD}, V_G
- Multimeter, Digital – I_{D1}, I_{D2}
- Function Generator – v_{IN}
- Oscilloscope, Dual-Channel – v_{o1}, v_{o2}
- Banana Cable Set(s)
- Oscilloscope Probes(s)
- BNC-to-BNC Cable
- BNC-to-Alligator Cable

Pre-Lab Analysis

► Analytical

Table 1: Active Balun & Common-Gate Circuits

Component	Description	Value
C_{G1}	Input bypass capacitor.	$20 \mu\text{F}$
R_{G1}	Input high-pass filter resistor.	$100 \text{k}\Omega$
C_{S2}, C_{D1}, C_{S1}	Output bypass capacitors.	$1 \mu\text{F}$
R_{DL}, R_{SL}	Load resistors.	$2 \text{k}\Omega$
V_{DD}	Main supply voltage.	10 V
v_{IN}	Input voltage.	1 V (Pk-Pk)
f_{IN}	Input frequency.	50 kHz
R_{IN}	Input resistance.	300Ω

Table 3: Gains & Transconductance

Parameter	Description	Value
$A_{CS} \triangleq v_{o1} / v_{g1}$	Common-Source gain.	-0.5 V/V
$A_{SF} \triangleq v_{o2} / v_{g1}$	Source-Follower gain.	0.5 V/V
$A_d = A_{SF} - A_{CS}$	Overall Differential gain.	1.0 V/V
$A_{CG} \triangleq v_{g1} / v_{s2}$	Common-Gate gain.	1.0 V/V
g_{m1}	Active Balun transconductance	1.0 mA/V
g_{m2}	Common-Gate transconductance	1.5 mA/V

Table 2: Device Data for CD4007 NMOS Component

Parameter	Description	Value
$k_n = \mu_N C_{ox} \left(\frac{W}{L} \right)$	Scale constant.	$333 \mu\text{A/V}^2$
V_{TH}	Threshold voltage.	2.0 V

MOSFET Operating Region

$V_{GS} - V_{TH} \leq 0$	Cutoff	$V_{OV} \triangleq V_{GS} - V_{TH} $
$V_{DS} > V_{GS} - V_{TH}$	Saturation	
$V_{DS} \leq V_{GS} - V_{TH}$	Triode	

Exercise 1

Parameter	Formula	Value
R_{D1}	(2)	$2 \text{k}\Omega$
R_{S1}	(1)	$2 \text{k}\Omega$
I_{D1}	(3)	1.502 mA
V_{OV1}	(7)	3.003 V
V_{D1}	(4)	6.997 V
V_{S1}	(5)	3.003 V
V_{G1}	(9)	8.006 V
V_{GS1}	(8)	5.003 V
V_{DS1}	(6)	3.994 V

$V_{DS1} > V_{OV1}$

Saturation

$$\begin{aligned}
 (1) \quad A_{SF} &= \frac{g_{m1}(R_L \parallel R_{S1})}{1 + g_{m1}(R_L \parallel R_{S1})} & (4) \quad V_{D1} &= V_{DD} - I_{D1}R_{D1} & (7) \quad V_{OV1} &= \sqrt{\frac{2I_{D1}}{k_n}} \\
 (2) \quad A_{CS} &\approx -\frac{(R_{D1} \parallel R_{S1})}{R_{S1}} & (5) \quad V_{S1} &= I_{D1}R_{S1} & (8) \quad V_{GS1} &= V_{OV1} + V_{TH} \\
 (3) \quad g_{m1} &= \sqrt{2k_n I_{D1}} & (6) \quad V_{DS1} &= V_{D1} - V_{S1} & (9) \quad V_{G1} &= V_{S1} + V_{GS1}
 \end{aligned}$$

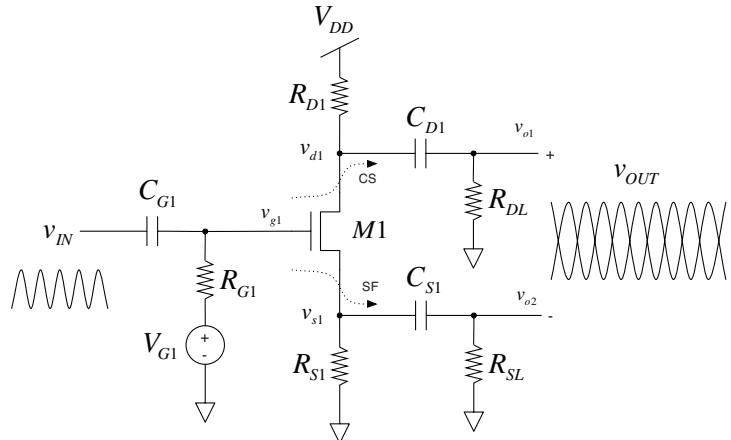


Figure 1: Active Balun Circuit

Exercise 2

Parameter	Formula	Value
R_{D2}	(2)	860.215 Ω
R_{S2}	(1)	545.455 Ω
I_{D2}	(3)	3.378 mA
V_{OV2}	(7)	4.505 V
V_{D2}	(4)	7.094 V
V_{S2}	(5)	1.843 V
V_{G2}	(9)	8.347 V
V_{GS2}	(8)	6.505 V
V_{DS2}	(6)	5.251 V

$$V_{DS2} > V_{OV2}$$

Saturation

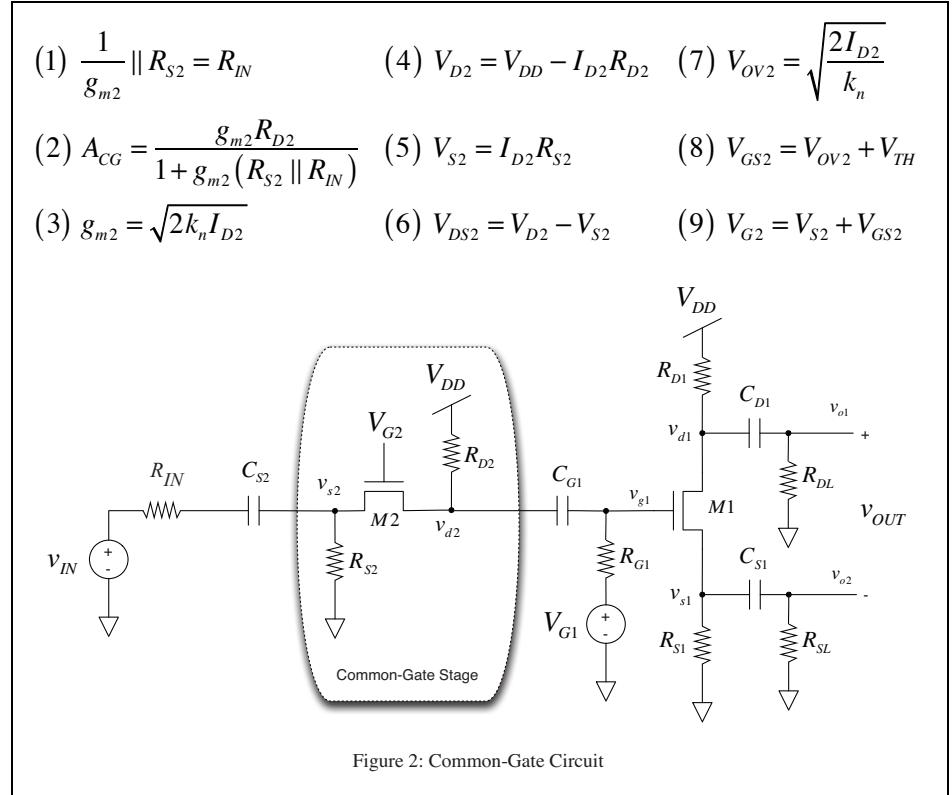
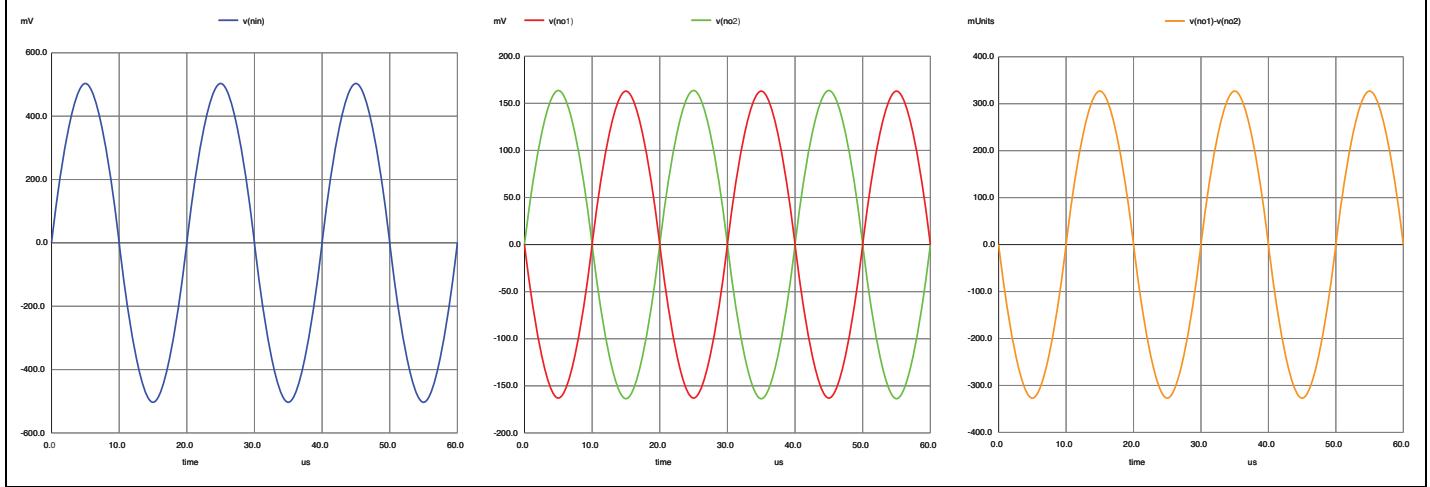


Figure 2: Common-Gate Circuit

Exercise 3

Parameter	v_{o1}	v_{o2}	v_{in}	$t_0(v_{o1})$	$t_0(v_{o2})$	ΔA	$\Delta \phi$
Value	326.9330 mV (Pk-Pk)	326.9328 mV (Pk-Pk)	1 V (Pk-Pk)	9.959758 μ s	9.960023 μ s	-73.9793 dBm	-83.2522 μ rad
Formulas	$\Delta A = 20 \log(\Delta v_o / (0.001 v_{in}))$ $\Delta \phi = 2\pi f \Delta t_0$ $\Delta v_o = v_{o1} - v_{o2} $ $\Delta t_0 = t_0(v_{o1}) - t_0(v_{o2}) $						



Source: NGSPICE (<http://ngspice.sourceforge.net>)

>Calculated

balun.sp >>

```
* Balun Circuit
* SPICE 5b
* ****
* By Chris Winstead
* Modified by Joel Meine
* ECE 3410, Utah State University
* ****

* See diagram CD.1 in Appendix.
.include ../lab_parts.md

* M1 parameters
.param VG1=8.0060060060
.param RD1=2k
.param RS1=2k

* M2 parameters
.param VG2=8.3472563473
.param RD2=860.2150537634
.param RS2=545.4545454545

* Voltage input
Vin nin 0 DC 0V SIN(0 500mV 50k)

* Gate voltage sources and VDD:
VDD ndd 0 DC 10V
VG1 nr1 0 DC VG1
VG2 ng2 0 DC VG2

* MOSFET connections:
* M# ndrain ngate nsouce nsubstrate
CD4007N W=# L=#
M1 nd1 ng1 ns1 0 CD4007N W=30u L=10u
M2 nd2 ng2 ns2 0 CD4007N W=30u L=10u

* Resistor and Capacitor connections:
RG1 ng1 nr1 100k
RIN nin pin 300
* M1 Components
RD1 ndd nd1 RD1
RDL no1 0 2k
CD1 nd1 no1 1u
RS1 ns1 0 RS1
RSL no2 0 2k
CS1 ns1 no2 1u
* M2 Components
RD2 ndd nd2 RD2
CG2 nd2 ng1 20u
RS2 ns2 0 RS2
CS2 pin ns2 1u

* Control commands to simulate the
* DC transfer characteristic:
.control
tran 50n 60u
meas tran pp1 PP v(no1)
meas tran pp2 PP v(no2)
meas tran ppin PP v(nin)

meas tran cross1 WHEN v(no1)=0
CROSS=1
►1
```

```
◀1
meas tran cross2 WHEN v(no2)=0
CROSS=2

echo "Measuring the Amplitude
Imbalance (in dBm):"
let dA = 20*log10(abs(pp1-
pp2)/(ppin*0.001))
print dA

echo "Measuring the Phase Imbalance
(in radians):"
let dPhi = 2*PI*50e3*(cross1-cross2)
print dPhi

plot v(nin)
hardcopy nin.ps v(nin)
plot v(no1) v(no2)
hardcopy no1_no2.ps v(no1) v(no2)
plot 'v(no1)-v(no2)'
hardcopy no1-no2.ps 'v(no1)-v(no2)'
.endc
.end
```

balun_approx.sp >>

```
* Balun Circuit - Standard Component
Values
* SPICE 5b
* ****
* By Chris Winstead
* Modified by Joel Meine
* ECE 3410, Utah State University
* ****

* See diagram CD.1 in Appendix.
.include ../lab_parts.md

* M1 parameters
.param VG1=8.01
.param RD1=2k
.param RS1=2k
** 10% Error Simulation
** RD1+0.10*RD1, RS1-0.10*RS1
*.param RD1=2.2k
*.param RS1=1.8k

* M2 parameters
.param VG2=8.35
.param RD21=820
.param RD22=39
.param RS21=510
.param RS22=36

* Voltage input
Vin nin 0 DC 0V SIN(0 500mV 50k)

* Gate voltage sources and VDD:
VDD ndd 0 DC 10V
VG1 nr1 0 DC VG1
VG2 ng2 0 DC VG2

►2
```

```
◀2
* MOSFET connections:
* M# ndrain ngate nsouce nsubstrate
CD4007N W=# L=#
M1 nd1 ng1 ns1 0 CD4007N W=30u L=10u
M2 nd2 ng2 ns2 0 CD4007N W=30u L=10u

* Resistor and Capacitor
connections:
RG1 ng1 nr1 100k
RIN nin pin 300
* M1 Components
RD1 ndd nd1 RD1
RDL no1 0 2k
CD1 nd1 no1 1u
RS1 ns1 0 RS1
RSL no2 0 2k
CS1 ns1 no2 1u
* M2 Components
RD21 ndd nr2 RD21
RD22 nr2 nd2 RD22
CG2 nd2 ng1 20u
RS21 ns2 nr3 RS21
RS22 nr3 0 RS22
CS2 pin ns2 1u
```

```
* Control commands to simulate the
* DC transfer characteristic:
.control
tran 50n 60u
meas tran pp1 PP v(no1)
meas tran pp2 PP v(no2)
meas tran ppin PP v(nin)

meas tran cross1 WHEN v(no1)=0
CROSS=1
meas tran cross2 WHEN v(no2)=0
CROSS=2

echo "Measuring the Amplitude
Imbalance (in dBm):"
let dA = 20*log10(abs(pp1-
pp2)/(ppin*0.001))
print dA

echo "Measuring the Phase Imbalance
(in radians):"
let dPhi = 2*PI*50e3*(cross1-cross2)
print dPhi

plot v(nin)
plot v(no1) v(no2)
plot 'v(no1)-v(no2)'
.endc
.end
```

log.txt >>

balun.sp >>

```
** Calculated Resistor Values **

Node          Voltage
-----
nin           0
ndd           10
nr1          8.00601
ng2          8.34726
nd1          6.95862
ng1          8.00601
ns1          3.04138
nd2          7.01366
ns2          1.89361
pin           0
no1           0
no2           0
vg2#branch   0
vg1#branch   -1.35525e-020
vdd#branch   -0.00499231
vin#branch   0

pp1 = 326.9330 mV
pp2 = 326.9328 mV
ppin = 999.9903 mV
cross1 = 9.959758 μs
cross2 = 9.960023 μs

Measuring the Amplitude Imbalance:
ΔA = -73.9793 dBm

Measuring the Phase Imbalance:
Δφ = -83.2522 μrad
```

balun_approx.sp (Standard Resistor Values) >>

```
** Standard Resistor Values **

Node          Voltage
-----
nin           0
ndd           10
nr1          8.01
ng2          8.35
nd1          6.95598
ng1          8.01
ns1          3.04402
nd2          7.01725
ns2          1.89591
pin           0
no1           0
no2           0
nrd2         7.15267
nrs2         1.7709
vg2#branch   0
vg1#branch   0
vdd#branch   -0.00499436
vin#branch   0

pp1 = 326.6644 mV
pp2 = 326.6642 mV
ppin = 999.9903 mV
cross1 = 9.959765 μs
cross2 = 9.960029 μs

Measuring the Amplitude Imbalance:
ΔA = -73.9793 dBm

Measuring the Phase Imbalance:
Δφ = -82.9380 μrad
```

balun_approx.sp (10% Error Sim.) >>

```
** 10% Error Simulation **

Node          Voltage
-----
nin           0
ndd           10
nr1          8.01
ng2          8.35
nd1          6.41385
ng1          8.01
ns1          2.93413
nd2          7.01725
ns2          1.89591
pin           0
no1           0
no2           0
nrd2         7.15267
nrs2         1.7709
vg2#branch   0
vg1#branch   0
vdd#branch   -0.00510242
vin#branch   0

pp1 = 356.2067 mV
pp2 = 322.1213 mV
ppin = 999.9903 mV
cross1 = 9.960244 μs
cross2 = 9.959920 μs

Measuring the Amplitude Imbalance:
ΔA = 30.65145 dBm

Measuring the Phase Imbalance:
Δφ = 101.7876 μrad
```

Lab Experiments

Procedures 1, 2

Parameter	Measured Value	Calculated Value Ideal Resistors	Calculated Value Non-Ideal Resistors	Error Ideal Resistors	Error Non-Ideal Resistors
R_{G1}	97.4 kΩ	100 kΩ	97.4 kΩ	2.60%	0.00%
R_{D1}	2.01 kΩ	2 kΩ	2.01 kΩ	0.50%	0.00%
R_{S1}	2.03 kΩ	2 kΩ	2.03 kΩ	1.50%	0.00%
R_{DL}	2.00 kΩ	2 kΩ	2.00 kΩ	0.00%	0.00%
R_{SL}	1.99 kΩ	2 kΩ	1.99 kΩ	0.50%	0.00%
V_{G1}	8.03 V	8.00601 V	8.00601 V	0.30%	0.30%
V_{DD}	10.04 V	10 V	10 V	0.40%	0.40%
v_{d1}	7.26 V	6.95862 V	6.97390 V	4.33%	4.10%
v_{s1}	2.77 V	3.04138 V	3.05621 V	8.92%	9.36%
v_{g1}	8.29 V	8.00601 V	8.00601 V	3.55%	3.55%
I_{D1}	1.53 mA	1.50150 mA	1.50150 mA	1.90%	1.90%

Procedures 3, 4, 5

See plot OP.1 in Appendix.

Parameter	Measured Value	Calculated Value Ideal Resistors	Calculated Value Non-Ideal Resistors	Error Ideal Resistors	Error Non-Ideal Resistors
f	50.1746 kHz	50 kHz	50 kHz	0.35%	0.35%
v_{o1} (Pk-Pk)	196 mV	498.7532 mV	497.5689 mV	60.70%	60.61%
v_{o2} (Pk-Pk)	192 mV	498.7534 mV	498.7636 mV	61.50%	61.50%
v_{in} (Pk-Pk)	1.00 V	1.00 V	1.00 V	0.00%	0.00%
$A_{CS} = v_{o1} / v_{in}$	196 mV/V	498.7532 mV/V	497.5689 mV/V	60.70%	60.61%
$A_{SF} = v_{o2} / v_{in}$	192 mV/V	498.7534 mV/V	498.7636 mV/V	61.50%	61.50%
$A_d = A_{CS} + A_{SF}$	388 mV/V	997.5066 mV/V	996.3325 mV/V	61.10%	61.06%
$t_0(v_{o1})$	11.158 μ s	9.992411 μ s	9.992384 μ s	11.66%	11.67%
$t_0(v_{o2})$	11.601 μ s	9.992676 μ s	9.992662 μ s	16.10%	16.10%
ΔA	51.7766 dBm	73.9793 dBm	1.545262 dBm	30.01%	E >> 100%
$\Delta \phi$	139.6585 mrad	83.2522 μ rad	87.6504 μ rad	E >> 100%	E >> 100%

Procedure 6

Parameter	Measured Value	Calculated Value Ideal Resistors	Calculated Value Non-Ideal Resistors	Error Ideal Resistors	Error Non-Ideal Resistors
R_{D21}	808 Ω	820 Ω	808 Ω	1.46%	0.00%
R_{D22}	39.1 Ω	39 Ω	39.1 Ω	0.26%	0.00%
R_{S21}	502 Ω	510 Ω	502 Ω	1.57%	0.00%
R_{S22}	34.8 Ω	36 Ω	34.8 Ω	3.33%	0.00%
R_{IN}	313 Ω	300 Ω	313 Ω	4.33%	0.00%
V_{G2}	8.62 V	8.34726 V	8.34726 V	3.27%	3.27%
V_{DD}	10.04 V	10 V	10 V	0.40%	0.40%
v_{d2}	7.02 V	7.01918 V	7.03697 V	0.01%	0.24%
v_{s2}	1.93 V	1.89467 V	1.87765 V	1.86%	2.79%
I_{D1}	3.43 mA	3.37838 mA	3.37838 mA	1.53%	1.53%

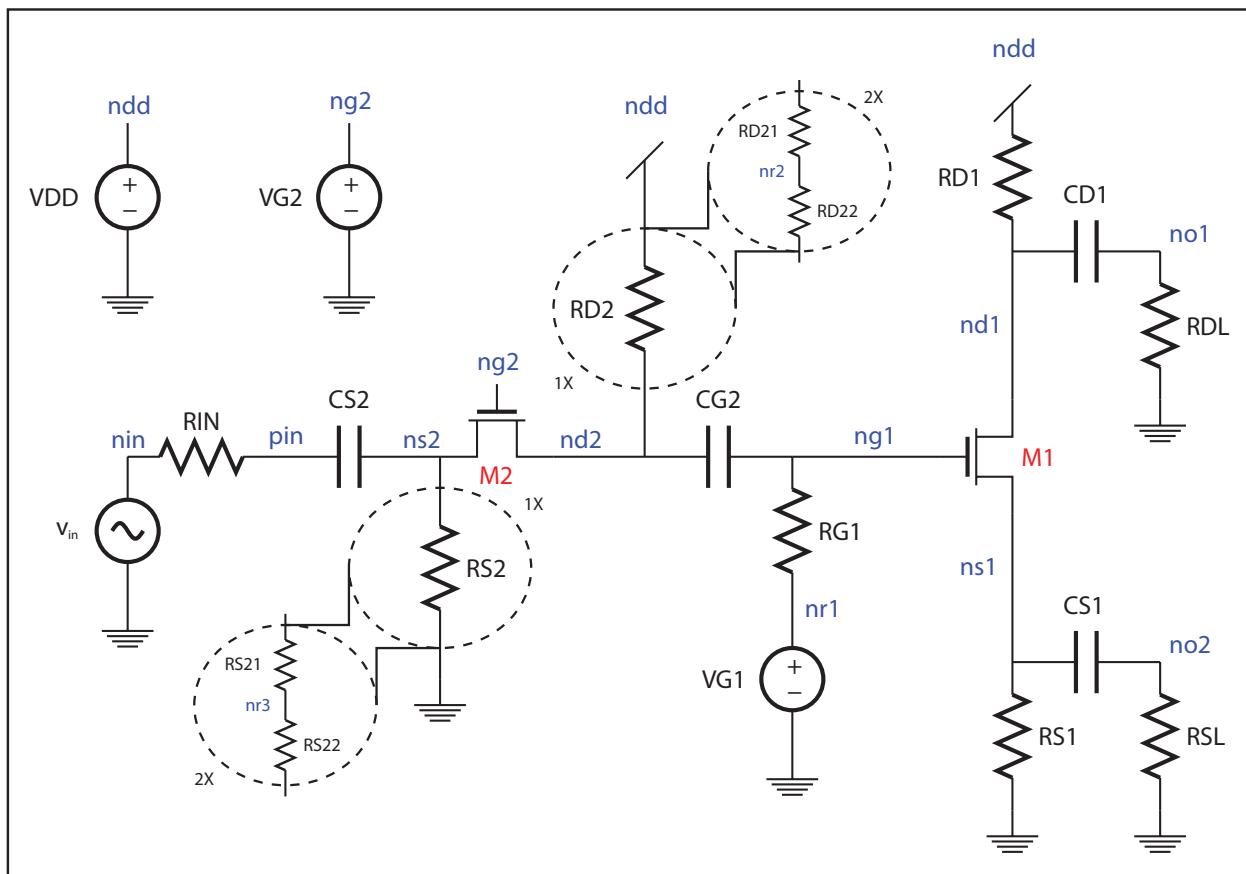
Parameter	Measured Value	Parameter	Measured Value	(1) $\frac{v_{g2}}{v_{in}} = \frac{R_{in}}{R_{in} + R_{IN}}$
v_{in} (Pk-Pk)	0.97 V	R_{in} (1)	3.26042 Ω	$\Rightarrow R_{in} = -v_{g2}R_{IN} / (v_{in} - v_{g2})$
v_{g1} (Pk-Pk)	1.00 V	$A_{CG} = v_{g1} / v_{g2}$	100 V/V	
v_{g2} (Pk-Pk)	0.01 V			

Commentary

- Improved familiarization and increased experience was obtained in MOSFET behavior analysis via the active balun circuit. Additionally, associated knowledge was utilized with respect to the basic MOSFET circuit configurations; including common-source, source-follower and common-gate amplifiers.
- The results derived from the experimental methods of the lab for procedures 1 through 2 yielded mostly passable values of marginal error. Probing the voltages at the drain, source, and gate terminals of the NMOS device yielded results that could be reasonably deemed as borderline failing specifications. However, the measured values do at least positively correlate with the calculated values. The bias current could not be directly measured as it was concluded that the amp-meter device for the given lab station used was non-functional. The value of bias current used as the measurement was derived from other lab associates.
- For lab procedures 3 through 5, the values measured and derived yielded results of exceedingly high error. The output voltage values measured were substantially lower than expected. In real-time it was observed that the voltage output values were rapidly decaying. The initial voltage output values may possibly have been more reasonably close to the calculated values, however, the decay behavior made declaring firm output voltages difficult to decide on. Thus, no conclusive account or explanation has been made regarding the decay behavior.
- Significant amplitude imbalance was observed, however, phase imbalance was reasonably negligible. Due to the decay behavior, that would suggest the most likely and probable cause of amplitude imbalance. As only an intuitive and uninformed insight to the cause of the decay behavior, this possibly suggests a faulty capacitor(s) that was shorted-out and unable to sustain a charge. Thus trying alternative capacitors may have yielded improved amplitude balance.
- Finally for procedure 6, the error between the measured and calculated values yielded passable results of lower error than previous procedures. However, as before the output voltages yielded lower values than expected.
- Overall, the largely undesirable measured results of the output voltages could admittedly be attributed to a lack of thorough troubleshooting. As the pre-lab calculations and analysis had not actually been completed thoroughly beforehand, the methods and findings of lab colleagues was used. Thus it was not discovered until later that the voltage outputs were substantially lower than expected. As this particular lab incorporated substantially more components connected together to form a circuit, inevitably there was an increased likelihood of substantial error.

Appendix

CD.1



OP.1

