SPICE 5b: Pre-Lab for Lab 5

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ECE 3410. Spring, 2015.

Preparing for the Exercises

In this session, we will continue working in the same directory used for MOSFET simulations in SPICE assignment 5:

```
3410/
└─ spice/
   ├─ lab1/
   ├─ lab2/
   ├─ lab3/
   ├─ lab4/
   └─ lab5/
```

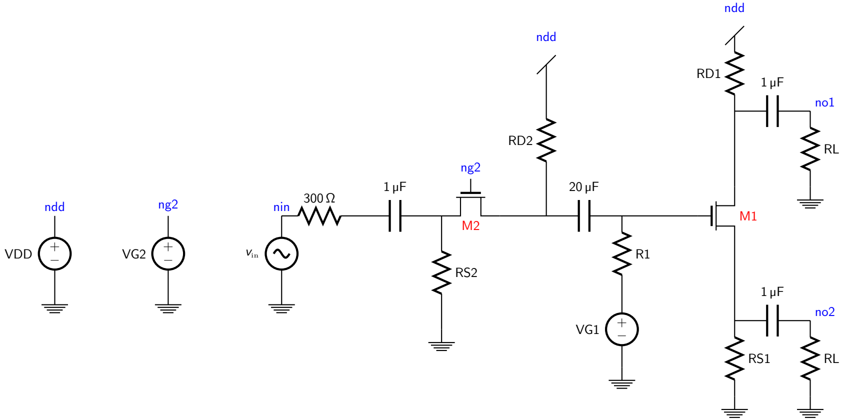
Obtain the Example Files

In this lab, you will download a testbench file into your session directory:

```
3410/
└─ spice/
   ├─ [files from previous labs]
   └─ lab5/
      ├─ [files from last time]
      └─ balun_testbench.sp
```

The Balun Circuit

We will be analyzing and designing this circuit:



With device values: VDD=10 V, R1=100 kΩ, RL=2 kΩ. Note that I've slightly changed the resistor labels to make the analysis steps a little more clear.

Create a SPICE File

Create a SPICE file to describe the circuit shown on the previous slide. Make sure that you use the node names indicated in blue, since these specific names are expected by the testbench. For other nodes you may use any names you want.

Since you have not yet analyzed the values for R2, R3, RD, RS, VG1 and VG2, set these as parameters so that you can easily change them later, like this:

```
.param R1=100k
...
R1 nx ng1 R1
```

In the above listing, SPICE can distinguish between the device named R1 and the parameter with the same name. For now, give them dummy values and we'll fill in the calculations as we go.

When you are finished, copy the text from `balun_testbench.sp` into the bottom of your SPICE file.

Declaring Real MOSFETs

In the previous session, we defined idealized MOSFETs with minimal parameters. In this lab, you will be using a commercial CD4007 MOSFET array chip. The parameters for these devices are provided by the manufacturer, and are placed in the `lab_parts.md` file. At the top of your file, make sure you include the model file:

```
.include ../lab_parts.md
```

The actual model contains several additional parameters, and is as follows:

```
.model CD4007N NMOS
+ Level=1 Gamma= 0 Xj=0 W=30e-6 L=10e-6
+ Tox=1200n Phi=.6 Rs=0 Kp=111u Vto=2.0 Lambda=0.01
+ Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p
+ Cgdo=0.1p Is=16.64p N=1
```

To place a MOSFET instance in your circuit, it is necessary to declare the correct width and length of 30 μm and 10 μm, respectively:

```
M1 <ndrain> <ngate> <nsource> <nsubstrate> CD4007N W=30u L=10u
```

Make sure the substrate terminals are connected to ground.

Analyzing the Circuit

The circuit is divided into two parts, the balun (M1) and an impedance-matching stage (M2). The pre-lab asks you to analyze them separately. In all analyses, we assume that r_o is very large compared to the other resistances in the circuit.

In other words, we let r_o go to infinity in our equations, and simply erase it from our circuit models.

The Common-Source Signal Path

For the common-source signal path, we know from class that:

$$\begin{aligned} A_{Vo} &= -g_m r_o \\ R_{\mathrm{OUT}} &= r_o + R_S + g_m r_o R_S \\ A_{VL} &= A_{Vo}\left(\frac{R_L \parallel R_D}{R_L \parallel R_D + R_{\mathrm{OUT}}}\right). \end{aligned}$$

Now plug-in the formulas into A_{VL} and let $r_o \to \infty$, and further suppose that $g_m R_S \gg 1$, then you should get

$$A_{CS} = \lim_{r_o \to \infty} \frac{-g_m r_o (R_D \parallel R_L)}{r_o(1 + g_m R_S)} \approx -\frac{(R_D \parallel R_L)}{R_S}.$$

You should be able to derive this same result from the simplified small-signal models shown in the lab assignment.

The Source Follower Signal Path

For the source follower signal path, we know from class that:

$$
\begin{aligned}
A_{Vo} &= \frac{g_m r_o}{1 + g_m r_o} \\
R_{\mathrm{OUT}} &= \frac{R_D + r_o}{1 + g_m r_o} \\
A_{VL} &= A_{Vo} \left(\frac{R_L \parallel R_S}{R_L \parallel R_S + R_{\mathrm{OUT}}} \right).
\end{aligned}
$$

Now plug-in the formulas into A_{VL} and let $r_o \to \infty$, then you should get

$$
\begin{aligned}
A_{Vo} &\to 1 \\
R_{\mathrm{OUT}} &\to \frac{1}{g_m} \\
A_{SF} &\to \frac{g_m (R_L \parallel R_S)}{1 + g_m (R_L \parallel R_S)}
\end{aligned}
$$

You should be able to derive this same result from the simplified small-signal models shown in the lab assignment.

Solve for R_S

You are given that $g_m = 1\,\text{mA/V}$ and $R_L = 2\,\text{k}\Omega$. For the source follower stage, we desire a gain of $A_{SF} = 0.5\,\text{V/V}$, i.e.:

$$\frac{g_m(R_L \parallel R_S)}{1 + g_m(R_L \parallel R_S)} = 0.5.$$

You can verify that this is satisfied if $g_m(R_L \parallel R_S) = 1$. Using this equation, solve for R_S.

Solve for R_D

Next, we can use the common-source solution to solve for R_D. Since we want $A_{CS} = -0.5\,\mathrm{V/V}$, we can use this equation:

$$\frac{(R_D \parallel R_L)}{R_S} = 0.5$$
$$\Rightarrow \frac{R_D R_L}{R_S(R_D + R_L)} = 0.5$$

Use this equation to solve for R_D.

Balun DC Solution I

Once you have the solutions for R_S and R_D, you can solve the balun's DC state.

First, since we are given $g_m = 1\,\text{mA/V}$ and $k_n = 333\,\mu\text{A/V}^2$, and we know that $g_m = \sqrt{2k_n I_D}$, we can solve for the DC current:

$$I_D = \frac{g_m^2}{2k_n}.$$

After obtaining I_D, we can solve for the drain and source terminal voltages:

$$V_{D1} = V_{\text{DD}} - I_D R_D$$
$$V_{S1} = I_D R_S$$

Balun DC Solution II

Next we can use the square law formula to solve for the voltages related to the gate:

$$\begin{aligned} I_D &= \frac{1}{2} k_n V_{\mathrm{OV}}^2 \\ \Rightarrow V_{\mathrm{OV}} &= \sqrt{\frac{2 I_D}{k_n}} \\ \Rightarrow V_{\mathrm{GS}} &= V_{\mathrm{OV}} + V_{\mathrm{Th}} \\ \Rightarrow V_{G1} &= V_{S1} + V_{\mathrm{GS}}. \end{aligned}$$

Solve all of these, in order, and record the results in your lab book.

Balun DC Solution III

As a last step, we need to verify that device M1 is biased in its saturation region. To check this, verify that:

$$V_{\mathrm{DS}} > V_{\mathrm{OV}}$$

Perform this calculation and record the results in your lab book.

Impedance Matching Stage

The next part of this lab is the impedance matching stage, based on a common-gate configuration. From the lectures, we know that the CG stage has these characteristics:

$$\begin{aligned}
A_{Vo} &= 1 + g_{m2} r_{o2} \\
R_{\mathrm{OUT}} &= (R_{S2} \parallel 300\,\Omega) + r_{o2} + g_{m2} r_{o2} (R_{S2} \parallel 300\,\Omega) \\
R_{\mathrm{IN}} &= \frac{R_{D2} + r_{o2}}{1 + g_{m2} r_{o2}} \parallel R_{S2} \\
A_{VL} &= A_{Vo} \left(\frac{R_{\mathrm{IN}}}{R_{\mathrm{IN}} + 300\,\Omega} \right) \left(\frac{R_{D2}}{R_{D2} + R_{\mathrm{OUT}}} \right)
\end{aligned}$$

If we let r_{o2} go to ∞, then $R_{\mathrm{IN}} \to (1/g_{m2}) \parallel R_{S2}$. Since we plan to make $R_{\mathrm{IN}} = 300\,\Omega$, we can write the loaded gain as

$$A_{VL} = g_{m2} r_{o2} \left(\frac{1}{2} \right) \left(\frac{R_{D2}}{r_{o2} + g_{m2} r_{o2} R_{S2}} \right) \to \frac{1}{2} \left(\frac{g_{m2} R_{D2}}{1 + g_{m2} (R_{S2} \parallel 300\,\Omega)} \right)$$

Because of the matched-impedance coupling, the signal amplitude will be reduced by half. We want the CG amplifier stage to act as a buffer from the source to drain terminals, so that $v_{d2}/v_{s2} = 1$ (for an overall loaded gain of 0.5). From this result, our tasks are to solve R_{S2} and R_{D2} so that $R_{\mathrm{IN}} = 300\,\Omega$ and $A_{VL} = 0.5\,\mathrm{V/V}$.

Solve for R_{S2}

Since we are given $g_{m2} = 1.5\,\mathrm{mA/V}$, and our total input resistance is $1/g_{m2} \parallel R_{S2}$, you can solve this equation to obtain R_{S2}:

$$\frac{1}{g_{m2}} \parallel R_{S2} = 300\,\Omega.$$

Solve for R_{D2}

Using your solution for R_{S2}, now solve this equation to obtain R_{D2}:

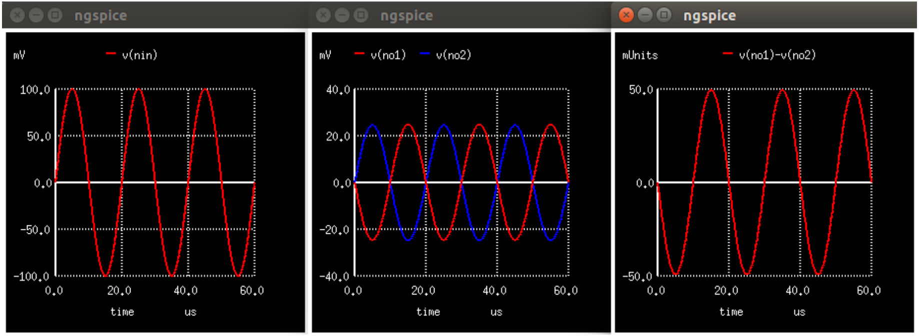
$$\left(\frac{g_{m2}R_{D2}}{1+g_{m2}(R_{S2}\parallel 300\,\Omega)}\right)=1.$$

DC Solution for the Common-Gate Stage

Repeat the same steps used for the balun section to obtain the DC solution of the impedance matching section. Solve for I_{D2}, V_{D2}, V_{OV2}, V_{GS2} and V_{G2}, and verify that M2 is in saturation. Make sure to use the correct values for g_{m2}, R_{S2} and R_{D2}, since those values are all different in this portion of the circuit.

Simulation

Enter your solutions for R_{S1}, R_{D1}, R_{S2} and R_{D2}, V_{G1} and V_{G2} into your SPICE model, and run a simulation. You should see something like this:



In the SPICE console, you should see a printout of DC bias point results. Create a file called log.txt and record these results. In your lab book, record a table that compares these SPICE results to your calculated DC bias points.

Measurements

Note that the requested measurements of amplitude balance and phase balance are already computed in the testbench, using these lines:

```
meas tran ppin PP v(nin)
meas tran cross1 WHEN v(no1)=0 CROSS=1
meas tran cross2 WHEN v(no2)=0 CROSS=2

echo "Measuring the Amplitude Imbalance (in dBm):"
let dA = 20*log10(abs(pp1-pp2)/(ppin*0.001))
print dA

echo "Measuring the Phase Imbalance (in radians):"
let dPhi = 2*PI*50e3*(cross1-cross2)
print dPhi
```

Note the measurement results in the SPICE console, and copy them into your log.txt file.

Making Practical Adjustments

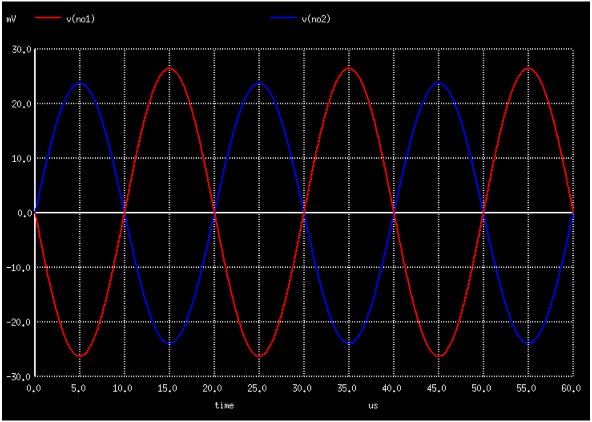
Your solutions may require non-standard resistor values, which can be awkward in the lab. Copy your balun.sp file to a new file called balun_approx.sp. In the new file, change all resistor values to ones that can be obtained by combining no more than two standard resistor values. In other words, you can use resistor values $100\,\Omega$, $500\,\Omega$, $1\,\mathrm{k}\Omega$, etc.

As a further simplification, set $V_{G1} = V_{G2}$ so that we only need to adjust one voltage in the lab.

After making these changes, run a simulation and record the results as before. In your lab book, take note of any differences.

Effects of Resistor Mismatch

In the lab, we will be using real resistors that will not be exactly equal to their rated values. Suppose that R_{D1} is 10% too large, and R_{S1} is 10% too small. Enter these modified values into your balun_approx.sp code and repeat the simulation. Record the results as before, and take note of any differences. You will probably see an imbalanced waveform like this:



What to Turn In

Create a zip file containing the following files:

- `balun.sp`
- `balun_approx.sp`
- `log.txt`

Upload these files to Canvas to complete the assignment.