A MOSFET Active Balun Circuit

Spring 2015

Objectives

- To use knowledge of common-source, source-follower and common-gate amplifier configurations to design a practical active balun circuit.
- To confirm design predictions using hand analysis and simulation tools.
- To build and test the designed balun circuit; to practice systematic laboratory troubleshooting skills.

Introduction

A *balun* is a circuit that converts a single-ended signal to a differential one. The single-ended signal could be generated by a sensor or antenna. Differential signals are often better for transmitting across long wires because they cancel out environmental interference and noise. Differential signals are also required for signal processing with differential circuits like modulators.

Most baluns are made using passive devices – transformers, resistors, inductors, etc. An *active balun* uses an amplifying device like a MOSFET or BJT. A standard MOSFET active balun circuit is shown in Fig. 1. The MOSFET device in this circuit is biased in **saturation**, and **works both as a common-source (CS) amplifier and as a source-follower (SF)**. When considering the signal transferred from v_g to v_{o1}, we have a CS circuit. When considering the signal transferred from v_g to v_{o2}, we have a SF circuit. **To make a good balun, we want the CS and SF circuits to have equal gain, so that the differential output is *balanced*.**

Parts and Equipments Required

Parts

- (1) CD4007 chip.
- (4) 1μF capacitors.

- (1) 100kΩ resistor.
- (2) 1kΩ resistors.
- (1) 300Ω resistor.
- (4) calculated resistor values.

Equipment

- Dual power supply – use to supply V_{DD} and V_G.
- Digital multimeter – use to verify bias voltage and current.
- Function generator – use to generate v_{in}.
- Dual-channel oscilloscope – use to measure the input and output signals.

1 Pre-Lab

Exercise 1. You will design the active balun circuit of Fig. 1 by choosing appropriate resistor values and bias voltages. Several of the resistances and bypass capacitor values are given in Table 1. The MOSFET $M1$ is an N-type device from the CD4007 package. The characteristics of $M1$ are given in Table 2.

Active Balun Design Problem

Derive small-signal expressions for the mid-band Common-Source and Source-Follower gains of the balun circuit:

$$A_{CS} \triangleq \frac{v_{o1}}{v_g}$$
$$A_{SF} \triangleq \frac{v_{o2}}{v_g}.$$

Use the small-signal equivalent circuit model shown in Fig. 2. Note that "mid-band" means you can ignore all capacitances in this analysis. **Record the derivations in your lab book, and put the expressions in your final report.**

We want the two gains to be $A_{SF} = 0.5\text{V/V}$ and $A_{CS} = -0.5\text{V/V}$. Then the overall differential gain will be $A_d = A_{SF} - A_{CS} = 1.0\text{V/V}$. Suppose the MOSFET has $g_m = 1\text{mA/V}$. **Solve for $\mathbf{R_S}$ and $\mathbf{R_D}$** under the assumption that r_o is very large (i.e. $r_o \to \infty$), and **verify that the gains are $\pm\mathbf{0.5V/V}$**. Also **determine the MOSFET's large-signal bias current, $\mathbf{I_D}$** (use the formula $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$), and **determine the gate voltage, $\mathbf{V_G}$**, needed to generate this current. **Put all your analysis and calculations in your lab book**. List your final results in a table:

Parameter	Value	Parameter	Value	$M1$ Operating Region	(check one)
R_D		V_{S1}		Linear	
R_S		V_{G1}		Triode	
I_D		V_{D1}		Saturation	
$V_{GS1} - V_{T0N}$		V_{DS1}		Cutoff	

Include this table in your lab book and in your final report. You should find that $M1$ is operating in saturation. Recall that saturation is where $V_{DS} \geq V_{GS} - V_{Th}$. If your result is not in saturation, you should re-do all your design calculations.

Exercise 2. Suppose the balun's input signal is delivered from a 300Ω transmission line, and the balun is required to act as a matched line termination, i.e. the balun's input resistance should equal 300Ω. The NMOS active balun circuit has a very high input impedance due to the gate of $M1$, which causes reflections in the transmission line. To provide the proper input resistance, a common-gate amplifier circuit is inserted in series with the balun's input, as shown in Fig. 3. The common-gate circuit is designed to have a total input impedance of 300Ω and a low gain.

Matched Impedance Design Problem

Derive expressions for the gain and input resistance of the Common-Gate stage. Using these expressions, calculate values of R_2, R_3 and $M2$'s bias current, I_{D2}, to satisfy the following constraints:

- $g_{m2} = 1.5mA/V$.
- $A_{CG} = 1$V/V, where $A_{CG} \triangleq v_{g1}/v_{s2}$.
- $R_{in} = 300\Omega$.

Use the mid-band equivalent small-signal circuit model shown in Fig. 4. Note that in the mid-band model, the C_1 acts like a short circuit, so $v_{d2} = v_{g1}$. The input resistance, R_{in}, is the effective resistance seen looking into the common-gate circuit. Derive an expression for R_{in} using by applying a test voltage v_x to the input, as illustrated in Fig. 5. Then solve for the total current, i_x, that goes into the amplifier. The input resistance is $R_{in} = v_x/i_x$. Using the small-signal model, show that the input resistance is $R_2 \parallel 1/g_m$, and the gain (from source to drain) is approximately $g_m R_3$ (note that R_1 is ignored in this analysis because it is very large, so that $R_3 \parallel R_1 \approx R_3$). Calculate the values for R_2 and R_3 that are required to yield the specified input resistance and gain.

Once your resistor values are chosen, solve the DC values of V_{D2}, V_{S2} and V_{G2} and verify that $M2$ is in saturation. Record your final expressions and calculated values in a table like this one:

Parameter	Expression	Calculated Value	Parameter	Value	$M2$ Operating Region	(check one)
R_{in}			$V_{GS2} - V_{T0}$		linear	
A_{CG}			V_{S2}		triode	
R_2			V_{G2}		saturation	
R_3			V_{D2}		cutoff	
I_{D2}			V_{DS2}			

Record all derivations and calculations in your lab book. In your final report, give the derived expressions and calculated values in a table.

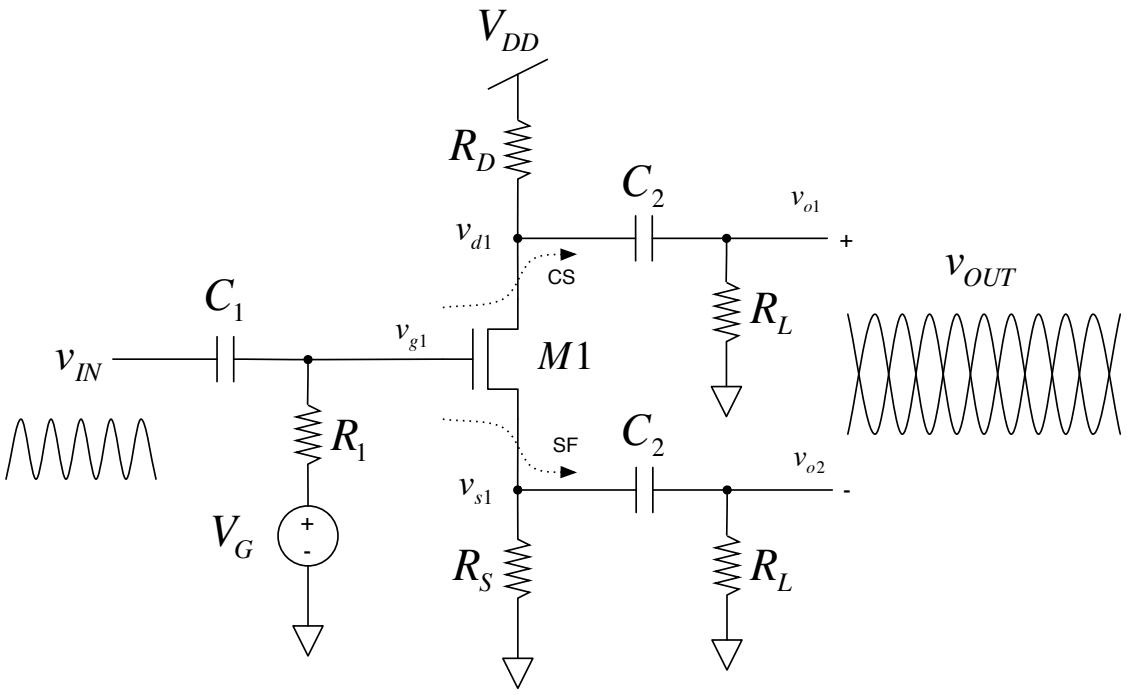

Figure 1: A MOSFET active balun circuit.

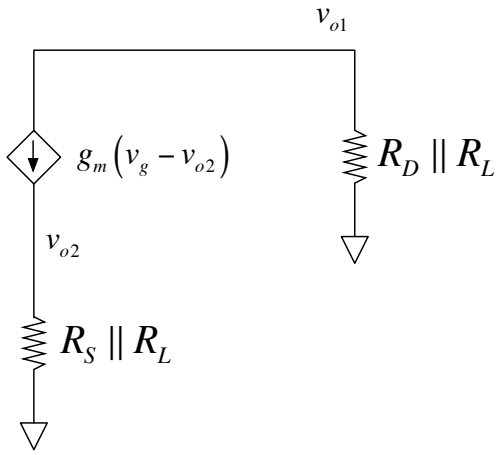

Figure 2: Small-signal mid-band equivalent circuit for the active balun.

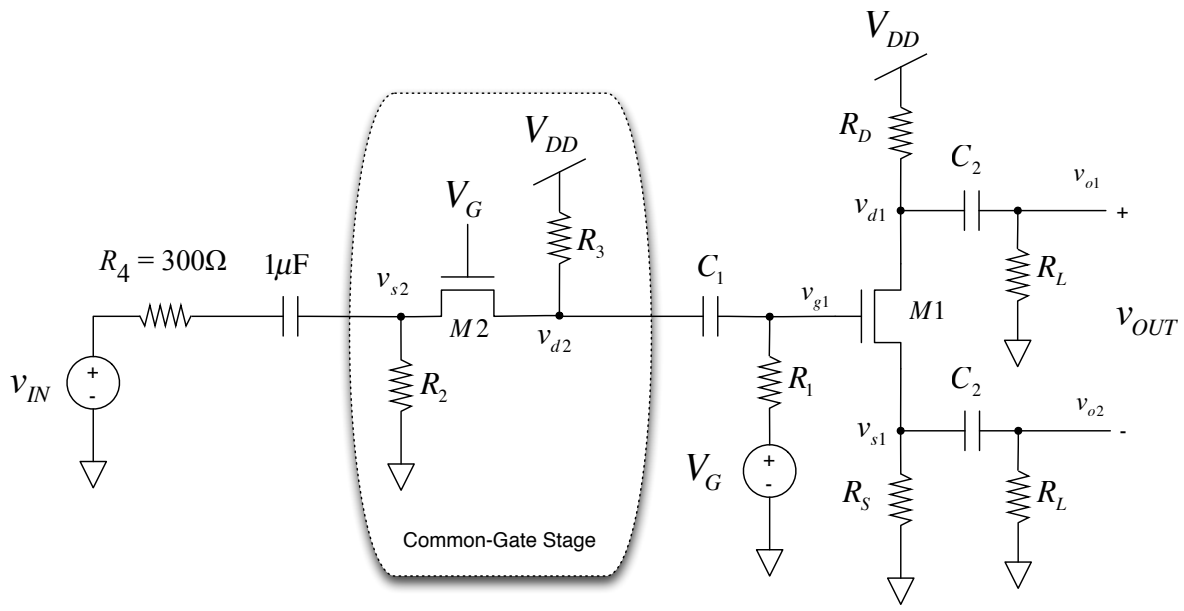

Figure 3: A common-gate circuit is inserted to match the balun's input impedance.

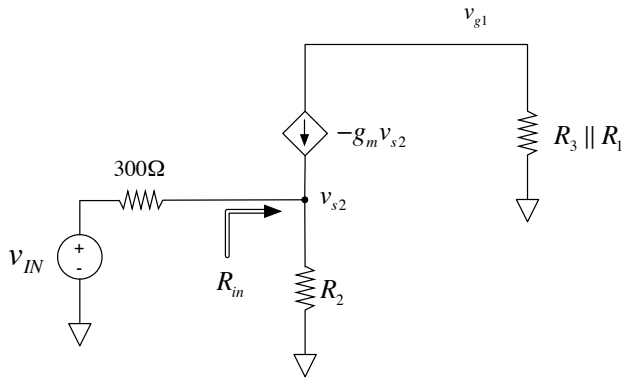

Figure 4: Small-signal mid-band equivalent circuit for the common-gate stage.

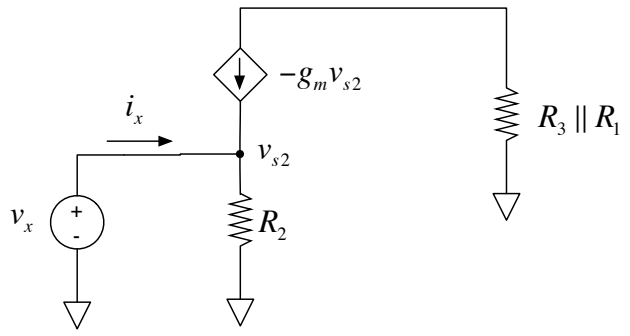

Figure 5: Model for calculating the effective input resistance, R_{in}, of the Common-Gate amplifier.

Table 1: Given Data for the Active Balun Circuit.

Component	Description	Value
C_1	Input bypass capacitor.	20μF
R_1	Input high-pass filter resistor.	100kΩ
C_2	Output bypass capacitor.	1μF
R_L	Load resistance.	2kΩ
V_{DD}	Main supply voltage	10V

Table 2: Device data for CD4007 NMOS component.

Parameter	Description	Value
$\mu_N C_{ox}\left(\frac{W}{L}\right)$	Scale constant.	$333\mu\text{A}/\text{V}^2$
V_{T0}	Threshold voltage.	2.0V

Exercise 3. You should now have a complete active balun design with values for all components and bias voltages. Create a SPICE description of the active balun circuit with Common-Gate input stage (Fig. 3). For the input signal, use a 50kHz sinusoidal voltage source with a peak-to-peak amplitude of 1V. Perform a transient simulation covering three periods of the input signal. **Plot the single-ended input and the differential output signals, and include these plots in your lab book and final report.**

Verify that the output signals are *amplitude-balanced* and *phase-balanced*. To do this, measure the amplitude of v_{o1} and v_{o2}. If their amplitudes are equal, then the signal is amplitude balanced. If they are not equal, **record the amount of amplitude imbalance in your lab book, and explain what design change could be made to improve the amplitude balance**.

Measure the amplitude imbalance as the difference in amplitudes, in dBm:

$$\Delta A = 20\log\left(\frac{|A_{CS}+A_{SF}|}{0.001}\right),$$

where A_{CS} is assumed to be a negative quantity, and A_{SF} is assumed to be positive.

To measure the phase balance, zoom in to where the transient output curves cross zero. They should ideally cross zero at the same time. If they don't, measure the time difference, Δt, between the zero-crossings. Then the phase imbalance is given by

$$\Delta\phi = 2\pi f \Delta t.$$

Record the phase imbalance in your lab book, and include it in your final report. Also include your SPICE input file as an appendix to the report.

2 Physical Experiments

Procedure 1. First construct the active balun circuit of Fig. 1[1]. Use the bench power supply to provide $V_{DD} = 10V$, and to provide the desired gate bias voltage V_G.Use the digital multimeter to precisely measure the value of all resistances. Record these measurements in a table in your lab book.

Procedure 2. Measure the DC operating point.

Step A. Step Use the digital multimeter to measure the DC voltage at every node in your circuit.

Step B. Use the multimeter to measure the bias current, I_D, by connecting the meter probes *in series* between R_D and V_{DD}.

Step C. Record the measurements in a table and compare them with your design predictions.

[1] **Caution**: CMOS devices are very sensitive to electro-static discharge (ESD). To avoid damaging your components, always touch a grounded surface before handling any MOS chips. Ideally, you should wear a grounded wrist strap when handling sensitive components.

Step D. Re-calculate your design predictions using the measured resistor values, and add these results to your table.

Step E. Take note of any remaining discrepancies, and try to explain them in your report.

Procedure 3. Verify the small-signal behavior.

Step A. Connect the function generator to create a 50kHz signal with a peak-to-peak amplitude of 1V. Verify the waveform using the oscilloscope before connecting it to your circuit.

Step B. After the waveform is verified, connect it to your circuit. Use the oscilloscope probe to measure the output waveforms v_{o1} and v_{o2}.

Step C. If you are using a digital-capture oscilloscope, record the waveform and include it in your lab book and final report. Alternatively, use a digital camera to take a snapshot of the scope display. As a last resort, you may sketch the waveform, but be sure to include as much detail as possible.

Procedure 4. Measure the amplitude balance.

Step A. Using the oscilloscope, obtain precise measurements of v_{in}, v_{o1} and v_{o2}.

Step B. Record a table of gain values in your lab book:

$$A_{CS} = \frac{v_{o1}}{v_{in}}$$
$$A_{SF} = \frac{v_{o2}}{v_{in}}$$
$$A_d = \frac{v_{o1} + v_{o2}}{v_{in}}.$$

Step C. Do the measured results agree with the predictions? How much amplitude imbalance is observed?

- Record the measurements in a table and compare them with your design predictions.
- Re-calculate your design predictions using the measured resistor values, and add these results to your table.
- Take note of any remaining discrepancies, and try to explain them in your report.

Step D. Include the amount of amplitude imbalance in your final report.

Procedure 5. Measure the phase balance.

Step A. Use the zero-crossing procedure to measure the phase imbalance of your circuit.

Step B. Record this value in your lab book and include it in your final report.

Procedure 6. Build and verify the Common-Gate stage.

Step A. Disconnect the function generator from your circuit, and construct the Common-Gate circuit of Fig. 3.Use the digital multimeter to measure the precise value of all resistors.Record these measurements in a table in your lab book.

Step B. Measure the DC voltages and bias current of the Common-Gate stage.

- Record the measurements in a table and compare them with your design predictions.
- Re-calculate your design predictions using the measured resistor values, and add these results to your table.
- Take note of any remaining discrepancies, and try to explain them in your report.

Step C. Connect the signal generator to your circuit as indicated in Fig. 3.

Step D. Verify the input impedance as follows. First, use the oscilloscope to precisely measure the amplitudes of v_{in} , v_{g2} and v_{g1}.

- The ratio of amplitudes is $v_{g2}/v_{in} = R_{in}/(R_{in}+R_4)$.
- Using this formula and your measurement of R_4, determine the value of R_{in}.
- Also calculate the gain $A_{CG} = v_{g1}/v_{g2}$.
- Record this measurement in your lab book, and in your final report.

3 Report

Your final report should be a carefully written, formal summary of your lab results. It should include the following specific information:

- A short introduction (one or two paragraphs) to the balun circuit, identifying its applications and explaining how it works.
- Your derived expressions for the gains and input resistance: A_{CS}, A_{SF}, A_d, A_{CG} and R_{in}. It is not necessary to include the details of your derivation if they are in your lab book and have been checked by the instructor or TA.
- A table reporting the DC operating point, the small-signal gains, and the input resistance of your circuit. Include three columns:
  - Your original design predictions.
  - Your revised predictions based on measured resistor values.
  - Your actual measurements.
- Your measured amplitude and phase imbalance, as measured from SPICE simulations and the actual circuit.
  - If you observed significant imbalance, offer a reasonable hypothesis to explain why. Suggest at least one solution to remove the imbalance.
- A plot showing your SPICE transient simulation results.
- A figure showing the oscilloscope waveform from the lab.
- Conclusions should summarize the success of your design choices and succinctly report any pitfalls that may affect users of this circuit in the future.
- Your SPICE circuit description should be attached as an appendix.