Lab 4 – Diodes

Objectives

- To execute the instructions of Lab 4 as provided for ECE 3410 from Canvas (https://usu.instructure.com/).
  - Gain practical experience with the behavior of silicon diodes under forward and reverse bias.
  - Explore the use of diode devices in rectifying, limiting, and DC restoration circuits.

Preparation

Component and Materials
- 10kΩ resistor (1)
- 10nF capacitor (1)
- 1N914 diodes (4)
- Datasheet for the 1N914 diodes

Equipment
- Banana Cable Sets (5)
- Oscilloscope Probes (2)
- BNC-to-BNC Cable (1)
- BNC-to-Alligator Cable (1)

Pre-Lab Analysis

➤Analytical

$R = 10\ \text{k}\Omega \quad C = 10\ \text{nF} \quad n = \text{Grading Coefficient},\ \approx 2$

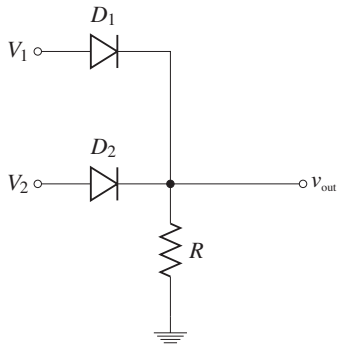
$V_D = \text{Forward Voltage Drop, } 655\ \text{mV}$

$I_D = \text{Forward Current, } 1\ \text{mA}$

Exercise 1

V_1	V_2	$v_{out} = \max(V_1, V_2) - V_D$	$v_{out} = \min(V_1, V_2) + V_D$
3.0 V	2.0 V	3.0 V − 655 mV = 2.345 V	2.0 V + 655 mV = 2.655 V
3.0 V	2.8 V	3.0 V − 655 mV = 2.345 V	2.8 V + 655 mV = 3.455 V
3.0 V	3.2 V	3.2 V − 655 mV = 2.545 V	3.0 V + 655 mV = 3.655 V
3.0 V	4.0 V	4.0 V − 655 mV = 3.345 V	3.0 V + 655 mV = 3.655 V

Figure 1: Diode logic circuits.



max-value configuration with V_D drop

Exercise 2

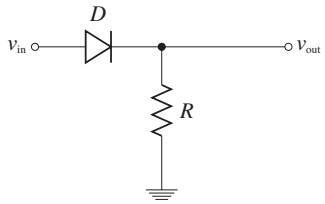
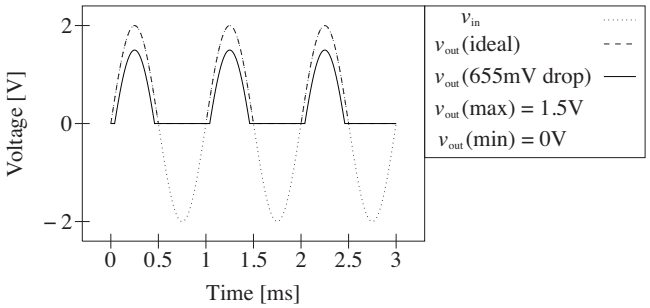
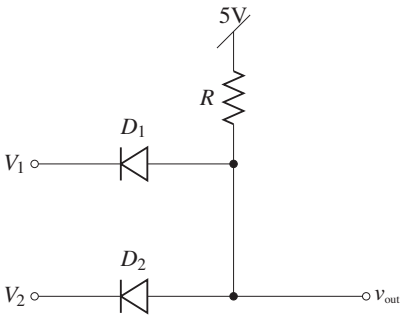


Figure 2: Half-wave rectifier circuit.





min-value configuration with V_D drop

Exercise 3

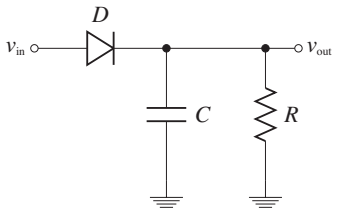
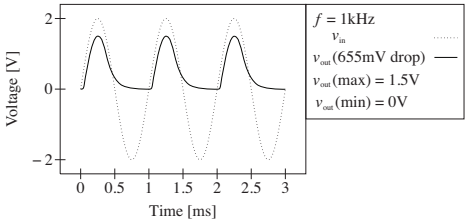
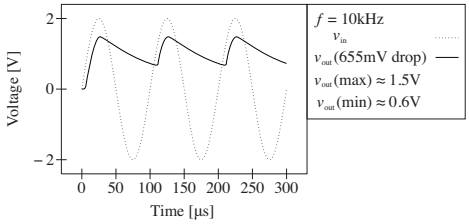
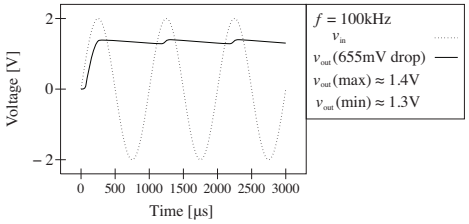


Figure 3: Peak rectifier circuit.







Exercise 4

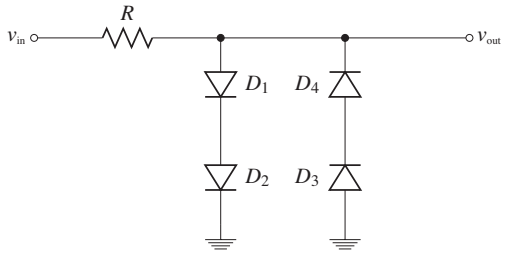
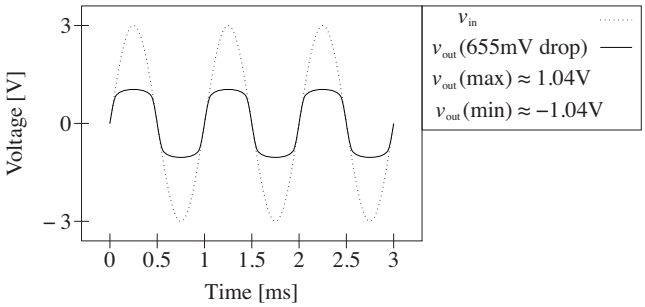


Figure 4: Voltage limiter circuit.



Exercise 5

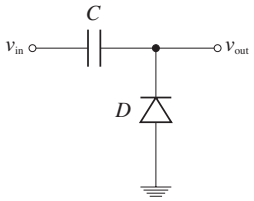
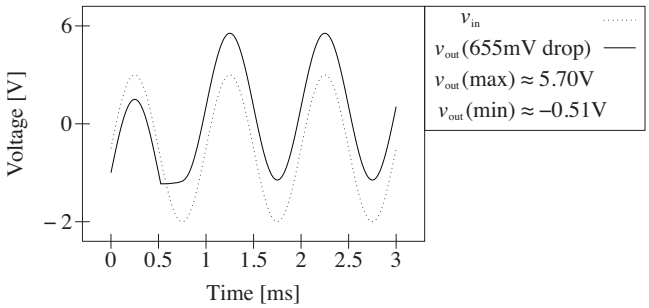


Figure 5: DC restoration circuit.



➤Calculated

exercise0.sp >>

```
* Test diode forward drop
.include ../lab_parts.md

V1 n1 0  DC 1V
D1 n1 n2 D1N914
R1 n2 0  10k

.control
DC V1 0 50 0.01

let vd=v(n1)-v(n2)
let id=-i(V1)
plot id vs vd

echo Forward drop at 1mA:
meas DC vd0 FIND vd WHEN id=1mA
.endc
.end
```

See Plot E.0 in Appendix.

exercise2.sp >>

```
Lab 4, Exercise 2, ECE 3410
**************************
* By Chris Winstead
* Modified by Joel Meine
* Diode Half-Wave Rectifier circuit
**************************

* Include the model file:
.include ../lab_parts.md

* Voltage Inputs
Vin n1 0 DC 0V SIN(0 2V 1k)

* Diodes
D1 n1 nout D1N914

* Resistors
R1 nout 0 10k

**************
* ANALYSIS
**************
.control
tran 10us 2ms
plot v(nout)
hardcopy halfwave.ps v(nout)

meas TRAN vpeak MAX v(nout)
.endc
.end
```

exercise1a.sp >>

```
Lab 4, Exercise 1(A), ECE 3410
**************************
* By Chris Winstead
* Diode MAX circuit
**************************

* Include the model file:
.include ../lab_parts.md

* Voltage Inputs
V1 n1 0 DC 3V
V2 n2 0 DC 2V

* Diodes
D1 n1 nout D1N914
D2 n2 nout D1N914

* Load resistor
R1 nout 0 10k

**************
* ANALYSIS
**************
.control
op
print v(n1) v(n2) v(nout)

alter V2 DC 2.8V
op
print v(n1) v(n2) v(nout)

alter V2 DC 3.2V
op
print v(n1) v(n2) v(nout)

alter V2 DC 4V
op
print v(n1) v(n2) v(nout)

DC V2 0 6 0.1
plot v(nout) v(n1) v(n2)
plot 'v(nout)-v(n2)'

let vd=v(nout)-v(n2)
meas DC vdmin MIN vd
.endc
.end
```

exercise3.sp >>

```
Lab 4, Exercise 3, ECE 3410
**************************
* By Chris Winstead
* Peak rectifier circuit
**************************

* Include the model file:
.include ../lab_parts.md

* Voltage Inputs
V1 n1 0 DC 0V SIN(0 2V 1k)

* Diode
```

exercise1b.sp >>

```
Lab 4, Exercise 1(B), ECE 3410
**************************
* By Chris Winstead
* Modified by Joel Meine
* Diode MIN circuit
**************************

* Include the model file:
.include ../lab_parts.md

* Voltage Inputs
V1 n1 0 DC 3V
V2 n2 0 DC 2V
V3 n3 0 DC 5V

* Diodes
D1 nout n1 D1N914
D2 nout n2 D1N914

* Load resistor
R1 nout n3 10k

**************
* ANALYSIS
**************
.control
op
print v(n1) v(n2) v(nout)

alter V2 DC 2.8V
op
print v(n1) v(n2) v(nout)

alter V2 DC 3.2V
op
print v(n1) v(n2) v(nout)

alter V2 DC 4V
op
print v(n1) v(n2) v(nout)

DC V2 0 6 0.1
plot v(nout) v(n1) v(n2)
plot 'v(nout)-v(n2)'

let vd=v(nout)-v(n2)
meas DC vdmin MIN vd
.endc
.end
```

exercise4.sp >>

```
Lab 4, Exercise 4, ECE 3410
**************************
* By Chris Winstead
* Limiter circuit
**************************

* Include the model file:
.include ../lab_parts.md

* Voltage Inputs
V1 n1 0 DC 0V SIN(0 3V 1k)
```

exercise5.sp >>

```
Lab 4, Exercise 5, ECE 3410
**************************
* By Chris Winstead
* Modified by Joel Meine
* Clamped-Capacitor circuit
**************************

* Include the model file:
.include ../lab_parts.md

* Voltage Inputs
Vin n1 0 DC 0V SIN(1V 3V 1k)

* Diode
D1 0 nout D1N914

* Capacitor
C1 n1 nout 10n

**************
* ANALYSIS
**************
.control
tran 1u 5m
plot n(n1) v(nout)
hardcopy clampedcap.ps n(n1) v(nout)

* Measurements:
echo Results at 1kHz:
meas TRAN vpeak   MAX v(nout)
meas TRAN vtrough MIN v(nout)
meas TRAN vpp     PP  v(nout)
FROM=3m TO=5m
.endc
.end
```

```
D1 n1 nout D1N914

* Load resistor
R1 nout 0 10k
C1 nout 0 10nF

**************
* ANALYSIS
**************
.control
tran 1u 5m
plot v(n1) v(nout)
echo Results at 1kHz:
meas TRAN vpeak MAX v(nout)
meas TRAN vpp PP v(nout)
FROM=3m TO=5m

alter @V1[sin] = [ 0 2V 10k ]
tran .1u .5m
plot v(n1) v(nout)
echo Results at 10kHz:
meas TRAN vpeak MAX v(nout)
meas TRAN vpp PP v(nout)
FROM=.3m TO=.5m

alter @V1[sin] = [ 0 2V 100k ]
tran .01u .05m
plot v(n1) v(nout)
echo Results at 100kHz:
meas TRAN vpeak MAX v(nout)
meas TRAN vpp PP v(nout)
FROM=.03m TO=.05m
.endc
.end
```

```
* Diode
D1 nout n2   D1N914
D2 n2   0    D1N914
D3 n3   nout D1N914
D4 0    n3   D1N914

* Resistor
R1 n1 nout 10k

**************
* ANALYSIS
**************
.control
tran 1u 5m
plot n(n1) v(nout)

* Measurements:
meas TRAN vpeak   MAX v(nout)
meas TRAN vtrough MIN v(nout)
meas TRAN vpp     PP  v(nout)
FROM=3m TO=5m
.endc
.end
```

log.txt >>

exercise1a.sp >>

```
v(n1) = 3.0
v(n2) = 2.0
v(nout) = 2.470

v(n1) = 3.0
v(n2) = 2.8
v(nout) = 2.471

v(n1) = 3.0
v(n2) = 3.2
v(nout) = 2.667

v(n1) = 3.0
v(n2) = 4.0
v(nout) = 3.452

See Plot E.1A in Appendix.
```

exercise1b.sp >>

```
v(n1) = 3.0
v(n2) = 2.0
v(nout) = 2.530

v(n1) = 3.0
v(n2) = 2.8
v(nout) = 3.310

v(n1) = 3.0
v(n2) = 3.2
v(nout) = 3.504

v(n1) = 3.0
v(n2) = 4.0
v(nout) = 3.505

See Plot E.1B in Appendix.
```

exercise2.sp >>

```
vpeak = 1.495

See Plot E.2 in Appendix.
```

exercise3.sp >>

```
Results at 1kHz:
vpeak = 1.495
vpp = 1.493

See Plot E.3A in Appendix.

Results at 10kHz:
vpeak = 1.478
vpp = 0.813

See Plot E.3B in Appendix.

Results at 100kHz:
vpeak = 1.402
vpp = 0.115

See Plot E.3C in Appendix.
```

exercise4.sp >>

```
vpeak = 1.037
vtrough = -1.037
vpp = 2.074

See Plot E.4 in Appendix.
```

exercise5.sp >>

```
vpeak = 5.701
vtrough = -0.515
vpp = 6.006

See Plot E.5 in Appendix.
```

Lab Experiments

Procedure 1

V_1	V_2	Measured (V_{OUT}), max	Measured (V_{OUT}), min
3.0 V	2.0 V	2.45 V (0.8% err.)	2.55 V (0.8% err.)
3.0 V	2.5 V	2.46 V (0.4% err.)	3.03 V (0.3% err.)
3.0 V	3.0 V	2.48 V (0.8% err.)	3.48 V (0.3% err.)
3.0 V	3.5 V	2.95 V (0.3% err.)	3.53 V (0.9% err.)
3.0 V	4.0 V	3.43 V (0.6% err.)	3.53 V (0.9% err.)

Procedure 2

Forward Bias Duration, Calc. =	500 µs
Forward Bias Duration, Meas. =	440 µs
Forward Bias Duration, Err. =	12.8%
Peak Output Voltage, Calc. =	1.50 V
Peak Output Voltage, Meas. =	1.42 V
Peak Output Voltage, Err. =	5.5%
Output Voltage (Rev. Bias), Calc. =	0.00 V
Output Voltage (Rev. Bias), Meas. =	0.04 V
Output Voltage (Rev. Bias), Err. =	200.0%

Procedure 3

Frequency (f)	Measured (V_{OUT}), Pk-Pk
1 kHz	1.44 V (3.4% err.)
10 kHz	0.84 V (3.6% err.)
100 kHz	0.12 V (0.0% err.)

Procedure 4

v_{in}, Pk-Pk	V_{OUT}, Calc. Pk-Pk	V_{OUT}, Meas. Pk-Pk	V_{OUT}, Err.
1.0 V	0.98 V	1.00 V	2.0%
4.0 V	1.94 V	2.00 V	3.0%

Procedure 5

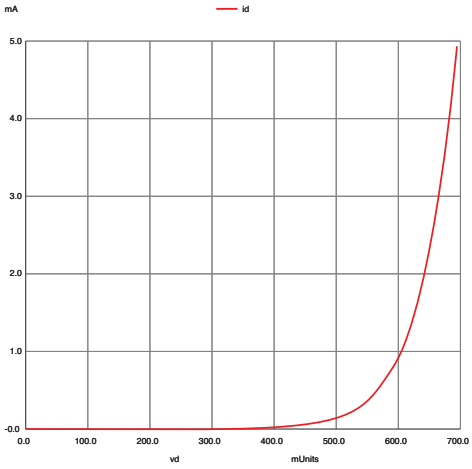
V_{OUT}, Calc. min	V_{OUT}, Meas. min	V_{OUT}, Err.
-515 mV	-480 mV	7.0%

Commentary

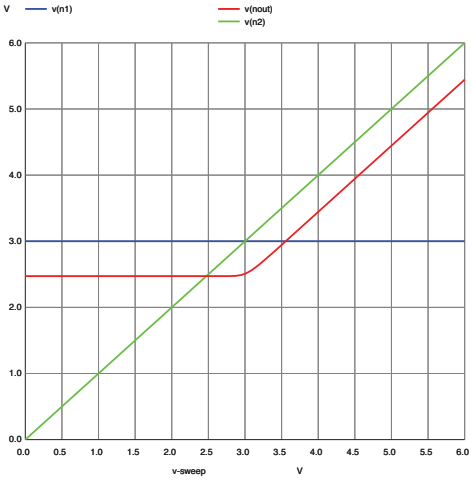
- Improved familiarization and increased experience was obtained in silicon diode behavior analysis and calculations under forward and reverse bias conditions. Additionally, the effects of signal rectifying, limiting, and DC restoration for specific diode circuit configurations was observed and analyzed.
- The results derived from the analytical, calculated, and experimental methods of the lab for exercise 1 and the associated procedure 1 yielded positive correlation and consistency with marginal error. This demonstrates that the simple maximum and minimum voltage detector circuits using diodes yields reliable results when using DC voltage input.
- Conversely, while the analytical and calculated results of exercise 2 positively correlated with each other, the experimental analysis in the associated procedure 2 yielded results within acceptable tolerances, but not marginal error.
- Likewise, while the analytical and calculated results of exercise 3 positively correlated with each other, the experimental analysis in the associated procedure 3 yielded results within acceptable tolerances, but not marginal error; at least at the frequencies of 1 kHz and 10 kHz. At the frequency 100 kHz, the measured voltage output was nearly identical to the calculated value. However, with the expected voltage output yielding a very small peak-to-peak value, the oscilloscope was at the limit of its viewable scale since the output signal appears as nearly a straight, horizontal line. Therefore it was expected that the oscilloscope cursors would appear as being a single horizontal line.
- Finally, the results derived from the analytical, calculated, and experimental methods of the lab for exercises 4 and 5 and associated procedures 4 and 5 also yielded positive correlation and consistency but only within acceptable tolerances. Consistent with the calculated and experimental observations, the clipping voltage in procedure 4 is only known to exist somewhere between a peak-to-peak voltage of 1 V and 4 V. The lab instructions of procedure 4 does not stipulate for a more exact measurement of the clipping voltage or analysis thereof.

Appendix

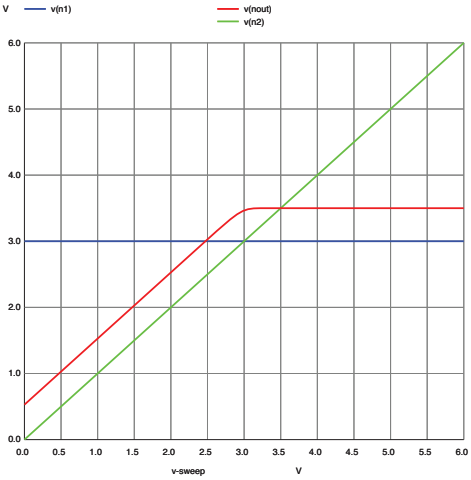
Plot E.0



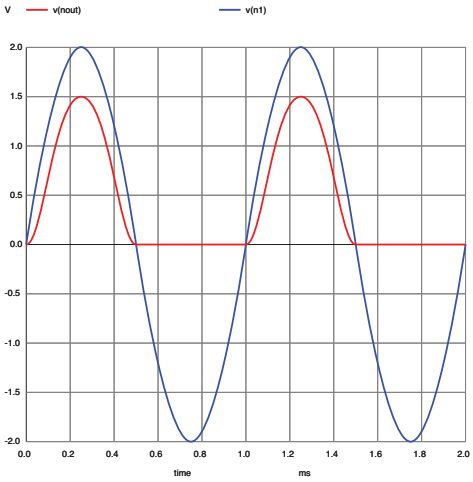
Plot E.1A



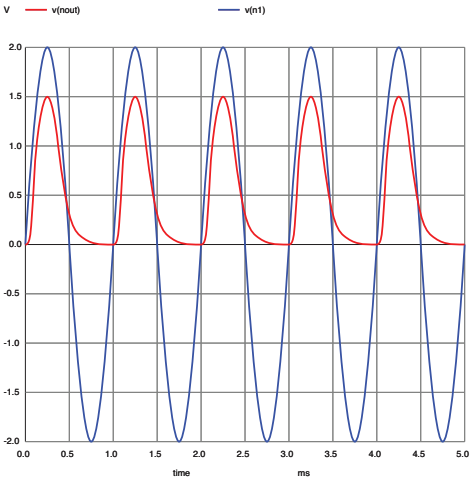
Plot E.1B



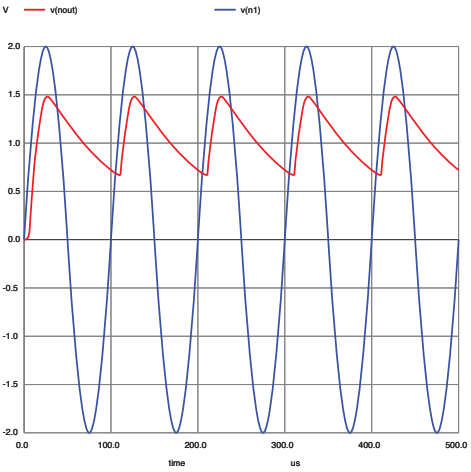
Plot E.2



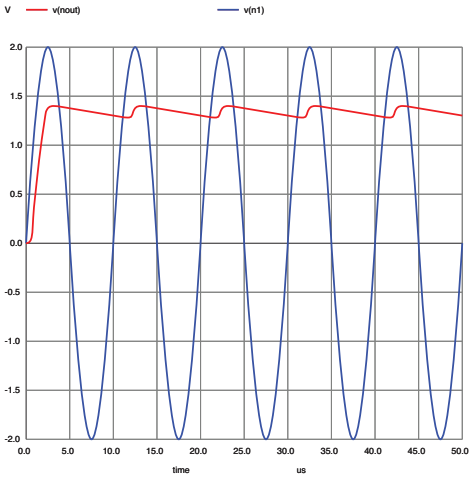
Plot E.3A



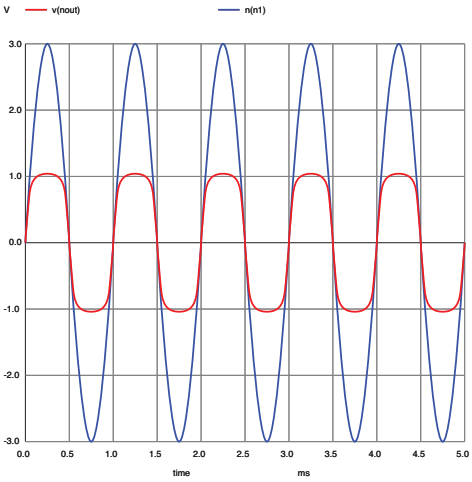
Plot E.3B



Plot E.3C



Plot E.4



Plot E.5