Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 6, 14:00

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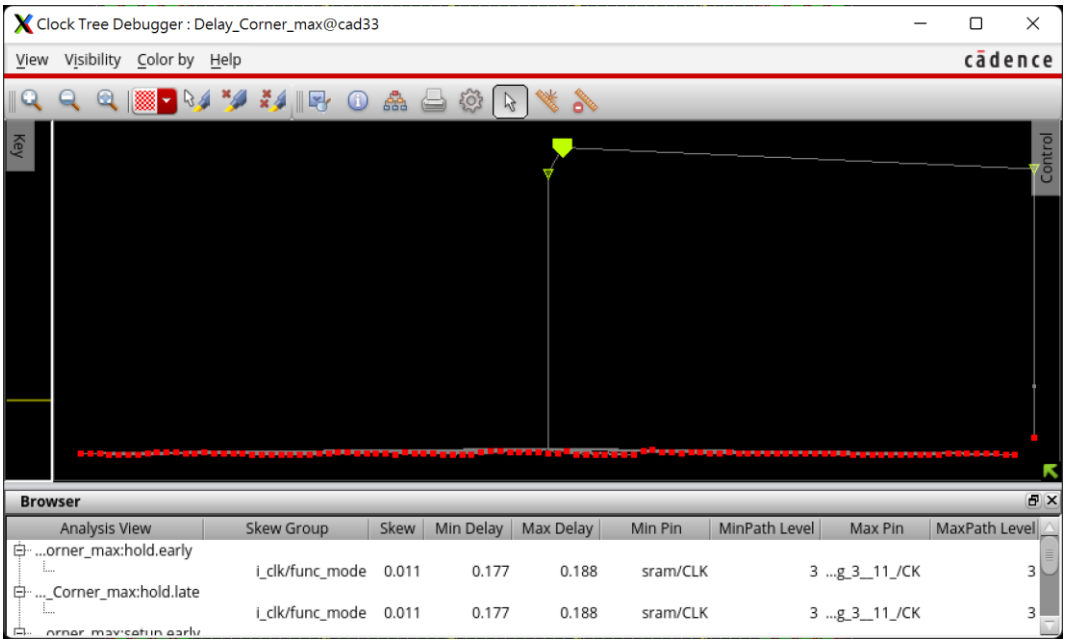
APR Results

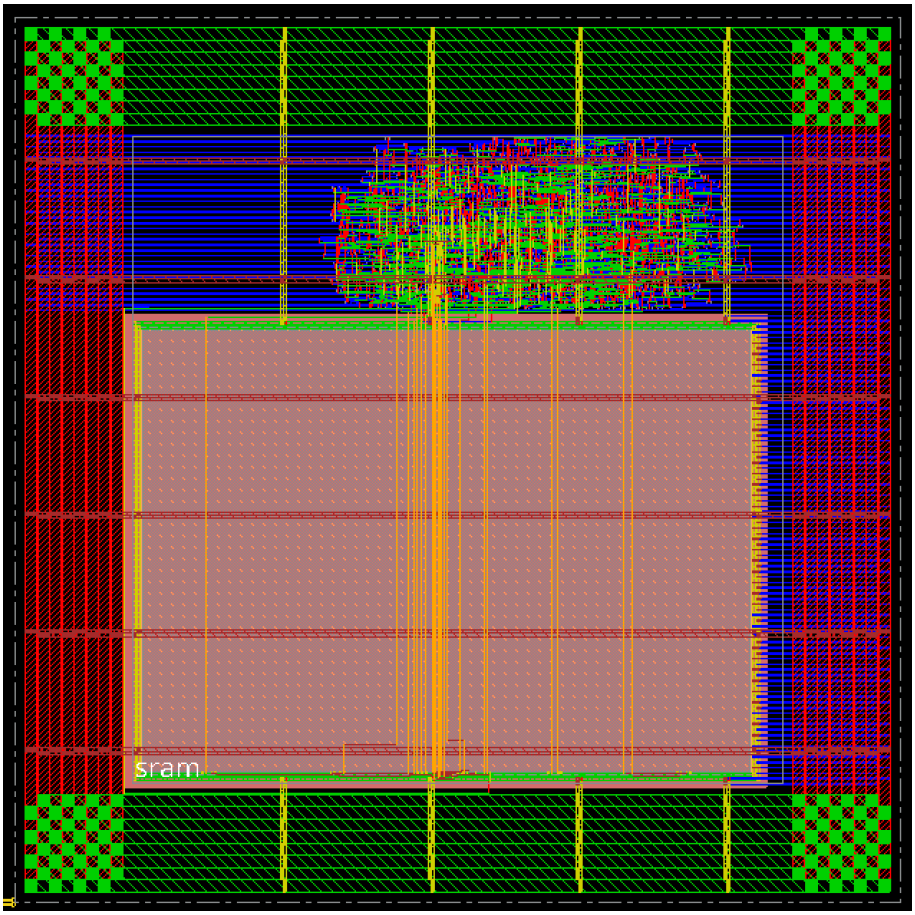
1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	359802.03
	Core Area (um^2)	193103.01
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	10ns
Follow your design in HW3? (If not, write down the student ID of the designer)		Yes

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result, and show the routing result in the layout (10%).





2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
*** Starting Verify DRC (MEM: 1723.7) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 201.280 201.280} 1 of 9
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {201.280 0.000 402.560 201.280} 2 of 9
 VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {402.560 0.000 599.840 201.280} 3 of 9
 VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 201.280 201.280 402.560} 4 of 9
 VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {201.280 201.280 402.560 402.560} 5 of 9
 VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {402.560 201.280 599.840 402.560} 6 of 9
 VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 402.560 201.280 599.830} 7 of 9
 VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {201.280 402.560 402.560 599.830} 8 of 9
 VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {402.560 402.560 599.840 599.830} 9 of 9
 VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.6  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Dec  3 10:38:22 2022

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (599.8400, 599.8300)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Dec  3 10:38:22 2022
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.2  MEM: 0.000M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.004  |  0.315  |  2.051  |  0.004  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   168   |   113   |   45    |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 17.995%
Total number of glitch violations: 0
------------------------------------------------------------
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.655  |  0.655  |  3.251  |  4.129  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   168   |   113   |   45    |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 17.995%
------------------------------------------------------------
```

4. Show the critical path after post-route optimization. What is the path type? (5%) (The slack of the critical path should match the smallest slack in the timing report)

   This critical path belongs to reg2out.

```
Path 1: MET Late External Delay Assertion
Endpoint:   o_out_data[6] (^) checked with  leading edge of 'i_clk'
Beginpoint: sram/Q[6]     (^) triggered by  leading edge of 'i_clk'
Path Groups: {reg2out}
Analysis View: av_func_mode_max
Other End Arrival Time          0.000
- External Delay                3.250
+ Phase Shift                   6.500
+ CPPR Adjustment               0.000
= Required Time                 3.250
- Arrival Time                  3.246
= Slack Time                    0.004
     Clock Rise Edge                      0.000
     + Clock Network Latency (Prop)       0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------+
     | Instance |       Arc       |    Cell     | Delay | Arrival | Required |
     |          |                 |             |       |  Time   |   Time   |
     |----------+-----------------+-------------+-------+---------+----------|
     | sram     | CLK ^           |             |       |   0.000 |    0.004 |
     | sram     | CLK ^ -> Q[6] ^ | sram_4096x8 | 2.635 |   2.636 |    2.639 |
     | U1383    | A ^ -> Y v      | NAND2X2     | 0.057 |   2.693 |    2.697 |
     | U1384    | B0 v -> Y ^     | OAI31X4     | 0.528 |   3.220 |    3.224 |
     |          | o_out_data[6] ^ |             | 0.026 |   3.246 |    3.250 |
     +-------------------------------------------------------------------------+
```

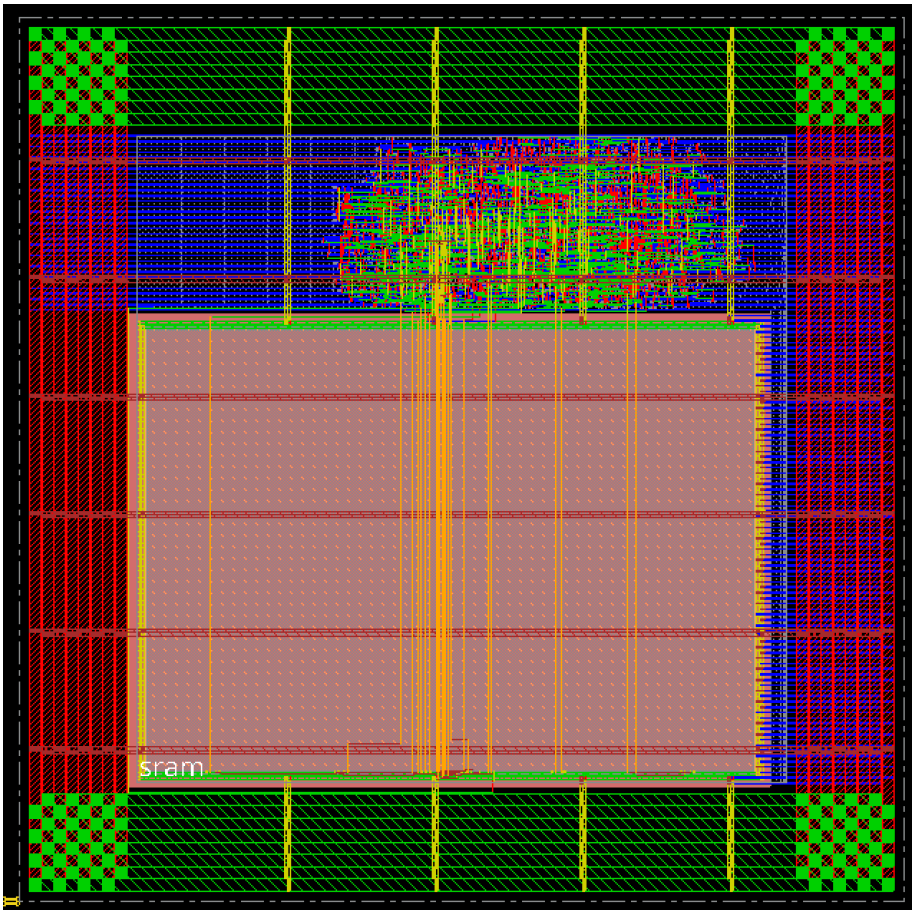
5. Attach the snapshot of GDS stream out messages. (10%)

```
Merging with GDS libraries
Scanning GDS file gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file gds/sram_4096x8.gds to register cell name ......
Merging GDS file gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file gds/sram_4096x8.gds ......
        ****** Merge file: gds/sram_4096x8.gds has version number: 5.
        ****** Merge file: gds/sram_4096x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
************************* Analyze Floorplan **************************
    Die Area(um^2)             : 359802.03
    Core Area(um^2)            : 193103.01
    Chip Density (Counting Std Cells and MACROs and IOs): 49.942%
    Core Density (Counting Std Cells and MACROs): 93.056%
    Average utilization        : 100.000%
    Number of instance(s)      : 4177
    Number of Macro(s)         : 1
    Number of IO Pin(s)        : 32
    Number of Power Domain(s) : 0
************************* Estimation Results **************************
***********************************************************************
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

   Since I only use one SRAM, I put the SRAM on the corner of the design and make the i/o pin facing to the center. I think it is helpful for routing. Besides, I add block halo around SRAM in order to keeping out standard cells.