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Homework 1

1. A MISD, or Multiple Instruction, Single Data, processor is unusual for it processes the same information multiple times as a safeguard against data corruption. It relies on its redundant data processing to ensure accurate calculations and is used in instruments that rely on high precision and reliable calculations such as a missile or rocket.

2. Instruction-level parallelism is the ability to process multiple instructions at the same time/ in parallel. Three implemented forms of this are: Out-of-Order, Superscalar, and Speculative Execution. Superscalar processors can execute two or more processes at a single time, while Out-Of-Order processors execute processes within the most efficient order (as long as they do not have any limiting dependencies). Speculative Execution processors, on the other hand, try to predict the next instruction and complete it. This optimizes a running a process by feeding it the needed information and preventing wait time delays.

   Temporal parallelism, also called pipelining, is partitioning of a process/task into units. This allows the overlapping of multiple instructions in a clock cycle. The greater the number of partitions, the greater possibility for overlap.

   Thread-level parallelism is the capability of software to run routines of code that are independent of the main program; it contains all the data and instructions necessary for it to execute by itself.

   Process level parallelism is the act of dividing up a program into multiple threads across multiple processors. For this type of parallelism, one may use the MPI interface to help synchronize and communicate processes.

   Data parallelism is the act of have the same data set process by multiple programs or processes at the same time.

3. Amdahl's Law

$$S(P) = \frac{1}{F + \frac{(1-F)}{P}}$$

Percent of Sequential: 30%
Percent of Parallelizable: 70%

A) # of CPU = 1

$$S(1) = \frac{1}{\frac{3}{10} + \frac{(\frac{7}{10})}{1}} = \frac{1}{\frac{3}{10} + \frac{7}{10}} = \frac{1}{1} = 1$$

B) # of CPU = 2

$$S(2) = \frac{1}{\frac{3}{10} + \frac{(\frac{7}{10})}{2}} = \frac{1}{\frac{6}{20} + \frac{7}{20}} = \frac{20}{13} = 1.53846$$

C) # of CPU = 4

$$S(4) = \frac{1}{\frac{3}{10} + \frac{(\frac{7}{10})}{4}} = \frac{1}{\frac{12}{40} + \frac{7}{40}} = \frac{40}{19} = 2.10526$$

D) # of CPU = 8

$$S(8) = \frac{1}{\frac{3}{10} + \frac{(\frac{7}{10})}{8}} = \frac{1}{\frac{24}{80} + \frac{7}{80}} = \frac{80}{31} = 2.5806$$

E) # of CPU = 16

$$S(16) = \frac{1}{\frac{3}{10} + \frac{(\frac{7}{10})}{16}} = \frac{1}{\frac{48}{160} + \frac{7}{160}} = \frac{160}{55} = 2.90909091$$

F) # of CPU = Infinity

$$S(\infty) = \frac{1}{\frac{3}{10} + \frac{(\frac{7}{10})}{\infty}} = \frac{1}{\frac{3}{10} + 0} = \frac{10}{3} = 3.333333\ldots$$

4.
Number of Vertices: 20 Nodes
Span/Longest Path: 9 Node $Tp = \frac{T1}{P}$

$T_1 = 20$;
$T_5 = 20/5 = 4$
$T_6 = 20/6 = 3.3333\ldots$
The critical path is of length 9.

5. Concurrency is the superset of parallelism. Concurrency is the act of having two or more processes alive at the same time as well as switching between them while processing I/O. This is done by the use of a scheduler that decides which process will run by switching them in and out. Parallelism is the act of having two processes alive and executed at the same time by the processor. For this to happen, the processor must have at least 2 cores in order to process both.w

6. Cache is a nice compromise between the fast processor and the slower DRAM. Instead of having the processor constantly read/write data to and from the DRAM, it can store frequently needed data in the cache. There, it saves on time by having the information readily available within 1-2 clock cycles. On multicore processors, having an efficient and working cache is harder to implement due to the known cache coherency problem (trying to keep information up to date while having more than cores trying to access the same information). Generally, cache for a multicore processor has 2 levels where each core has its individual 1st tier layer as well as group shared 2nd tier cache. Some have additional 3rd layers. For a single core processor everything is dedicated for the single core.