CD74HCT4052, CD54/74HC4053, CD54/74HC54053
HIGH-SPEED CMOS LOGIC ANALOG MULTIPLEXERS/DEMULTIPLEXERS

Check for Samples: CD/74HC4051, CD54/74HCT4051, CD54/74HC4052,

FEATURES

- **Wide Analog Input Voltage Range. . ±5 V Max**
- **Low ON Resistance**
  - **70 Ω Typical (V_{CC} – V_{EE} = 4.5 V)**
  - **40 Ω Typical (V_{CC} – V_{EE} = 9 V)**
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **Break-Before-Make Switching**
- **Wide Operating Temperature Range –55°C to 125°C**
- **CD54HC/CD74HC Types**
  - **Operation Control Voltage . . . . . 2 V to 6 V**
  - **Switch Voltage . . . . . 0 V to 10 V**

  «
- **CD54HCT/CD74HCT Types**
  - **Operation Control Voltage . . . 4.5 V to 5.5 V**
  - **Switch Voltage . . . . . 0 V to 10 V**
  - **Direct LSTTL Input Logic Compatibility V_{IL} = 0.8 V Max, V_{IH} = 2 V Min**
  - **CMOS Input Compatibility I_I ≤ 1 µA at V_{OL}, V_{OH}**

DESCRIPTION

These devices are digitally controlled analog switches which utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low ON resistance and low OFF leakages. In addition, all three devices have an enable control which, when high, disables all switches to their OFF state.

ORDERING INFORMATION(1)

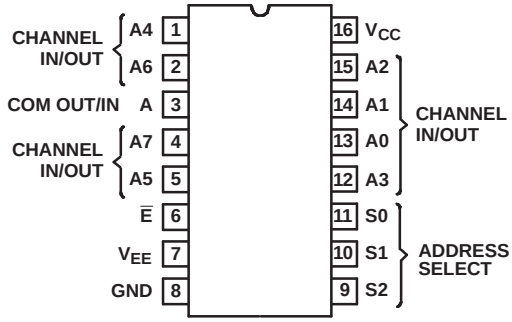
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4051F3A	–55 to 125	16 Ld CERDIP
CD54HC4052F3A	–55 to 125	16 Ld CERDIP
CD54HC4053F3A	–55 to 125	16 Ld CERDIP
CD54HCT4051F3A	–55 to 125	16 Ld CERDIP
CD74HC4051E	–55 to 125	16 Ld PDIP
CD74HC4051M	–55 to 125	16 Ld SOIC
CD74HC4051MT	–55 to 125	16 Ld SOIC
CD74HC4051M96G3	–55 to 125	16 Ld SOIC
CD74HC4051NSR	–55 to 125	16 Ld SOP
CD74HC4051PWR	–55 to 125	16 Ld TSSOP
CD74HC4051PWT	–55 to 125	16 Ld TSSOP
CD74HC4052E	–55 to 125	16 Ld PDIP
CD74HC4052M	–55 to 125	16 Ld SOIC
CD74HC4052MT	–55 to 125	16 Ld SOIC
CD74HC4052M96G3	–55 to 125	16 Ld SOIC
CD74HC4052NSR	–55 to 125	16 Ld SOP
CD74HC4052PW	–55 to 125	16 Ld TSSOP
CD74HC4052PWR	–55 to 125	16 Ld TSSOP

(1) When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

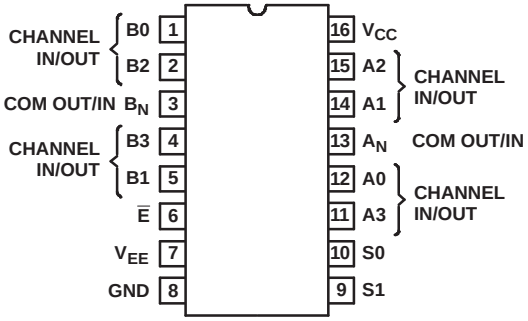
ORDERING INFORMATION(1) (continued)

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4052PWT	–55 to 125	16 Ld TSSOP
CD74HC4053E	–55 to 125	16 Ld PDIP
CD74HC4053M	–55 to 125	16 Ld SOIC
CD74HC4053MT	–55 to 125	16 Ld SOIC
CD74HC4053M96G3	–55 to 125	16 Ld SOIC
CD74HC4053NSR	–55 to 125	16 Ld SOP
CD74HC4053PW	–55 to 125	16 Ld TSSOP
CD74HC4053PWRG3	–55 to 125	16 Ld TSSOP
CD74HC4053PWT	–55 to 125	16 Ld TSSOP
CD74HCT4051E	–55 to 125	16 Ld PDIP
CD74HCT4051M	–55 to 125	16 Ld SOIC
CD74HCT4051MT	–55 to 125	16 Ld SOIC
CD74HCT4051M96	–55 to 125	16 Ld SOIC
CD74HCT4052E	–55 to 125	16 Ld PDIP
CD74HCT4052M	–55 to 125	16 Ld SOIC
CD74HCT4052MT	–55 to 125	16 Ld SOIC
CD74HCT4052M96	–55 to 125	16 Ld SOIC
CDHCT4053E	–55 to 125	16 Ld PDIP
CDHCT4053M	–55 to 125	16 Ld SOIC
CDHCT4053MT	–55 to 125	16 Ld SOIC
CDHCT4053M96	–55 to 125	16 Ld SOIC
CDHCT4053PWR	–55 to 125	16 Ld TSSOP
CDHCT4053PWT	–55 to 125	16 Ld TSSOP

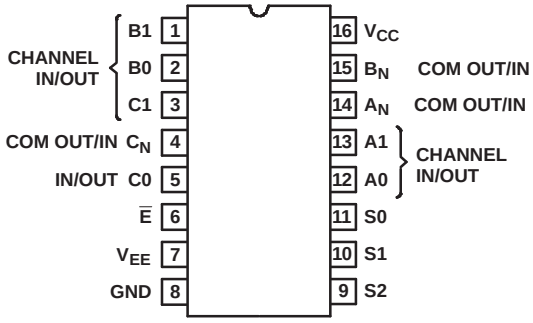
CD54HC4051, CD54HCT4051
(CERDIP)
CD74HC4051
(PDIP, SOIC, SOP, TSSOP)
CD74HCT4051
(PDIP, SOIC)
TOP VIEW



CD54HC4052
(CERDIP)
CD74HC4052
(PDIP, SOIC, SOP, TSSOP)
CD74HCT4052
(PDIP, SOIC)
TOP VIEW



CD54HC4053
(CERDIP)
CD74HC4053
(PDIP, SOIC, SOP, TSSOP)
CD74HCT4053
(PDIP, SOIC, TSSOP)
TOP VIEW



FUNCTIONAL DIAGRAM OF HC/HCT4051

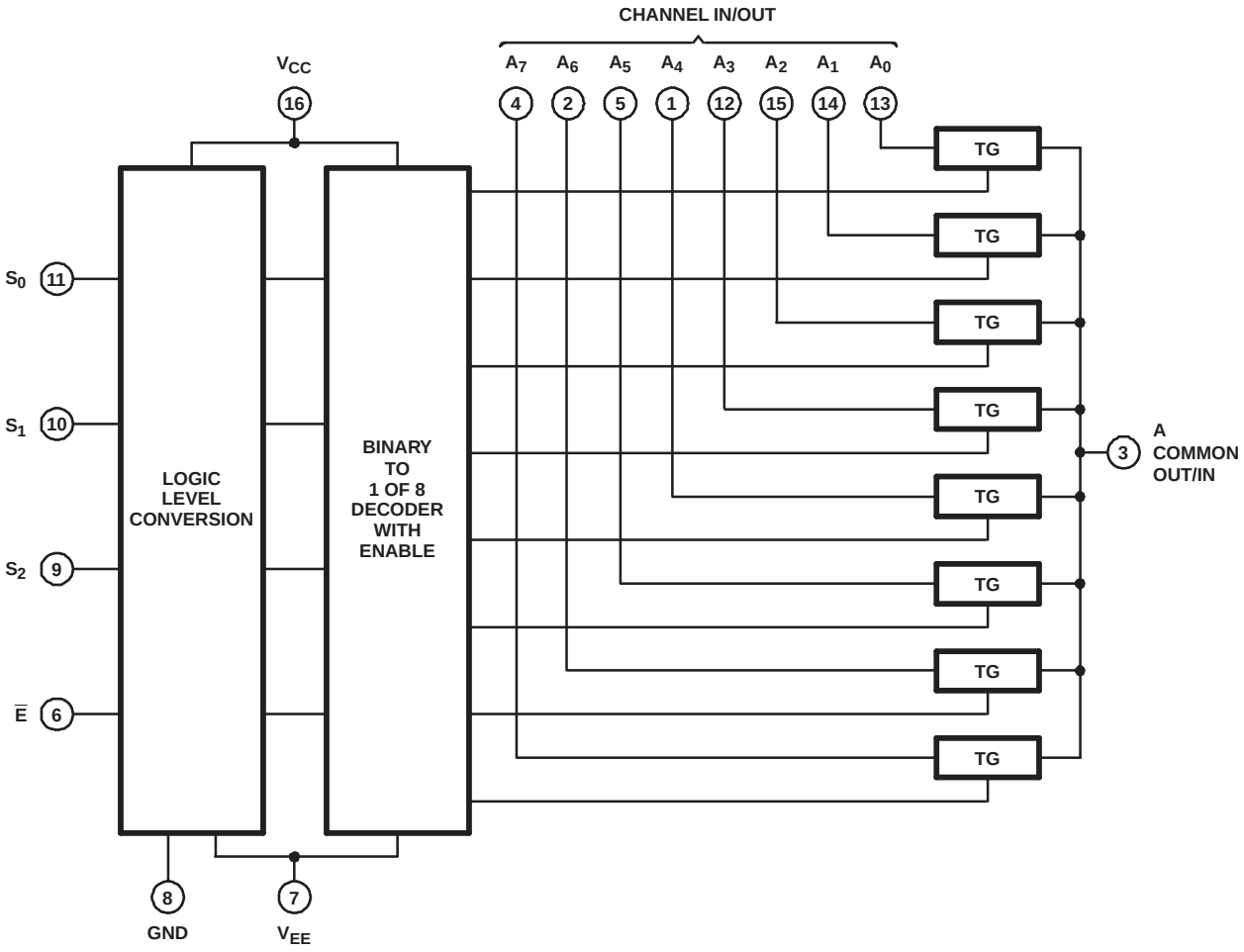


Table 1. TRUTH TABLE 'HC/CD74HCT4051 (1)

INPUT STATES				ON CHANNELS
ENABLE	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

(1) X = Don't care

FUNCTIONAL DIAGRAM OF HC4052, CD74HCT4052

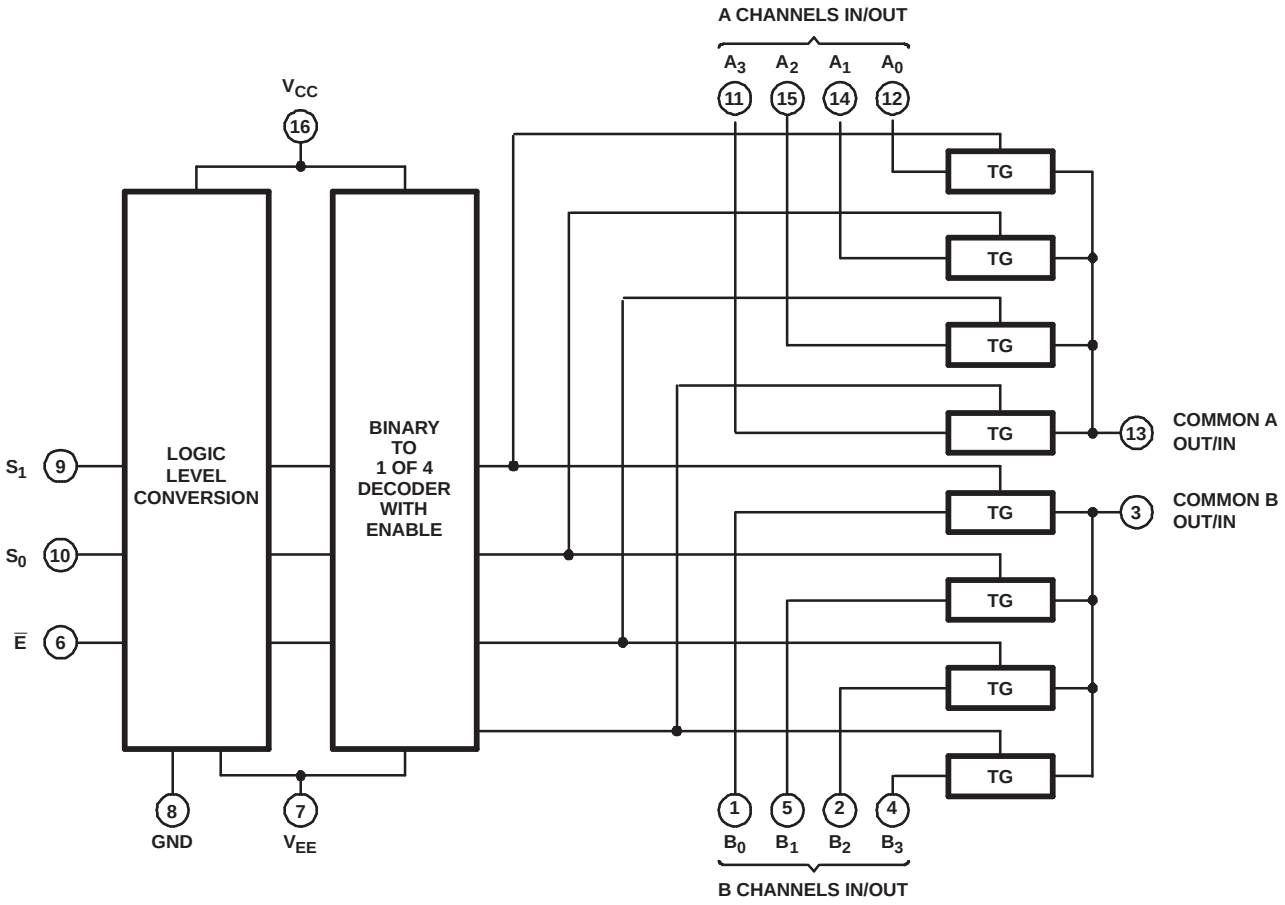


Table 2. FUNCTION TABLE 'HC4052, CD74HCT4052(1)

INPUT STATES			ON CHANNELS
ENABLE	S_1	S_0	
L	L	L	A0, B0
L	L	H	A1, B1
L	H	L	A2, B2
L	H	H	A3, B3
H	X	X	None

(1) X = Don't care

FUNCTIONAL DIAGRAM OF 'HC4053, CD74HCT4053

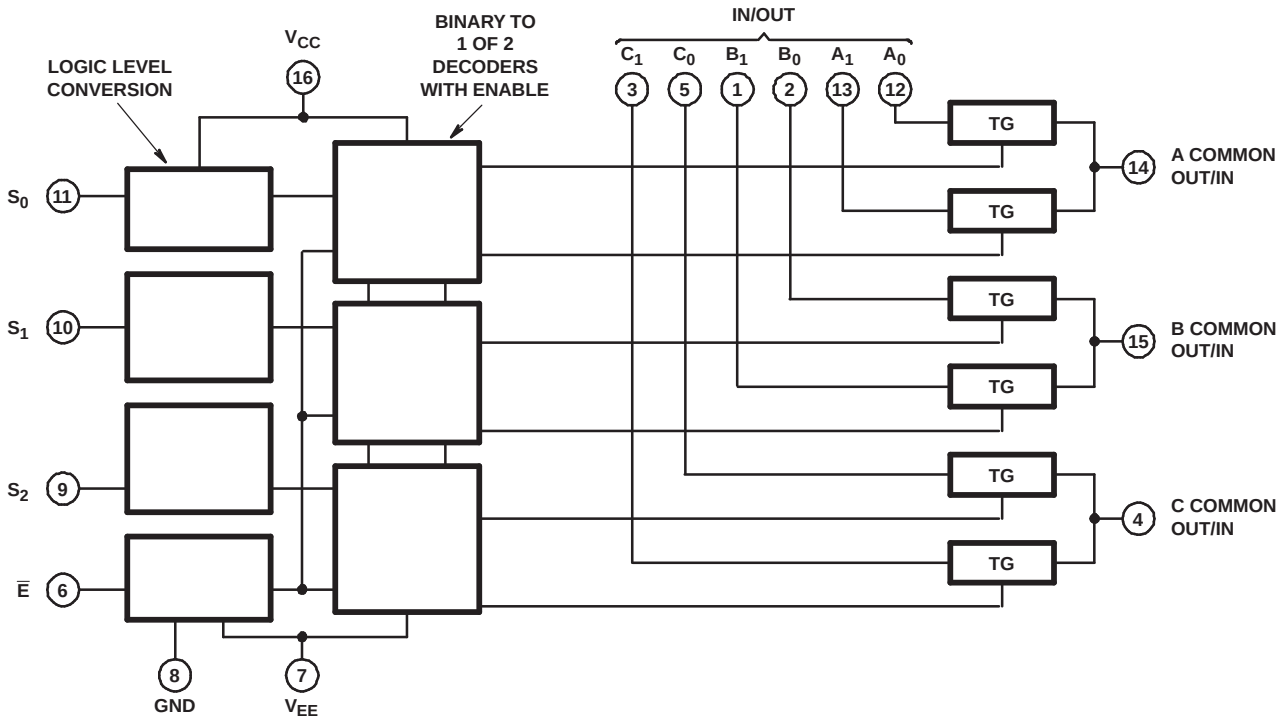


Table 3. FUNCTION TABLE 'HC4053, CD74HCT4053(1)

INPUT STATES				ON CHANNELS
ENABLE	S_0	S_1	S_2	
L	L	L	L	C0, B0, A0
L	H	L	L	C0, B0, A1
L	L	H	L	C0, B1, A0
L	H	H	L	C0, B1, A1
L	L	L	H	C1, B0, A0
L	H	L	H	C1, B0, A1
L	L	H	H	C1, B1, A0
L	H	H	H	C1, B1, A1
H	X	X	X	None

(1) X = Don't care

Absolute Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} – V_{EE}	DC supply voltage		–0.5	10.5	V
V_{CC}	DC supply voltage		–0.5	7	V
V_{EE}	DC supply voltage		0.5	–7	V
I_{IK}	DC input diode current	V_I < – 0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	DC switch diode current	V_I < V_{EE} – 0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
	DC switch current	V_I > V_{EE} – 0.5 V or V_I < V_{CC} + 0.5 V		±25	mA
I_{CC}	DC V_{CC} or ground current			±50	mA
I_{EE}	DC V_{EE} current			–20	mA
θ_{JA}	Package thermal impedance(3)	E (PDIP) package		67	°C/W
		M (SOIC) package		73	
		NS (SOP) package		64	
		PW (TSSOP) package		108	
	Maximum junction temperature			150	°C
	Maximum storage temperature range		–65	150	°C
	Maximum lead temperature (soldering 10 s)			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND unless otherwise specified.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

PARAMETER			MIN	MAX	UNIT
V_{CC} (1)	Supply voltage range (T_A = full package temperature range)	CD54/74HC types	2	6	V
		CD54/74HCT types	4.5	5.5	
V_{CC} – V_{EE}	Supply voltage range (T_A = full package temperature range)	CD54/74HC types, CD54/74HCT types (see Figure 1)	2	10	V
V_{EE} (2)	Supply voltage range (T_A = full package temperature range)	CD54/74HC types, CD54/74HCT types (see Figure 2)	0	–6	V
V_I	DC input control voltage		GND	V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}	V_{CC}	V
T_A	Operating temperature		–55	125	°C
t_r, t_f	Input rise and fall times	2 V	0	1000	ns
		4.5 V	0	500	
		6 V	0	400	

(1) All voltages referenced to GND unless otherwise specified.
(2) In certain applications, the external load resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{ON} values shown in Electrical Specifications table). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4051; terminals 3 and 13 on the HC/HCT4052; terminals 4, 14, and 15 on the HC/HCT4053.

Recommended Operating Area as a Function of Supply Voltages

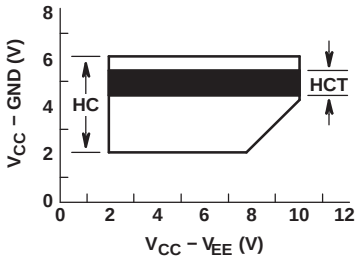


Figure 1.

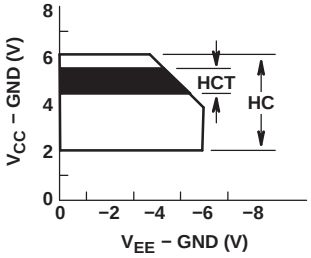


Figure 2.

DC Electrical Specifications

PARAMETER			TEST CONDITIONS				AMBIENT TEMPERATURE, T_A							UNIT
							25°C			–40°C to 85°C		–55°C to 125°C		
			V_{IS} (V)	V_I (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC Types														
V_{IH}	High-level input voltage					2	1.5			1.5		1.5		V
						4.5	3.15			3.15		3.15	0	
						6	4.2			4.2		4.2		
V_{IL}	Low-level input voltage					2			0.5		0.5		0.5	V
						4.5			1.35		1.35		1.35	
						6			1.8		1.8		1.8	
r_{ON}	ON resistance	I_O = 1 mA (see Figure 11)	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5		70	160		200		240	Ω
					0	6		60	140		175		210	
					–4.5	4.5		40	120		150		180	
			V_{CC} to V_{EE}		0	4.5		90	180		225		270	
					0	6		80	160		200		240	
					–4.5	4.5		45	130		162		195	
Δr_{ON}	Maximum ON resistance between any two channels				0	4.5		10						Ω
					0	6		8.5						
					–4.5	4.5		5						
I_{IZ}	Switch ON/OFF leakage current	1 and 2 channels	For switch OFF: When V_{IS} = V_{CC}, V_{OS} = V_{EE} , When V_{IS} = V_{EE}, V_{OS} = V_{CC}, For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels	V_{IL} or V_{IH}	0	6			±0.1		±1		±1	µA
		4053			–5	5			±0.1		±1		±1	
		4 channels			0	6			±0.1		±1		±1	
		4052			–5	5			±0.2		±2		±2	
		8 channels			0	6			±0.2		±2		±2	
		4051			–5	5			±0.4		±4		±4	
I_{IL}	Control input leakage current			V_{CC} or GND	0	6			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	I_O = 0	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	V_{CC} or GND	0	6			8		80		160	µA
			When V_{IS} = V_{CC}, V_{OS} = V_{EE}		–5	5			16		160		320	µA

DC Electrical Specifications (Continued)

PARAMETER			TEST CONDITIONS				AMBIENT TEMPERATURE, T_A							UNIT
							25°C			–40°C to 85°C		–55°C to 125°C		
			V_{IS} (V)	V_I (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT Types														
V_{IH}	High-level input voltage					4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage					4.5 to 5.5			0.8		0.8		0.8	V
r_{ON}	ON resistance	I_O = 1 mA (see Figure 15)	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5		70	160		200		240	Ω
					–4.5	4.5		40	120		150		180	
			V_{CC} to V_{EE}		0	4.5		90	180		225		270	
					–4.5	4.5		45	130		162		195	
Δr_{ON}	Maximum ON resistance between any two channels				0	4.5		10						Ω
					–4.5	4.5		5						
I_{IZ}	Switch ON/OFF leakage current	1 and 2 channels	For switch OFF: When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$, When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels	V_{IL} or V_{IH}	0	6			±0.1		±1		±1	µA
		4053			–5	5			±0.1		±1		±1	
		4 channels			0	6			±0.1		±1		±1	
		4052			–5	5			±0.2		±2		±2	
		8 channels			0	6			±0.2		±2		±2	
		4051			–5	5			±0.4		±4		±4	
I_{IL}	Control input leakage current			(1)		5.5			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	I_O = 0	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$	V_{CC} or GND	0	5.5			8		80		160	µA
			When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$		–4.5	5.5			16		160		320	µA
ΔI_{CC} (2)	Additional quiescent device current per input pin: 1 unit load		ΔI_{CC} (2)	V_{CC} – 2.1		4.5 to 5.5		100	360		450		490	µA

(1) Any voltage between V_{CC} and GND
(2) For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

Table 4. HCT INPUT LOADING TABLE

TYPE	INPUT	UNIT LOADS (1)
4051, 4053	All	0.5
4052	All	0.4

(1) Unit load is ΔI_{CC} limit specified in DC Specifications table, e.g., 360 mA MAX at 25°C.

Switching Specifications

V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TEST CONDITIONS	CL (pF)	TYPICAL						UNIT
				4051		4052		4053		
				HC	HCT	HC	HCT	HC	HCT	
t_{PHL}, t_{PLH}	Propagation delay	Switch IN to OUT	15	4	4	4	4	4	4	ns
t_{PHZ}, t_{PLZ}		Switch turn-off (S or E)	15	19	19	21	21	18	18	
t_{PZH}, t_{PZL}		Switch turn-on (S or E)	15	19	23	27	29	18	20	
C_{PD} (1)	Power dissipation capacitance			50	52	74	76	38	42	pF

(1) C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_I + \sum (C_L + C_S) V_{CC}^2 f_O$
f_O = output frequency
f_I = input frequency
C_L = output load capacitance
C_S = switch capacitance
V_{CC} = supply voltage

Switching Specifications

C_L = 50 pF, input t_r, t_f = 6 ns

PARAMETER			V_{EE} (V)	V_{CC} (V)	AMBIENT TEMPERATURE, T_A								UNIT
					25°C				–40°C to 85°C		–55°C to 125°C		
					HC		HCT		HC	HCT	HC	HCT	
					MIN	MAX	MIN	MAX	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{PLH}, t_{PHL}	Propagation delay, switch in to out		0	2		60			75		90		ns
			0	4.5		12		12	15	15	18	18	
			0	6		10			13		15		
			–4.5	4.5		8		8	10	10	12	12	
t_{PHZ}, t_{PLZ}	Maximum switch turn OFF delay from S or $\overline{E}$ to switch output	4051	0	2		225			280		340		ns
			0	4.5		45		45	56	56	68	68	
			0	6		38			48		57		
			–4.5	4.5		32		32	40	40	48	48	
		4052	0	2		250			315		375		
			0	4.5		50		50	63	63	75	75	
			0	6		43			54		65		
			–4.5	4.5		38		38	48	48	57	57	
		4053	0	2		210			265		315		
			0	4.5		42		44	53	55	63	66	
			0	6		36			45		54		
			–4.5	4.5		29		31	36	39	44	47	
t_{PZL}, t_{PZH}	Maximum switch turn ON delay from S or $\overline{E}$ to switch output	4051	0	2		225			280		340		ns
			0	4.5		45		55	56	69	68	83	
			0	6		38			48		57		
			–4.5	4.5		32		39	40	49	48	59	
		4052	0	2		325			405		490		
			0	4.5		65		70	81	68	98	105	
			0	6		55			69		83		
			–4.5	4.5		46		48	58	60	69	72	
		4053	0	2		220			275		330		
			0	4.5		44		48	55	60	66	72	
			0	6		37			47		56		
			–4.5	4.5		31		34	39	43	47	51	
C_I	Input (control) capacitance					10		10	10	10	10	10	pF

Analog Channel Specifications

Typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	HC/HCT TYPES	V_{EE} (V)	V_{CC} (V)	HC/HCT	UNIT
C_I	Switch input capacitance		All			5	pF
C_{COM}	Common output capacitance		4051			25	pF
			4052			12	
			4053			8	
f_{MAX}	Minimum switch frequency response at –3 dB (see Figures 12, 14, 16)	See Figure 3 (1) (2)	4051	–2.25	2.25	145	MHz
			4052			165	
			4053			200	
			4051	–4.5	4.5	180	
			4052			185	
			4053			200	
	Sine-wave distortion	See Figure 5	All	–2.25	2.25	0.035	%
			All	–4.5	4.5	0.018	
	Switch OFF signal feedthrough (see Figures 13, 15, 17)	See Figure 7 (2) (3)	4051	–2.25	2.25	–73	dB
			4052			–65	
			4053			–64	
			4051	–4.5	4.5	–75	
			4052			–67	
			4053			–66	

(1) Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz
(2) V_{IS} is centered at (V_{CC} – V_{EE})/2.
(3) Adjust input for 0 dBm

APPLICATION INFORMATION

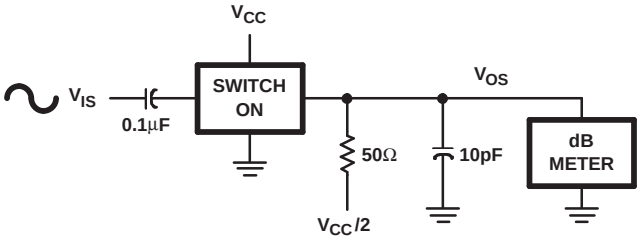


Figure 3. Frequency Response Test Circuit

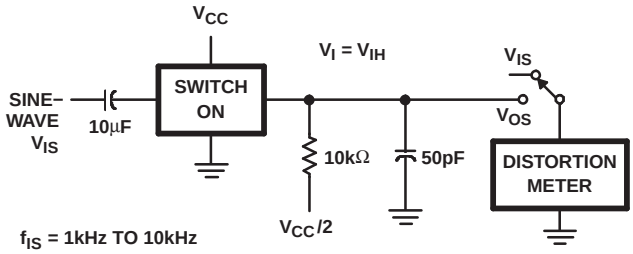


Figure 5. Sine-Wave Distortion Test Circuit

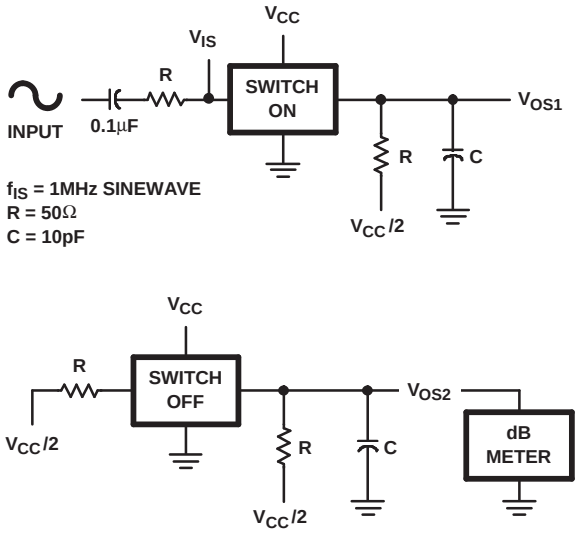


Figure 4. Crosstalk Between Two Switches Test Circuit

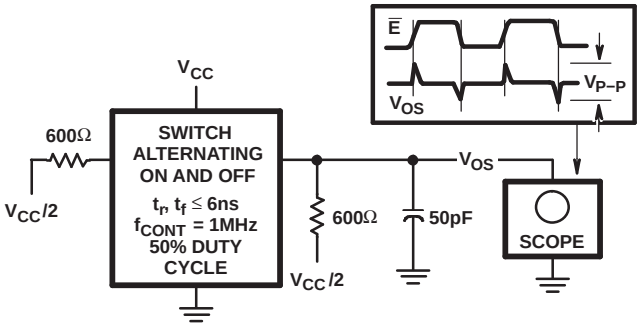


Figure 6. Control to Switch Feedthrough Noise Test Circuit

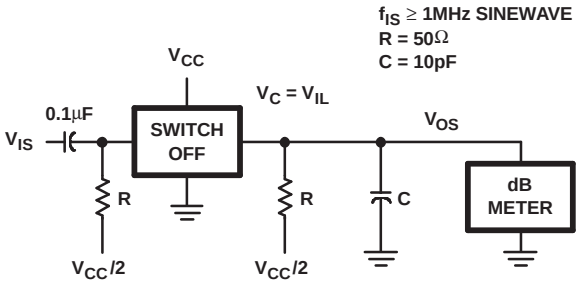


Figure 7. Switch OFF Signal Feedthrough

APPLICATION INFORMATION

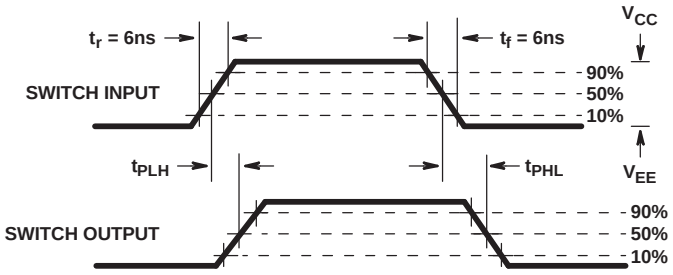


FIGURE 8A.

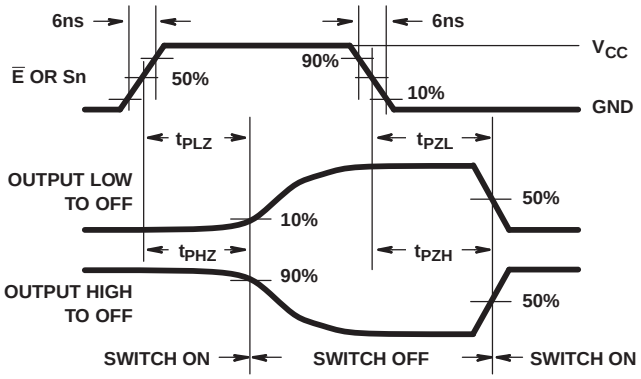


FIGURE 8B. HC TYPES

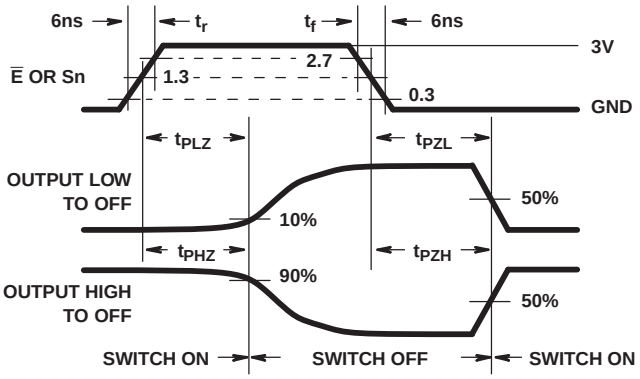


FIGURE 8C. HCT TYPES

Figure 8. Switch Propagation Delay, Turn-On, Turn-Off Times

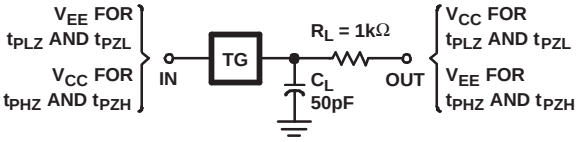


Figure 9. Switch ON/OFF Propagation Delay Test Circuit

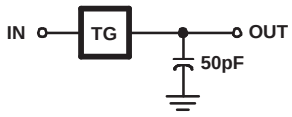


Figure 10. Switch In to Switch Out Propagation Delay Test Circuit

TYPICAL PERFORMANCE CURVES

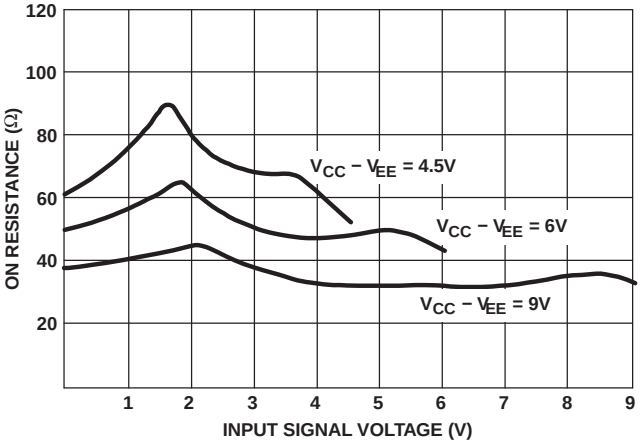


Figure 11. Typical ON Resistance vs Input Signal Voltage

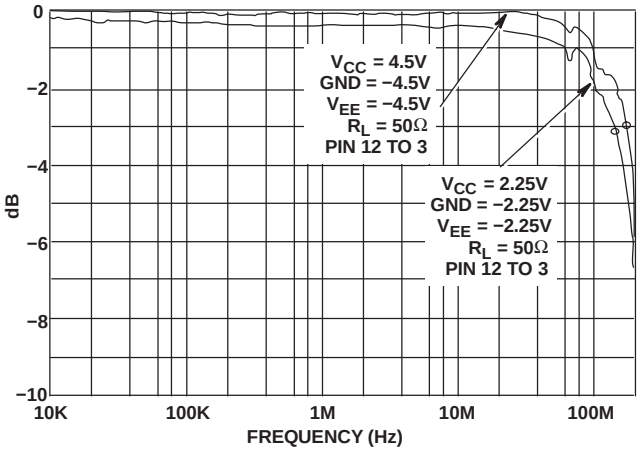


Figure 12. Channel ON Bandwidth (HC/HCT4051)

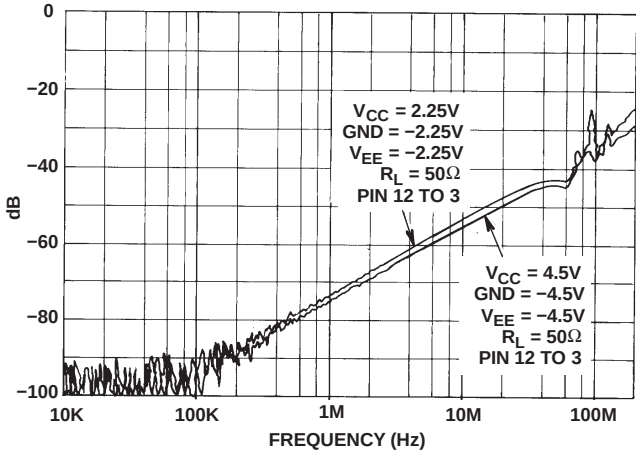


Figure 13. Channel OFF Feedthrough (HC/HCT4051)

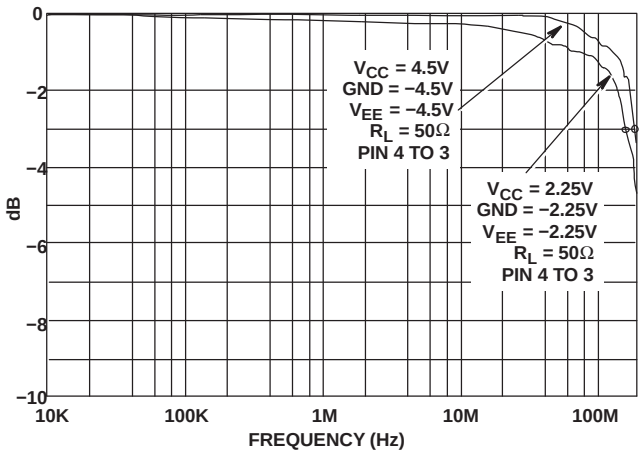


Figure 14. Channel ON Bandwidth (HC/HCT4052)

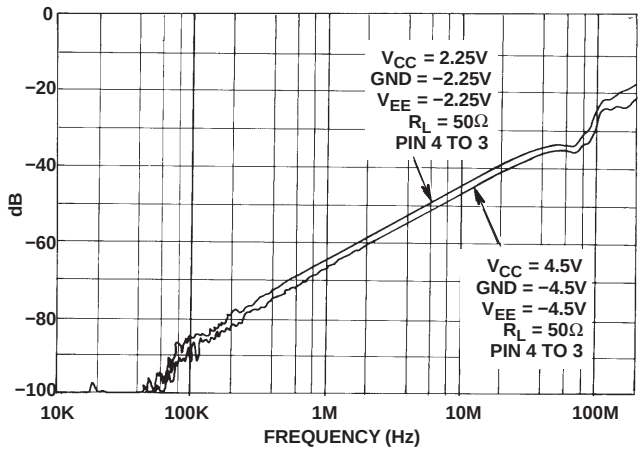


Figure 15. Channel OFF Feedthrough (HC/HCT4052)

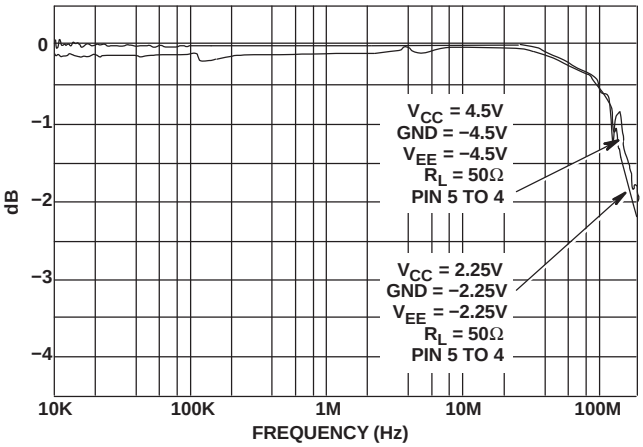


Figure 16. Channel ON Bandwidth (HC/HCT4053)

TYPICAL PERFORMANCE CURVES

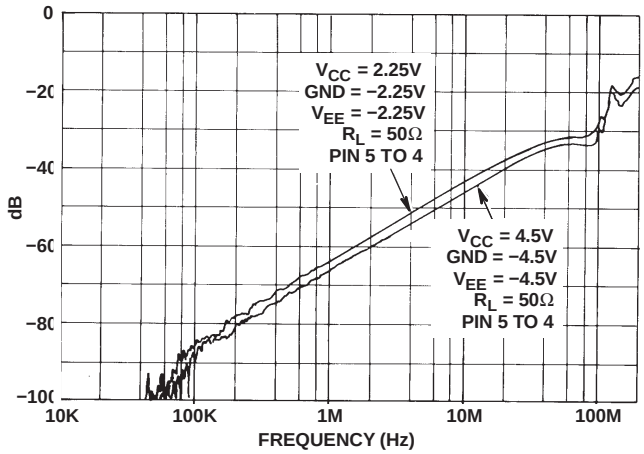


Figure 17. Channel OFF Feedthrough (HC/HCT4053)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8775401EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A	Samples
5962-8855601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A	Samples
5962-9065401MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9065401MEA CD54HCT4051F3A	Samples
CD54HC4051F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4051F	Samples
CD54HC4051F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4051F3A	Samples
CD54HC4052F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4052F	Samples
CD54HC4052F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A	Samples
CD54HC4053F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4053F	Samples
CD54HC4053F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A	Samples
CD54HCT4051F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9065401MEA CD54HCT4051F3A	Samples
CD74HC4051E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4051E	Samples
CD74HC4051EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4051E	Samples
CD74HC4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4051	Samples
CD74HC4051PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	Samples
CD74HC4051PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	Samples
CD74HC4051PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	Samples
CD74HC4052E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4052E	Samples
CD74HC4052EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4052E	Samples
CD74HC4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4052MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4053E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4053E	Samples
CD74HC4053EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4053E	Samples
CD74HC4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samples
CD74HC4053PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samples
CD74HC4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samples
CD74HC4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samples
CD74HC4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samples
CD74HCT4051E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4051E	Samples
CD74HCT4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4051MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samples
CD74HCT4052E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4052E	Samples
CD74HCT4052EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4052E	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4053E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4053E	Samples
CD74HCT4053EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4053E	Samples
CD74HCT4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	HK4053	Samples
CD74HCT4053PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	Samples
CD74HCT4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC4051, CD54HC4052, CD54HC4053, CD54HCT4051, CD74HC4051, CD74HC4052, CD74HC4053, CD74HCT4051 :

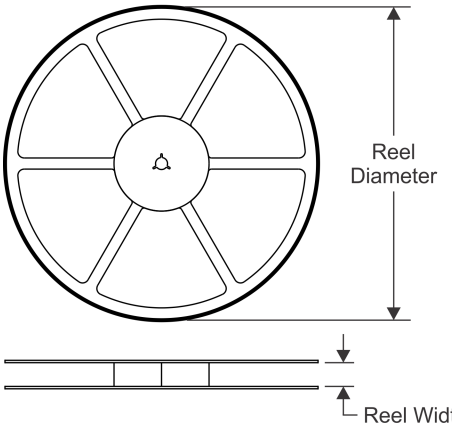
- Catalog: CD74HC4051, CD74HC4052, CD74HC4053, CD74HCT4051
- Automotive: CD74HC4051-Q1, CD74HCT4051-Q1, CD74HC4051-Q1, CD74HCT4051-Q1
- Enhanced Product: CD74HC4051-EP, CD74HC4051-EP
- Military: CD54HC4051, CD54HC4052, CD54HC4053, CD54HCT4051

NOTE: Qualified Version Definitions:

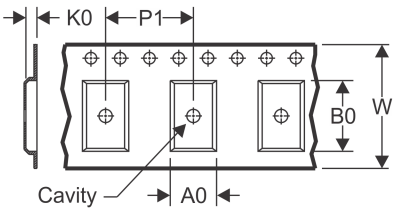
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

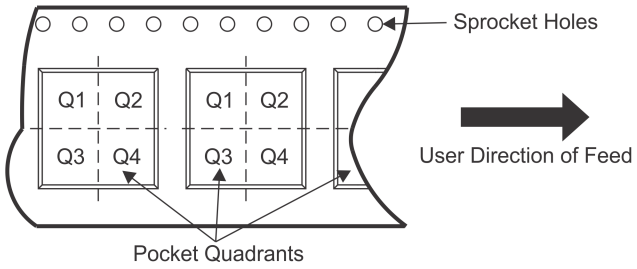


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

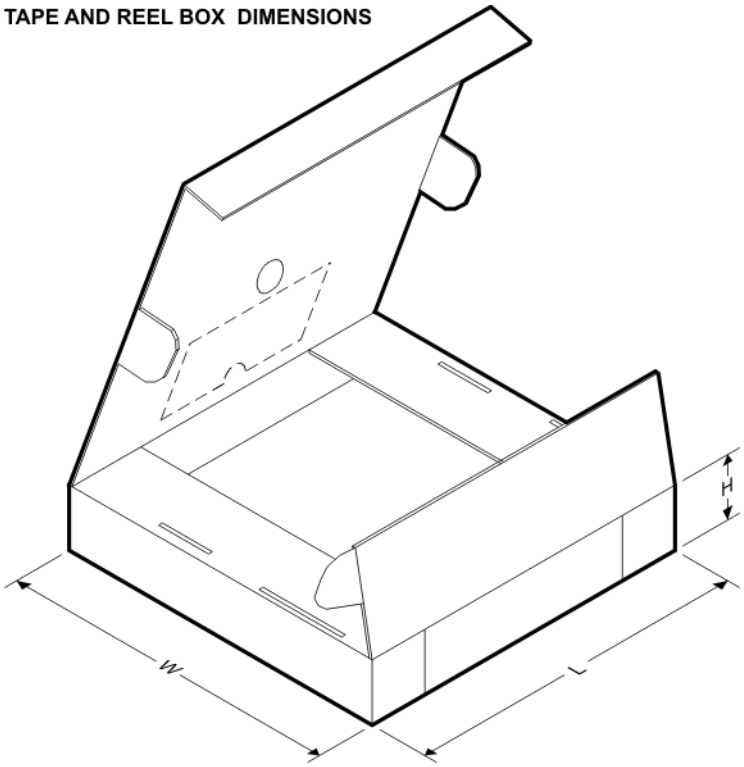


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

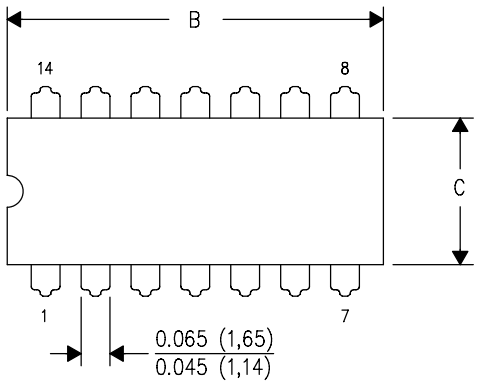
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4051M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4051M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4051PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4051PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051PWT	TSSOP	PW	16	250	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4052M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4052M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4052NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC4052PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4052PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4052PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4052PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HC4053M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4053M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4053M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4053PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4053PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4053PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4053PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HCT4051M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4052M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4053M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4053PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HCT4053PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HCT4053PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HCT4053PWT	TSSOP	PW	16	250	367.0	367.0	35.0

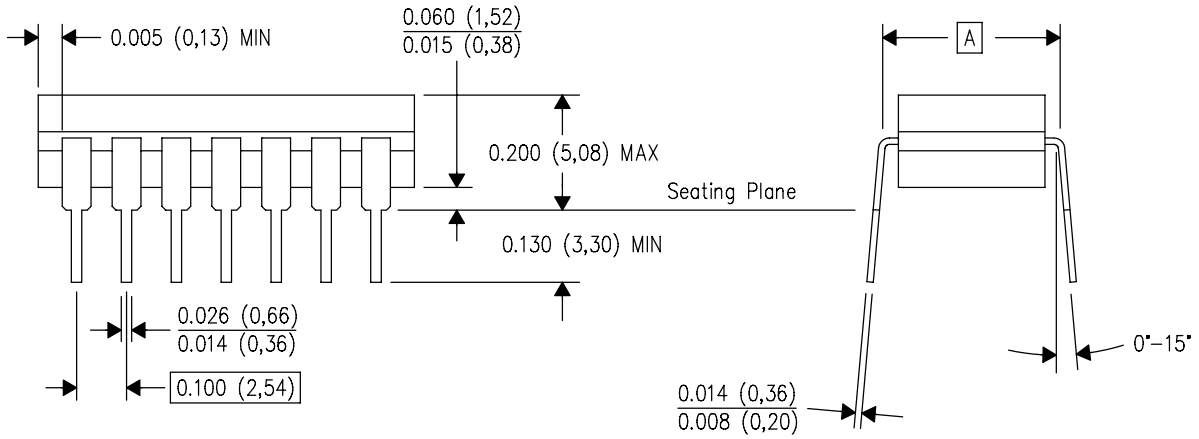
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



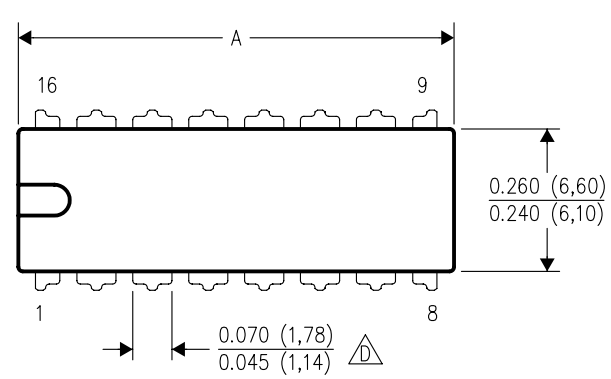
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

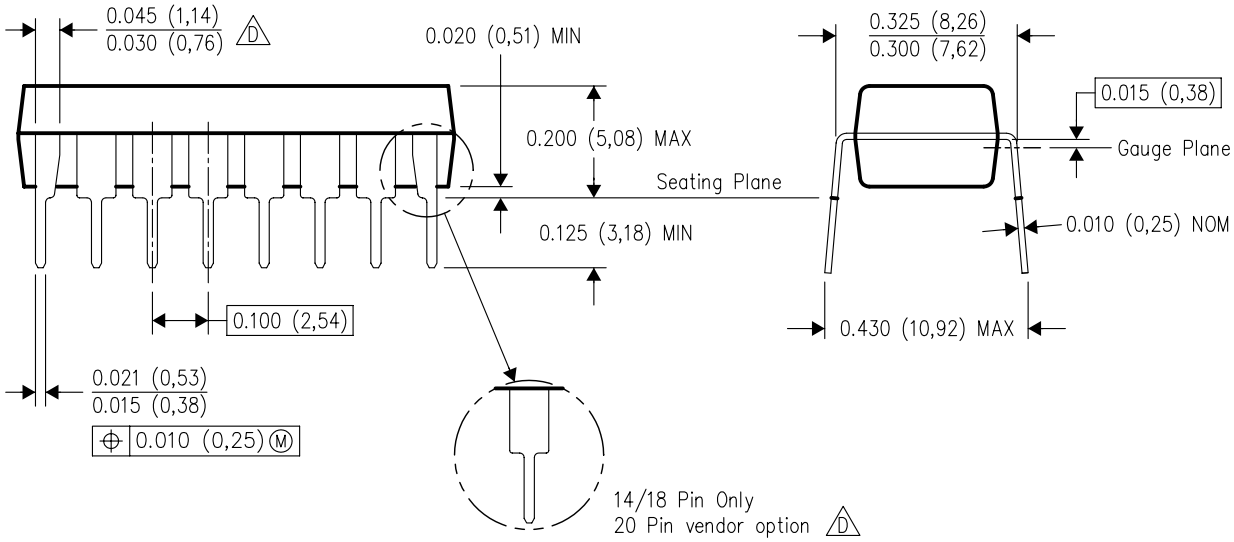
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



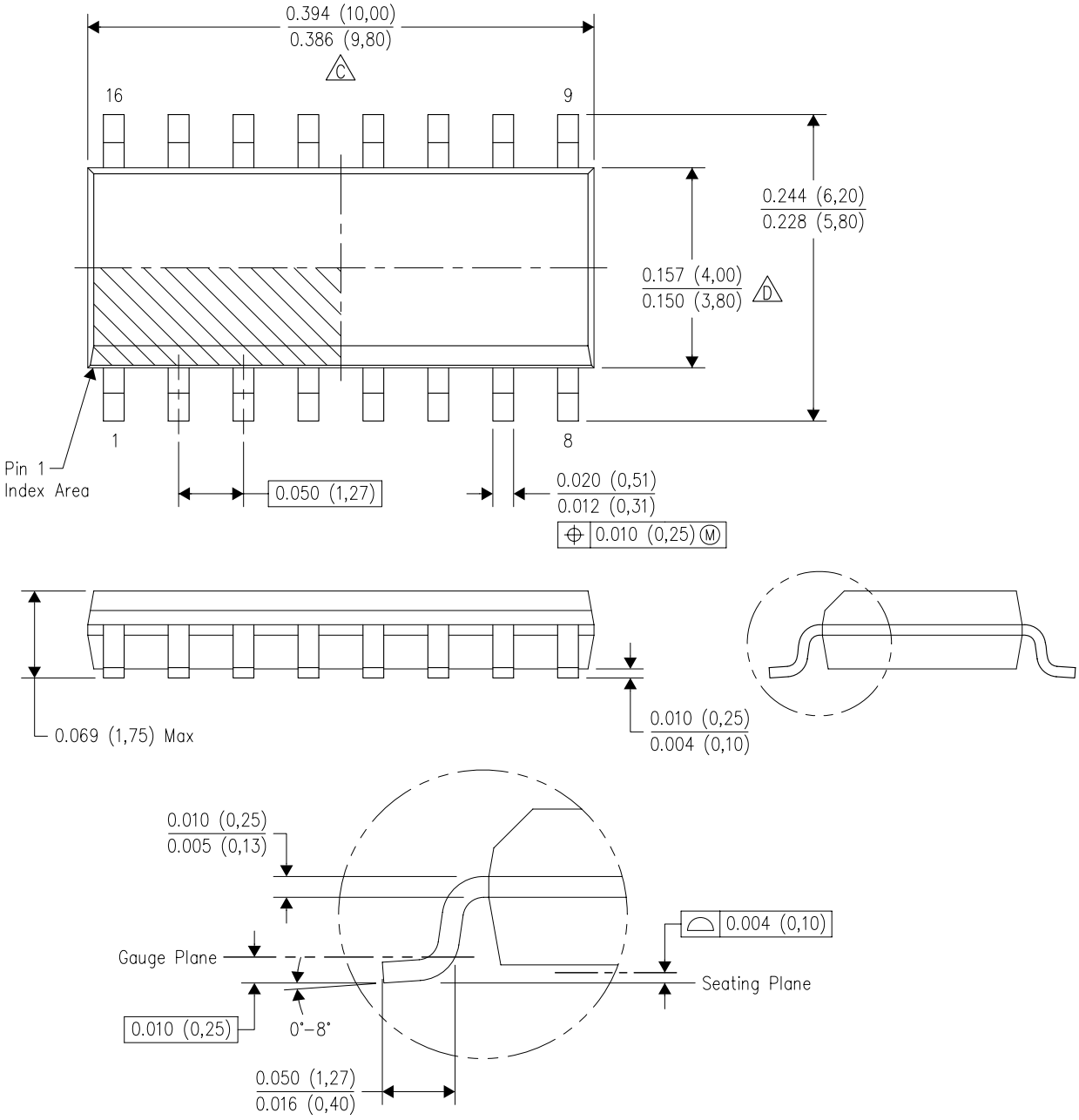
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

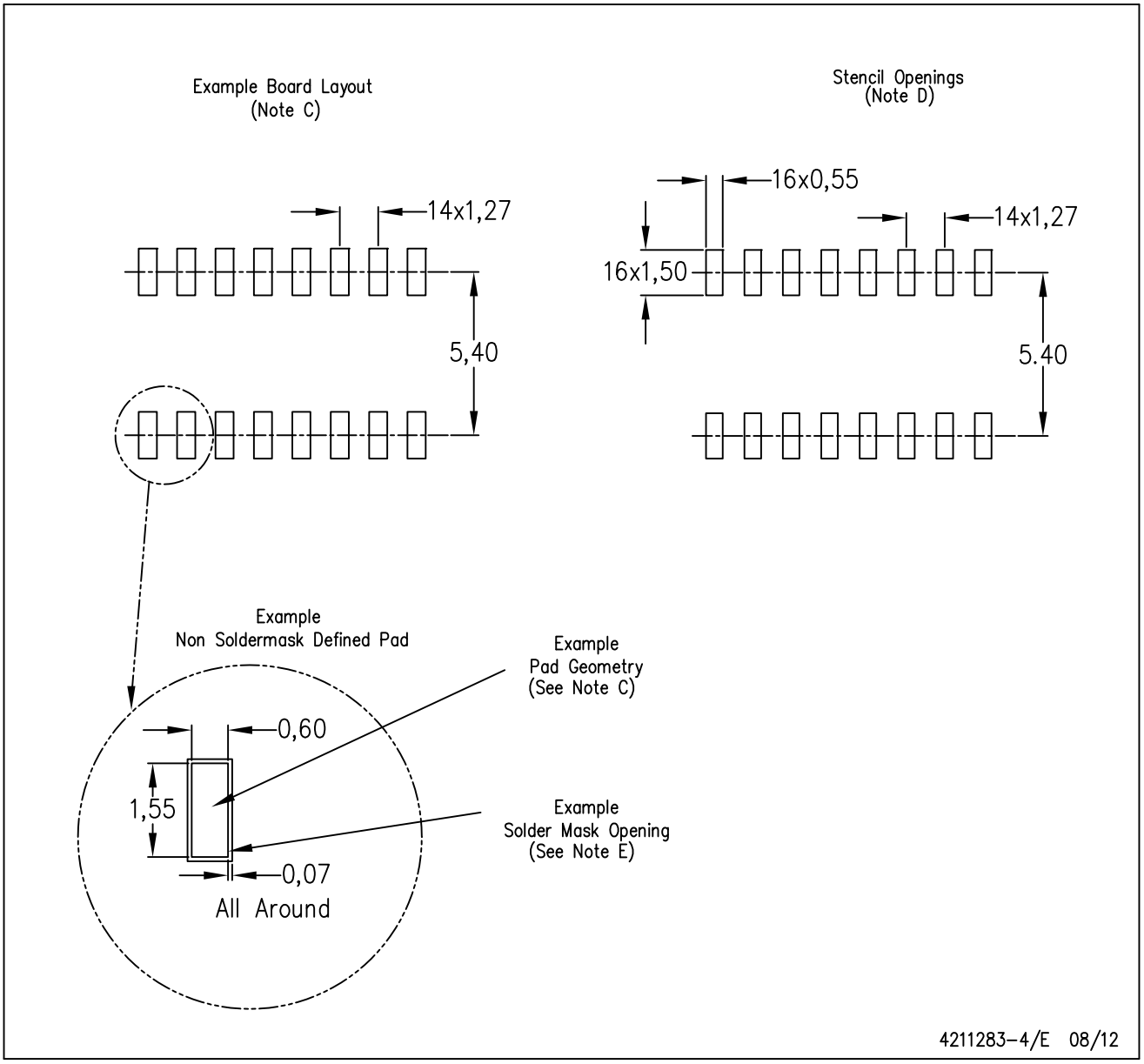
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



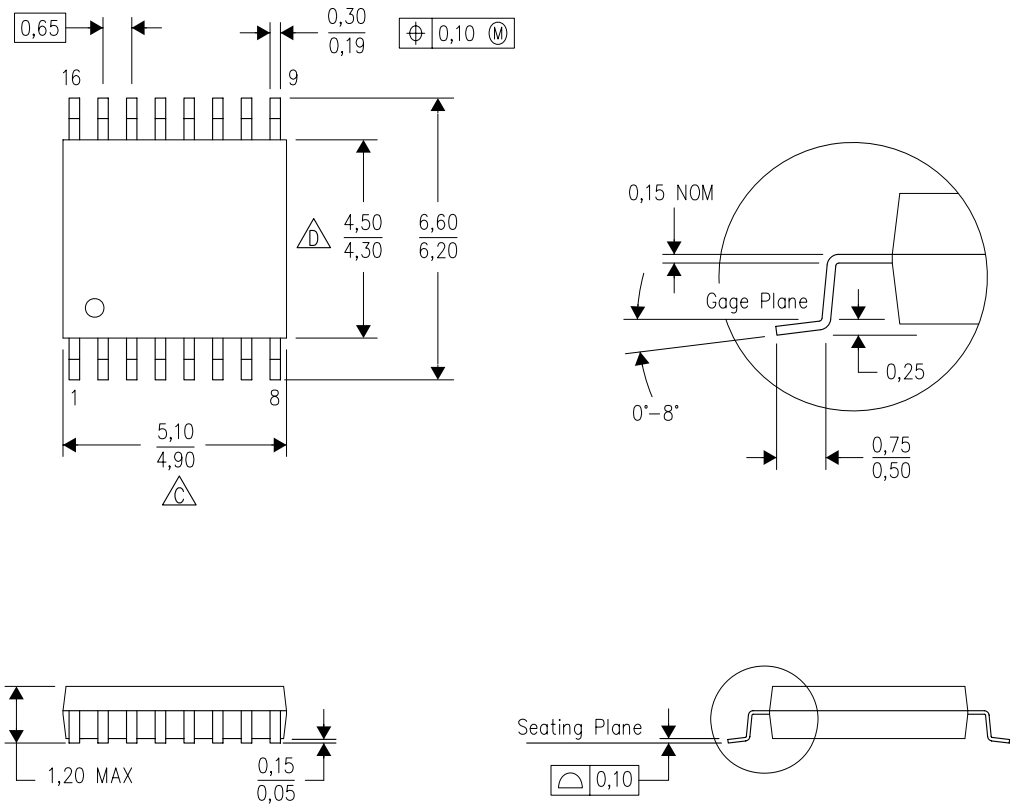
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

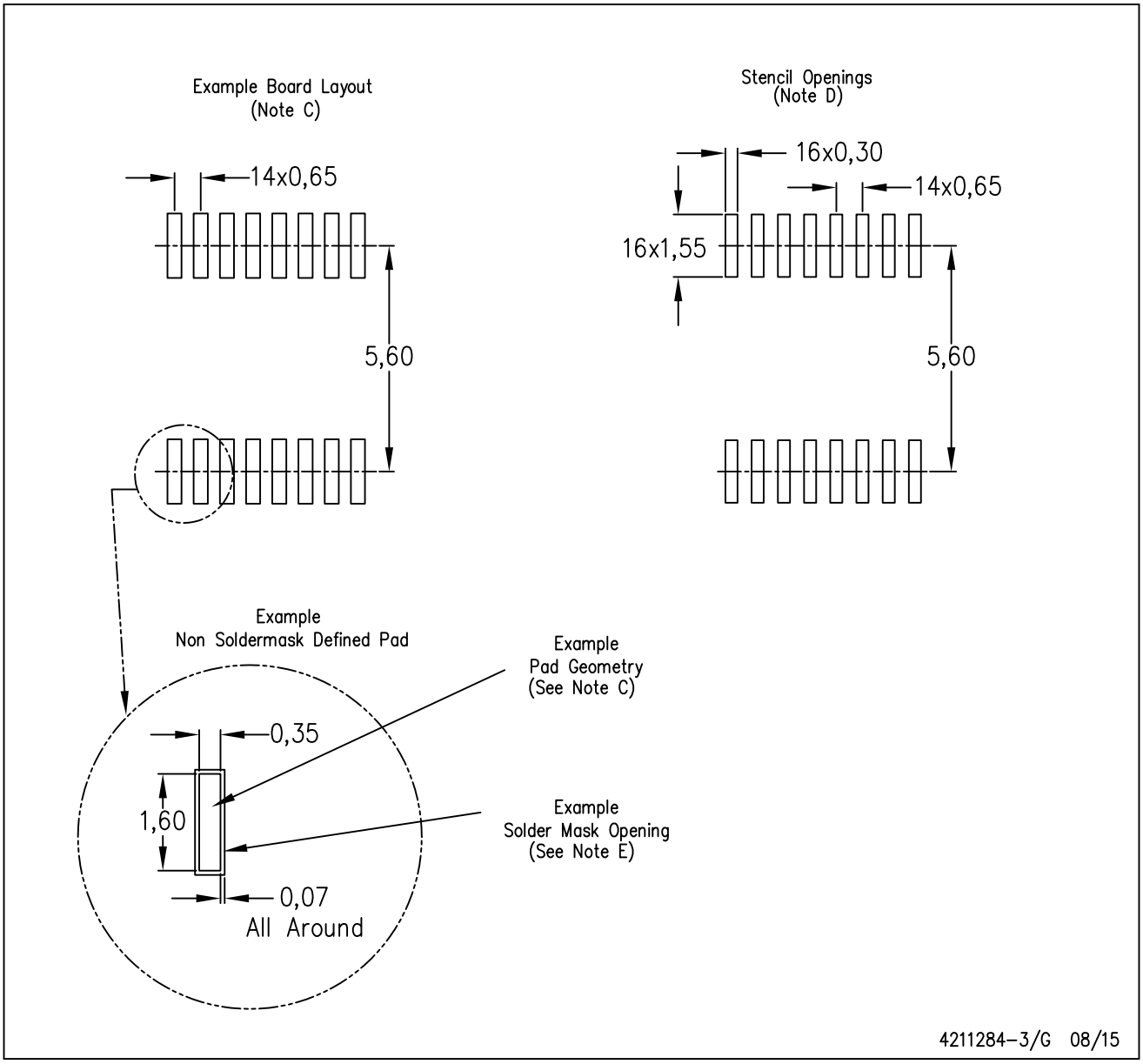
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

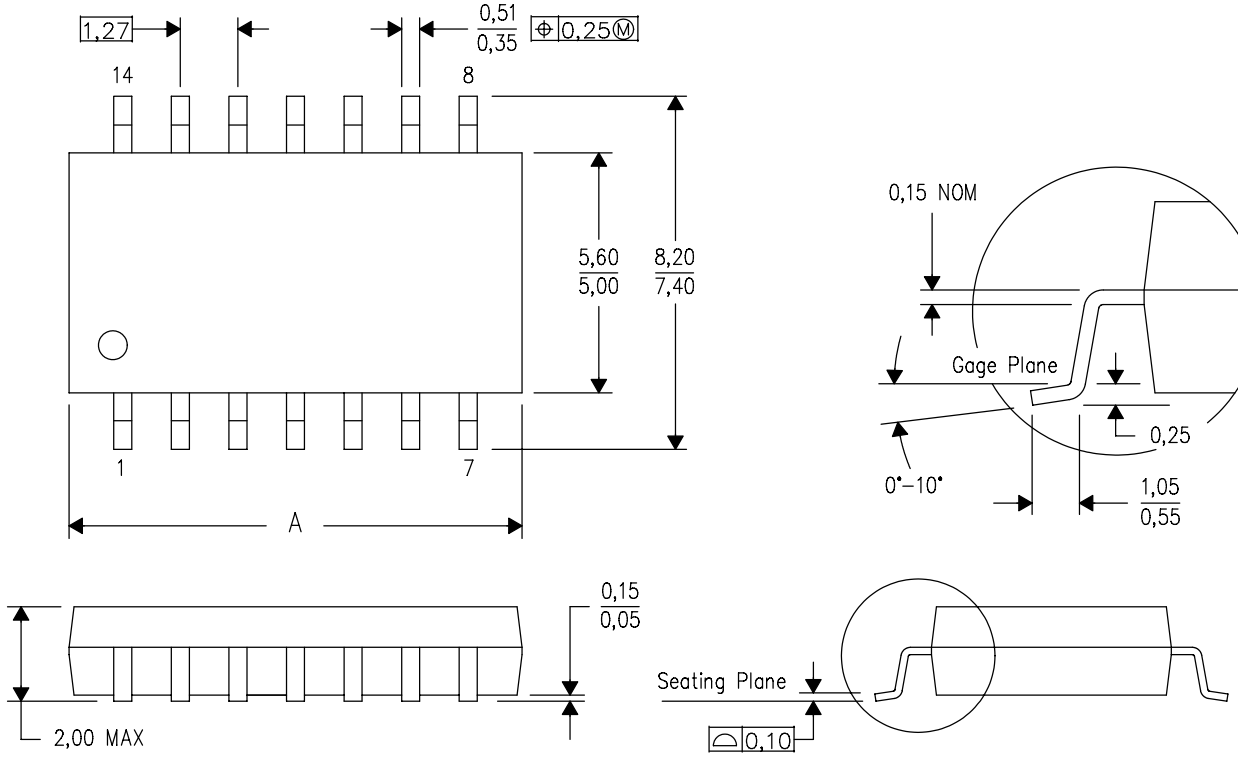


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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RFID	www.ti-rfid.com		
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