ECGR 6264

Project 1: Low-Noise Amplifier

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Introduction

The purpose of this exercise was to learn how to use Cadence to simulate an LNA and to serve as a brief introduction to RF design through the design of a narrowband, 2.4GHz low-noise amplifier using Cadence Virtuoso which meets the following specifications:

$V_{DD} \leq 1.1V$

Power Dissipation $\leq 20mW$

$S_{11} \leq -15dB$

$S_{12} \leq -15dB$

$S_{21} \geq 20dB$

$IIP_3 \geq -10dBm$

$NF \leq 2dB$

Input Port: 50Ω

C_{out}: 200*fF*

There are four upcoming sections which discuss the thoughts that went into the design and implementation as well as the results of the amplifier. They are as follows:

1) **Schematics** – Schematic level overview of the amplifier architecture.
2) **Design and Analysis** – Discussion of design decisions and equations.
3) **Simulation Results** – Graphs of important results such as S_{11}, S_{21}, IIP_3, and NF as well as tables enumerating the properties and bias conditions of transistors.
4) **Conclusion** – A conclusion containing reflections and thoughts on the exercise.

Schematics

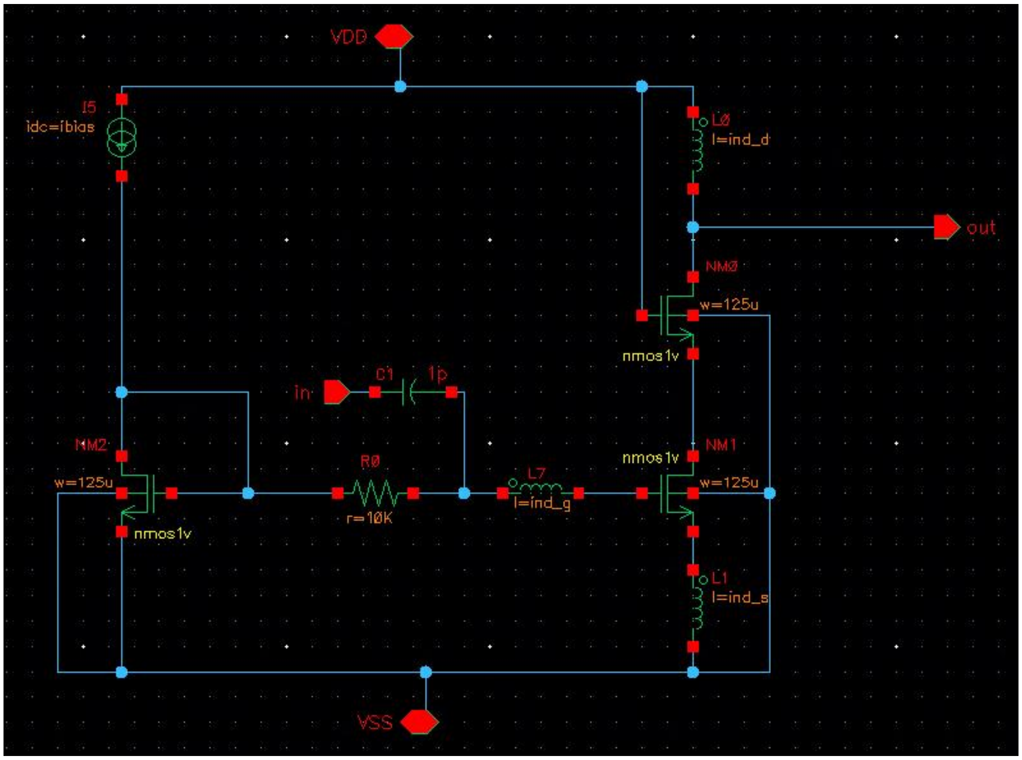

Figure 1 – Completed Design

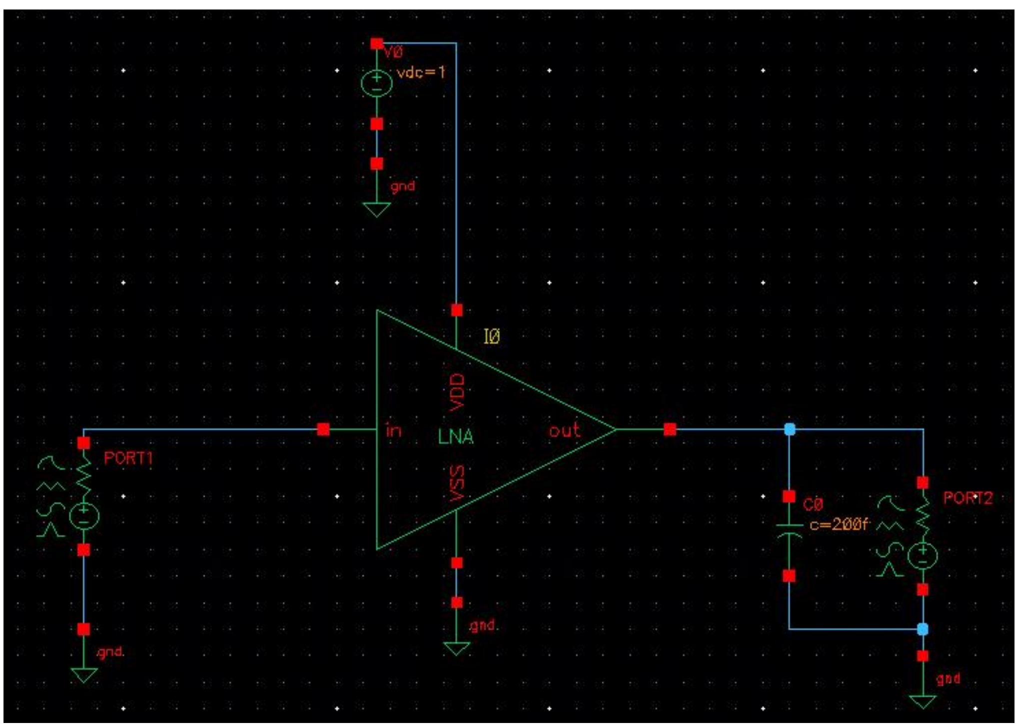

Figure 2 – Test Bench

Design and Analysis

I - Calculations

For this design, the cascode topology was used. This layout was chosen because it is narrowband, there is a lot of reading material on it, and because it negates the miller effect of the gate-to-drain capacitance that limits gain at high frequencies. The amplifier was biased with *400uA* which gives good swing room on the ID vs V_{GS} plot. The dimensions of the transistors are listed below:

Length: $45nM$

Finger Width: $5uM$

No. Fingers: 25

Total Width: $125uM$

To derive the value of L_s, we can start by applying an input voltage and measuring the resulting current to calculate the impedance looking into the gate.

By doing this we get the equation

$$Zin = \frac{1}{C_{gs}\omega} + L_s\omega + \frac{gmL_s}{C_{gs}}$$

The third term in this equation creates a real resistance which can be set to 50Ω and then used to solve for L_s.

$$L_s = \frac{R_{in}C_{gs}}{gm} = \frac{50\left(40*10^{-15}\right)}{6(10^{-3})} = \boldsymbol{333pH}$$

L_g is calculated using

$$L_g = \frac{1}{\omega^2 C_{gs}} - 333pH = \frac{1}{\left((2.4*10^9)2\pi\right)^2(40*10^{-15})} - 333pH$$

$$= \boldsymbol{109.667nH}$$

The drain inductor resonates with the $200fF$ parallel output capacitance if it satisfies the equation

$$f_{Res} = \frac{1}{2\pi\sqrt{L_d C_{out}}}$$

Therefore, $L_d = \mathbf{21}\boldsymbol{nH}$.

The starting values of the components and bias conditions are as follows

$$\boldsymbol{L_d = 21nH}$$

$$\boldsymbol{L_g = 109.667nH}$$

$$\boldsymbol{L_s = 333pH}$$

$$\boldsymbol{C_{gs} = 40fF}$$

$$\boldsymbol{ibias = 400u}$$

II - Initial Response

The initial response of the circuit with these values was an S_{11}, S_{12}, and S_{21} that showed strong peaks at around 1.8GHz, a margin of error of about 600MHz. Examining the *ZM* parameter of the input port showed a resistance of 133Ω and a reactance of 700Ω.

III - Adjustments

Since the imaginary part of the impedance was very positive, L_s and L_g were scaled down while observing *ZM* until *10pH* and *55nH*, respectively, provided a closer value of 89Ω real and -12Ω reactive. At this point the desired input impedance was achieved by leaving L_s and $L_g$alone and adjusting the drain inductor. The results of these adjustments led to the values below.

$$\boldsymbol{L_d = 16nH}$$

$$\boldsymbol{L_g = 55nH}$$

$$\boldsymbol{L_s = 10pH}$$

IV - FOM and Components

The Figure of Merit equation given to us was:

$$10log\left[100 * \frac{S_{21}*f^2C(GHz)*IIP_3(mW)*10{,}000}{(F-1)*P_{Total}^2(mW)*Area(um^2)}\right]$$

Using values from *Table 1* and *Table 3,* the following FOM is obtained:

$$10log\left[100 * \frac{437mW*(2.4*10^9)^2*3mW*10{,}000}{(1.4-1)*1.87^2mW*1{,}422{,}568um^2}\right] = 215.8$$

The table below displays the area of the components given their values.

Component	Value	Area
NMOS 0, 1, 2	**X**	$\mathbf{68.4um^2}$
$\boldsymbol{R_0}$	**10K**	$\mathbf{2000um^2}$
$\boldsymbol{C_1}$	**1pF**	$\mathbf{250um^2}$
$\boldsymbol{L_g}$	**55nH**	$\mathbf{1,100,000um^2}$
$\boldsymbol{L_s}$	**10pH**	$\mathbf{200um^2}$
$\boldsymbol{L_d}$	**16nH**	$\mathbf{320,000um^2}$
$\boldsymbol{C_0}$	**200fF**	$\mathbf{50um^2}$

Table 1 – Component Sizes

Simulation Results

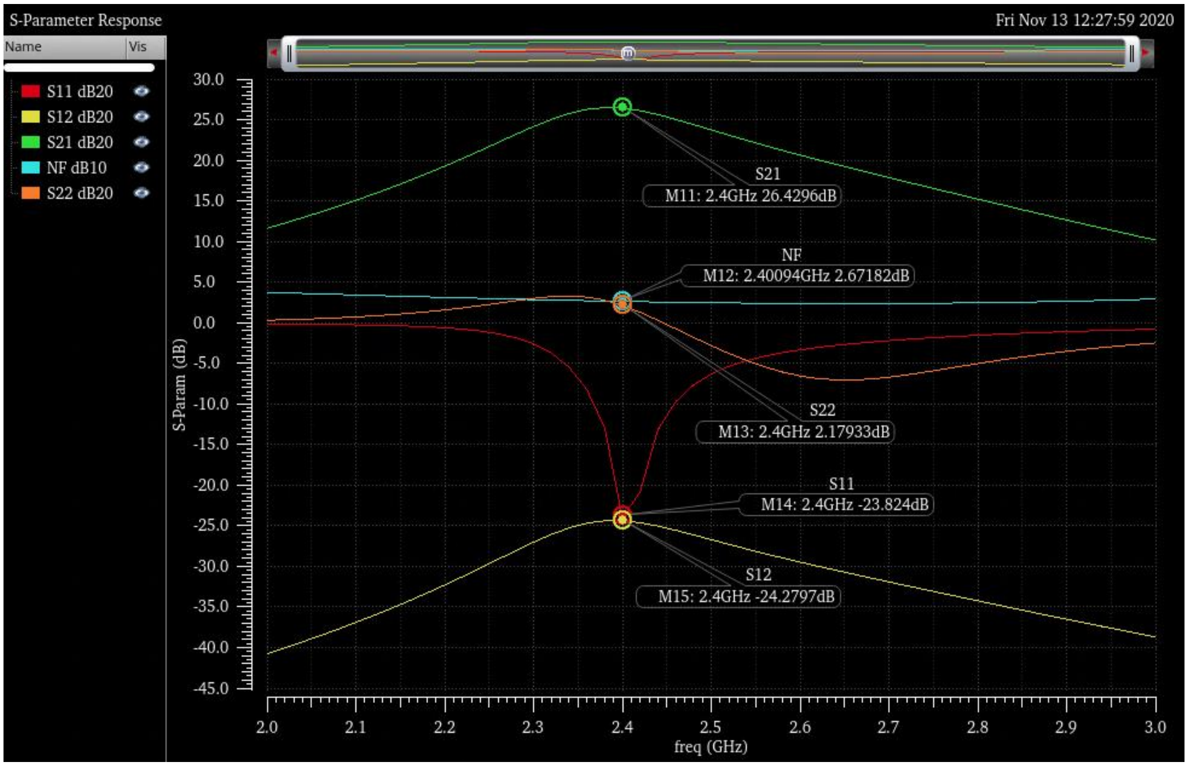

Figure 4 - $S_{11}, S_{12}, S_{22}, S_{21,}$ ***and*** NF.

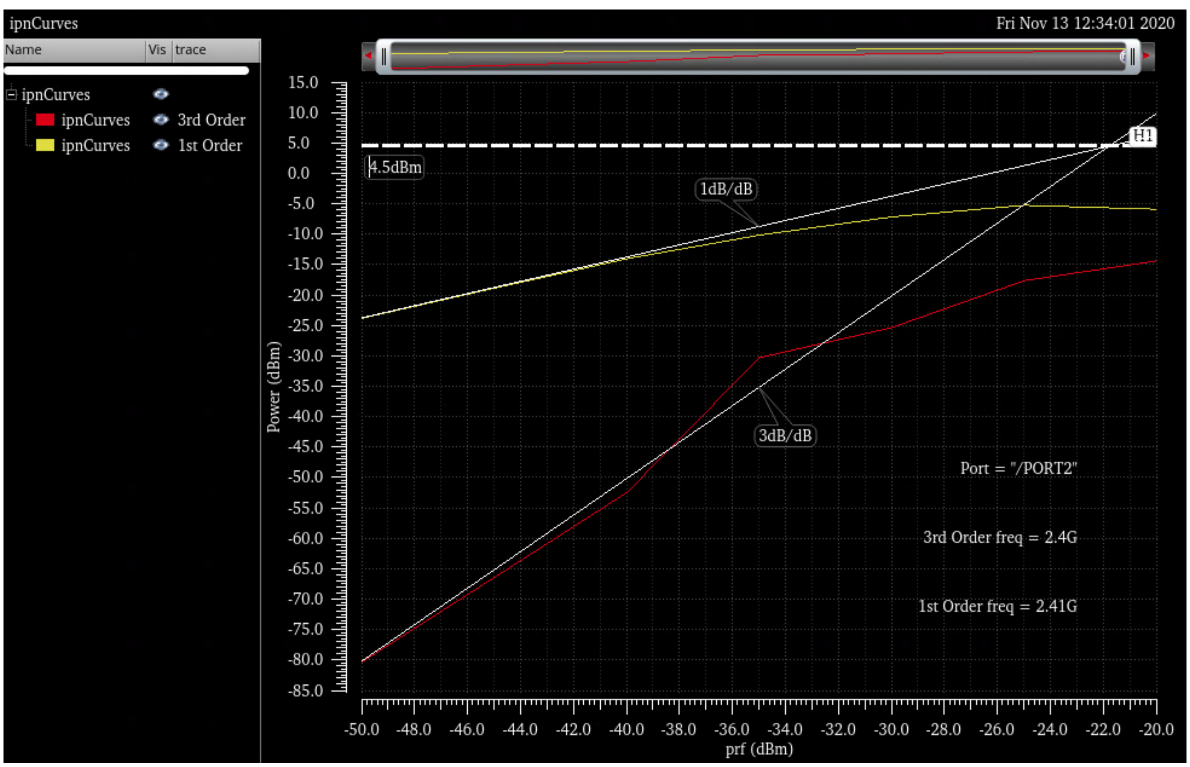

Figure 5 - IIP_3

I - Transistor Properties and Performance Summary

All three transistors have the same dimensions. This was done because it was less likely to introduce design challenges, and the total dissipated power was low enough that the dimension of the current mirror did not need to be scaled down.

	NMOS1	NMOS2	NMOS3	
W	$125um$	$125um$	$125um$	
L	$45nm$	$45nm$	$45nm$	
I_{DS}	$400uA$	$400uA$	$400uA$	
V_{TH}	$591mV$	$591mV$	$591mV$	
V_{GS}	$453mV$	$453mV$	$453mV$	
V_{DS}	$453mV$	$453mV$	$453mV$	
g_m	$6.8mA/V$	$6.8mA/V$	$6.8mA/V$	

Table 2 – Transistor Properties

	2.4GHz LNA Parameter Performance Summary
S_{21}	26.4dB
S_{11}	-23.8dB
S_{12}	-24.3dB
S_{22}	2.2dB
NF	2.7dB
IIP_3	4.5dBm
P_{Tot}	1.9mW
V	1V DC
I_{Tot}	1.9mA

Table 3 – Performance Summary

Conclusion

Some of the greatest difficulties of this project were learning how to use the Cadence software package and where to begin deriving values for components. I ended up using equations presented in the class lectures but still had to tweak the values by a fair amount before achieving reasonable results. In the future, I would like to investigate other design methodologies to see how well they work compared to this process because much of it felt like a brute force approach.

One of the most surprising aspects of this project was operating the transistors in the subthreshold region. I learned that this mode of operation is a common tactic in low power RF amplifier design and that MOS transistors start to behave like bipolar devices where their transconductance equation looks like the transconductance equation that governs BJTs. Another point of interest was seeing how much the physical dimensions of the transistors affected things like noise, gain, and power dissipation. *W/L* always cropped up in equations, but this was the first time I got to see how crucial that term was in the design process.

Overall, this project was a good learning experience, although frustrating because despite having an intuitive knowledge of what was going on, it felt like much of the work comprised “hacking and slashing” at component values to get them to work.