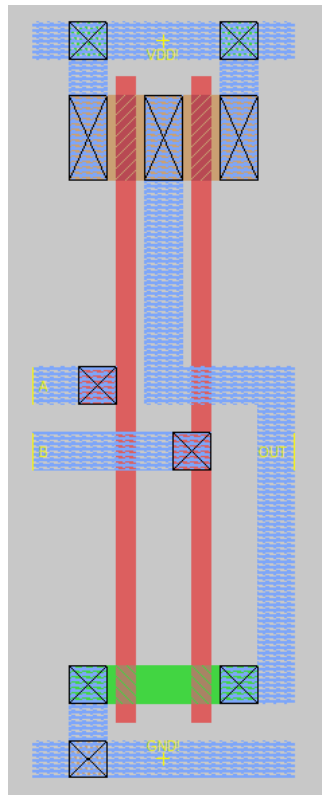
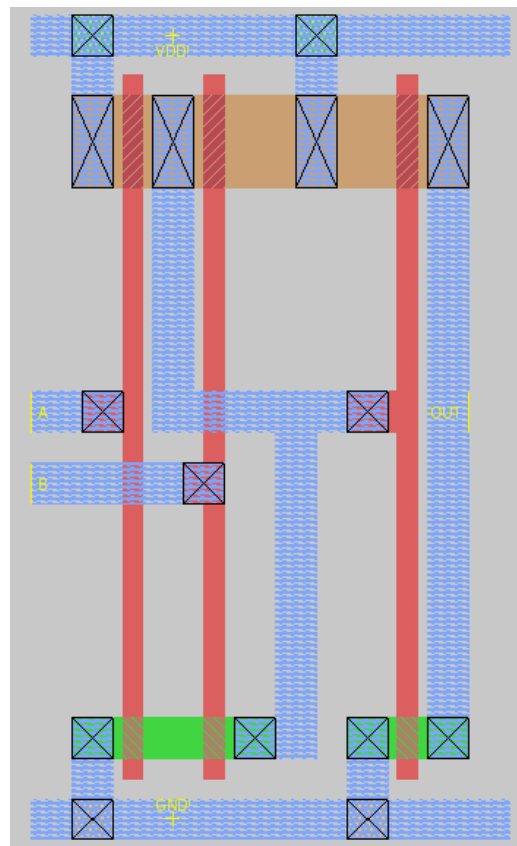


I - NAND



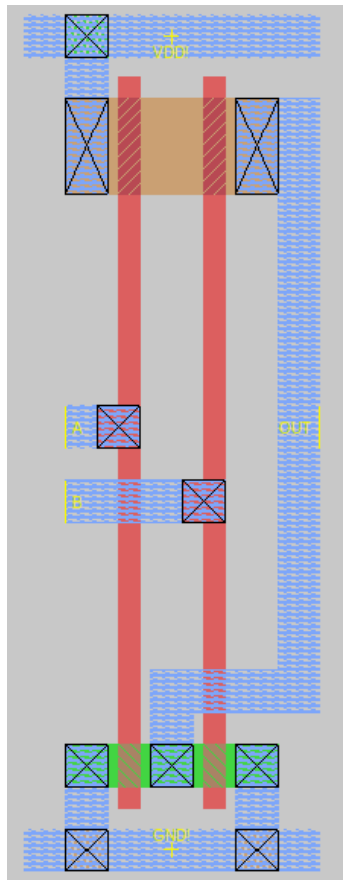
| logic analyzer display | | | | | Zoom | Base | Window | Print |
|------------------------|----|----|----|----|------|------|--------|--------|
| 0.00 | | | | | | | | 200.00 |
| IN | 00 | 01 | 10 | 11 | | | | |
| OUT | | | | | | | | |
| | | | | | | | | |

II - AND



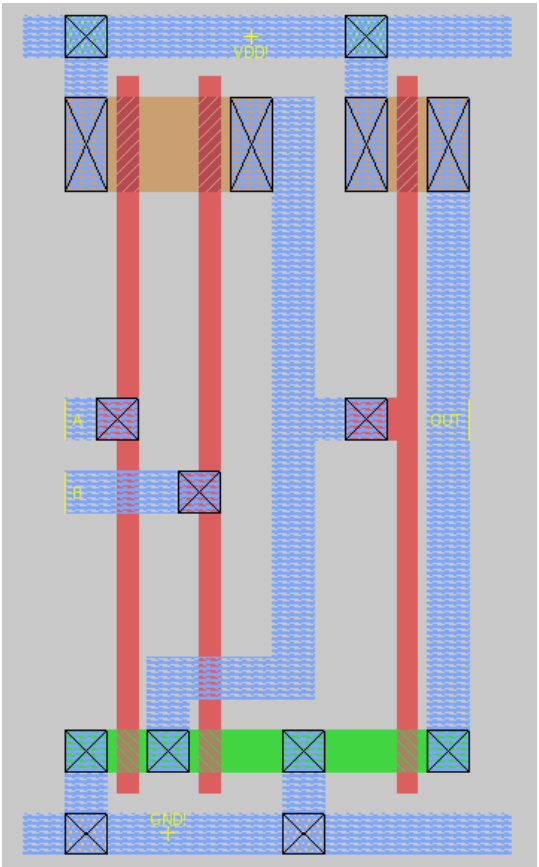
| logic analyzer display | | | | | Zoom | Base | Window | Print |
|------------------------|------|----|----|----|------|------|--------|--------|
| 0.00 | 0.00 | | | | | | | 200.00 |
| IN | 00 | 01 | 10 | 11 | 00 | | | |
| OUT | | | | | X | | | |
| | | | | | | | | |

III - NOR



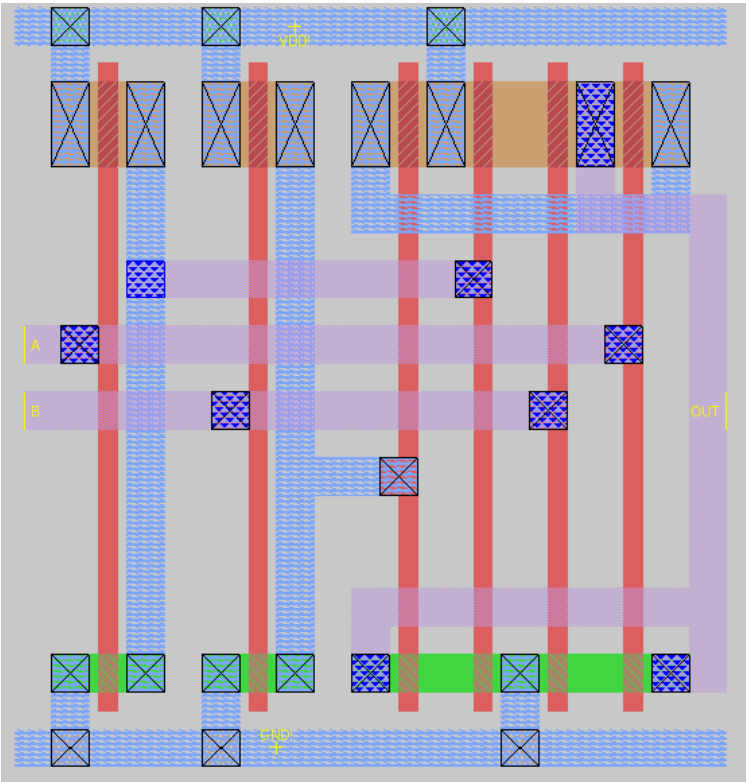
| logic analyzer display | | | | | Zoom | Base | Window | Print |
|------------------------|----|----|----|----|------|------|--------|--------|
| 0.00 | | | | | | | | 200.00 |
| IN | 00 | 01 | 10 | 11 | | | | |
| OUT | | | | | | | | |
| | | | | | | | | |

IV - OR



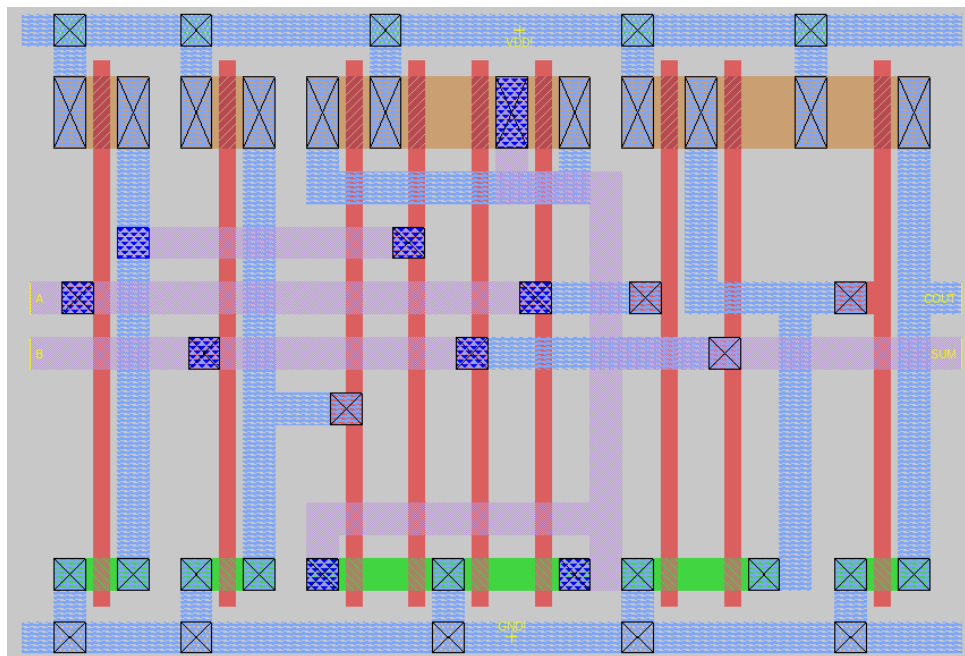
| logic analyzer display | | | | | Zoom | Base | Window | Print |
|------------------------|------|----|----|----|------|------|--------|--------|
| | 0.00 | | | | | | | 200.00 |
| IN | 00 | 01 | 10 | 11 | | | | |
| OUT | | | | | | | | |
| | | | | | | | | |

V - XOR



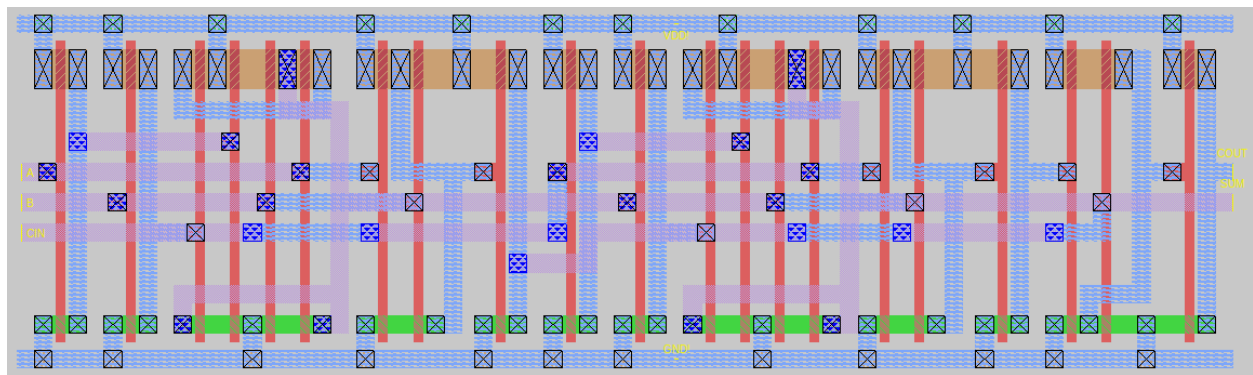
| logic analyzer display | | | | | Zoom | Base | Window | Print |
|------------------------|----|----|----|----|------|------|--------|--------|
| 0.00 | | | | | | | | 200.00 |
| IN | 00 | 01 | 10 | 11 | | | | |
| OUT | | | | | | | | |
| | | | | | | | | |

VI – Half Adder



| logic analyzer display | | | | Zoom | Base | Window | Print |
|------------------------|----|----|----|------|------|--------|--------|
| 0.00 | | | | | | | 200.00 |
| IN | 00 | 01 | 10 | 11 | | | |
| SUM | | | | | | | |
| COUT | | | | | | | |
| | | | | | | | |

VII – Full Adder

[illegible]

VII – Data Flip Flop

