ECGR 5133

Final Project – Array Multiplier

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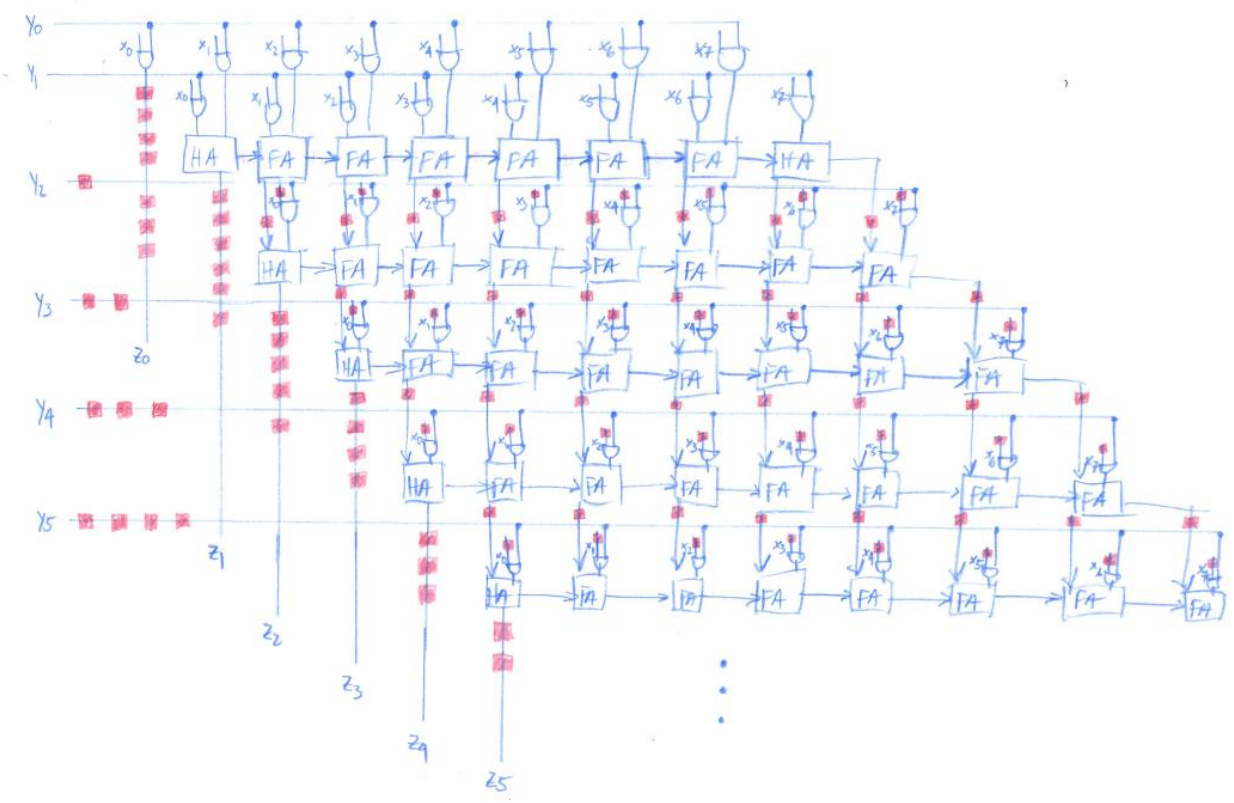
Overview

The goal of this project was to lay out a pipelined, 8-bit array multiplier with a zero-skew clock network in a 0.6um process using Magic VLSI. The schematic below tersely summarizes how the multiplier is built. Each red square represents a DFF for pipelining. Y-values are the multiplicand, X-values are the multiplier, and Z-values are the outputs of the circuit. This project was done in three parts:

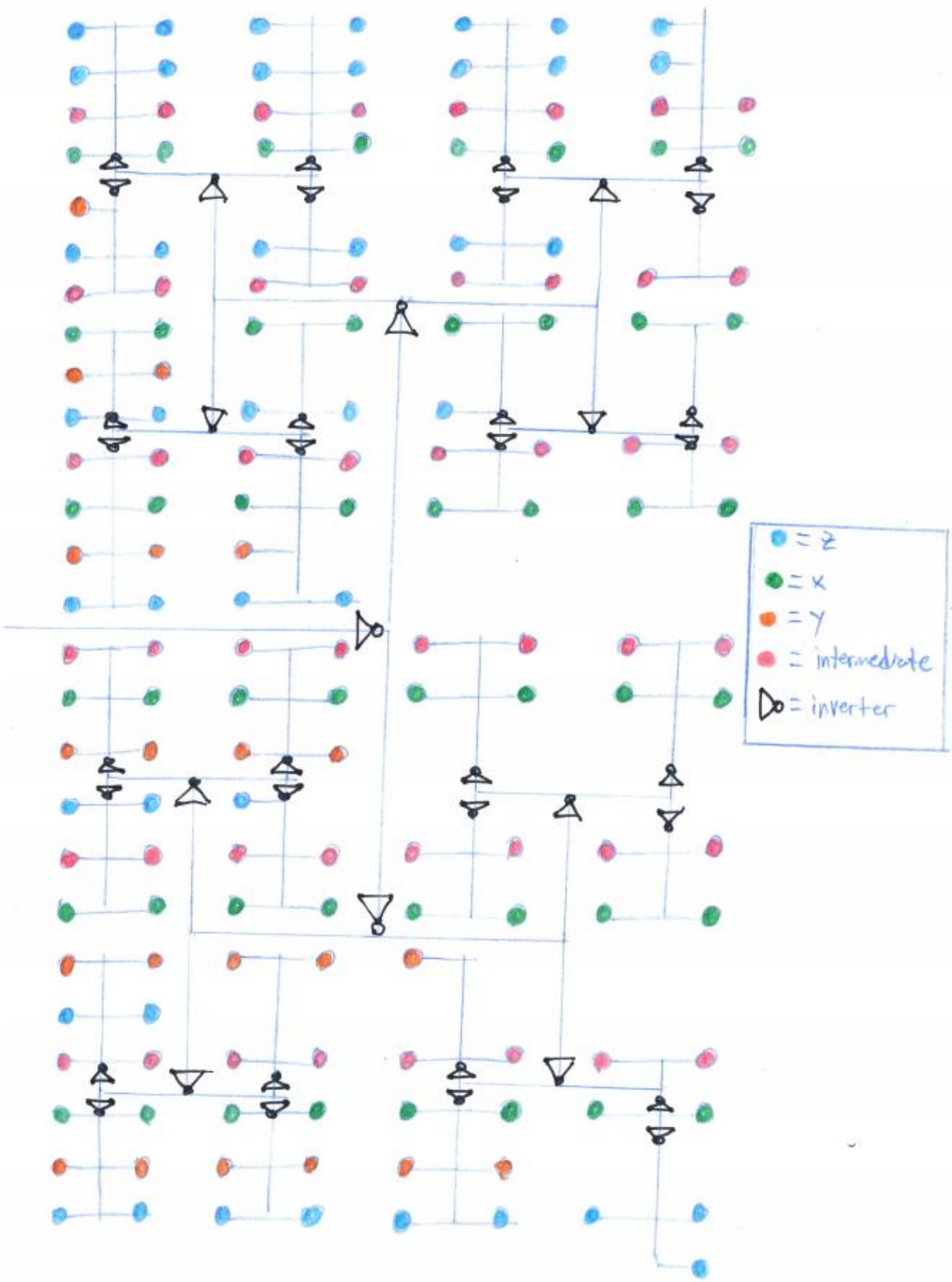
Part I – Unpipelined layout

Part II – Layout with DFF and without clock routing

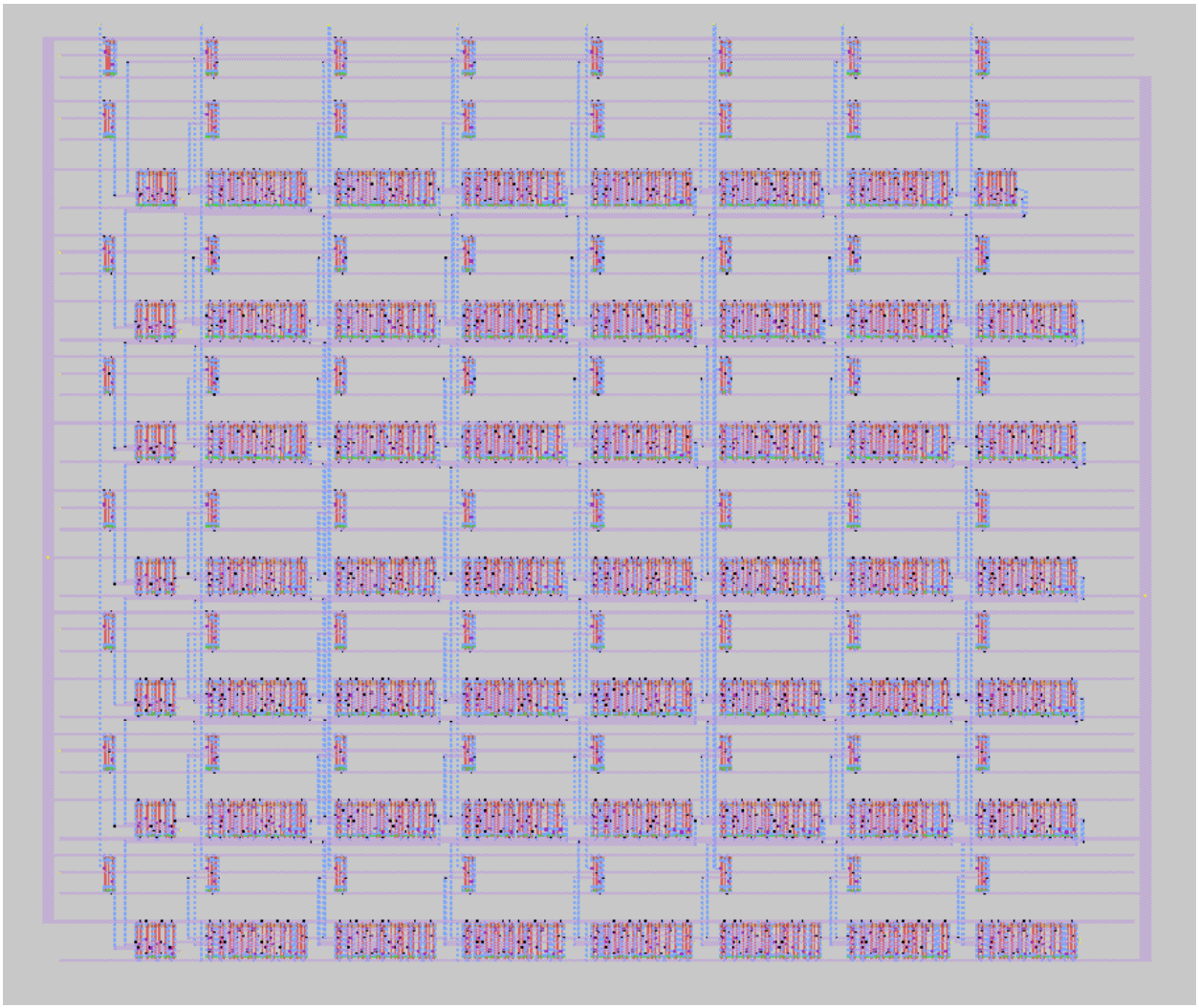
Part III – Fully pipelined layout with zero-skew clock tree

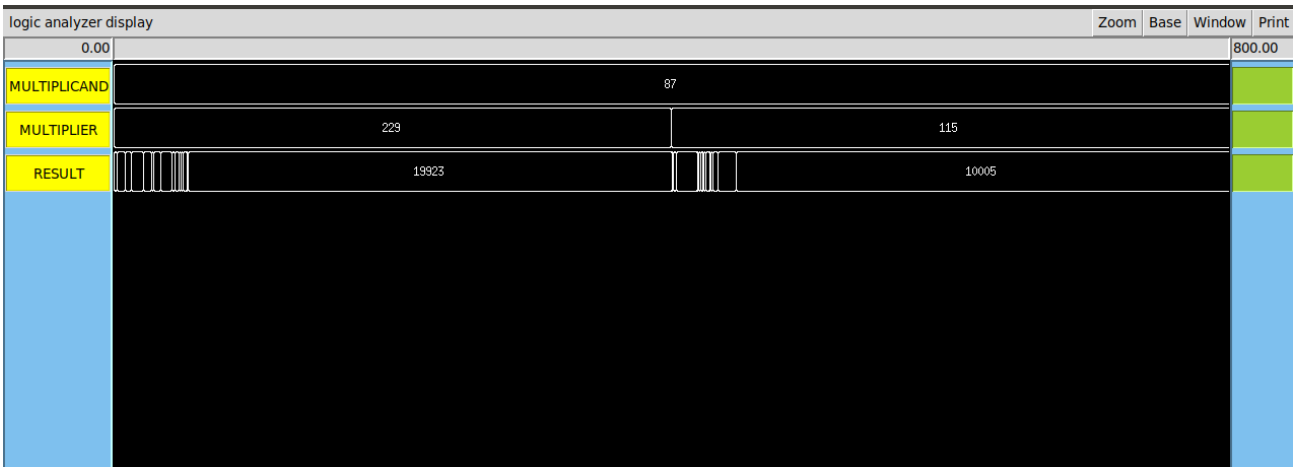


For part III of the project, the zero-skew clock network was prototyped with the drawing below and then executed in layout. Each dot represents a flip-flop. Blue dots are the flip-flops which latch the z-values(outputs), orange dots latch y-values(multiplicand), red dots latch partial sums from the adders, and green dots latch the x-values(multiplier).

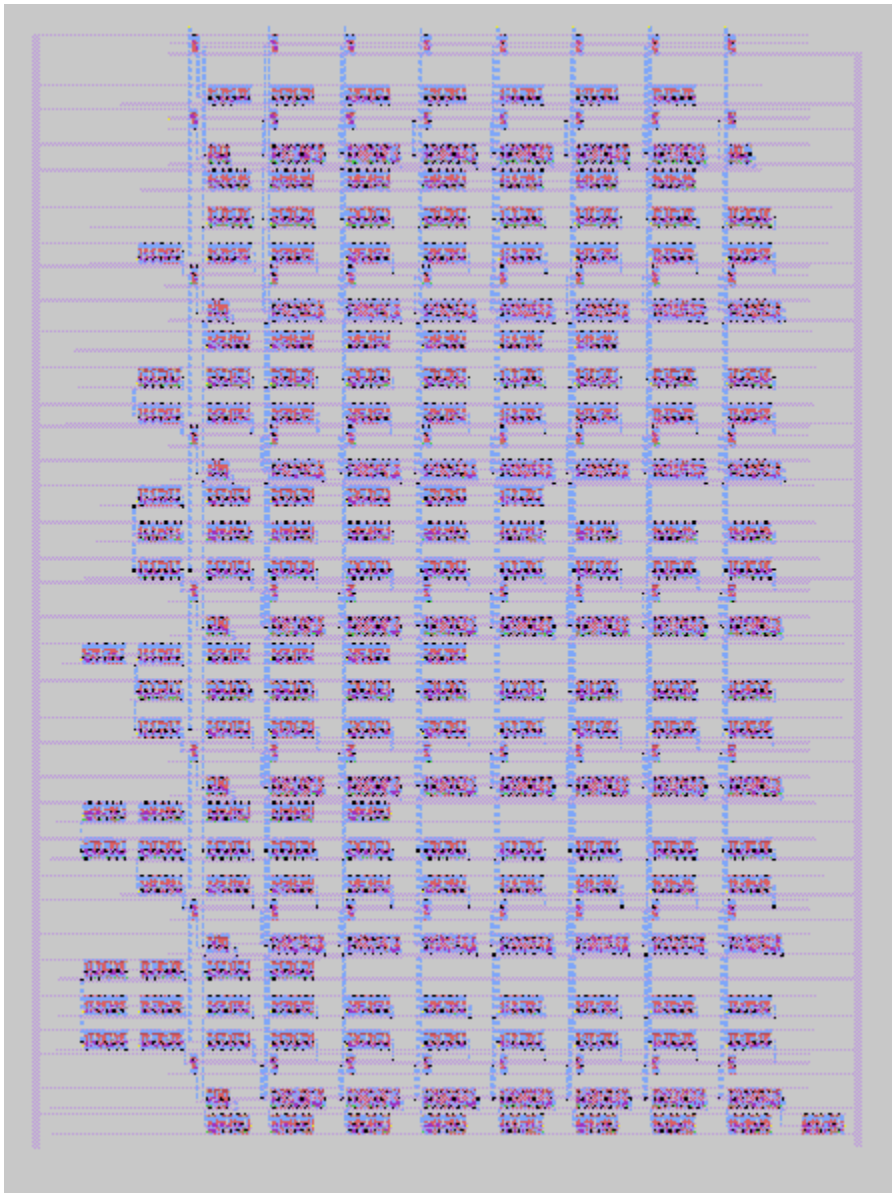

= z
= x
= y
= intermediate
= inverter

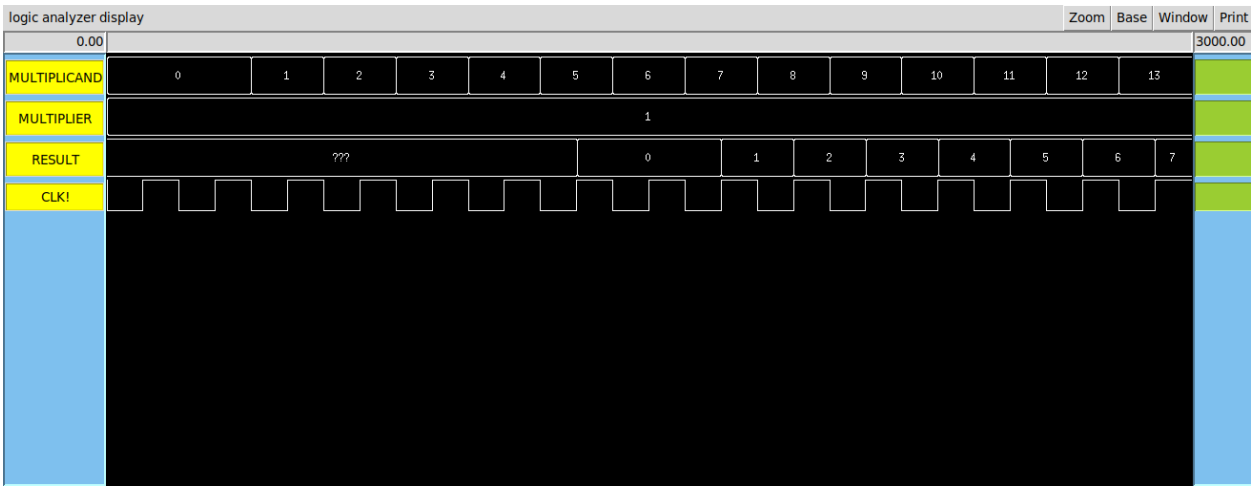
Part I – Non-Pipelined Layout



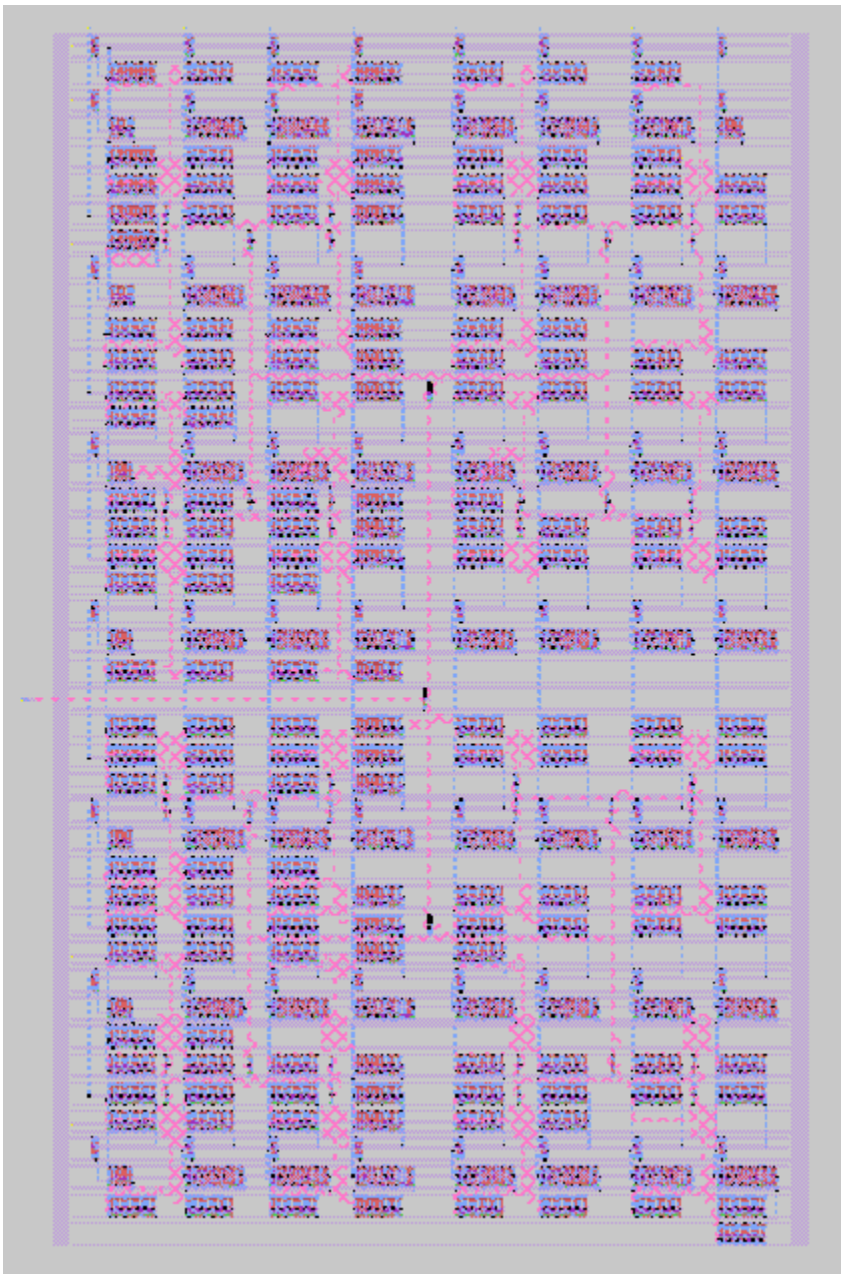

logic analyzer display
Zoom
Base
Window
Print
0.00
800.00
MULTIPLICAND
87
MULTIPLIER
229
115
RESULT
19923
10005

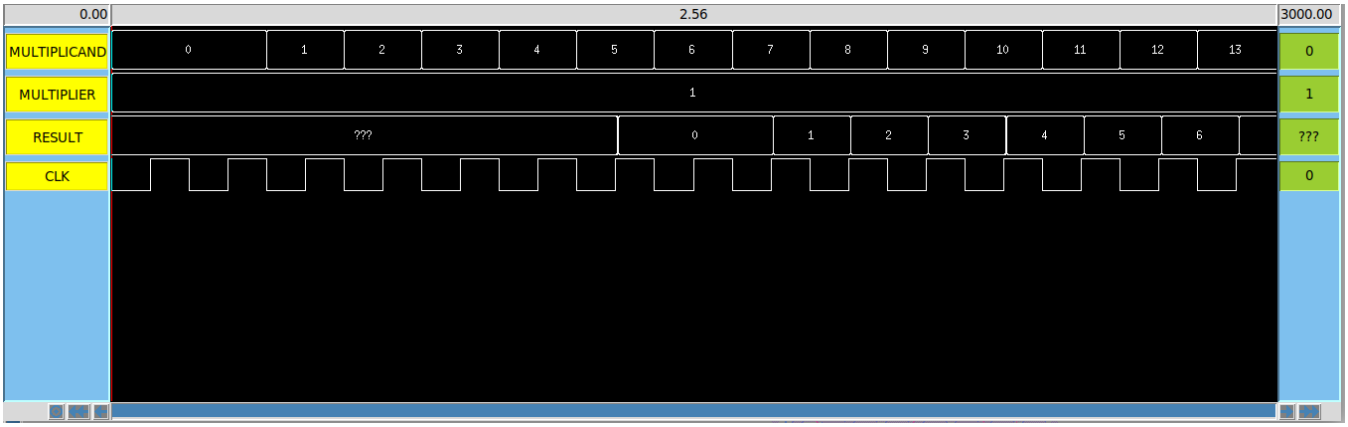
Part II – Pipelined Layout Without Clock Routing




logic analyzer display
Zoom
Base
Window
Print
0.00
3000.00
MULTIPLICAND
0
1
2
3
4
5
6
7
8
9
10
11
12
13
MULTIPLIER
1
RESULT
???
0
1
2
3
4
5
6
7
CLK!

Part III – Pipelined Layout With Zero-Skew Clock Routing




0.00
2.56
3000.00
MULTIPLICAND
0
1
2
3
4
5
6
7
8
9
10
11
12
13
0
MULTIPLIER
1
1
RESULT
???
0
1
2
3
4
5
6
???
CLK
0