ECGR 5133

Final Project – Array Multiplier

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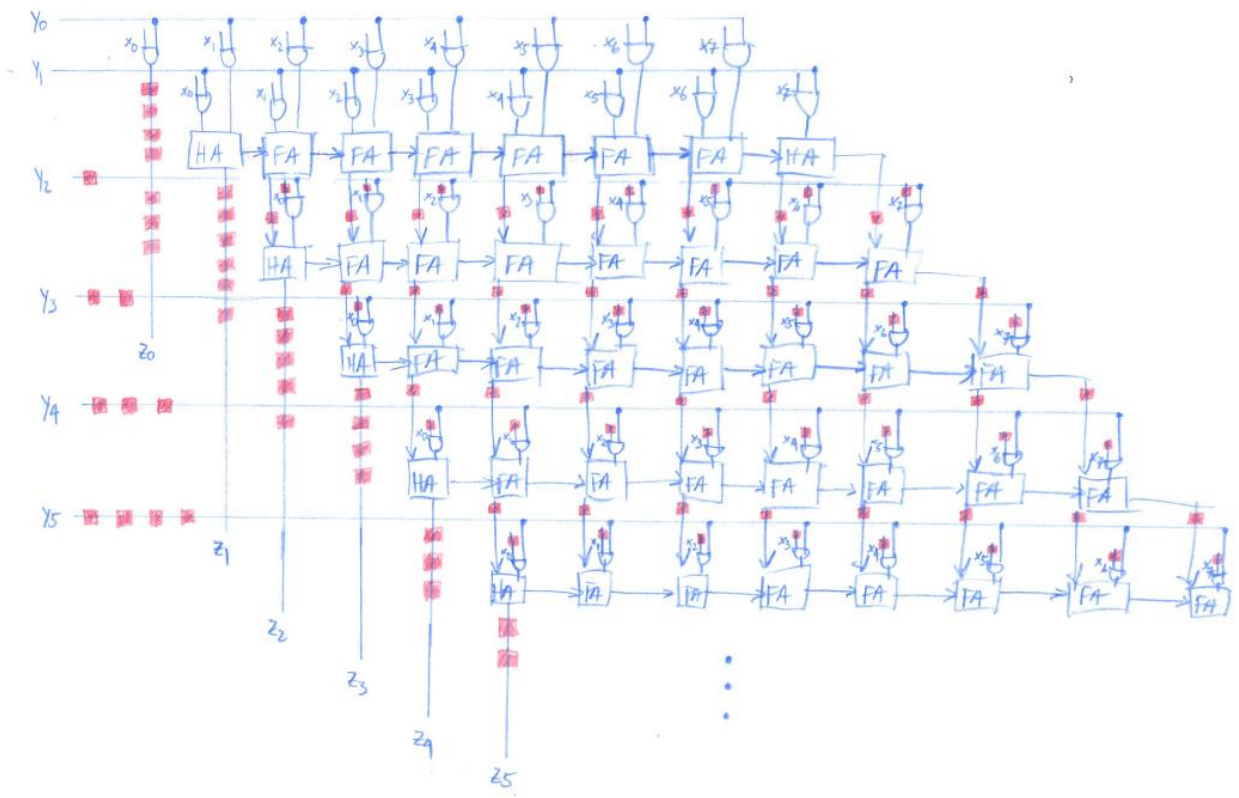
Overview

The goal of this project was to lay out a pipelined, 8-bit array multiplier with a zero-skew clock network in a 0.6um process using Magic VLSI. The schematic below tersely summarizes how the multiplier is built. Each red square represents a DFF for pipelining. Y-values are the multiplicand, X-values are the multiplier, and Z-values are the outputs of the circuit.



This project was completed in three parts:

Part I – Unpipelined layout

Part II – Layout with DFF and without clock routing

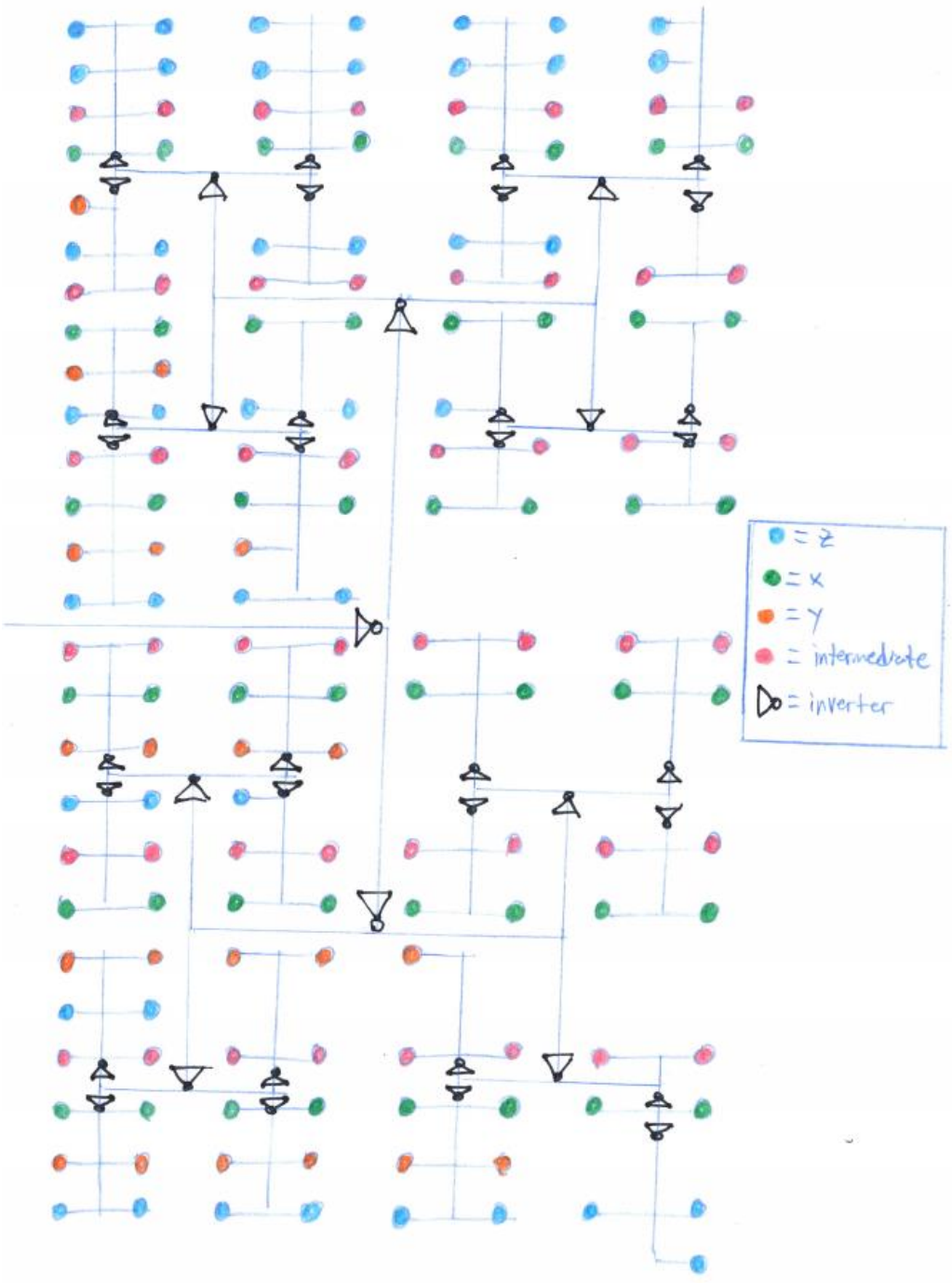
Part III – Fully pipelined layout with zero-skew clock tree

The dimensions of the standard cell in each of the three stages is provided in the table:

	Part I	Part II	Part III
Height	1327.2um	3094.2um	3075um
Width	1596um	2331.6um	1914um

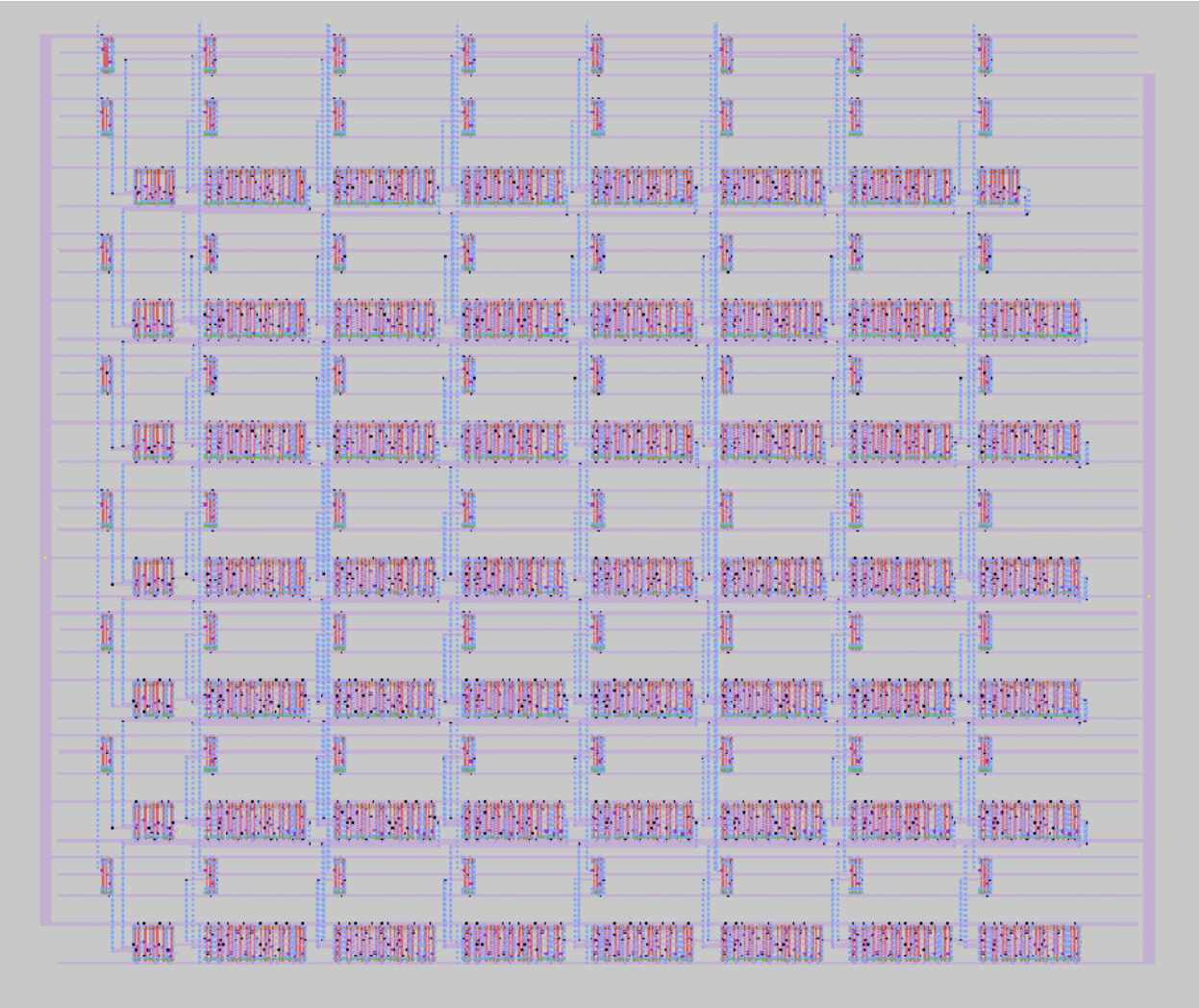
Width and height of multiplier at each stage.

For part III of the project, the zero-skew clock network was prototyped with the drawing below and then executed in layout. Each dot represents a flip-flop. Blue dots are the flip-flops which latch z-values(outputs), orange dots latch y-values(multiplicand), red dots latch partial sums from the adders, and green dots latch the x-values(multiplier). Additionally, four inverter stages are used throughout the network to eliminate noise from the signal as it makes its way to the flip-flops.



Part I – Non-Pipelined Layout

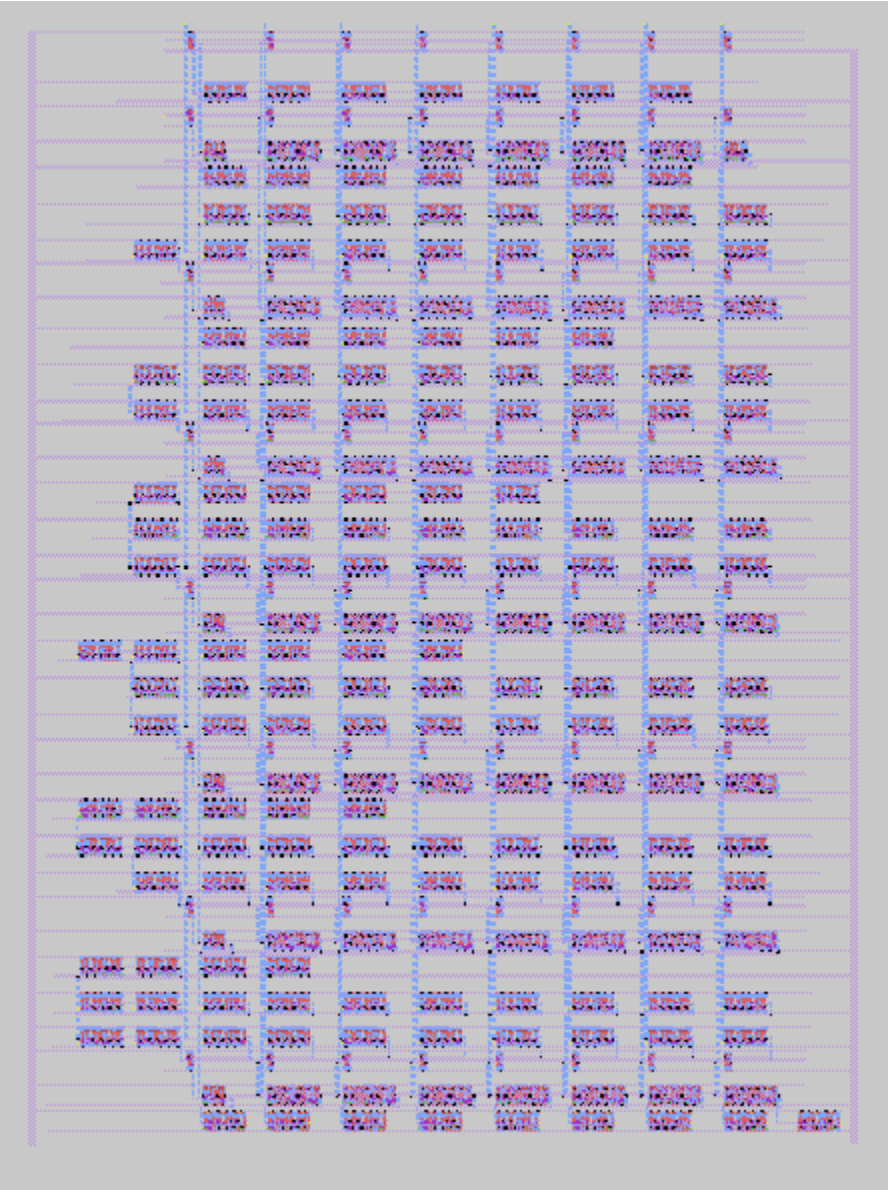
Summary: For the non-pipelined layout, the overall cell width and height was 1327um by 1596um. The simulation shows the multiplicand being multiplied by two different multipliers. According to the simulation, it takes roughly 55ns for the values to stabilize, which means the critical path in this layout is around 55ns.

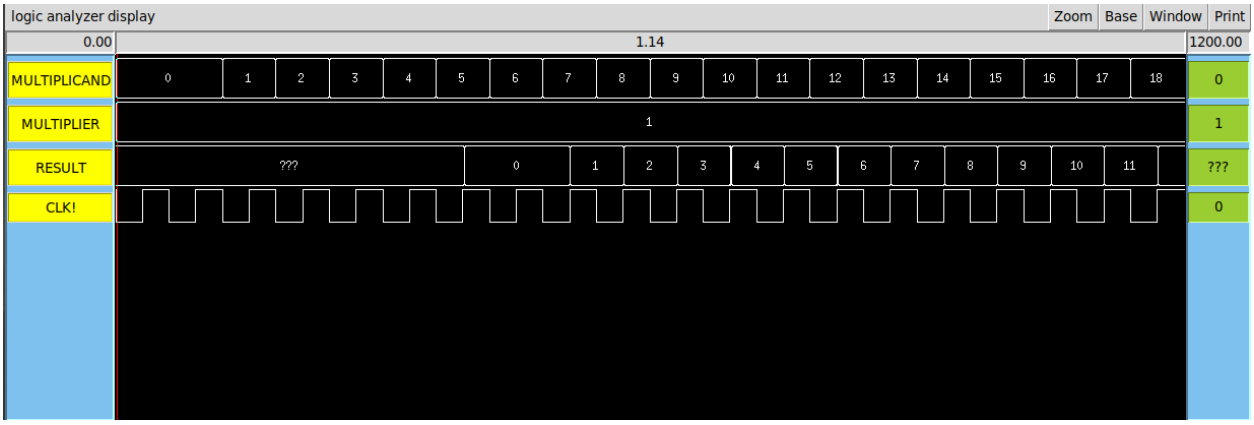



logic analyzer display
Zoom
Base
Window
Print
0.00
800.00
MULTIPLICAND
87
MULTIPLIER
229
115
RESULT
19923
10005

Part II – Pipelined Layout Without Clock Routing

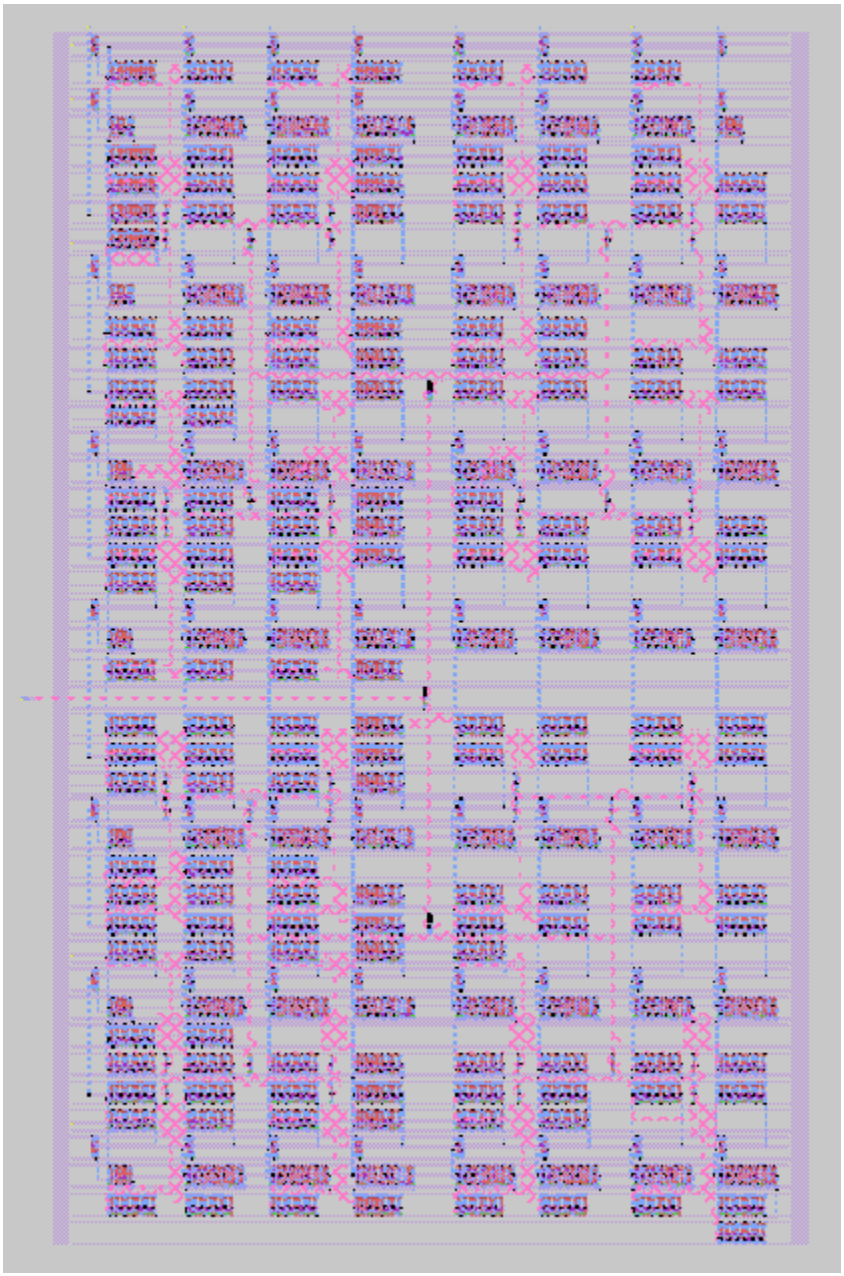
Summary: In the pipelined layout without clock routing, the overall cell width and height increased to 3094.2um by 2331.6um. For simulation, the clock period was set to 60ns, which is slightly higher than the critical path constraint of 55ns deduced from part I. A multiplicand value was fed into the circuit every clock period for a throughput of 60ns and a total latency of seven DFF stages * 60ns = 420ns.

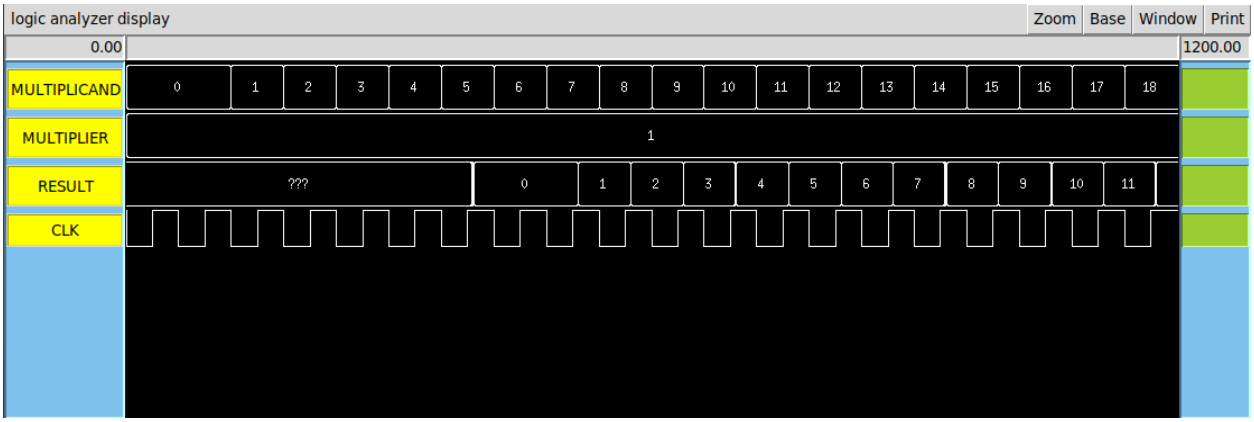



logic analyzer display
Zoom
Base
Window
Print
0.00
1.14
1200.00
MULTIPLICAND
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
0
MULTIPLIER
1
1
RESULT
??? 0 1 2 3 4 5 6 7 8 9 10 11
???
CLK!
0

Part III – Pipelined Layout with Zero-Skew Clock Routing

Summary: For the last part, after everything was cleaned up and made as compact as possible, the final cell width and height came out to be 3075um by 1914um. In this stage, the H-tree for the clock signal was routed between DFFs using metal3, and all the sizes were length-matched to a margin of error of around 30λ. There are four levels of inverters with the first two levels sized by 24λ x 12λ and 16λ x 8λ, and the remaining two levels sized to 8λ x 4λ. The simulation is the same as in part two, with a new value being fed into the pipeline every 60ns.




logic analyzer display
Zoom
Base
Window
Print
0.00
1200.00
MULTIPLICAND
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
MULTIPLIER
1
RESULT
???
0
1
2
3
4
5
6
7
8
9
10
11
CLK