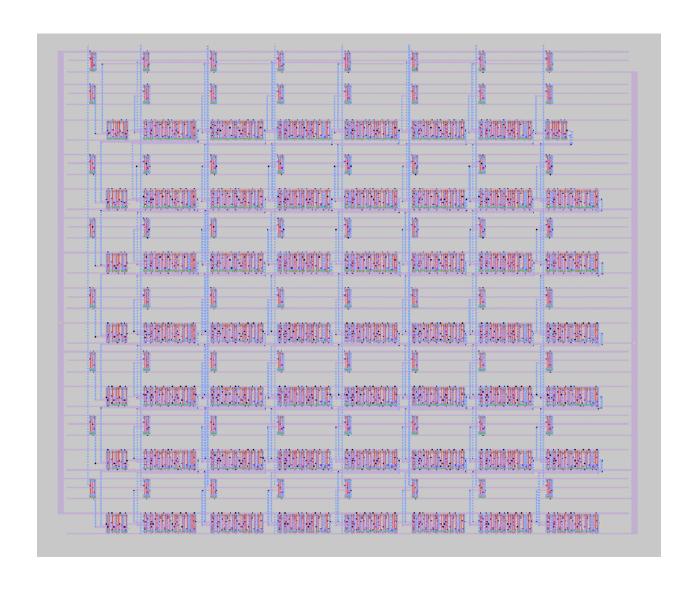
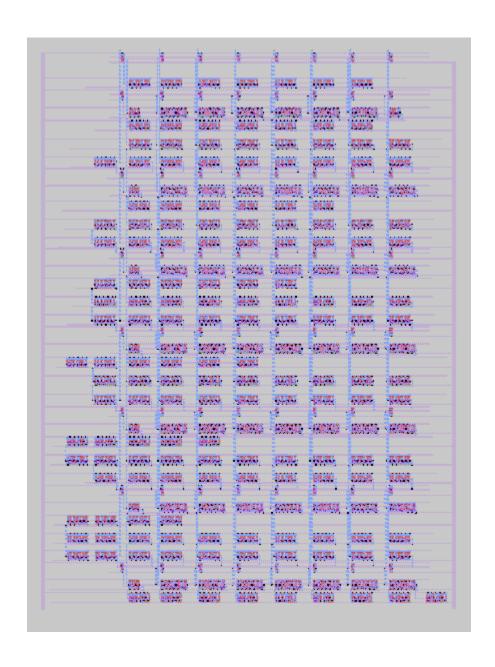
Final Project
ECGR 5133
Dr. Mukherjee

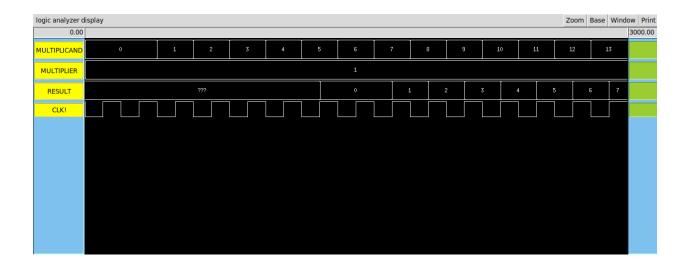
Part 1 – Non-Pipelined Layout



logic analyzer display			Zoom	Base V	Vindow	Print
0.00					80	00.00
MULTIPLICAND		87				
MULTIPLIER	229	115				
RESULT	19923	10005				

Part 2 – Pipelined Layout Without Zero Clock Skew Routing





Part 3 – Pipelined Layout With Zero-Skew Clock Routing



