Parcial-19-20.pdf

martineitor

Estructura de Computadores

2º Grado en Ingeniería Informática

Escuela Técnica Superior de Ingeniería Informática
Universidad de Málaga

Solution

COMPUTER ORGANIZATION, 3rd Partial Exam Dept. Computer Architecture Jan. 21, 2020

SURNAME:_____ NAME:_____

1) (9 points) Consider the next code for a pipelined ***MIPS*** processor, where the operating system places the code in the main memory (MM) as follow:

MM Address		
A2000h	*addi*	*$1,$0,15*
	lw	*$11, C3FC($0)*
	----	*(no j, no beq, no bne)*

A2014h	*j*	*B4018h*

B4018h	*addi*	*$8, $0,17h*
	sw	*$8, C3F0($0)*
	or	*$12,$29,$1*
	slt	*$12,$3,$7*
	----	*(no j, no beq, no bne)*

	----	
	sub	*$14,$5,$18*
	addi	*$1, $1, -1*
	sw	*$1,C3F4($0)*
B4048h	*bne*	*$1, $0, A2004h*

In addition, the operating system loads the constant FFFFh from memory position C300h through C3FFh.

Assume a main memory (MM) of 16 MBytes, and two separate caches for instructions (I$) and data (D$). The I$ has 8Kbytes, 2-way set associative, blocks of 8 words. The D$ has 4Kbytes, direct mapped, writhe-through and write allocate policy for write and with blocks of 4 words.

A. (4 points) For the I$, provide:
   0.5 1. Format of a physical address (different fields and sizes)
   0.5 2. Sequence of addresses generated for fetching instructions (use ranges (...) when needed)
   2 3. Write down the evolution of the **control and data area** of the cache for the full execution of this code (write down only the blocks of the cache that involve this code; assume that all *valid bit =0)*).
   0.5 4. Calculate the number of misses after the first and second iterations and the final miss and hit rate (in %) for the full execution of the code.
   0.5 5. How many comparators are needed to check the hit/miss condition? What is the size (in number of bits) of the numbers to be compared?
   3
B. (3 points) For the D$, provide:
   0.5 1. Format of a physical address (different fields and sizes)
   2 2. Sequence of addresses of the data cache and provide the content of the data cache (**control and data area**) after the first iteration and after the last iteration (write down only the blocks of the cache that involve this code; assume that the cache is empty before the execution of the code). Calculate the miss rate
   0.5 3. Draw the connection between different fields of the physical address and the **data cache** and give the values on the buses just during the last execution of the instruction *lw $11, C3FC($0)* (fill the gaps in the figure on the back of this sheet) .
   1.5
C. (0 points) Consider that processor works at 0.5 GHz with a miss penalty of 15 cycles for the I$ and 20 cycles for the D$. Calculate:
   0.5 1. Average access time (AMAT in both clock cycles and ns.) obtained for the execution of this code
   1 2. Calculate the speed-up regarding a system with no cache assuming where the memory access time is 30 ns. Consider the approach that for the non- cache system each instruction takes 30 ns. for execution except the lw/sw instructions that take 60 ns. (due to two memory accesses). The CPI_{base}=1.3 (CPI with a perfect cache).
D. (0.5 point) We incorporate a Virtual Memory to our system. What is the number of bits of the page offset field of the virtual address if we want that the search in the TLB and the in the cache be carried out in parallel?

2) (1 point) Consider a two-level cache system L1, L2. The miss rate for L1 is 4 % and for L2 is 6 %. Calculate: a)Global miss rate of the memory system. b) If the total number of references is 150.000, calculate the number of misses of L1 , the number of references of L2 and the number of times that the system accesses the Main Memory

Solution 1

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NOMBRE: _____

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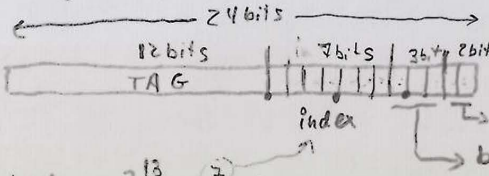
(1) A. 1) 4 points

16MB = 2^{24} B (24 bits address of MM)

1 Block = 8 words

Cache = 4 Kbytes

2-way set assoc.



0.5

Cache 8KBytes $\frac{1\text{word}}{4\text{bytes}} \cdot \frac{1\text{block}}{8\text{words}} \cdot \frac{1\text{set}}{2\text{blocks}} = \frac{2^{13}}{2^6} = 2^7$ sets

2) A2000, A2004 A2008 ... A2014, B4018, ... B4048

14 times

0.5

3)

2

	index			set	TAG	1st	2nd
A2000	A2	0000 000	0 0000	0	A2	X	
A2004			0 0100	0	A2	✓	
A2008			0 1000	0	A2	✓	
A200C			0 1100	0	A2	✓	
A2010			1 0000	0	A2	✓	
A2014	A2		1 0100	0	A2	✓	
B4018	B4	0000 000	1 1000	0	B4	X	
B401C	"	"	1 1100	0	B4	✓	
B4020	B4	0000 001	0 0000	1	B4	X	
B4024	"	"	0 0100	1	B4	✓	7✓
B4028						✓	
B402C	B4	0000 001	1 1100	1		✓	
B4030	B4	0000 010	0 0000	2	B4	X	
B4044			0100			✓	
B4048			1000			✓	

SET	V	TAG	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	A2	-	-	j	-	-	-	-	-	lw	addi			
	1	B4	sw	addi	-	-	←	-	-	-	-	-			
1	1	B4	sub	-	→	sw	-	-	-	-	slt	or			
			-	-	-	-	-	-	-	-	-	-			
2	1	B4	-	-	-	-	-	-	-	-	bne	sw	addi		
	0														

4) misses 1st → 4
2nd → 0

$R_{miss}(I\$) = \frac{4}{1+(5+2+11)\cdot 15} = \frac{4}{271} = 0.0147 \rightarrow 1.47\%$ (98.53%)

0.5

5) 2 computers (2-way set assoc), 12 bit numbers

0.5

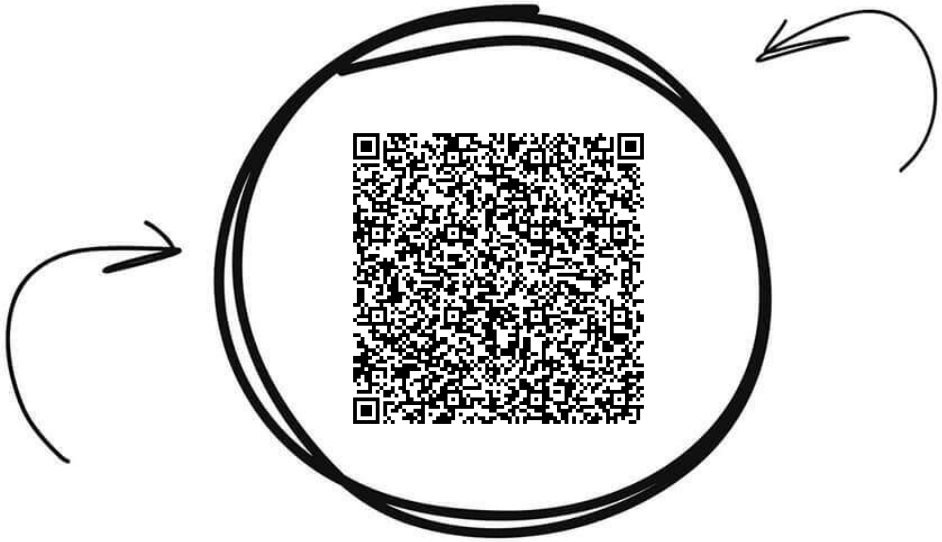
BEST LIFE EXPERIENCE

Viajar nunca fue tan *Barato*

Marruecos *en 3 días*

- **Transporte privado** en autobús
- Pasajes **de Barco** ida y vuelta
- Visitas a **Chefchaouen**, **Assilah**, **Tánger** y **Tetuán**
- **Guías nativos** profesionales durante todo el viaje
- Pequeño **paseo en camello**
- 2 Noches en Hotel de **3 o 4 estrellas**
- **Desayunos** y **cenas** incluidos
- **Fotos** del viaje

Estructura de Computadores



Banco de apuntes de la

WUOLAH

Comparte estos flyers en tu clase y consigue más dinero y recompensas

1. Imprime esta hoja
2. Recorta por la mitad
3. Coloca en un lugar visible para que tus compis puedan escanar y acceder a apuntes
4. Llévate dinero por cada descarga de los documentos descargados a través de tu QR

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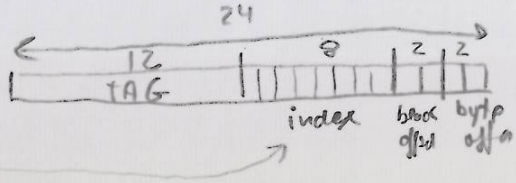
B) D$ → 4KB, direct mapped, write-through, 1 block = 4 words

(3)

1)



0.5

Cache → 4KBytes · 1 word / 4 bytes · 1 block / 4 words = $2^{10}/2^2 = 2^8$ blocks

2) C3FCh, C3F0, C3F4 0.5

15 times

		index			block	TAG	miss 1st	miss 2nd
C3FC →	1100	0011 1111	1100		3F	C	✓	✓
C3F0 →	1100	0011 1111	0000		3F	C	✓	✓
C3F4 →	1100	0011 1111	0100		3F	C	✓	✓

	V	TAG	3	2	1	0
1st →	3F	1	Ch	FFFFh	FFFFh	14 (Eh)	17h
last →	3F	1	Ch	FFFFh	FFFFh	0	17h

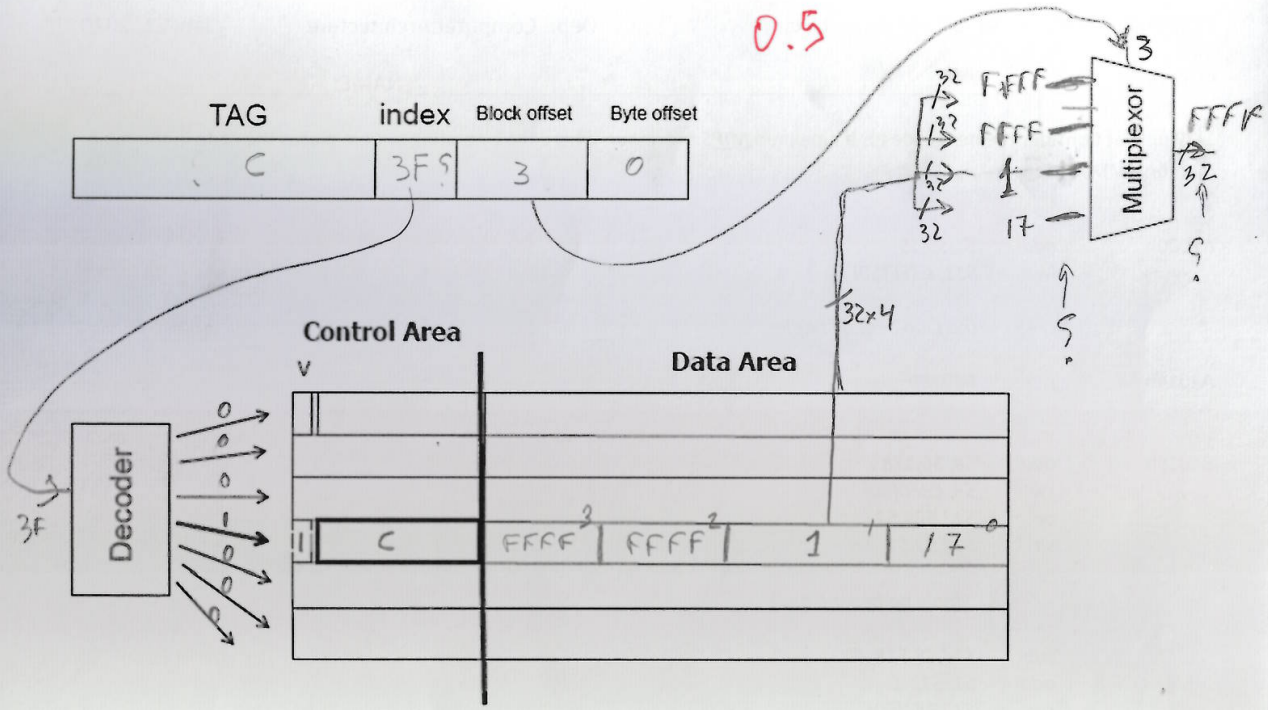
1.5

Miss (D$) = $\frac{1}{3 \cdot 15} = \frac{1}{45} = 0.022 \rightarrow (2.2\%)$

3) See next page 0.5

Solution 3

0.5



Solution 4

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NOMBRE: _____

C) 0.5 GHz (2ns=cc) $P_{miss}(I\$) = 15cc$ $P_{miss}(D\$) = 20$

1.5

1.) $AMAT = T_{hit} + P_{miss}(I\$) P_{miss}(I\$) + \%_{Inst} \cdot P_{mis}(D\$) \cdot P_{miss}(D\$) =$

0.5 $= 1cc + 0.0147 \cdot 15 + \frac{3.15}{271} \cdot 0.022 \cdot 20 = 1.29 cc$

$= 2.58 ns$

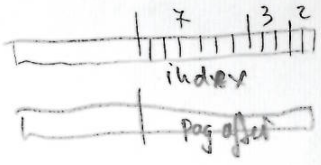
2) $T_{No\_caché} = 271 \cdot 30ns + 3.15 \cdot 30ns = 9480 ns$

1 $CPI_{effect} = CPI_{base} + P_{miss}(I\$) P_{miss}(I\$) + \%_{Inst} \cdot P_{mis} \cdot P_{miss} =$

$= 1.3 + 0.0147 \cdot 15 + \frac{3.15}{271} \cdot 0.022 \cdot 20 = 1.593 cc$

$T_{CPU} = IC \cdot CPI \cdot CC = 271 \cdot 1.593 \cdot 2ns = 863.4$

$Speedup = \frac{9480}{863.4} = 10.97$

D) 

→ 12 bits

0.5

2) $R_{missL1} = 4\%$ $R_{missL2} = 6\%$

1 0.25 a) $R_{miss\ global} = R_{missL1} \cdot R_{missL2} = 0.04 \cdot 0.06 = 0.0024$

b) $NR = 150000$

0.75 • $R_{missL1} = \frac{N_{missL1}}{NR}$

$N_{missL1} = R_{missL1} \cdot NR =$

$= 0.04 \cdot 150.000 =$

$= 6000$

• $NR_{L2} = N_{missL1} =$

$= 6000$

• $N_{accessMM} = N_{missL2} =$

$= R_{missL2} \cdot NR_{L2} =$

$= 0.06 \cdot 6000 = 360$

si lees esto me debes un besito