Integrated Masters in Aerospace Engineering, Técnico, University of Lisbon

Circuit Theory and Electronics Fundamentals

Laboratory Report 3

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1 Introduction

For the third experimental activity in the Circuit Theory and Electronics Fundamentals course, we had to design and analyse an AC/DC converter circuit. In order to do it, the group chose the architecture of both the Envelope Detector and Voltage Regulator circuits. The circuit is shown in the image below.

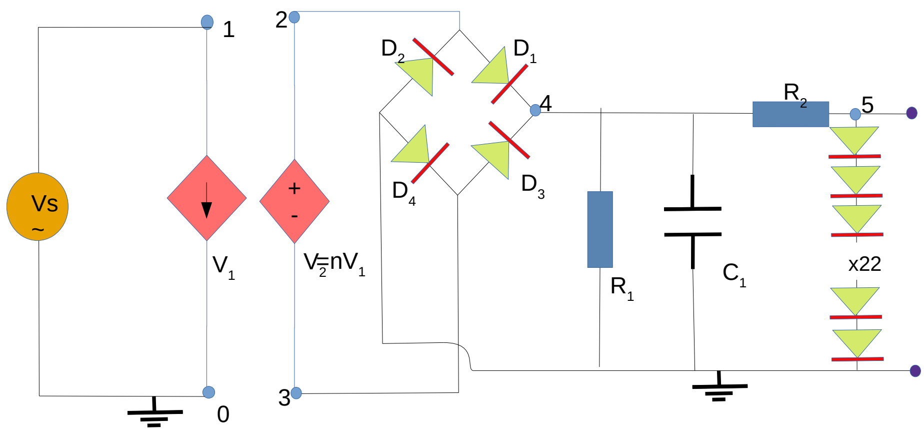

Figure 1: Circuit

In the first part of the circuit we use a transformer to decrease the voltage, then we use a full-wave rectifier circuit, using four diodes, and finally we have the Envelope Detector and Voltage Regulator circuits. With this configuration we pretend to obtain an output voltage at the desired value (12V), with the minimum variations.

2 Theoretical Analysis

In this section, we are going to show how we proceed to fulfill the goal of this lab.

1) We used a transformer to transform Vs=230V in a smaller value (V_s/n with n=10), but with this we still had an AC voltage, and we want a DC voltage.

2)Using four diodes we did a full wave rectifier circuit which allows us to transform the sinusoidal signal in a module function of a sinusoidal function, as you can see in the plots below.

3)Then, a capacitor was used to make the voltage more close to a DC voltage, as it damps the sinusoidal ripple. To compute this we had to decide when the diodes are ON and OFF. So, we compute toff and ton using the Newton-Raphson's iterative method. To compute toff we use the equation

$$(Vs/n) * C * w * sin(w * t_{off}) = (1/R1) * (Vs/n) * cos(w * t_{off}) + I_s * (exp(12/(eta * Vt * k)) - 1) \tag{1}$$

which represents $i_D = i_R + i_C$;
and to compute ton we use the equation

$$(Vs/n) * cos(w * t_{on}) = -(Vs/n) * cos(w * t_{off}) * exp(-(1/(Req * C)) * (t_{on} - t_{off})) \tag{2}$$

Periodically, if $t < t_{off}$ we got

$$v0_{env}(i) = abs((230/n) * cos(w * t(i))) \tag{3}$$

and if $t > t_{off}$ we got

$$v0_{env}(i) = (230/n) * abs(cos(w * t_{off})) * exp(-(1/(Req * C)) * (t(i) - t_{off})) \tag{4}$$

Ripple Envelope	3.190392e-04 V
Average Envelope	2.299984e+01 V

Table 1: Ripple and Average Voltages of the Envelope

4)Lastly, we use a total of 22 diodes and a resistor to make the voltage in the output of the voltage regulator circuit an almost perfect 12V DC voltage. To do this we did an incremental analyses. So, the $v0_{reg} = v0reg_{ac} + v0reg_{dc}$. To compute the $v0reg_{ac}$ we use the voltage divider between the resistance and the equivalent resistances of the diodes in the incremental analyses. The average voltage and the ripple obtained are shown in the table below.

Ripple Regulator	8.428860e-06 V
Average Regulator	1.200000e+01 V

Table 2: Ripple and Average Voltages of the Regulator

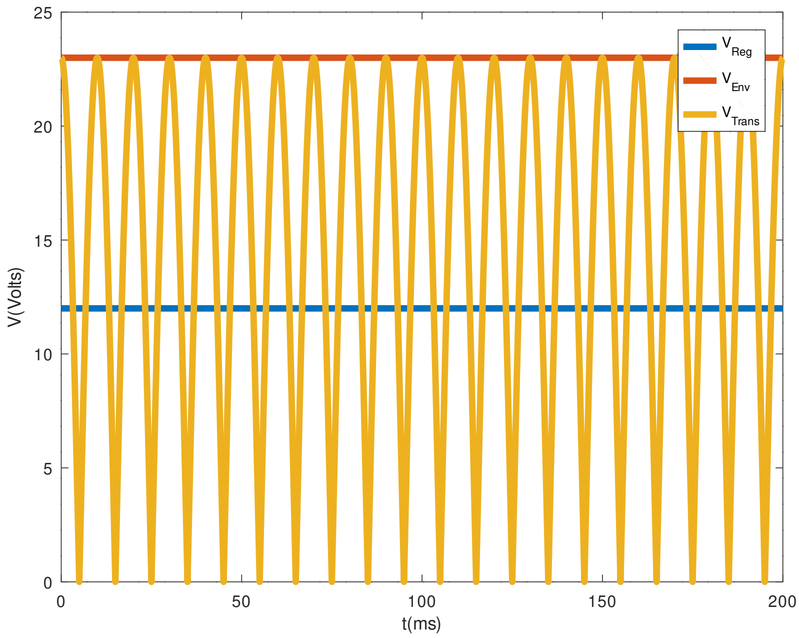

Figure 2: Regulator, Envelope and Transformer Voltages

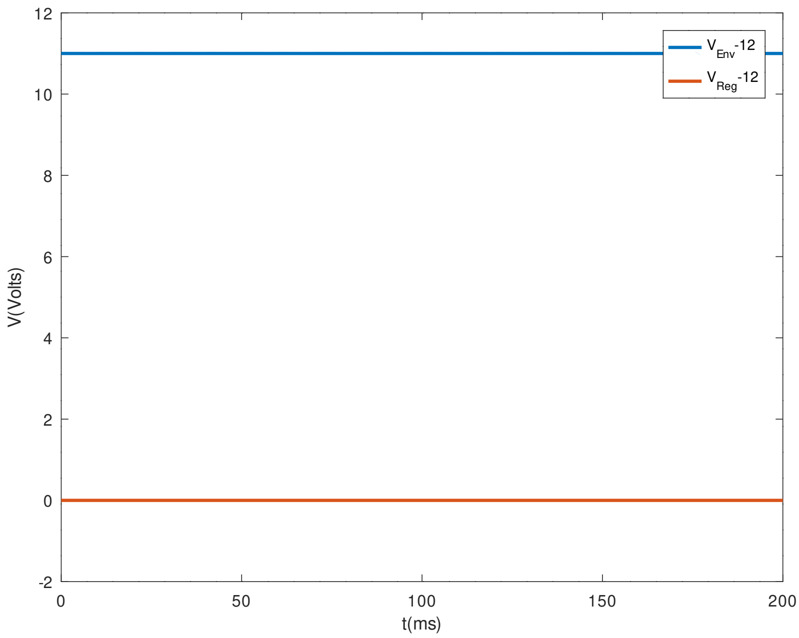

Figure 3: Output AC component - DC deviation

3 Simulation Analysis

In this section we used NGSpice to simulate our solution for the ac/dc converter. Firstly, to simulate the transformer we used a dependent current source (instead of the primary) and a dependent voltage source (instead of the secondary). Then, the values of n (parameter of dependency of the dependent sources), the capacitance of the capacitor and the values of the resistances of the resistors, were obtained by an optimization program done in Matlab, with the help of Simulink. But, because our theoretical model is not perfectly coincident with the real one, that NGSpice simulate, we had to do small adjustments in this values in order to obtain the best solution.

In the table below, you can see the voltage of the secondary circuit (Vs/n), output Voltage of the Envelope Detector (V(4), the output voltage of the Voltage Regulator (v(5)), and Voltage Regulator-12.

maximum(v(4))-minimum(v(4))	5.369989e-03
mean(v(4))	2.177128e+01

Table 3: Results for the envelope detector (Ngspice)

maximum(v(5))-minimum(v(5))	2.955111e-04
mean(v(5))	1.200000e+01

Table 4: Results for the voltage regulator (Ngspice)

As you can see Voltage Regulator - 12 is almost a straight line close to 0, that was the main goal of the assignment.

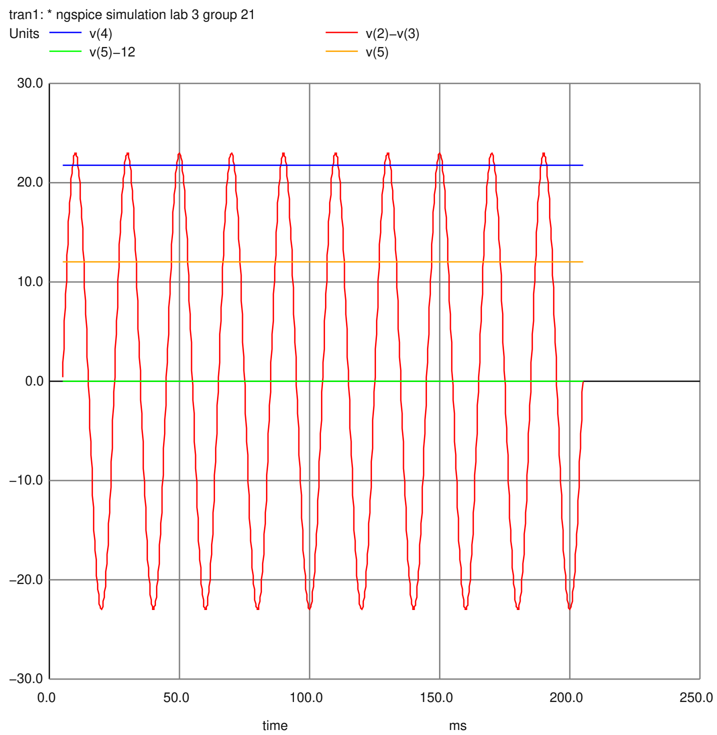

Figure 4: Input Voltage of the secondary circuit(v(2)), Output voltage of the Envelope Detector(v(4)), Voltage Regulator (v(5)) and v(5)-12

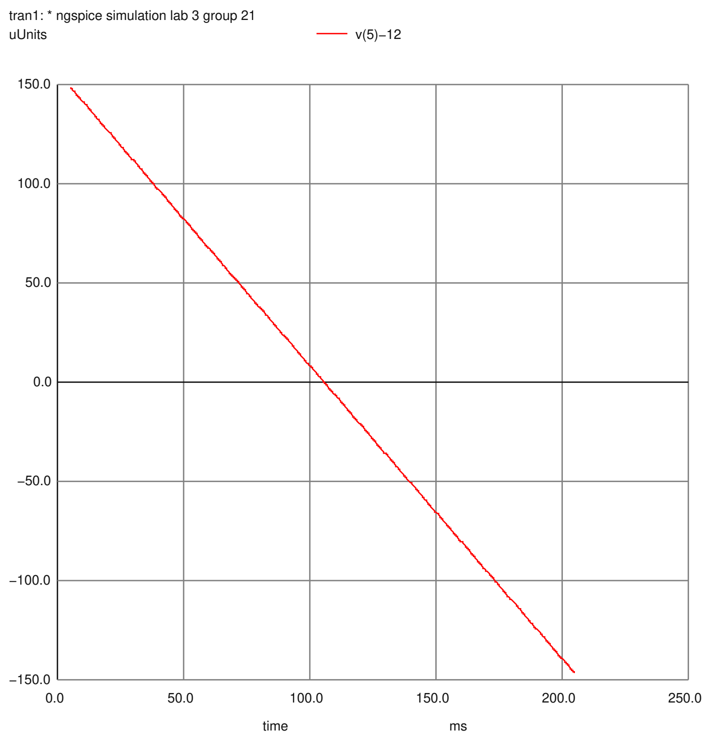

Figure 5: v(5)-12

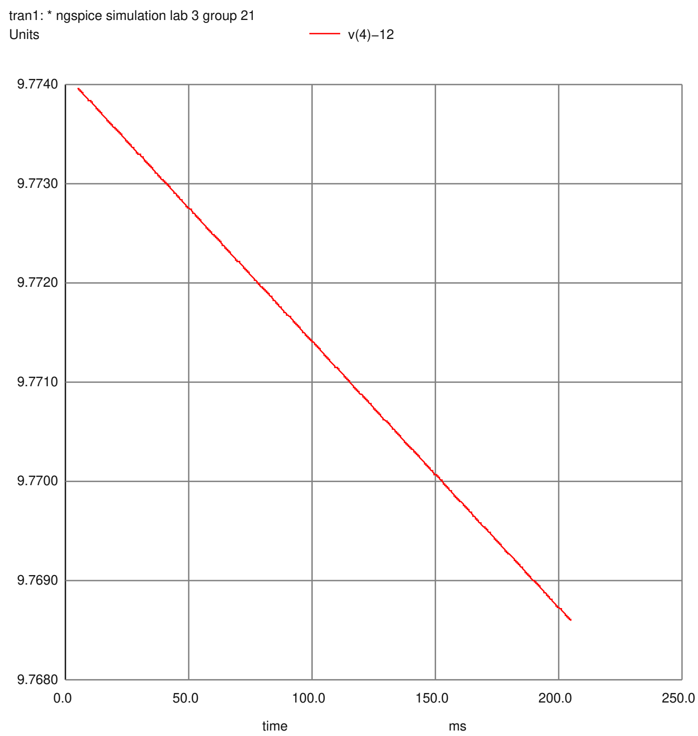

Figure 6: v(4)-12

4 Comparison

In this section, a comparison between the ripple voltages, the average output voltages were made. In addition, the cost of the components and the figure of merit were also calculated. Average voltage and the ripple voltage of the envelope detector (v(4)). [tabela]

maximum(v(4))-minimum(v(4))	5.369989e-03
mean(v(4))	2.177128e+01

Table 5: Results for the output of the Envelope Detector (Ngspice)

Ripple Envelope	3.190392e-04 V
Average Envelope	2.299984e+01 V

Table 6: Results for the output of the Envelope Detector (Octave)

After analysis of the tables above, some discrepancies are observed. These are due to the oscillations that naturally occur in Ngspice. Nevertheless, the group achieved with accuracy and precision good results for the model of the envelope detector to be validated.

Average voltage and the ripple voltage of the voltage regulator (v(5)).

maximum(v(5))-minimum(v(5))	2.955111e-04
mean(v(5))	1.200000e+01

Table 7: Results for the output of the Voltage Regulator (Ngspice)

Ripple Regulator	8.428860e-06 V
Average Regulator	1.200000e+01 V

Table 8: Results for the output of the Voltage Regulator (Octave)

To improve the Ngspice simulation results we made small adjustments on the components' value. Although we could never get the results as accurate as in Octave. The oscillations between theoretical and simulation results that happened in the output voltage of the envelope detector are extended to the voltage regulator for the same reasons. Hence, a small discrepancy between the results of both models was expected to happen. Nevertheless and once more, we believe that once the output voltage is approximately 12V, as wanted, the model worked successfully.

As for the cost and figure of merit, these are shown in table 9.

$$1/(509 * ((maximum(v(5)) - minimum(v(5))) + abs(mean(v(5) - 12)) + 10e - 6)) \tag{5}$$

1/(7800.6*((maximum(v(5))-minimum(v(5))) + abs(mean(v(5)-12)) + 10e-6))	4.183756e-01

Table 9: Merit Figure (Ngspice)

5 Conclusion

All analyses have been performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. To conclude, we believe that the main goal of the task proposed was achieved. Considering the output voltage and the ripple voltage of the regulator, in both theoretical and simulation analyses, we agreed that an accurate solution to this problem was reached. This solution was not only accurate but at the same time a very cheap solution, as you can see by the merit function. So, a good quality-cost balance was found. Overall this solution was a very successful one.