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This paper has been accepted for publication by

**IEEE Journal of Emerging and Selected Topics in Power Electronics.**

**DOI**

10.1109/JESTPE.2019.2904290

**Citation**

Z. Tong, G. Zulauf, J. Xu, J. Plummer, and J. Rivas-Davila, "Output Capacitance Loss Characterization of Silicon Carbide Schottky Diodes," *IEEE J. Emerging and Selected Topics in Power Electronics*, pp. 865-878, Jun. 2019.

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# Output Capacitance Loss Characterization of Silicon Carbide Schottky Diodes

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**Abstract**—In high-frequency (HF) and very high-frequency (VHF) rectifiers, silicon carbide (SiC) Schottky diodes exhibit higher losses compared to what is reported in manufacturer-provided simulation models, with additional power loss stemming from energy dissipation during the charging and discharging of the junction output capacitance ( $C_J$ ). Because these losses are not included in manufacturer simulation models and have not been well-studied for commercially-available SiC Schottky diodes, we have experimentally measured them using the Sawyer-Tower circuit. From these measurements, we compare the losses across manufacturers, current rating, generation, voltage rating, and packaging. We then demonstrate the performance of these devices on a 20 MHz class-DE rectifier and compare their power dissipation from the simulation and experimental measurements. Lastly, by incorporating these losses in device power dissipation calculations in various rectifier topologies, we propose suggestions on device selection to optimize converter efficiencies.

## I. INTRODUCTION

Power electronics circuit designers have pushed switching frequencies into the high (3-30 MHz) and very high (30-300 MHz) radio frequency (RF) ranges, as a means to increase the power density of dc-to-dc systems. Additionally, applications such as wireless power transfer [1], plasma generation for semiconductor processing [2], and compact fluorescent lighting [3] demand power transfer in the megahertz (MHz) frequencies, drawing further interest in building converters switching at MHz speeds. The challenge of developing power converters at higher frequency ranges is managing the losses of the various components in the converter, whether the magnetic components, such as the inductors and transformers, or the power semiconductor switches. While operating in these

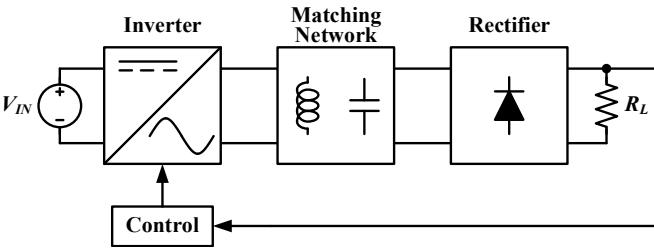


Fig. 1. Conventional dc-dc power converter system utilizing an RF inverter, rectifier, and impedance matching network as an intermediate stage.

frequency ranges, previous literature has shown the possibility of eliminating core losses by implementing air-core inductors [4]. However, analyzing and solving the losses from the semiconductors pose another challenge. In conventional hard-switching topologies, switching losses from the time overlap

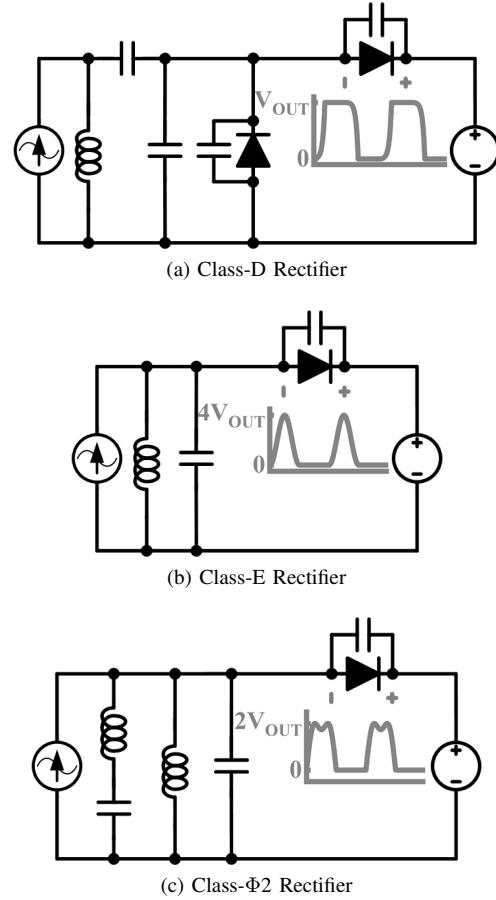


Fig. 2. Simplified schematics of class-D, class-E, and class- $\Phi$ 2 rectifiers, along with the diode voltage stressed labeled in gray.

of voltage and current through the device grows linearly with frequency. The technique to overcome this is to transition to resonant topologies. However, losses in the power semiconductor devices are still limiting efficiencies in HF/VHF circuits, especially when recently published papers like [5] highlight hysteretic charging and discharging of the output capacitance  $C_{OSS}$  in wide bandgap devices. [6], [7] study the losses in GaN high-electron-mobility transistors (HEMTs) and silicon superjunction metal-oxide-semiconductor field-effect transistors (MOSFETs), but there has not been an extensive quantity of loss characterizations done on diodes.

In this study, we focus primarily on SiC Schottky diodes. These devices are attractive for high-frequency rectifier applications, because firstly, they offer significantly larger reverse blocking voltages, close to ten times, their silicon counterparts

[8]. Higher voltage-rated devices are useful for soft-switching rectifier topologies, such as the class-D, class-E, and class- $\Phi_2$ , where the voltage stress across the device can range from the output voltage ( $V_{OUT}$ ) to four times  $V_{OUT}$ , as seen in Figure 2 [9]–[11]. Secondly, SiC Schottky diodes are majority carrier devices, which do not suffer from reverse recovery losses [12]. Traditional P-N and P-I-N junctions transfer charge carriers through minority carrier injection, where holes are injected into the N-doped region and electrons are injected into the P-doped region [13]. If the external circuitry forces the diode to transition from conducting to non-conducting, the minority carriers must be released so the diode has a sharp reverse-direction current, generating additional losses [14].

Despite these advantages, the technology of wide-bandgap devices like SiC and GaN is not as mature as Si, with decades worth of development. Therefore, it is not a surprise that recent papers such as [5], [6] observe additional losses from charging and discharging of  $C_{OSS}$  for wide-bandgap devices, pushing converter efficiencies much lower than expected in simulation using devices at frequencies much higher than what manufacturers market them for. In this study, we see a similar phenomenon for commercially available SiC Schottky diodes, and measure as well as quantify the losses across various manufacturers and ratings. This paper extends from a previously published conference paper [15]. This paper verifies the precision of the Sawyer-Tower circuit by measuring control studies of a C0G capacitor and C0G capacitor with a large series resistance, which the conference paper does not address. In addition, we experimentally remeasured and updated using new devices tested in the previous paper using newer equipment. We also include an additional section that discusses device selection strategies to improve efficiencies for HF resonant rectifiers by taking into account both conduction losses and charging and discharging losses from the junction capacitance. Section II reviews previous literature discussing the off-state losses. Section III describes the Sawyer-Tower measurement procedure. Section IV and V analyze the measurement results and the loss implications in a resonant rectifier topology. Lastly, Section VI provides circuit design techniques to minimize total losses in a rectifier design.

## II. BACKGROUND

The following work is motivated by previous literature that has evaluated diode performance in resonant rectifiers. A study by Santiago-Gonzalez et al. [16] compares the performance of commercially available silicon diodes in a class-E rectifier. Because this paper investigates under 100 V-rated silicon devices, we believe that the output capacitance losses are not well-observed, which is why the devices show small (under 0.5 W) differences in power dissipation across comparisons [16]. On the contrary, [17] examines losses in SiC Schottky diodes in a class-D rectifier operating at 27.12 MHz with output voltage and power ranging from 170 V to 1 kV and 8.5 W to 100 W respectively, exhibiting several watts of distinction between device power dissipation. [17] reports that the power losses are independent of the current through the device but highly dependent on frequency and voltage swing of the reverse-biased voltage. Furthermore, the authors' results hint that there

exist power losses unrelated to conduction, but possibly due to energy dissipation in charging and discharging of  $C_J$ , which would scale with both voltage and frequency and thus lead to the dV/dt dependency [17]. Secondly, [18] investigates soft-switching losses among SiC devices and reports that devices stressed under 7 kV and switching at 200 kHz experience over 37 W of switching power dissipation but only 90 mW of conduction losses, where the difference results from losses occurring from capacitive charging and discharging. Their results highlight that off-state losses in converters switching even under HF can greatly hinder efficiency.

A paper by Park et al. extends the findings from [17] by measuring the power losses between SiC Schottky diodes and GaN HEMTs implemented as diodes in a class-DE rectifier [19]. The authors claim that the losses from these devices, which show significant deviation from simulation and implementation, do not stem from faulty design by highlighting close matching between measured voltage waveforms and simulation voltages [19]. Also, the losses are highly unlikely to be caused from underestimation of conduction losses because the converters designed in this study operate at 9, 18, and 25 W output powers, meaning the average currents through the diodes would be below 100 mA. This would equate to the diodes having an equivalent resistance in the k $\Omega$  range for them to dissipate the powers shown in Figure 3. Using the results from the later Section IV, where we measured the capacitance losses in devices from [19], we observe in Figure 3 that there are close similarities between our predicted off-state losses and [19]'s result. This shows that it is likely that these losses do originate from the charging and discharging of  $C_J$ .

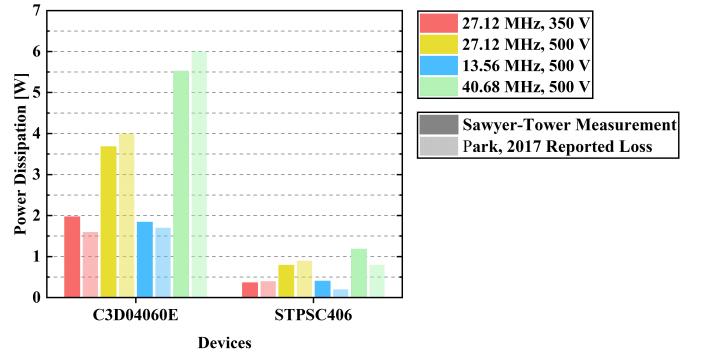


Fig. 3. Comparison of power losses from devices tested in a class-DE rectifier from [19] with what we measure from the Sawyer-Tower circuit, examined in Section IV, at the same operating peak voltages and frequencies.

Lastly, we would like to note that this investigation does not claim any physical causes or mechanisms behind the output capacitance losses, because all of the devices tested in this experiment are commercially available which we do not have propriety information on. However, it is interesting to note that there is prior literature that investigates  $C_{OSS}$  loss mechanisms of sister devices such as silicon superjunction MOSFETs. [20] reports significant energy loss due to stranded charges that are trapped along the edges of the trenches in the superjunction devices as the depletion region grows when  $C_{OSS}$  is charged.

Although speculative, it is not unlikely that trapped charges is similarly the mechanism behind the losses in SiC devices.

### III. MEASUREMENT PROCEDURE

When a Schottky diode is turned off, the device can be modeled as a capacitor with a nonlinear capacitance inversely proportional to the reverse-biased voltage. To measure the losses of the output capacitance, we must cyclically charge and discharge the capacitor while ensuring that the diode never conducts. We use the Sawyer-Tower circuit, with similar methodology to [6], [7] to measure the charge-voltage hysteresis corresponding to the per cycle energy loss of the device's  $C_J$ .

#### A. Sawyer-Tower Circuit Operation

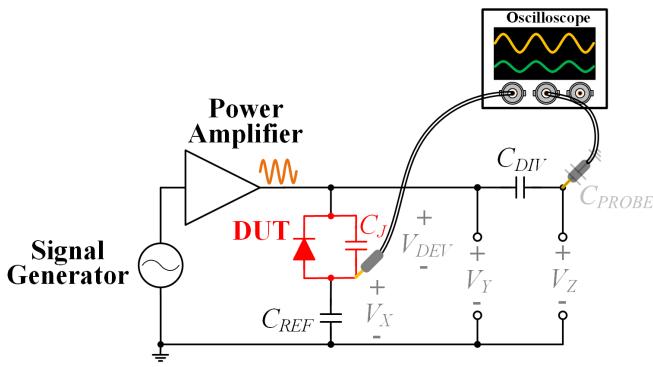
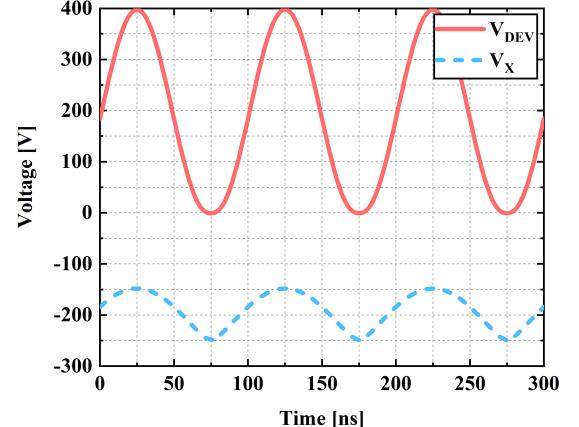


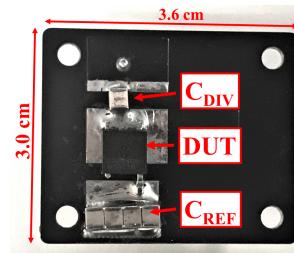
Fig. 4. Schematic of Sawyer-Tower circuit used in the measurement procedure.

The Sawyer-Tower circuit operates as follows. We apply a large sinusoidal signal from the output of the power amplifier across  $V_Y$ . Because  $C_J$  and  $C_{REF}$  form a capacitive voltage divider, the voltages  $V_{DEV}$  and  $V_X$  are also sinusoidal with amplitudes  $\frac{C_{REF}}{C_J+C_{REF}} \cdot V_Y$  and  $\frac{C_J}{C_J+C_{REF}} \cdot V_Y$  respectively.  $C_{REF}$  serves as a charge reference capacitor for the device under test (DUT) and allows us to trace the instantaneous charge stored in  $C_J$  through  $Q_{DEV} = C_{REF} \cdot V_X$ . We size  $C_{REF}$  to approximately 10 times the datasheet  $C_J$  value at 100 V<sub>DC</sub> so that  $V_{DEV} \approx V_Y$ . We use C0G ceramic capacitors to provide the best linearity and temperature stability. Additionally, we measure  $C_{REF}$  using a Keysight E5061B network analyzer. We set the network analyzer to impedance measurement mode and use the Keysight 16201A and 16092A test fixtures. Then, we calibrate using open, short, and 50 Ω load with the Keysight 16195B calibration kit. To record  $Q_{DEV}$ , we directly measure  $V_X$  using the oscilloscope probe, and to obtain  $V_Y$ , we measure  $V_Z$  with a second probe, where  $V_Z$  is the same sinusoidal signal as  $V_Y$  but attenuated by  $\frac{C_{DIV}}{C_{DIV}+C_{PROBE}}$ . The purpose of measuring an attenuated version of  $V_Y$  is the probes used in our experiment de-rate above 100 V<sub>RMS</sub> at 10 MHz. The tolerance of  $C_{DIV}$  is not as important as  $C_{REF}$  because we measure the attenuation from  $V_Y$  to  $V_Z$  directly using a 50 V peak-to-peak test signal. Also, all calibration is performed at every frequency to eliminate frequency-dependent variables from our measurement. We

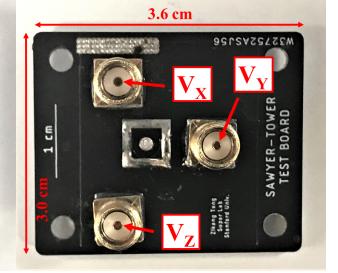
then obtain  $V_{DEV}$  through  $V_Y - V_X$ . Lastly, the Sawyer-Tower circuit ensures that the diode does not conduct in steady-state through forcing a dc offset upon  $V_{DEV}$  such that  $V_{DEV}$  swings from 0 V to its peak voltage, indicated by an example SPICE simulation of the Sawyer-Tower circuit in Figure 5a.



(a) Simulation of  $V_{DEV}$  and  $V_X$



(b) Sawyer-Tower PCB Top-side



(c) Sawyer-Tower PCB Bottom-side

Fig. 5. LTSpice simulation of  $V_{DEV}$  and  $V_X$  (refer to Figure 4) emphasizing that the diode never conducts as well as images of the printed circuit board (PCB) used in the test setup.

#### B. Measurement Calculations

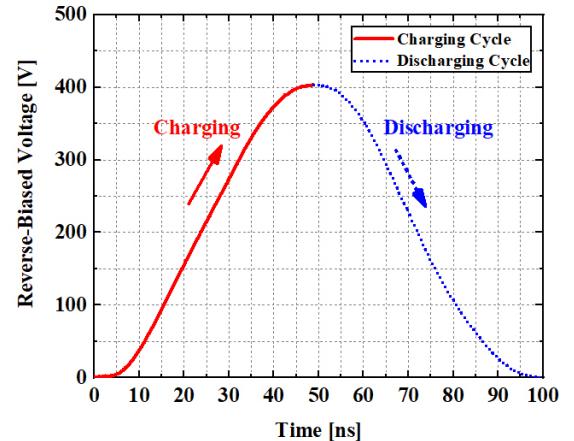


Fig. 6. Time dependent voltage swing across the device highlighting the charging and discharging half-cycles.

Once we obtain  $V_{DEV}$  and  $Q_{DEV}$ , taking one period of the recorded waveform, we can integrate  $V_{DEV}$  to get the

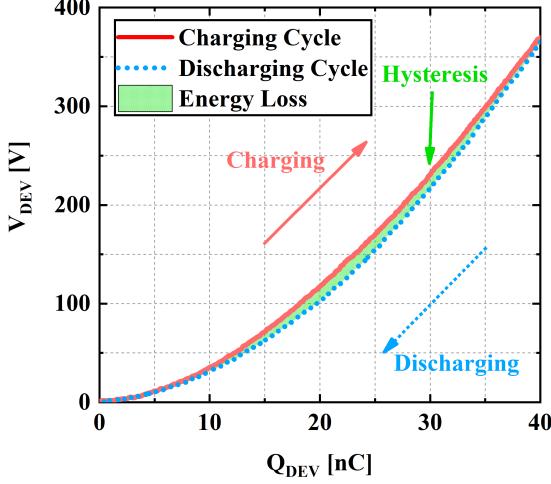


Fig. 7. Device voltage swing with respect to stored charge highlighting the hysteresis.

energy stored ( $E_{STORE}$ ) in the charging cycle and the energy released during the discharging cycle by  $C_J$  through Equation 1. Subtracting the two energies results to the net energy loss per cycle ( $E_{DISS}$ ).

$$E_{DISS} = \left\{ \int_{Q_0}^{Q_1} V_{DEV} dQ_{DEV} \right\}_{\text{CHARGING}} - \left\{ \int_{Q_1}^{Q_0} V_{DEV} dQ_{DEV} \right\}_{\text{DISCHARGING}} \quad (1)$$

Figure 7 shows a sample  $V_{DEV}$  vs  $Q_{DEV}$  curve, highlighting the hysteresis. In this study, we sweep the peak voltage from 200 V to 550 V in 50 V increments and repeat for 5, 10, and 20 MHz, up to the limits of the ENI power amplifier. Figure 8 shows a sample measurement sweep for FFSD10120A from ON Semiconductor. Because we observe negligible variation

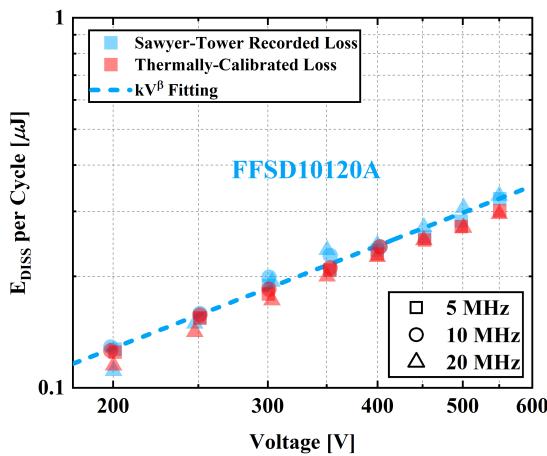
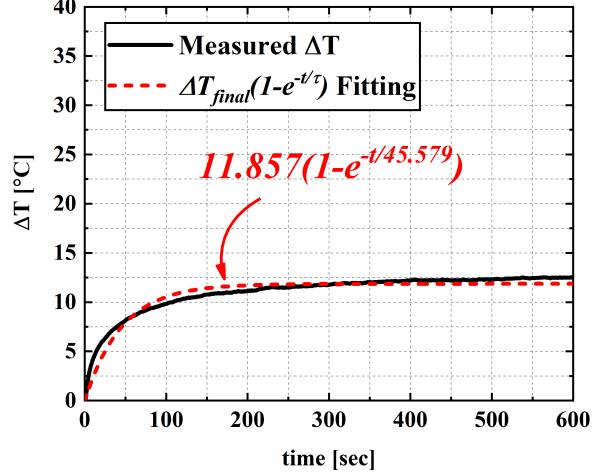


Fig. 8. Example per cycle energy dissipation versus peak voltage swing curve for FFSD10120A measured electrically from the Sawyer-Tower circuit as well as thermal measurements calculated using Equation 3.

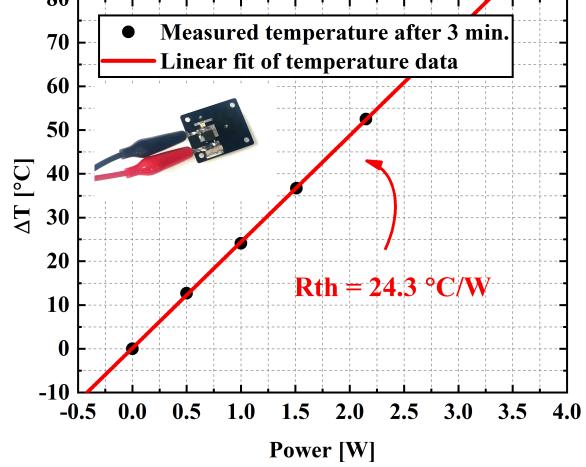
across the frequencies tested, we create a voltage-dependent power law fitting using Equation 2. This is similar to Steinmetz fittings done for core losses in magnetic components.

$$E_{DISS} = k \cdot V^\beta, P_{DISS} = k \cdot f \cdot V^\beta \quad (2)$$

Finally, after every measurement point collected, we ther-



(a) Temporal Temperature Rise



(b) dc Thermal Measurement of FFSD10120A

Fig. 9. (a) Temporal temperature rise ( $\Delta T$ ) with 0.5 W applied power for 10 minutes. The dashed red line shows the  $A(1 - e^{-t/\tau})$  fitting, with a thermal time constant ( $\tau$ ) of 45 seconds. In all of our measurements, we record the temperature after 3 minutes ( $4\tau$ ), which is approximately 98% of the final steady-state temperature rise. (b) Device max temperature rise from ambient temperature after a 3 minute thermal soak at various applied dc power points. Thermal impedance ( $R_{th}$ ) were extrapolated from the slope. Shown thermal data are using DUT in a D-Pak package.

mally verify our result, after a 3 minute thermal soak, by obtaining the temperature of the device and calculating the energy dissipation through Equation 3. Figure 9b shows the methodology of obtaining the thermal impedance ( $R_{th}$ ), which is the slope of temperature rise when dc power is injected into the device. For this experiment, the temperature measurements were performed in an open laboratory environment rather than a thermally controlled chamber. Regardless, the thermal measurements are used to validate the electrical measurements. The thermal measurements typically agree with the electrical measurements within 0.05  $\mu$ J.

$$E_{DISS} = \frac{\Delta T}{R_{th} f_{sw}}, \Delta T = T_{device} - T_{ambient} \quad (3)$$

To present control measurements, we start with measuring the hysteretic loss in a 33 pF C0G capacitor from Wurth

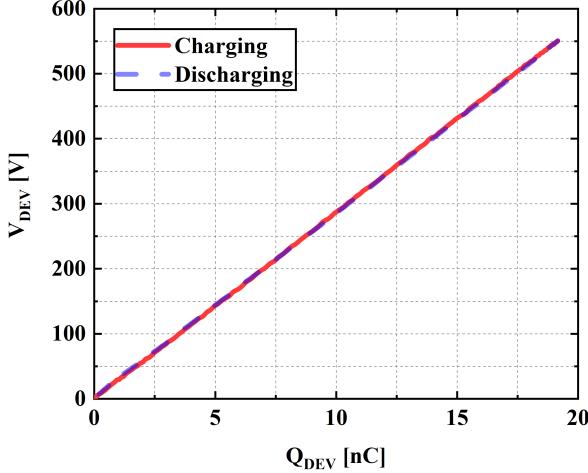


Fig. 10. Charge-Voltage plot of the Sawyer-Tower measurement of a 33 pF C0G capacitor at 20 MHz and 550 V, which exemplifies no noticeable hysteresis. The  $C_{REF}$  used was 330 pF.

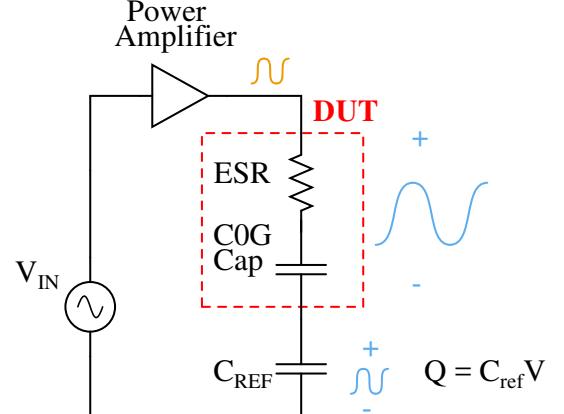
Electronics with part number 885352010007, which is 10% of the  $C_{REF}$  used. Based on Figure 10 which shows the charge-discharge of a 550 V swing, at 20 MHz, the capacitor exhibits unobservable hysteresis. Figure 11b also shows that the C0G capacitor presents negligible losses across voltages and frequencies tested. These results confirm that C0G capacitors are suitable choices to use as  $C_{REF}$  due to their low loss, which would not severely impact our measurement setup, and that the measurement setup is accurate enough to not record hysteresis for C0G capacitors, which have imperceptible internal series resistance. Secondly, we measured the losses of a reference capacitor with a 3 Ω externally-attached equivalent series resistance (ESR). Figure 11a displays the schematic of the measurement setup, and in Figure 11b, the experimentally measured losses agree well with the LTspice simulation of the same setup. Lastly, Table I lists the components used in the experiment.

TABLE I  
LIST OF COMPONENTS USED IN THE MEASUREMENT PROCEDURE.

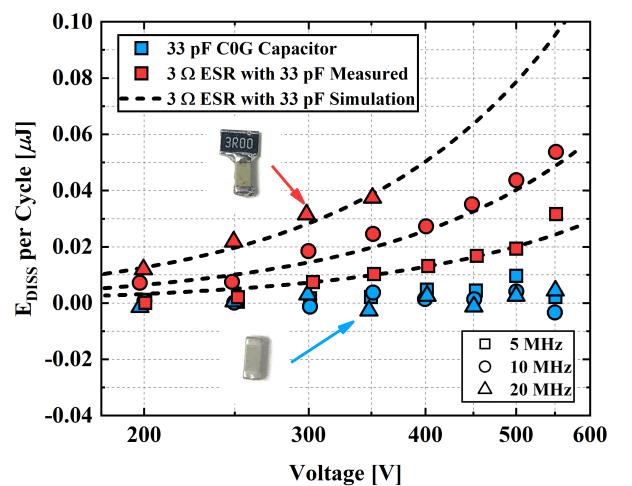
Component	Manufacturer/Part Value
Power Amplifier	ENI A1000 RF PA
Oscilloscope Probes	Agilent N2875A
Oscilloscope	Agilent MSO9404A
Signal Generator	Agilent 81150A
Thermal Camera	FLIR A655SC
$C_{DIV}$	1 pF, C0G/NP0 Dielectric
$C_{REF}$	$10 \cdot C_J$ at 100 V, C0G/NP0 Dielectric

### C. Summary of Experimental Steps

- 1) Measure  $V_{DEV}$  and  $Q_{DEV}$  of the DUT's  $C_J$  for one period using the Sawyer-Tower circuit.
- 2) Calculate the energy dissipated per cycle through Equation 1.



(a) Measurement with ESR



(b)  $E_{DISS}$  Losses with and without ESR

Fig. 11. (a) Schematic of Sawyer-Tower setup of a 33 pF C0G capacitor with a 3 Ω ESR. (b)  $E_{DISS}$  losses of the 33 pF C0G capacitor, which shows negligible losses, and of the capacitor with a 3 Ω ESR, which agrees with the LTspice simulation well. The losses are presented in linear scale in order to discriminate that the C0G capacitor has losses close to 0.

- 3) Verify the measurement with a 3 minute thermal soak, using the temperature of the device and Equation 3 to calculate  $E_{DISS}$ .
- 4) Repeat the measurements from 200 to 550 V in 50 V increments and across 5, 10, 20 MHz.
- 5) Fit the  $E_{DISS}$  per Cycle vs  $V_{DEV}$  curves with Equation 2.

### IV. MEASUREMENT RESULTS

Throughout this investigation, we measured the output capacitance losses for seventeen SiC Schottky diodes, and compared the losses across device packaging, manufacturer, current rating, device generation, and voltage rating. We offer these five different comparisons to provide predictive insight for circuit designers to select for optimal converter performance and efficiency, as well as to provide device manufacturers indications for the physical causes of these losses.

### A. Packaging Comparison

TABLE II  
LIST OF DEVICES TESTED IN THE PACKAGING COMPARISON.

Part Number	Manufacturer	Packaging	Rated V	Rated I
STPSC10H12G	STMicroelectronics	D <sup>2</sup> -Pak	1200 V	10 A
STPSC10H12B	STMicroelectronics	D-Pak	1200 V	10 A
STPSC10H12D	STMicroelectronics	TO-220	1200 V	10 A

We analyzed devices with three different packages from STMicroelectronics with packagings and ratings listed in Table II. Based on the results in Figure 12, we observe small differences in dissipated energy at high voltages. At 200 V, which is the lowest voltage measured, the D<sup>2</sup>-Pak device has 40% less energy dissipated than the other two devices.

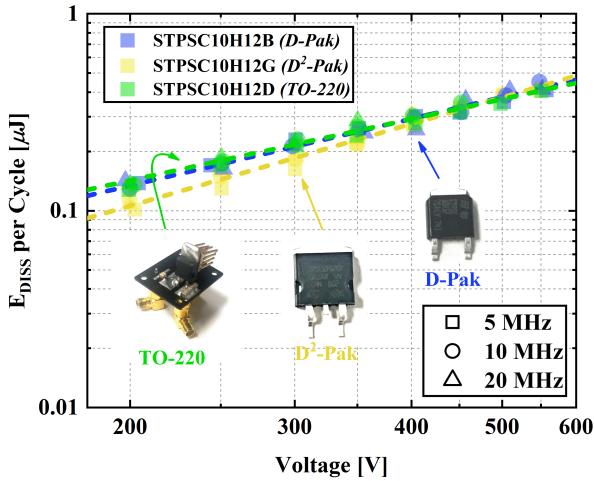


Fig. 12. Comparison of losses from 200 to 550 V across 5, 10, 20 MHz for different packagings of STMicroelectronics devices. For the TO-220 package, the device was soldered to the board using the leads and the backside was connected to a heat sink to reduce the thermal impedance of the device.

### B. Manufacturer Comparison

TABLE III  
LIST OF DEVICES TESTED IN MANUFACTURER COMPARISON.

Part Number	Manufacturer	Packaging	Rated V	Rated I
STPSC10H12B	STMicroelectronics	D-Pak	1200 V	10 A
FFSD10120A	ON Semiconductor	D-Pak	1200 V	10 A
IDM10G120C5	Infineon	D-Pak	1200 V	10 A
STPSC406B	STMicroelectronics	D-Pak	600 V	4 A
C3D04060E	Cree/Wolfspeed	D-Pak	600 V	4 A

To compare devices across multiple manufacturers, we ensured that the devices tested in this comparison have the same voltage rating, current rating, and packaging. We compare three 1200 V, 10 A rated components from STMicroelectronics, Infineon, and ON Semiconductor and two 600 V and 4 A rated parts from Cree/Wolfspeed and STMicroelectronics as listed in Table III. Results in Figures 13a and 13b show that even for the same ratings, devices from different manufacturers exhibit different quantities of losses. For the 1200 V, 10 A

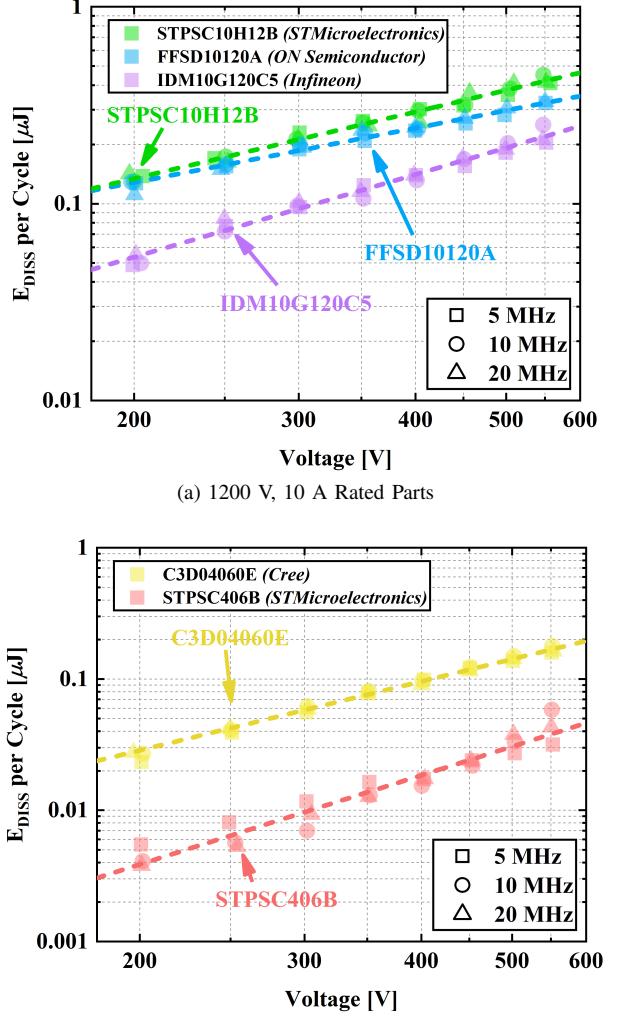


Fig. 13. Comparison of losses from 200 to 550 V across 5, 10, 20 MHz for different device manufacturers at 1200 V rating and two different devices at 600 V rating.

rated set, the Infineon device dissipates less energy than the ON Semiconductor and STMicroelectronics devices. Additionally, the 600 V, 4 A rated STMicroelectronics device dissipates less energy than the Cree/Wolfspeed device.

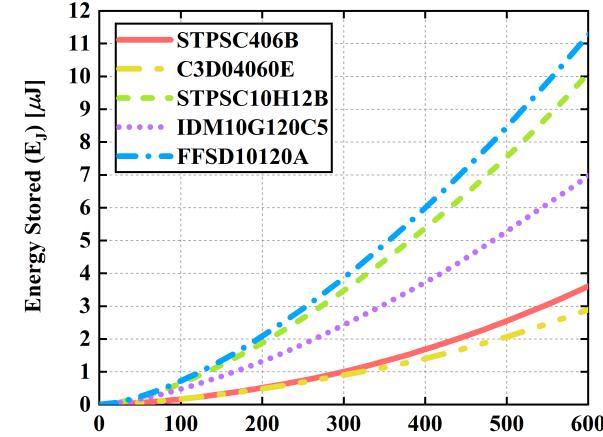
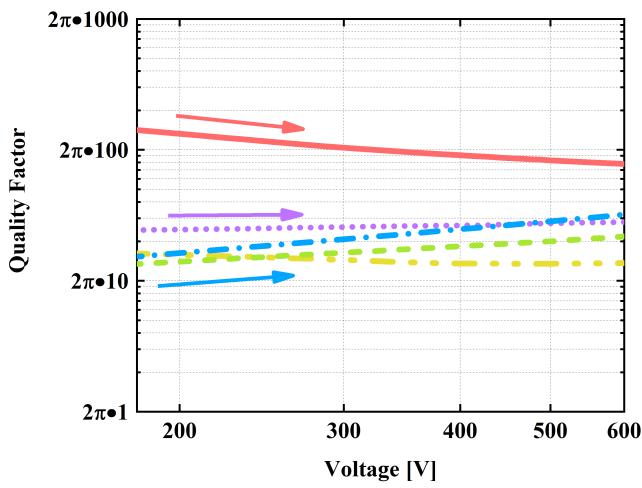
One hypothesis for why the losses vary is that despite having the same ratings, these devices store different amounts of energy at the same reverse voltages. We use Equation 4 to calculate the energy stored within the device based upon the small-signal junction capacitance.

$$E_J(V_R) = \int_0^{V_R} C_J(V) V dV \quad (4)$$

In addition, since the energy dissipated per cycle is independent of frequency, we can characterize these devices by a frequency-invariant quality (Q) factor defined by Equation 5.

$$Q(V_R) \stackrel{\text{def}}{=} 2\pi \cdot \frac{\text{energy stored per cycle}}{\text{energy dissipated per cycle}} = \frac{2\pi \cdot E_J(V_R)}{kV_R^\beta} \quad (5)$$

Figure 14b shows that the Q factors for the devices also differ significantly with the STPSC406B device having a

(a)  $E_J$  of the Five Devices

(b) Q Factors of the Five Devices

Fig. 14. Energy stored and Q factors at different voltage levels for the five devices tested in the manufacturer comparison.

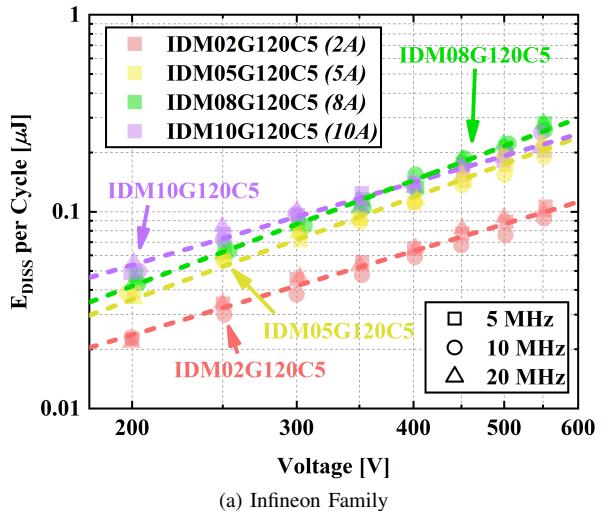
significantly higher Q factor than the rest of the devices. We also observe that devices have Q factors that vary differently with voltage. For instance, STPSC406B varies inversely with voltage, IDM10G120C5 is constant with voltage, and FFSD10120A increases with increasing voltage. Lastly, we argue that manufacturers should publish the output capacitance loss information in their datasheets and SPICE models because it is difficult to predict the losses from current datasheet information due to the voltage dependency of the Q factors.

### C. Current Rating Comparison

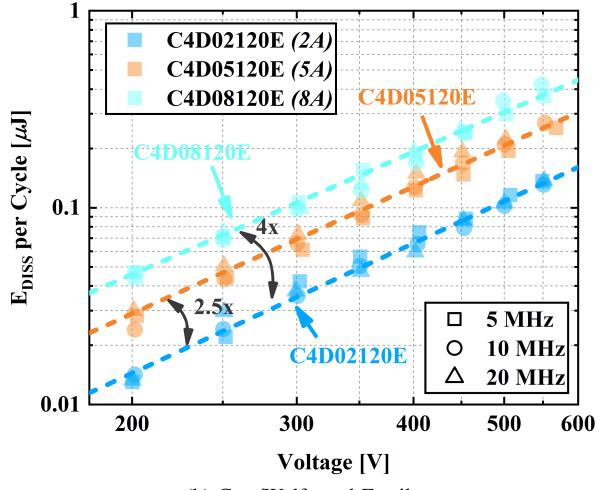
We compare families of devices from Cree/Wolfspeed and Infineon listed in Table IV, where all devices are 1200 V rated and are packaged in a D-Pak case. Figures 15a and 15b indicate that, in general, the output capacitance energy dissipation increases as the current rating increases. Very often, device manufacturers increase the current rating by scaling the die area, highlighting that the losses are dependent on die geometry. This agrees with [6], which postulates that  $C_{OSS}$  losses scale with die area in GaN HEMTs. We also observe for the family of Cree/Wolfspeed devices, the losses

TABLE IV  
LIST OF DEVICES TESTED IN CURRENT RATING COMPARISON.

Part Number	Manufacturer	Packaging	Rated V	Rated I
IDM02G120C5	Infineon	D-Pak	1200 V	2 A
IDM05G120C5	Infineon	D-Pak	1200 V	5 A
IDM08G120C5	Infineon	D-Pak	1200 V	8 A
IDM10G120C5	Infineon	D-Pak	1200 V	10 A
C4D02120E	Cree/Wolfspeed	D-Pak	1200 V	2 A
C4D05120E	Cree/Wolfspeed	D-Pak	1200 V	5 A
C4D08120E	Cree/Wolfspeed	D-Pak	1200 V	8 A



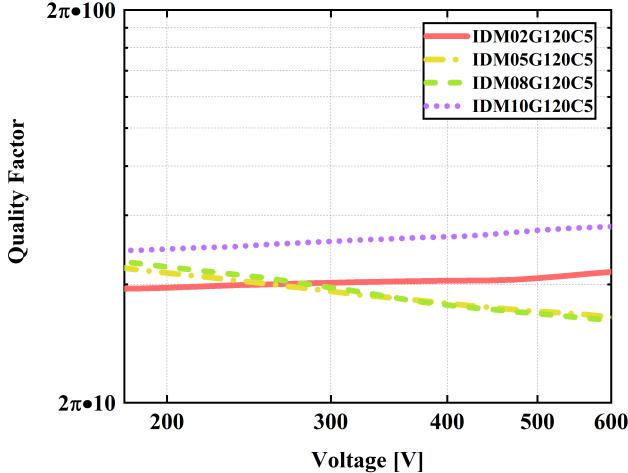
(a) Infineon Family



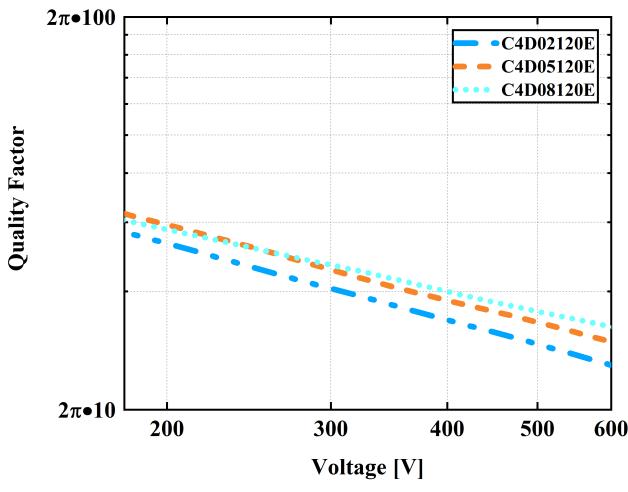
(b) Cree/Wolfspeed Family

Fig. 15. Comparison of from 200 to 550 V across 5, 10, 20 MHz for different current ratings of Infineon and Cree/Wolfspeed devices.

scale proportionally with the current rating, where the 5 A device exhibits approximately 2.5 times more loss than the 2 A rated device and the 8 A device exhibits 4 times the energy dissipation of the 2 A device. Additionally, the devices in the Cree/Wolfspeed family have the same Q factors. Although the Infineon family does show increasing losses with increasing current rating, it is interesting to note that there is not much significant difference in losses between the 5 A, 8 A, and 10 A devices, and the Q factors differ slightly among the four devices. This result indicates that active area of the device



(a) Infineon Family



(b) Cree/Wolfspeed Family

Fig. 16. Q factors of the Infineon and Cree/Wolfspeed families of devices tested in the current rating comparison.

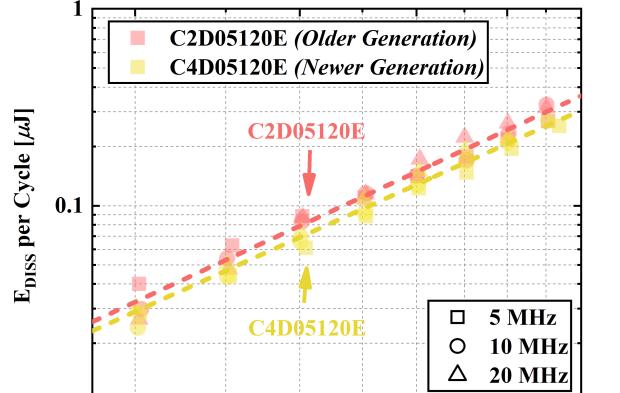
might not be the primary driver of  $C_J$  losses.

#### D. Device Technology/Generation Comparison

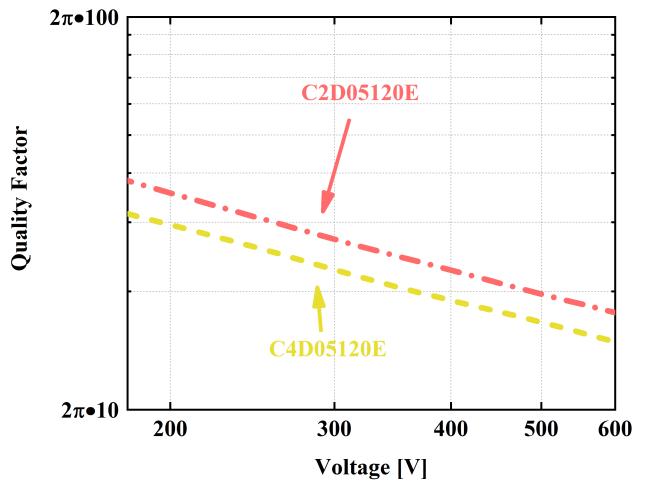
TABLE V  
LIST OF CREE/WOLFSPEED DEVICES TESTED IN GENERATION COMPARISON.

Part Number	Manufacturer	Packaging	Rated V	Rated I
C2D05120E	Cree/Wolfspeed	D-Pak	1200 V	5 A
C4D05120E	Cree/Wolfspeed	D-Pak	1200 V	5 A

We compare two 1200 V, 5 A rated Cree/Wolfspeed devices from different generations shown in Table V. Figure 17a indicates that the two devices have negligible differences in energy dissipation. However, the older generation C2D05120E device has a lower on-resistance, leading to smaller conduction losses. Furthermore, Figure 17b also highlights that both devices have very similar Q factors. The lower conduction losses and similar losses in  $C_J$  convince that the older C2D device is a more preferable device in HF rectifier applications.



(a) Energy Dissipation



(b) Q Factor

Fig. 17. Comparison of losses from 200 to 550 V across 5, 10, 20 MHz for two different generations of Cree/Wolfspeed devices and their corresponding Q factor.

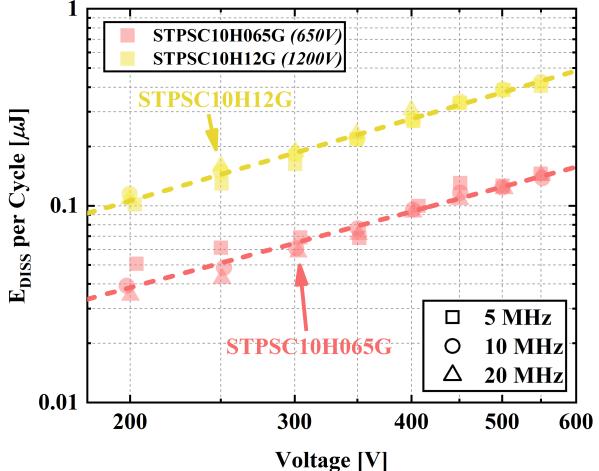
The observation of devices from different generations having similar losses substantiates that  $C_J$  losses are not eliminated as device technology advances.

#### E. Voltage Rating Comparison

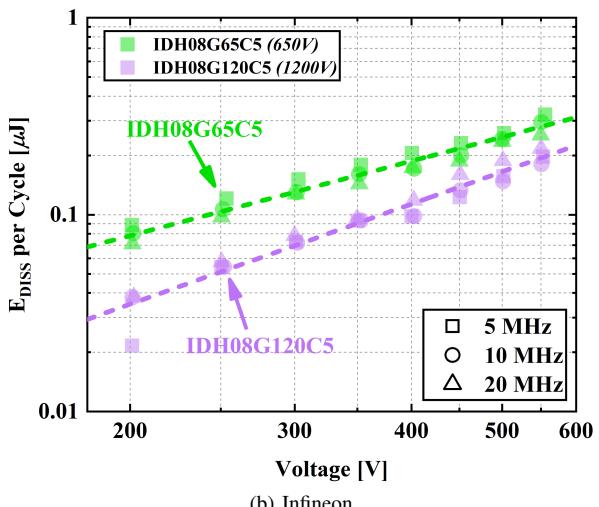
TABLE VI  
LIST OF DEVICES TESTED IN VOLTAGE RATING COMPARISON.

Part Number	Manufacturer	Packaging	Rated V	Rated I
IDH08G65C5	Infineon	D-Pak	650 V	8 A
IDH08G120C5	Infineon	D-Pak	1200 V	8 A
STPSC10H065G	STMicroelectronics	D-Pak	650 V	10 A
STPSC10H12G	STMicroelectronics	D-Pak	1200 V	10 A

To compare across voltage ratings, we tested a 650 V and 1200 V, 8 A device from Infineon in a TO-220 package and a 650 V and a 1200 V, 10 A STMicroelectronics device in a D<sup>2</sup>-Pak package listed in Table VI. The results in Figure 18a from the STMicroelectronics set shows that the 1200 V rated device dissipates more energy than the 650 V device while the



(a) STMicroelectronics



(b) Infineon

Fig. 18. Comparison of losses from 200 to 550 V across 5, 10, 20 MHz for different voltage ratings of Infineon and STMicroelectronics devices.

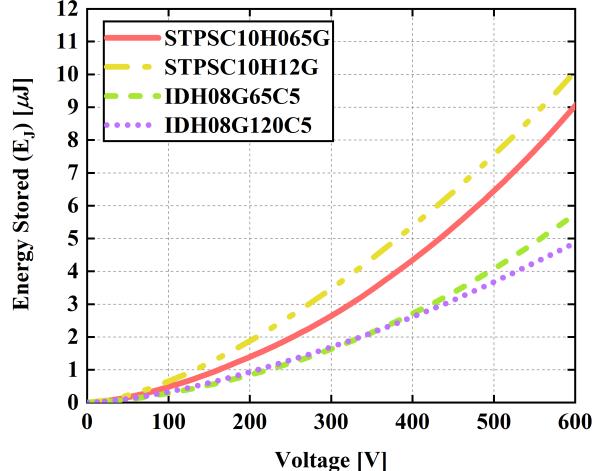
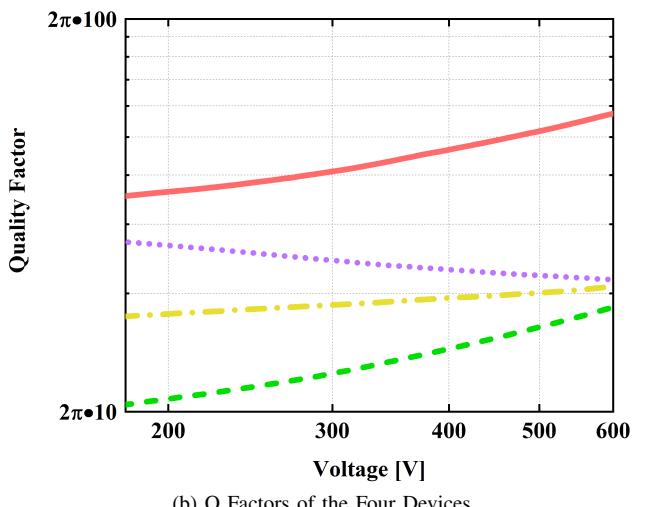
opposite is true for the Infineon set in Figure 18b. The fact that we observe the opposite effect occurring in the Infineon set of devices shows that the output capacitance losses could be a result of more than just simply die area scaling.

## V. HARDWARE VERIFICATION

To demonstrate the impact the off-state losses in a HF resonant converter, we designed and constructed a class-DE rectifier operating at 20 MHz with 400 V output voltage and 80 W output power.

### A. Design of Class-DE Rectifier

In the class-DE topology, as shown in Figure 20, both  $D_1$  and  $D_3$  experience the same voltage swing from 0 to  $V_{OUT}$ . We set the output voltage to 400 V because at this voltage, C3D04060E and STPSC406B experience largely different levels of off-state losses. Specifically, C3D04060E exhibits 5 to 6 times the amount of per cycle energy dissipation. Secondly, we incorporated an additional diode ( $D_2$ ) into our rectifier design, which does not conduct dc current due to the series capacitor

(a)  $E_J$  of the Four Devices

(b) Q Factors of the Four Devices

Fig. 19. Energy stored and Q factors of the devices tested in the voltage rating comparison.

$C_{REF}$ . Thus,  $D_2$  does not experience conduction loss but serves as a parallel external capacitor in conjunction to the  $C_J$  of  $D_1$ . We selected  $C_{REF}$  to be 800 pF, which is substantially larger than the  $C_J$  of  $D_2$  so that  $D_1$  and  $D_2$  experience the same amount of peak voltage swing. We set the dc blocking capacitor  $C_B$  to be 10 nF. The load resistor was selected as 2 kΩ in order to set the output power to 80 W. Lastly, we tuned the parallel input inductor  $L_R$  to 775 nH in order to achieve a resistive input impedance at the fundamental frequency, which resulted to a magnitude of 338 Ω. We verified our design on LTSpice, using the manufacturer-provided SPICE models for the three SiC Schottky diodes.

In order to achieve the proper output voltage and output power of 400 V and 80 W, we injected a 20 MHz input current with 700 mA amplitude. This is equivalent to setting the power amplifier to 285 V amplitude, which can be modeled as voltage source with a 50 Ω series resistor. We ensured that proper output voltage was maintained by measuring the output with a digital multimeter as well as measuring the voltage swings across  $D_1$  and  $D_3$ . Table VII lists the components and equipment used in the experiment, and Figure 21 displays a

photograph of the rectifier PCB and setup.

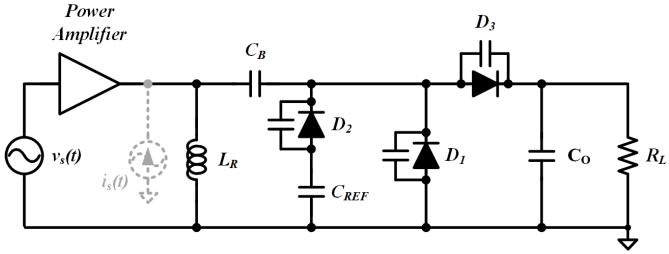


Fig. 20. Schematic of class-DE rectifier driven by a power amplifier serving as a sinusoidal current source.

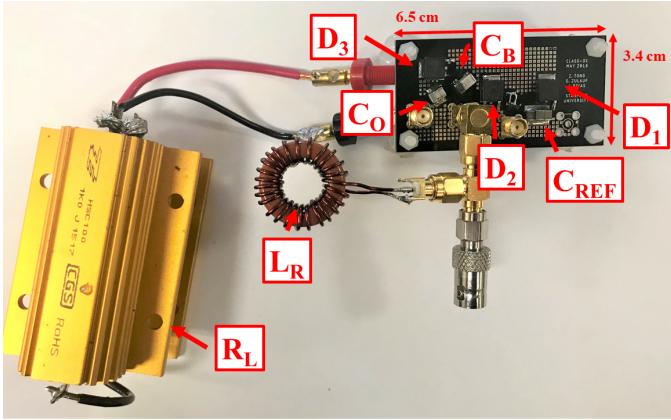


Fig. 21. Image of class-DE rectifier PCB.

TABLE VII  
LIST OF COMPONENTS USED IN THE CLASS-DE RECTIFIER.

Component	Part Number
Power Amplifier	ENI A1000 RF PA
Digital Multimeter	Agilent 34411A
$C_B$	10 nF, C0G/NP0 Dielectric
$C_{REF}$	800 pF, C0G/NP0 Dielectric
$C_O$	20 nF, C0G/NP0 Dielectric
$L_R$	775 nH, Air-Core/Plastic-Core
$D_1$	C3D04060E
$D_2$	C3D04060E
$D_3$	STPSC406B
$R_L$	2000 $\Omega$ ARCOL dc Loads

### B. Results from Class-DE Rectifier

Figure 22 shows the measured and simulated waveforms across  $D_1$  and  $D_3$ . The close overlap of the experimental results with simulation highlights proper design of the rectifier. However, the device power dissipation recorded in the experiment differs from the expected loss from simulation.

We obtained the device losses thermally by measuring the cross-coupled thermal impedances of  $D_1$ ,  $D_2$ , and  $D_3$  when each of the devices are injected with dc power. The temperature of the devices were measured using a FLIR A655SC

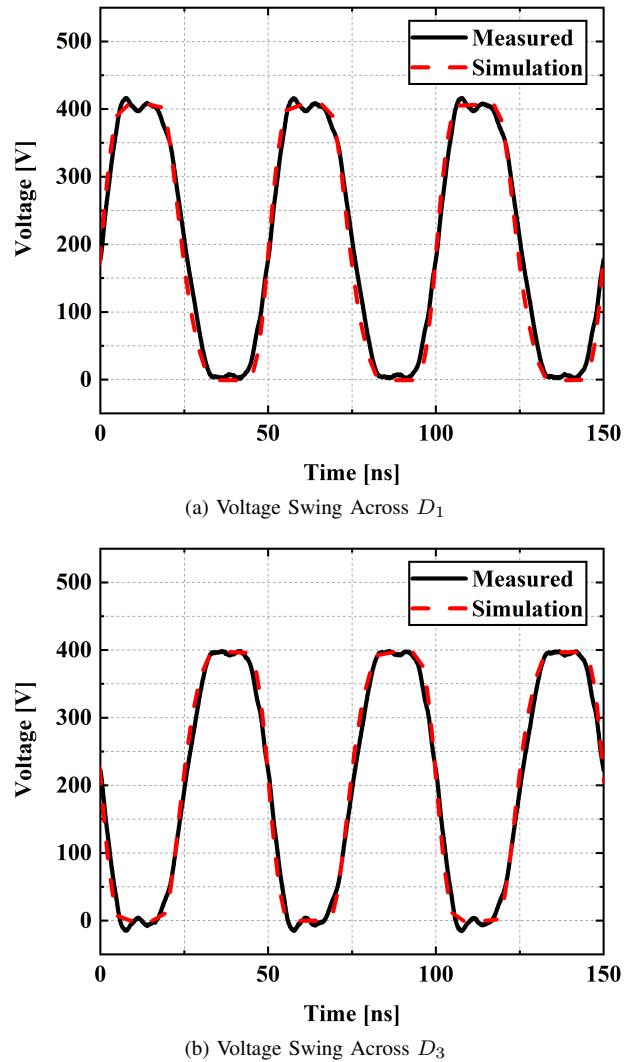


Fig. 22. Comparison of measured and simulated voltages across diodes  $D_1$  and  $D_3$

thermal camera with temperature color map shown in Figure 23a. The resulting thermal impedances are merged into a 3-by-3 matrix. From Equation 6, we obtain the resulting power dissipation of each device by multiplying the inverse matrix by the vector containing the temperature deltas of each device.

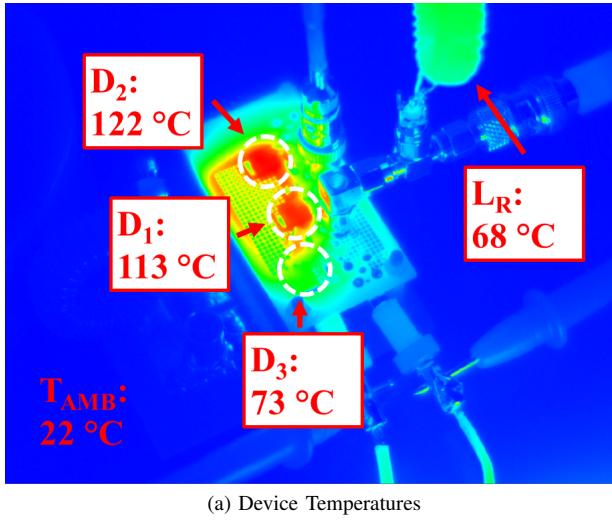
$$\begin{bmatrix} P_{D1} \\ P_{D2} \\ P_{D3} \end{bmatrix} = \begin{bmatrix} R_{Th11} & R_{Th12} & R_{Th13} \\ R_{Th21} & R_{Th22} & R_{Th23} \\ R_{Th31} & R_{Th32} & R_{Th33} \end{bmatrix}^{-1} \begin{bmatrix} T_{D1} - T_{Amb} \\ T_{D2} - T_{Amb} \\ T_{D3} - T_{Amb} \end{bmatrix} \quad (6)$$

Figure 23b records the losses of the three devices from simulation (conduction loss), Sawyer-Tower measurements ( $C_J$  loss), and thermal measurement. It is evident that the simulation, which only accounts for conduction loss (labeled in green in Figure 23b), severely underpredicts the power dissipation in the rectifier. When we account for the  $C_J$  losses, which we obtained from the fitted power equation from Section IV of C3D04060E and STPSC406B at 400 V using Equations 7 and 8 respectively (with units of  $\mu\text{J}$ ), the thermal measurement and the sum of conduction and  $C_J$  losses agree

better.

$$E_{DISS} = 2.73 \cdot 10^{-6} \cdot (V)^{1.74} \quad (7)$$

$$E_{DISS} = 2.47 \cdot 10^{-8} \cdot (V)^{2.25} \quad (8)$$



(a) Device Temperatures

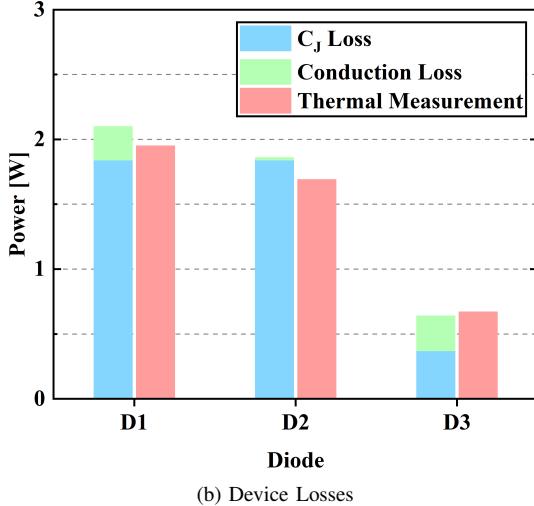


Fig. 23. FLIR thermal camera images of the rectifier setup as well as the loss breakdown from  $C_J$  (calculated from Sawyer-Tower measurement fitting), conduction (obtained from simulation), and thermal measurement (calculated using Equation 6).

In order to properly model efficiency and device power dissipation accurately in simulation, we push for manufacturers to incorporate these off-state losses into SPICE models. Furthermore, device power losses scale linearly with operating frequency, thus performance suffers more as frequency increases, so proper device selection must also consider off-state losses to achieve high efficiencies.

## VI. POWER DEVICE SELECTION FOR RESONANT RECTIFIERS

In general rectifier design, the circuit is constrained by output power ( $P_{OUT}$ ), output voltage ( $V_{OUT}$ ), switching frequency ( $f_{SW}$ ), and input impedance. In this section, we aim to provide a simple and approximate method when selecting

between different diodes to optimize converter efficiency. Because circuit designers have the freedom in selecting the converter topology, we cater an analytical approach to compare device losses in different rectifier architectures.

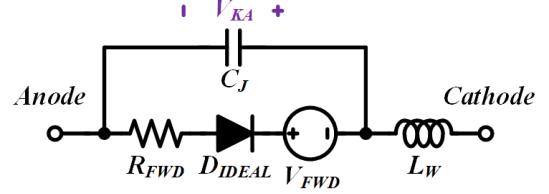


Fig. 24. Simplified model for Schottky diodes incorporating  $C_J$ , forward turn-on voltage  $V_{FWFD}$ ,  $R_{FWFD}$ , an ideal diode, and a parasitic package inductance  $L_W$ .

We propose Equation 9 to capture total power dissipation as the sum of conduction losses from  $R_{FWFD}$  and  $V_{FWFD}$  as well as the  $C_J$  loss, similarly in [5], which report losses for MOSFETs as the sum of gating, conduction, and  $C_{OSS}$  charge-discharge.

$$P_{LOSS} = R_{FWFD} \cdot I_{RMS}^2 + V_{FWFD} \cdot I_{AVG} + f_{SW} \cdot kV_{PK}^\beta \quad (9)$$

This is modeled in Figure 24, where the Schottky diode can be simplified as an ideal diode in series with a  $V_{FWFD}$  source and  $R_{FWFD}$  on-resistance, in parallel with the junction capacitance, and in series with package inductance  $L_W$ .

The selection between diode A and diode B for a given converter design aims to minimize  $P_{LOSS}$ . For this study, we focus on the class-DE and class-E rectifiers because they are two common resonant topologies suitable for HF/VHF design, and can be extended to other resonant topologies using similar analytical methods. Starting with the class-DE as depicted and labeled in Figure 25, we display in Figure 26 the current  $I_2$ , voltage  $V_2$ , and the conduction times for diodes  $D_1$  and  $D_2$ , similarly derived in [11]. The average currents through the

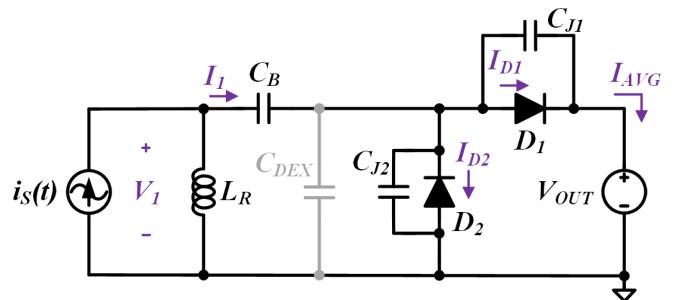


Fig. 25. Schematic of class-DE rectifier driven by current source.

diodes are equivalent to  $\frac{P_{OUT}}{V_{OUT}}$ . Thus, we follow Equations 10, 11, and 12 to obtain the diode's root mean square (RMS) current as a function of the output power, output voltage, and conduction starting phase ( $\phi$ ).

$$I_{AVG} = \int_{\phi}^{\pi} I_{PK} \sin(\theta) d\theta = I_{PK} \frac{\cos(\phi) + 1}{\pi} = \frac{P_{OUT}}{V_{OUT}} \quad (10)$$

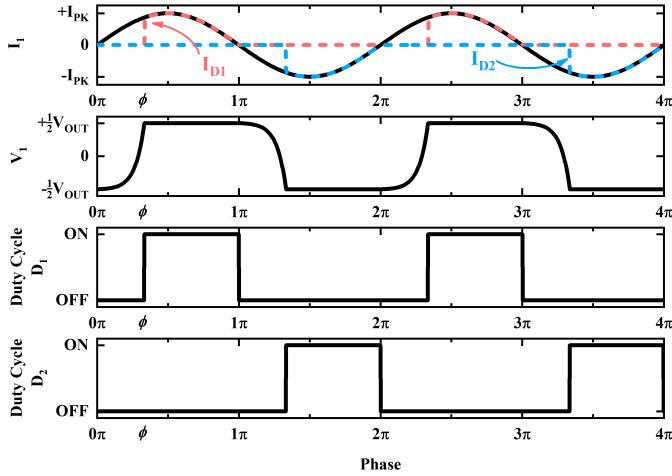


Fig. 26. Standard input voltage and current waveforms of a class-DE rectifier and the conduction times of  $D_1$  and  $D_2$  for 2 periods.

$$I_{RMS} = \sqrt{\frac{1}{\pi} \int_{\phi}^{\pi} I_{PK}^2 \sin^2(\theta) d\theta} = \alpha \frac{P_{OUT}}{V_{OUT}} \quad (11)$$

$$\alpha = \sqrt{\frac{\pi}{2} \left( \frac{-\phi + \sin(\phi)\cos(\phi) + \pi}{(\cos(\phi) + 1)^2} \right)} \quad (12)$$

Thus, for a class-DE rectifier, the total semiconductor losses can be extracted by Equation 13, where the factor of 2 results from two diodes required in the topology.

$$P_{LOSS} = 2 \left[ R_{FWD} \cdot \alpha^2 \left( \frac{P_{OUT}}{V_{OUT}} \right)^2 + V_{FWD} \cdot \left( \frac{P_{OUT}}{V_{OUT}} \right) + f_{SW} \cdot kV_{OUT}^\beta \right] \quad (13)$$

From Equation 13, we obtain a loss equation that only depends on 4 factors: output power, output voltage, switching frequency, and  $\phi$ .

#### A. Diode Selection Example

As a device selection example, we can use the previously defined  $P_{LOSS}$  metric to compare the performance of two 4 A, 600 V rated devices (C3D04060E and STPSC406). Ignoring temperature dependencies, we extracted the  $R_{FWD}$  and  $V_{FWD}$  from the devices' datasheets, documented in Table III in Section IV. Also, the output capacitance losses are based on the Sawyer-Tower measurement fittings. Additionally we assume that the diodes conduct with 50% duty cycle, which means  $\phi$  is equivalent to  $\frac{\pi}{2}$ . Figures 27a and 27b show the power dissipation heat maps for a 20 MHz class-DE rectifier implementing C3D04060E and STPSC406B swept from 10 to 250 W output powers and 100 to 600 V output voltages. We observe from these figures that both devices have very different power loss signatures because the devices have different conduction properties, where STPSC406B's  $R_{FWD}$  is over 3 times higher than C3D04060E's  $R_{FWD}$ , but has 6 times lower  $C_J$  loss. Furthermore, we see in Figure 28 that there are specific ranges of output voltages and output powers for a class-DE where implementing the converter with two STPSC406B offers higher rectifier efficiency than with two C3D04060E and vice versa. This result agrees with basic circuit intuition since we expect the lower conduction loss,

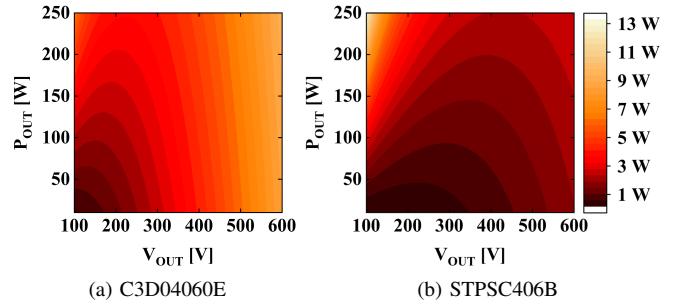


Fig. 27. Total device power loss heat map for a 20 MHz class-DE rectifier swept from 10 to 250 W output powers and 100 to 600 V output voltages using C3D04060E and STPSC406B implemented for both diodes.

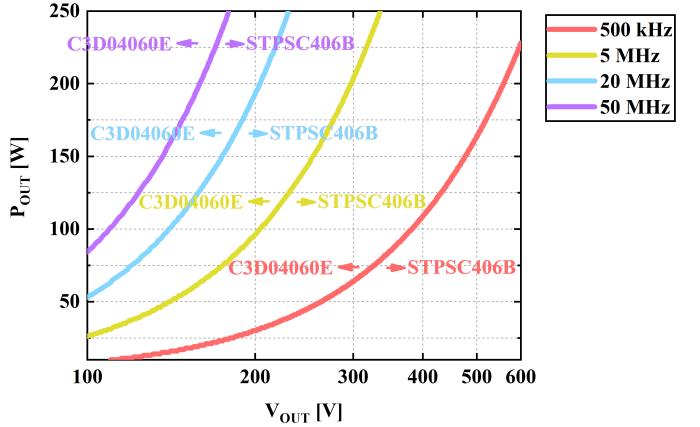


Fig. 28. At 500 kHz, 5 MHz, 20 MHz, and 50 MHz, we trace the point where the device power dissipation for a C3D04060E implemented class-DE rectifier and a STPSC406B implemented class-DE rectifier are equivalent. Left of the line is region of output powers and output voltages where C3D04060E exhibits less losses and is preferred. Right of the line is where STPSC406B is preferred.

higher  $C_J$  loss C3D04060E device to perform best at high power, low voltage applications where circulating current is large and voltage stress is small. In the high voltage, low power ranges, STPSC406B becomes the preferable device due to the smaller capacitance loss effect.

#### B. Converter Topology Comparison: Class-DE vs Class-E

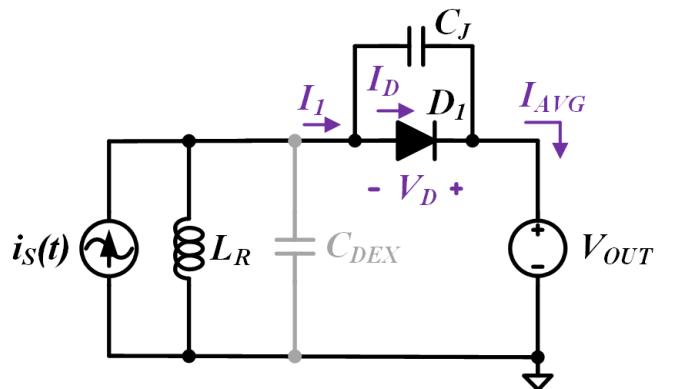


Fig. 29. Schematic of class-E rectifier driven by current source.

By the same method of analysis that we used to derive Equation 13, we extrapolate the loss metric for the switch in a class-E rectifier using Equation 14.

$$P_{LOSS} = R_{FWD} \cdot \alpha^2 \left( \frac{P_{OUT}}{V_{OUT}} \right)^2 + V_{FWD} \cdot \left( \frac{P_{OUT}}{V_{OUT}} \right) + f_{SW} \cdot k (4V_{OUT})^\beta \quad (14)$$

Figure 30 displays a sample diode voltage and current

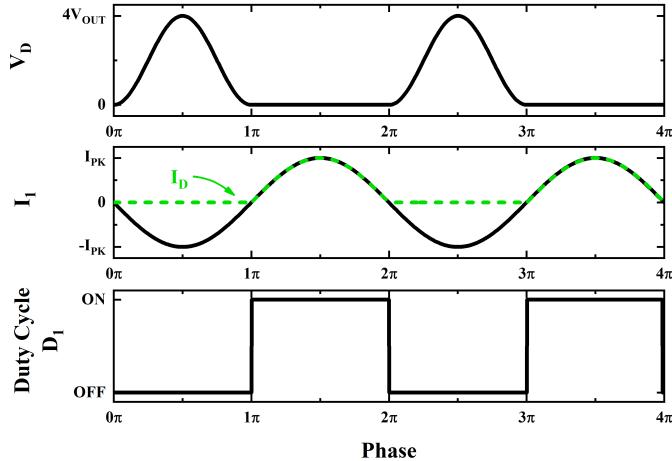


Fig. 30. Standard device voltage swing,  $I_1$ , and device conduction period in a class-E rectifier for 2 periods.

waveforms for two cycles in the class-E converter, shown in Figure 29. In comparison to the class-DE, the class-E exhibits half of the conduction loss seen in a class-DE with the same output voltage and power. However, the output capacitance loss in the class-E is scaled by  $2^{2\beta-1}$  compared to the class-DE because the voltage stress is four times the output voltage. By comparing the loss equation for a class-DE and a class-E

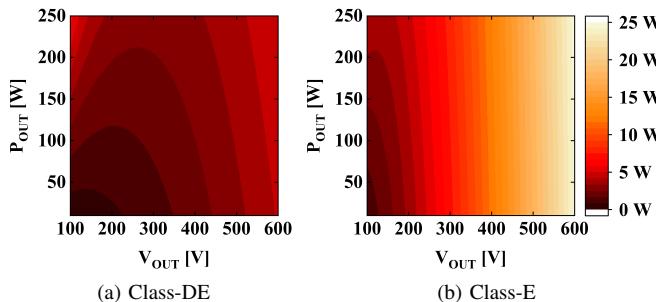


Fig. 31. Total device power loss heat map for a 10 MHz class-DE and class-E rectifier swept from 10 to 250 W output powers and 100 to 600 V output voltages.

topology, we note that, similar to tradeoffs between utilizing different devices, there are also tradeoffs in selecting between different converter topologies. Figures 31a and 31b display the device power loss mapping using C3D04060E across 10 to 250 V output powers and 100 to 600 V output voltages at 10 MHz. Additionally, Figure 32 shows the regions of output voltages and powers where implementing a class-E rectifier offers lower device losses than a class-DE rectifier and vice versa at various switching frequencies. Generally, the selection of rectifier topology is based upon the target input impedance, which depends upon design goals and application. However,

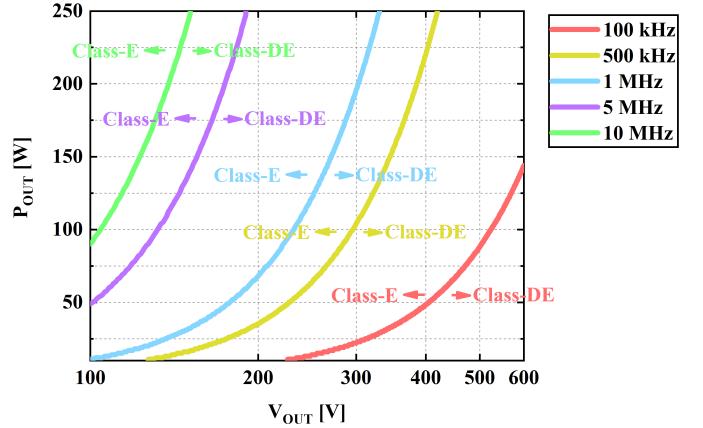


Fig. 32. At 100 kHz, 500 kHz, 1 MHz, 5 MHz, and 10 MHz, we trace the point where the device power dissipation for a class-E and a class-DE rectifier using C3D04060E as the diodes are equivalent. Left of the line is region of output powers and output voltages where the class-E exhibits less losses and is preferred. Right of the line is where the class-DE topology is preferred.

we suggest that the choice among rectifier topologies can impact system performance by the various loss mechanisms occurring, and this can be an additional consideration to include in the design process.

## VII. CONCLUSION

The significant off-state losses from the charging and discharging of  $C_J$  in SiC Schottky diodes are seen in converters from previous literature [17]–[19] but have not been experimentally measured and characterized. Therefore, we compare the losses among several different commercially-available SiC Schottky diodes across manufacturer, current rating, generation, voltage rating, and packaging to provide HF/VHF power circuit designers insight in selecting devices to minimize losses and provide manufacturers information on theories on possible mechanisms behind these losses. To stress the significance of these losses, we furthermore provide a demonstration using a class-DE rectifier to highlight their magnitude and especially how they increase with switching frequency. Finally, we propose device and rectifier topology selection considerations to minimize device power dissipation at various output voltages, powers, and switching frequencies.

## ACKNOWLEDGMENT

This work was supported by the National Science Foundation, the Stanford Graduate Fellowship program, and Stanford's SystemX Alliance.

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