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C_{OSS} Measurements for Superjunction MOSFETs: Limitations and Opportunities

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***Abstract*— Small-signal measurements of output capacitance (C_{OSS}) are ubiquitous in power semiconductor datasheets and determine critical features of power converters. For silicon superjunction power MOSFETs (SJs), we report C_{OSS} measurements with two key anomalies: variation with ac perturbation frequency and hysteresis with dc sweep direction. Using mixed-mode simulations, we attribute the frequency shift to the fundamental SJ structure and find that dc hysteresis is caused by charge trapping from uneven depletion fronts. We show that C_{OSS} measurements on SJs do not accurately characterize large-signal operation, underestimating stored energy by up to four times and giving no indication of C_{OSS} losses.**

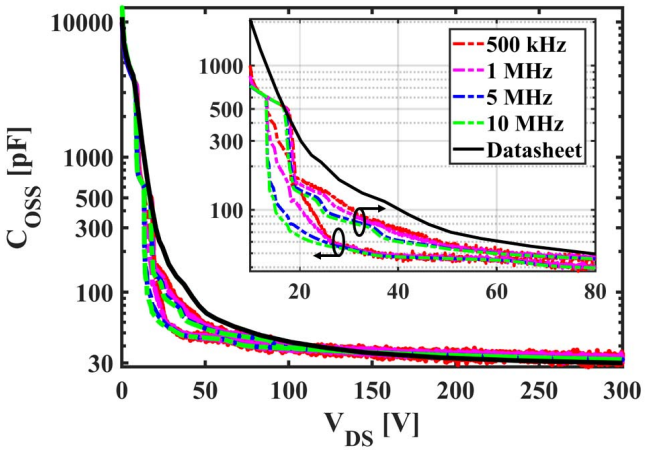
***Index Terms*— Capacitance-voltage characteristics, output capacitance (C_{OSS}), power MOSFETs, superjunction.**

I. Introduction

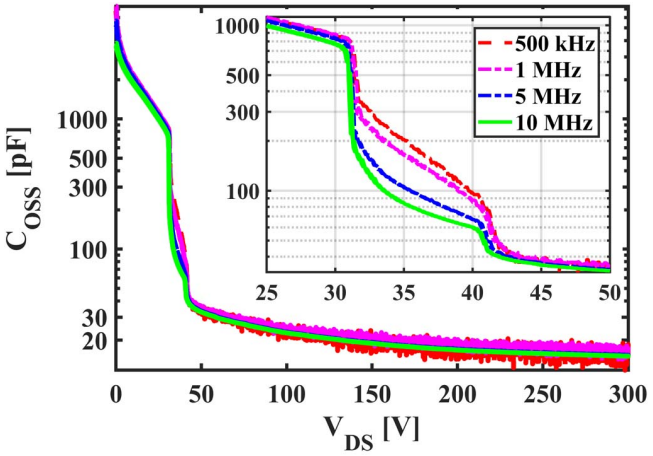
THE output capacitance of power semiconductors, C_O, directly defines a multitude of power converter parameters. In hard-switched converters, C_O is charged during the device's offtime and discharged through the channel at turn-ON. In zero-voltage-switched converters, the discharge of C_O occurs resonantly during the offtime, ideally incurring zero switching losses. In all power converters, the energy stored in C_O (E_O) determines component selection, thermal design, and efficiency, making the measurement and reporting of device output capacitance critical to design and performance.

C_O is reported in datasheets using small-signal measurements, labeled C_{OSS}, where a small ac perturbation is applied to a quasi-steady-state dc drain–source voltage (V_{DS}). A digitized datasheet C_{OSS} curve is shown as the black line in Fig. 1(a), and C_{OSS} is integrated across V_{DS} to compute E_O or E_{OSS} (Fig. 2, dashed line). These curves are ubiquitous, widely accepted, and well understood in the power electronics and power device communities.

Silicon superjunction power MOSFETs (SJs), with a drift region composed of alternating n and p columns [1], break the unipolar material limit of specific ON-resistance ($sR_{DS,ON}$)



(a)



(b)

Fig. 1. Measured C_{OSS}, with 100-mV$_{PP}$ ac magnitude and V_{DS} swept 0.1 V every 250 ms from 0 to 300 to 0 V$_{dc}$. (a) SJ A. Positive- and negative-going dc curves highlighted. (b) SJ B. Positive- and negative-going dc curves plotted. Device characteristics given in Table I.

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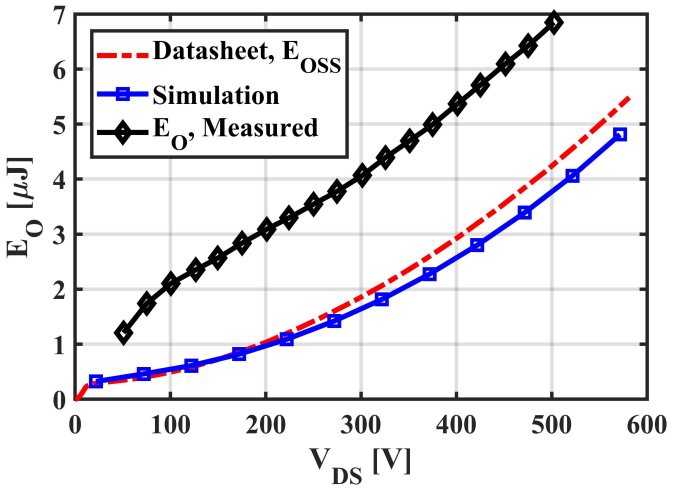

Fig. 2. Reported and measured E_O and E_{OSS} for SJ A. E_O measured using the Sawyer–Tower circuit at 300 kHz.

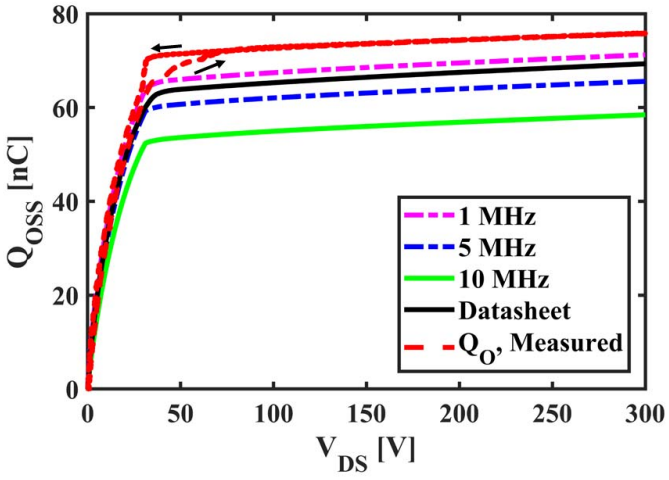

Fig. 3. Reported and measured Q_O and Q_{OSS} for SJ B. Q_O measured using the Sawyer–Tower circuit at 300 kHz.

for a given breakdown voltage and are widely used in commercial hard- and soft-switched converters. Generational progressions of SJs typically aim to lower $sR_{DS,ON}$ through smaller cell pitch, higher doping, or more precise charge balance [2]–[4]. Countering this progression, however, recent works [5]–[8] have reported large unexpected losses in SJs used in soft-switching applications from charging and discharging the output capacitor ("C_{OSS} losses"), with higher losses attributed to uneven column walls and decreasing cell pitch [9].

In this paper, we show that C_{OSS} measurements vary significantly with dc bias ramp direction and ac perturbation frequency and do not accurately describe SJ operation in power converters, mischaracterizing large-signal energy storage (E_O) and charge (Q_O) (Section II). In Section III, we introduce a mixed-mode simulation method to investigate the dc hysteresis (Section IV) and frequency shift (Section V) anomalies in SJ C_{OSS} measurements. In Section VI, we investigate whether these anomalies map to large-signal conditions and, finding that the extrapolation is fraught, propose an additional graph for inclusion in power SJ datasheets in Section VII.

II. Small- and Large-Signal Anomalies

Small-signal measurements inject an ac perturbation on top of a dc bias, measure the phase and magnitude of the response, and compute the capacitance as $-1/\omega/\mathrm{Im}\{Z\}$. Under the quasi-static approximation, which assumes that carriers respond to ac signals as if they were a varying dc bias [10], the small-signal C_{OSS} can be integrated to find large-signal capacitance [11], [12] and the E_{OSS} curves in datasheets and simulation models (Fig. 2).

By contrast, large-signal measurements apply a large ac signal, characterizing C_O at a particular dc offset, ac magnitude, and ac frequency. One method to measure large-signal capacitance (for others, see [13]–[15]) is the Sawyer–Tower circuit [6], [16], which applies a sinusoidal voltage across C_O between 0 V_{DS} and V_{PP} with the device held OFF. In converters, *only* large signals are applied to the output capacitance of power semiconductors, while small-signal measurements measure linear mode performance [6] and do not replicate the waveforms in any power converter.

TABLE I
Commercially Available Tested SJs. MEMI: Multi-Epitaxy Multi-Implant. TFEG: Trench-Filled Epitaxial Growth

Device	Construction	V_{DS}	$R_{DS,ON}$ (25 °C)
SJ A	MEMI	550 V	205 mΩ
SJ B	TFEG	600 V	430 mΩ
SJ C	MEMI	600 V	255 mΩ
SJ D	MEMI, low Q_{RR}	600 V	260 mΩ

For modern SJs, the quasi-static approximation that underpins the extrapolation from small-signal (C_{OSS}, Q_{OSS}, and E_{OSS}) to large-signal characteristics (C_O, Q_O, and E_O) does not hold. Fig. 2 shows that the integration of C_{OSS} significantly under-predicts the measured large-signal stored energy (E_O). With hard-switching losses proportional to $E_O \times f_{SW}$, this underestimation would result in much higher-than-expected losses in the SJ. Stored charge, Q_O, defines the inductor parameters for soft-switching [17], and Q_O is also underestimated by Q_{OSS}, appears dependent on the ac perturbation frequency, and exhibits hysteretic behavior (Fig. 3).

In summary, the ubiquitous C_{OSS} measurements may: 1) under-predict E_O by over 100%; 2) under-predict Q_O; 3) give no prediction of C_{OSS} losses; and 4) vary with ac frequency and the direction of the applied dc bias. Taken together, these necessitate further investigation of the widely used C_{OSS} measurements, and we examine the two anomalies highlighted in Fig. 1. In Fig. 1(a), C_{OSS} of SJ A is significantly lower in the negative-going V_{DS} bias sweep direction than in the positive-going one ("dc hysteresis"). For both devices in Fig. 1, C_{OSS} depends on the ac perturbation frequency at certain bias voltages ("frequency shift").

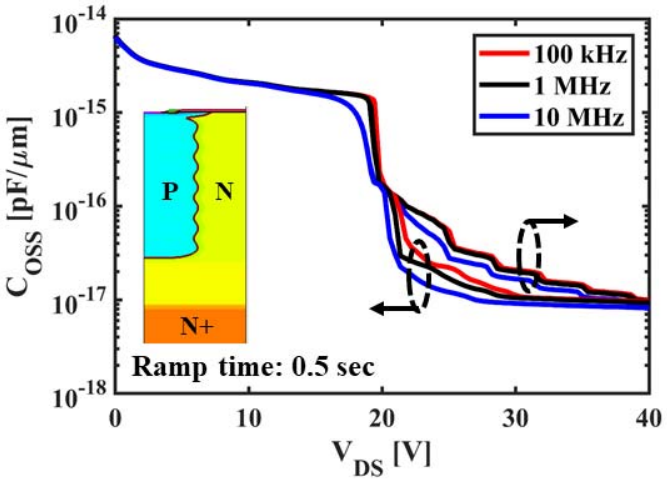

Fig. 4. Simulated C_{OSS} for the MEMI structure from [9]. Both anomalies measured in SJ A are observed here.

III. Simulation Methodology

Mixed-mode simulations are run using a commercial TCAD tool [18] and SPICE circuit to ramp V_{DS} across the TCAD structures with a variable slew rate. The linear algebraic solution at different times provides a real and imaginary response to the small-signal ac perturbation at the structure's contacts [19], from which we compute C_{OSS}. Our base structure for simulation is the half-cell, multi-epitaxy multi-implant (MEMI) SJ-FET structure shown in Fig. 4 (structure details are described in [9]). The physical models are based on drift-diffusion transport, including the Shockley–Read–Hall recombination model with the Scharfetter lifetime doping dependence. For the half-cell configuration, we use the reflecting Neumann boundary condition on the lateral boundaries.

We simulate the structure at varying ac frequencies and dc bias values, and Fig. 4 shows that the two key anomalies observed in Fig. 1 are qualitatively reproduced in this mixed-mode simulation environment. We use this core structure to more deeply investigate the root causes.

IV. DC Hysteresis

To our knowledge, C_{OSS} hysteresis with dc bias has not been previously published in the literature and is an unexpected phenomenon at the time scales considered here. The dc hysteresis anomaly is recreated in the simulated structure of Fig. 4, and we observe that, for both the simulated and measured devices, this hysteretic behavior only occurs during pinchoff of the SJ columns. Fig. 5 shows the structure across varying dc bias for both sweep directions. At 25 V_{DS}, where large hysteresis is evident in the simulated C_{OSS}, the charge structure in the columns is quite different between the ramp-up and ramp-down conditions. During depletion (ramp-up), large hole pockets form in the center of the p-pillar, but there are no charge pockets of electrons in the n-column. In undepletion (ramp-down), however, we observe smaller hole pockets that are spatially alternated with electron pockets that were not observed during depletion.

The ramp-down structures, then, could be said to show a nonequilibrium condition, and the state eventually settles to the positive-going one if V_{DS} is held constant for a long time. The trapped majority carriers must either recombine with minority carriers, which are sparse in that side of the column, or reach the contacts, which are accessible only through a narrow and high resistance or a completely depleted region. These slow processes result in measured time constants in commercial SJs that are unexpectedly large. For example, Fig. 6(a) shows the measured time for the negative-going C_{OSS} (stepped from 525 V_{DS}) to settle to the positive-going capacitance ($C_{OSS,+}$) at that particular dc bias voltage, with time constants of up to hours for the recombination of the trapped majority carriers.

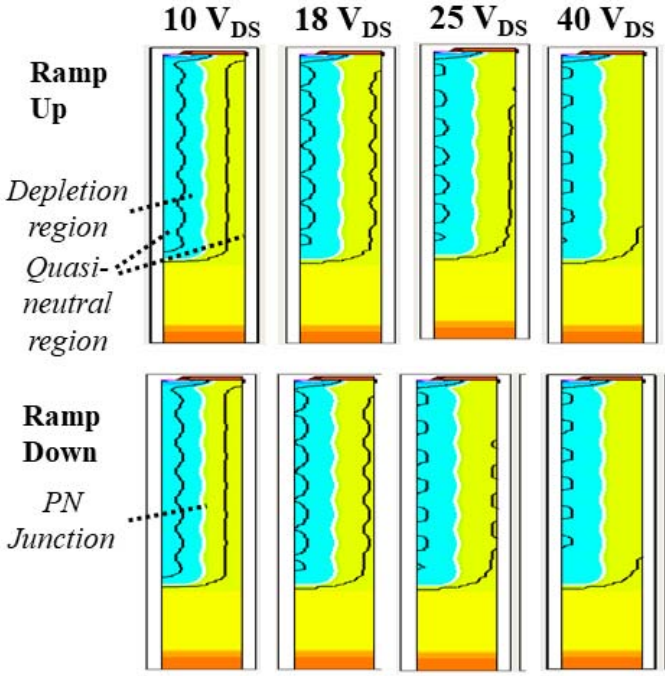

Fig. 5. Simulated depletion region (at 10 MHz) across V_{DS} with positive- and negative-going dc bias at 0.5s-ramp rate.

Carrier lifetime has a significant impact on the level of hysteresis, or equivalently, on the settling time of the trapped charges. In the simulated structure, reducing the carrier lifetime an order of magnitude ($\tau_e = 3\tau_h$ for both cases) reduces the settling time by four times. We confirm this simulation result in commercial devices by comparing two SJs, SJ C and SJ D, that are identical except that SJ D is optimized for low reverse-recovery charge (Q_{RR}), which we assume implies that SJ D has additional recombination centers to reduce carrier lifetime over SJ C. As expected, SJ C has settling times over 100× longer than SJ D in the pinchoff region [Fig. 6(b)], verifying the simulated finding.

The root cause of the observed dc hysteresis anomaly is charge trapped by the asymmetrical depletion and undepletion of the SJ columns, and the phenomenon only appears to be measurable in MEMI structures. This C_{OSS} measurement technique provides an estimate of majority carrier lifetimes with different depletion fronts and may be useful to ascertain relative levels of charge trapping between devices.

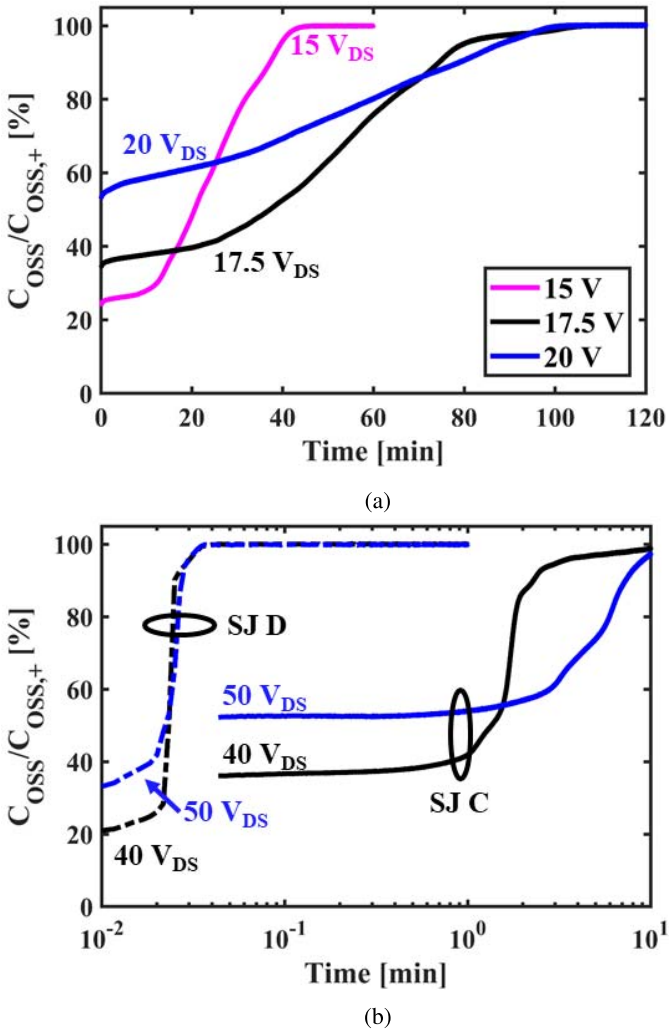

Fig. 6. Measured time for C_{OSS} to converge to the positive-going value ($C_{OSS,+}$) when bias is stepped from 525 V_{DS} to the legend value. (a) SJ A, 5-MHz ac perturbation. (b) SJ C and SJ D, 5-MHz ac perturbation.

V. Frequency Shift

In all measured SJs, we observe a frequency shift in C_{OSS}, where the measured capacitance in the pinchoff region significantly declines with increasing frequency at a given V_{DS}. The tested frequencies are common for C_{OSS} curves published in datasheets, and as C_{OSS} is used to determine the crucial figure-of-merit E_{OSS}, its accuracy is important for power devices. Furthermore, measurements by the authors on planar Si MOSFETs and wide bandgap devices (GaN-on-Si HEMTs and SiC MOSFETs) do not exhibit this C_{OSS} frequency shift.

Examining the curves in Fig. 4 with the depletion fronts in Fig. 5, we observe that the frequency shift only occurs at voltages where the p- and n-pillars are on the verge of full depletion. The depletion regions, of course, do not change with ac frequency, but the transient solution results in different C_{OSS} values across frequency, so we expect the small-signal perturbation to be responsible for the shift. Additional simulations with carrier lifetimes ranging from 10 ns to 10 μs also do not significantly impact this shift.

To explain this anomaly, a conventional p-n cell and an SJ cell in the pinchoff region are compared in Fig. 7. In the

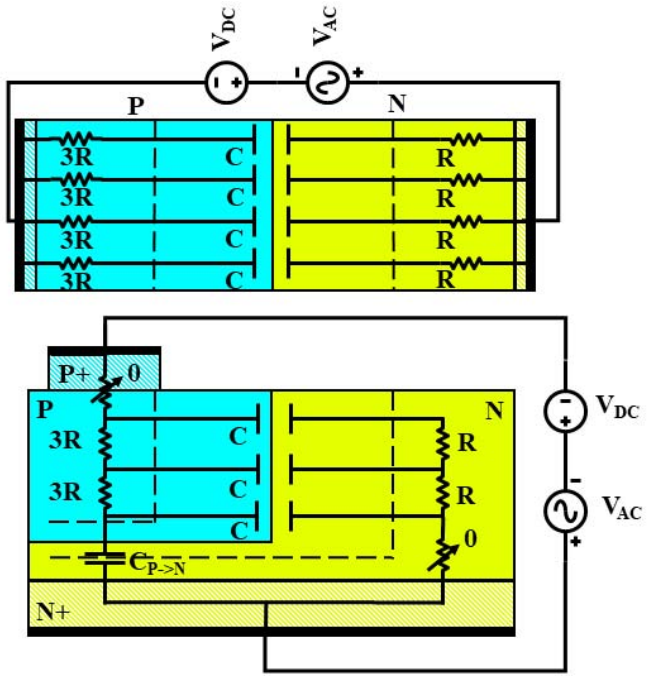

Fig. 7. Proposed *RC* circuit for a conventional p-n junction (top) and for an SJ device before full depletion (bottom).

SJ cell, the depletion region spreads laterally across the cell with the contacts to the drain and source located on the top and bottom of the cell structure. We consider each structure as a distributed *RC* network, where the capacitance per unit length (C) across the depletion region is in series with resistors (R) in either column (we assume equal doping such that $3\mu_p = \mu_n$, and to ignore the resistance in the N+ and P+ regions). In real cells of this type, this distributed network comprises a very large number of *RC cells*; here, we consider a small number to illustrate the behavior that leads to the C_{OSS} frequency shift that is unique to SJs.

The input impedance (Z_{IN}) for each equivalent circuit is plotted in Fig. 8 for equivalent values of C and R, and the capacitance is calculated as $-1/\omega/\mathrm{Im}\{Z\}$. The p-n structure network, which is a parallel combination of series R–C cells, produces a constant $\omega \cdot \mathrm{Im}\{Z\}$ term, resulting in a measured capacitance of 4C that is independent of frequency. The $\omega \cdot \mathrm{Im}\{Z\}$ term for the SJ structure, on the other hand, starts to increase with frequency one decade below the *RC* time constant of the network, resulting in a decrease of measured capacitance with increasing perturbation frequencies. Reasonable values of capacitance and resistance give *RC* time constants on the order of MHz, affecting standard measurement frequencies. We have used equal R values to highlight qualitative behaviors, but in SJ devices, the resistance will increase significantly with increasing dc bias as the current path width shrinks.

These simple circuits indicate that frequency shift is fundamental to the SJ structure, explaining why this anomaly is present in all measured SJs but not in other power devices. The narrow conduction paths of an SJ in pinchoff result in high unit length resistances, pushing the time constant into the range of standard C_{OSS} measurement frequencies. The frequency shift

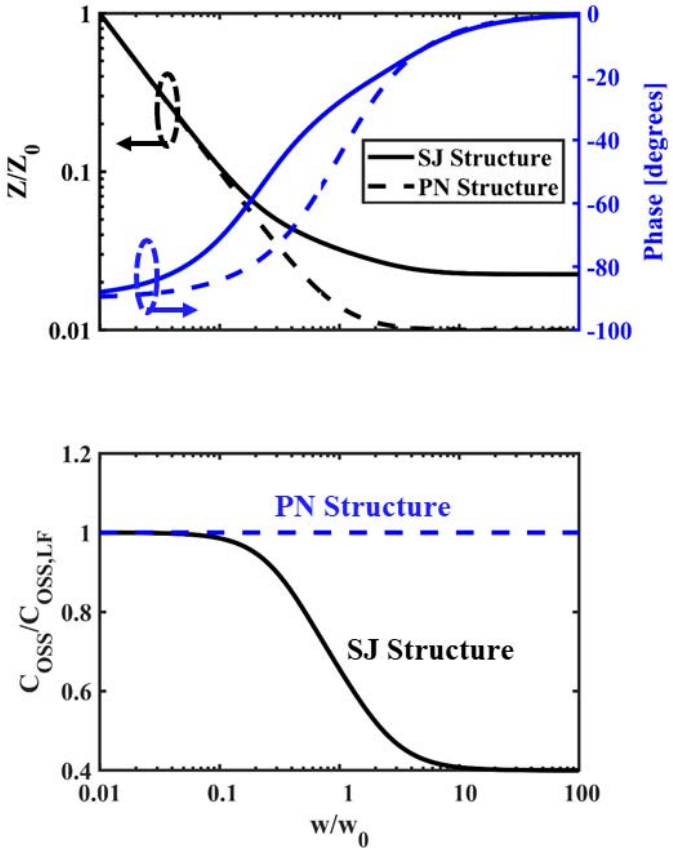

Fig. 8. Input impedance response for the equivalent circuits for the p-n structure and SJ structure in Fig. 7, normalized to the *RC* time constant of the p-n structure, $1/(2\pi 4RC)$. For this simulation, $R = 100\ \Omega$ and $C = 50$ pF, with $w_0 = 7.95$ MHz.

can be mitigated with cell structures that reduce this resistance [e.g., trench-filled epitaxial growth (TFEG) structure with a high trench slope] to push the *RC* time constant past standard measurement frequencies.

VI. Predicting Large-Signal Behavior

For the tested SJs, we attempt to use these anomalies to predict two large-signal characteristics: large-signal energy storage, E_O, and soft-switching loss from charging and discharging the output capacitor, C_{OSS} losses. These characteristics are measured with the Sawyer–Tower circuit [Fig. 9(a)], which applies a sine wave between 0 V_{DS} and V_{PP} across an SJ held in the OFF-state (see [6], [16] for circuit details).

As expected, SJ A, which exhibits both C_{OSS} anomalies, has the highest C_{OSS} losses and the largest ratio of large-signal E_O to E_{OSS}, and SJ B, a TFEG device with no hysteresis, has the smallest C_{OSS} losses and energy storage well predicted by E_{OSS}. The primary surprise is that the lifetime reduction between SJ C and SJ D has no effect on large-signal characteristics; we suspect this is due to the difference in ramp rate. In the small-signal measurement, the dc slew rate is 0.1 V_{dc} per 250 ms; at 300 kHz, the Sawyer–Tower test slews up to 550 V in 1.67 μs. This nine order of magnitude difference in slew rate could reintroduce hysteretic charge trapping despite the reduction in lifetime, and for the

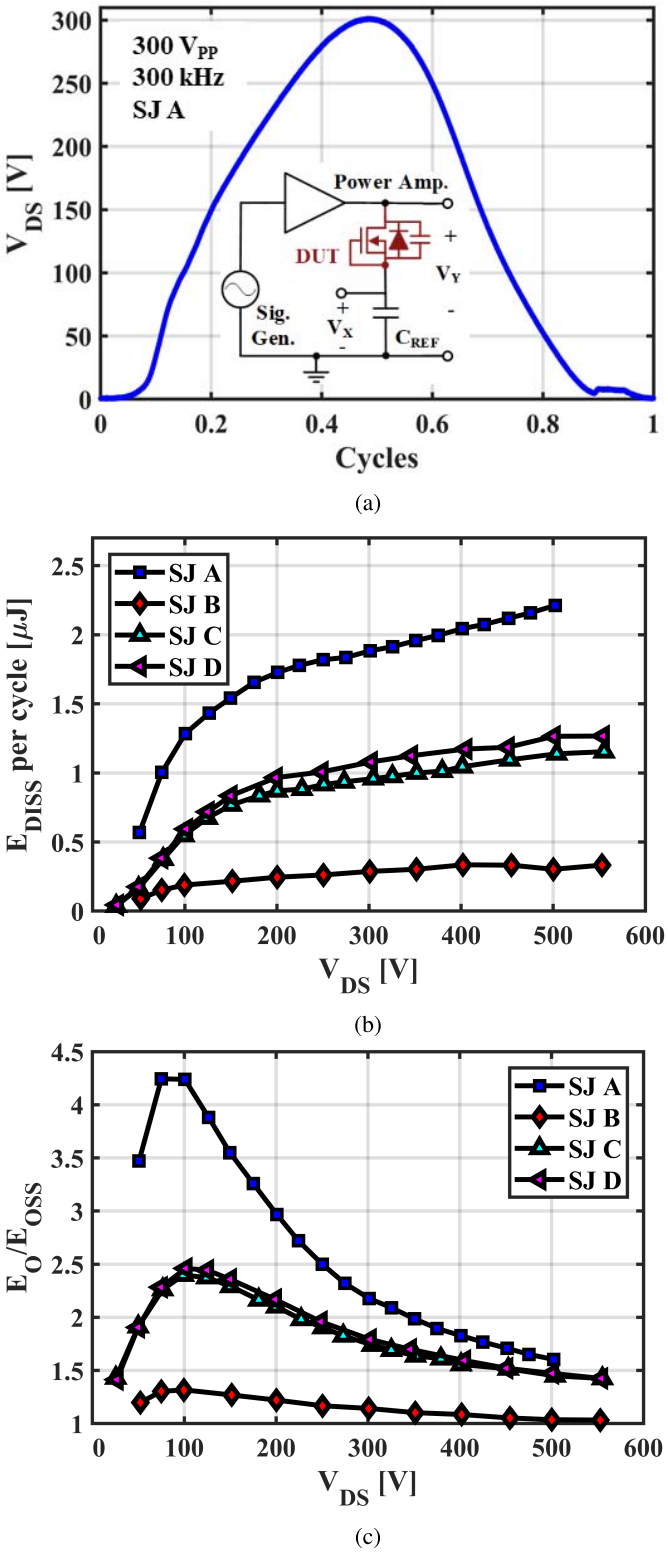

Fig. 9. Large-signal characteristics for the SJs in this paper, characterized at 300 kHz using the Sawyer–Tower circuit. (a) Sawyer–Tower circuit and representative V_{DS} waveform. (b) Measured C_{OSS} losses. (c) Ratio of measured E_O to small-signal datasheet E_{OSS}.

simulated structure of Fig. 4, we increase the dc ramp rate from 0.5 s to 1.6 μs to mimic the large-signal perturbation. Fig. 10 shows that the hysteresis between the two curves increases markedly, with different positive- and negative-going

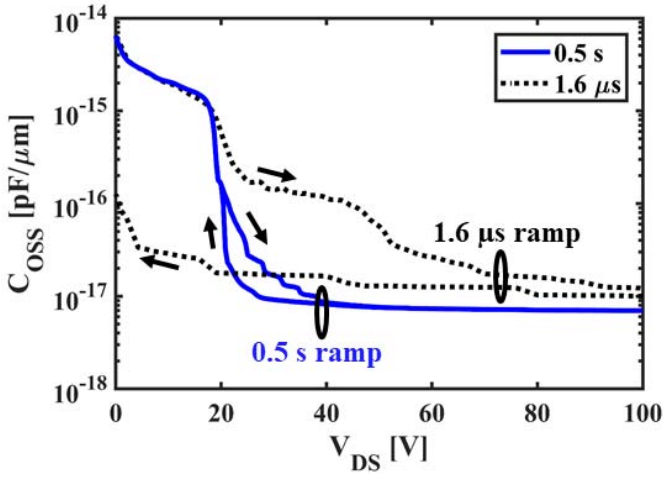

Fig. 10. Simulated C_{OSS} (10-MHz ac perturbation) with a six-order-of-magnitude difference in dc bias ramp rate.

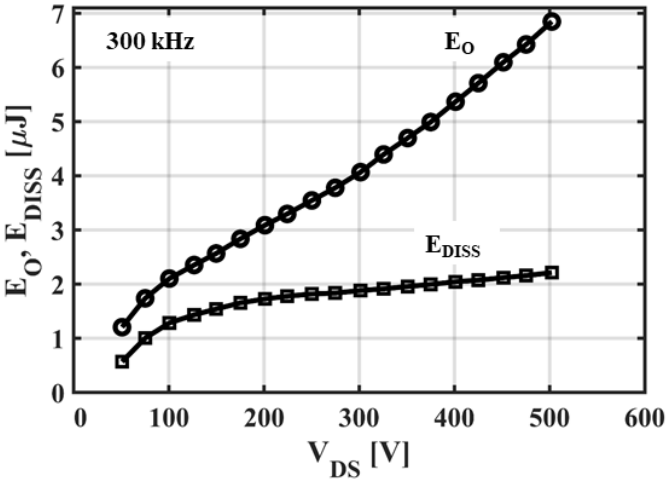

Fig. 11. Proposed large-signal datasheet graph for SJ A, showing total stored energy and dissipated energy per cycle.

capacitances. For the positive-going curve, this is due to larger p-pillar majority carrier pockets (relative to those shown in Fig. 5) at the higher ramp rate. In the negative-going sweep direction, the p-pillar pockets do not undeplete (in contrast to the 10 V_{DS}, ramp-down front in Fig. 5), leaving trapped charges—and lower measured C_{OSS}—even at 0 V_{DS}.

More broadly, small-signal C_{OSS} anomalies may give an indication of large-signal characteristics but are not directly predictive in any known way because the amount of charge trapping depends strongly on ramp rate. Devices with dc hysteresis at the relatively slow slew rate of C_{OSS} measurements will likely have poor large-signal characteristics, but the absence of small-signal dc hysteresis, unfortunately, does not indicate low C_{OSS} losses or a small E_O/E_{OSS} ratio at the slew rates in power converters. Because operating characteristics cannot be extrapolated in this manner, manufacturers should include large-signal E_O and C_{OSS} losses in power SJ datasheets, and we propose a graph for inclusion.

VII. Recommendations for SJ Datasheets

Datasheet and simulation reporting for C_{OSS} of silicon SJs need to be reconsidered and updated to address these anomalies. Large-signal analyses should be added to power device datasheets to provide accurate information on *in situ* device operation, and small-signal measurements should report ac frequency, dc ramp rate, and dc sweep direction.

An oft-cited shortcoming of large-signal measurements is a lack of extensibility; for discrete capacitors, characteristics would need to be reported at varying dc biases, ac frequencies, and ac magnitudes. Power device capacitors comprise a much more reasonable measurement space, however: C_O always starts near 0 V_{dc}, since the device conducts immediately before turn-OFF, a body diode or similar reverse characteristic guarantees the applied voltage is always positive, and the switching frequency is typically known within one or two orders of magnitude.

As such, manufacturers can and should include large-signal E_O and estimated C_{OSS} losses in datasheets, and we propose the plot shown in Fig. 11. E_O, the top curve, is the large-signal energy stored in C_O, which is valuable for both hard- and soft-switching applications. The bottom curve, E_{DISS}, indicates the energy per cycle that is dissipated in C_O in a soft-switching application. This plot provides a more accurate model of *in situ* operation for power SJs than small-signal C_{OSS} and E_{OSS} and should be added to datasheets at one or more relevant operating frequencies.

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