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Cascode GaN/SiC: A Wide-Bandgap Heterogenous Power Device for High-Frequency Applications

Jiale Xu, *Student Member, IEEE,* Lei Gu, *Student Member, IEEE,* Zhechi Ye, *Student Member, IEEE,* Saleh Kargarrazi, *Member, IEEE,* and Juan Rivas-Davila, *Senior Member, IEEE*

***Abstract*—Wireless power transfer systems and plasma generators are among the increasing number of applications that use high-frequency power converters. Increasing switching frequency can reduce the energy storage requirements of the passive elements that can lead to higher power densities or even the elimination of magnetic cores. However, operating at higher frequencies requires faster switching devices in packages with low-parasitics. Wide bandgap (WBG) power devices like Gallium Nitride (GaN) and Silicon Carbide (SiC) devices, have high critical fields and high thermal conductivity that make them good candidates for efficient high-voltage and high-frequency operations. Commercially available GaN and SiC devices have ratings targeting different applications. Lateral GaN devices dominate in lower-voltage (<650 V) and high-frequency applications as they have relatively small device capacitances (C_{oss}, C_{iss}), which make them easy to drive at high frequencies. On the other hand,, vertical SiC devices are often used in higher-voltage and low-frequency applications since they have higher blocking voltages and larger gate charge than their GaN counterparts. As a result, SiC devices usually require high-power and complicated gate drive circuitry. Recent work shows that in both GaN and SiC devices, losses in device C_{oss} can exceed the conduction losses at high switching frequencies and relatively high voltages under Zero-Voltage-Switching (ZVS) conditions. Moreover, the C_{oss} energy loss (E_{oss}) per switching cycle increases with frequency in GaN devices but remains roughly independent of frequency in SiC devices. This means that at high frequencies, SiC devices can be preferable due to their smaller C_{oss} energy loss even when taking into consideration the complexity of the gate drive circuit. In this paper, we present a WBG high-voltage cascode GaN/SiC power device, combining the advantages of both a GaN and a SiC device – namely, simple gate drive requirements, E_{oss} loss per cycle roughly independent of frequency, and relatively high voltage blocking capability. Comparing this cascode GaN/SiC device with a SiC MOSFET and a SiC JFET of similar voltage ratings and $R_{ds,ON}$, we find that the inverter using the cascode GaN/SiC device has the highest efficiency and simplest auxiliary gate drive circuitry. Finally, integrating the cascode GaN/SiC device has the potential benefits of achieving lower C_{oss} losses, higher device ratings, and better heat removal capability.**

I. Introduction

The demand for more compact electronic systems has pushed power electronics engineers to explore new topologies, use new semiconductor and packaging technologies that can lead to increases in power density. By increasing switching frequency, we can reduce the energy storage in the passive components that can lead to a smaller size. Recently, we have seen a growing number of applications using high-frequency power converters such as wireless power transfer [1], [2] and radio-frequency plasma generation [3], [4]. These high-frequency and high-power converters require faster switching devices with low conduction losses, which is difficult to achieve using Si MOSFETs. Wide bandgap (WBG) power devices, on the other hand, have low on-resistances, a wide operating temperature range, and can operate at high frequencies (HF, 3-30 MHz) and very high frequencies (VHF, 30-300 MHz). Gallium Nitride (GaN) and Silicon Carbide (SiC) devices are two commonly used WBG power devices and their different characteristics lead to different target applications.

GaN devices, especially lateral GaN High Electron Mobility Transistors (HEMTs), are suitable for relatively low-voltage and high-frequency applications. Since GaN layers are epitaxially grown on other substrates (Si, SiC, and Sapphire), the peak electric field occurs at the surface of a lateral GaN device. Limitations in the maximum electric field due to the lateral structure lead to relatively low voltage ratings (<650 V) in GaN HEMTs [5]. In addition, unlike Si devices, lateral GaN HEMTs are not avalanche-rated. Even though GaN has a higher critical field than Si (>10×), it is limited by the low dielectric strength of the surface material, which leads to breakdown in GaN HEMTs [6]. Recently, vertical GaN devices have attracted more attention [7], [8] with their higher device ratings, superior reliability, and better heat removal, as compared to the lateral GaN HEMTs. However, difficulties in material growth and processing in addition to high cost and the limitations of GaN wafers make them hard to manufacture and commercialize. Despite the device structure, a GaN device has the considerable benefit of being easy to drive at high frequencies due to its small gate charge. Unfortunately, recent research has shown that GaN HEMTs have high C_{oss} losses in the HF and VHF range even under Zero-Voltage-Switching (ZVS) conditions, and these losses increase with dV/dt [9]. C_{oss} losses are related to charging and discharging the output capacitor of a device; these losses are particularly non-negligible in soft-switching converters operating at high frequencies. C_{oss} losses are not part of the manufacturers' simulation models but can result in power dissipation that is an order of magnitude higher than the simulated value when operating in the HF or VHF range.

Unlike GaN devices, SiC devices are mostly used in higher voltage and lower frequency applications. They are vertical devices, which have higher voltage ratings than GaN HEMTs: ranging from a few hundred volts to a few kVs. SiC devices are often used at low-frequencies because they have large gate

J. Xu, L. Gu, S. Kargarrazi, and J. Rivas-Davila are with Stanford University, Stanford, CA, 94305 (e-mail:jialexu@stanford.edu; leigu@stanford.edu; skargar@stanford.edu; jmrivas@stanford.edu).

Z. Ye is with Tsinghua University, Beijing, China (e-mail:yezc15@mails.tsinghua.edu.cn).

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charge and require high-power gate drivers. These gate drive circuits are often bulky and difficult to design. For example, [10] shows a 2 kW Class Φ_2 inverter with a Si-based gate driver that is larger in size than the SiC MOSFET used as the switching device. At 6.78 MHz, the 20 V gate driver alone consumes 20 W to drive the 1.2 kV SiC MOSFET. To achieve a smaller and lighter power electronics system, integrated SiC-based gate drivers have been demonstrated for SiC devices [11]–[13]. However, the power dissipation for these gate drivers are still high, and they are not suitable for HF and VHF applications. Previous research implemented resonant gate drivers to efficiently drive the devices with large gate charge at high frequencies [14], [15]. However, the resonant gate drivers require additional components, increasing the complexity of the circuit.

Despite their large gate charge, recent studies on C_{oss} losses of SiC devices show that they have potential to outperform GaN devices at high frequencies and low currents [16], [17]. An interesting observation from these studies is that the C_{oss} energy loss per cycle of SiC devices is roughly independent of frequency as opposed to GaN devices, which show an $f_s^{0.6}$ dependency. Some SiC devices even show smaller C_{oss} losses at high frequencies than GaN devices of similar voltage ratings.

In this paper, we demonstrate a cascode GaN/SiC power device, which combines the benefits of a GaN device's fast switching ability, and a SiC device's high voltage blocking capability and low C_{oss} losses at high frequencies. This cascode device consists of a depletion-mode SiC Junction Gate Field-Effect Transistor (JFET) and an enhancement-mode GaN (eGaN) HEMT. The cascode device uses the same simple and low-power gate driver as GaN HEMTs, which greatly reduces the complexity and board area usage of the auxiliary gate drive circuitry for SiC devices.

Section II introduces the cascode GaN/SiC power device and describes its switching sequence. Detailed gate loss analysis in this section shows that the cascode device has the potential benefit of completely eliminating the gate loss of the SiC JFET with a negligible $R_{g,Jfet}$. In Section III, we show experimental results using the commercial SiC JFETs and GaN HEMTs. This cascode GaN/SiC device blocks 1 kV and achieves 91% efficiency in a 13.56 MHz, 700 W Class E inverter. In Section IV, we compare the performance of three Class E inverters using a SiC MOSFET, SiC JFET, and the cascode GaN/SiC device as the switching device, respectively. The results indicate that the cascode GaN/SiC device has a much simpler gate drive design which requires much smaller area on the board while achieving the highest efficiency. In Section V, we discuss the potential advantages of integrating the cascode GaN/SiC power device. The integrated cascode GaN/SiC device will have reduced threshold voltage drift, better heat removal capability, and reduced parasitics. Lastly, Section VI concludes the paper.

II. Cascode GaN/SiC Power Device Overview

To demonstrate the cascode GaN/SiC power device, we use two commercially available devices: a depletion-mode 1200 V SiC JFET (UJN1208K) and an enhancement-mode 100 V GaN HEMT (EPC2045). There are very limited number of SiC JFETs on market, and we selected UJN1208K based on its voltage rating and low device capacitance. We selected EPC2045 because it has a similar current rating to UJN1208K and a voltage rating that allows a margin for the transient behavior. Table I lists device parameters of these two FETs.

SiC JFETs have more stable device threshold voltages than SiC MOSFETs. SiC MOSFETs have more interface trap charges than Si MOSFETs, because the SiC/SiO_2 interface has more crystal defects than the Si/SiO_2 interface. These trap charges impact channel carrier mobility and subthreshold slope, which leads to variations in device threshold voltage [18]. Unlike SiC MOSFETs, SiC JFETs do not have a SiC/SiO_2 interface and theoretically avoid this problem. Since most of the drain-to-source voltage is blocked by the SiC JFET in the cascode device, we choose the GaN HEMT with moderate voltage rating, small gate charge and low on-resistance. Figure 1 shows the schematic of the cascode GaN/SiC power device. The source of the SiC JFET is

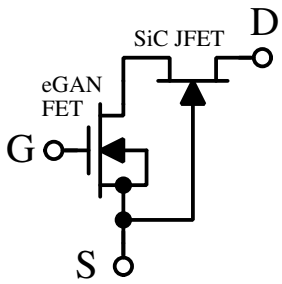

Fig. 1: Schematic of the cascode GaN/SiC power device.

connected to the drain of the GaN FET and the gate of the SiC JFET is connected to the source of the GaN FET. We are able to drive this cascode device easily at high frequencies by only driving the GaN FET. The voltage blocking capability of this cascode device is similar to that of the SiC JFET and can be explained by the switching sequence described in section II-A.

A. Cascode GaN/SiC Device Switching Sequence

Figure 2 shows the switching sequence of the cascode GaN/SiC device in a Class E inverter. At t_0, we switch the gate of the GaN FET from high to low. At t_1, the GaN FET is turned off, and its drain voltage starts to rise. From t_1 to t_2, the GaN FET is off while the SiC JFET is still on. Figure 3a illustrates the equivalent circuit during this period. The positive drain current (I_D) flows through the SiC JFET and charges C_{iss} of the JFET (C_{iss} = C_{gd} + C_{gs}) and C_{oss} of the GaN FET (C_{oss} = C_{gd} + C_{ds}) until V_{gs} of the SiC JFET reaches its threshold voltage (-7 V for UJN1208K) at t_2. From t_2 to t_3, the SiC JFET is turned off, and I_D continues to charge $C_{ds,Jfet}$ in series of $C_{oss,GaN}$ and $C_{gs,Jfet}$ (Figure 3b). At the same time, I_D is also charging $C_{gd,Jfet}$, but this charging path does not affect the voltage distribution between the SiC JFET and GaN FET [19]. The maximum drain voltage of the GaN FET in each turn-off switching process is determined by

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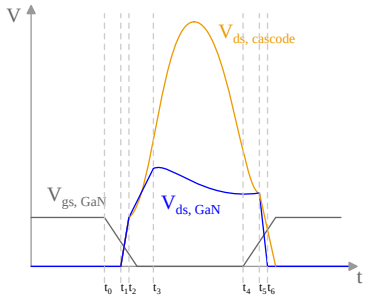
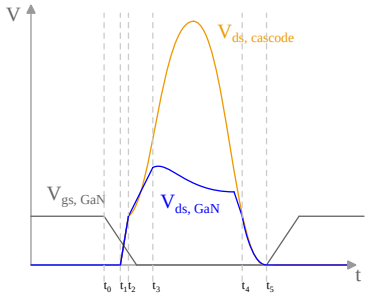
TABLE I: Device Parameters of the SiC JFET and GaN FET.

Device	Part Number	Package	$R_{ds,on}$ [mΩ]	C_{oss} [pF]	Q_G [nC]	V_{DS} [V]
SiC JFET	UJN1208K	TO247	77	42	62 (V_{DS}=600 V, V_{GS}=15.5 V)	1200
eGaN FET	EPC2045	die	5.6	260	5.2 (V_{DS}=50 V, V_{GS}=5 V)	100

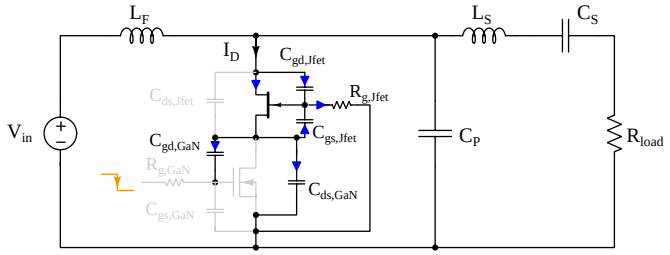


(a) Switching sequence with hard-switching turn-on.

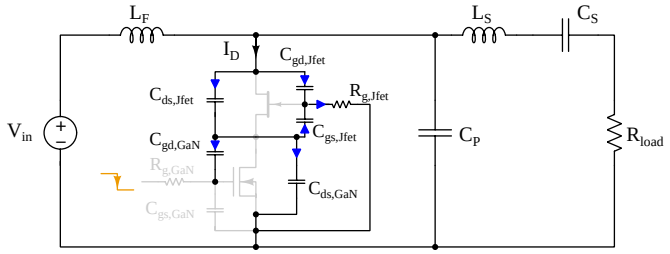


(b) Switching sequence with soft-switching turn-on.

Fig. 2: Switching sequence of the cascode GaN/SiC device in a Class E inverter with (a) hard-switching turn-on, (b) soft-switching turn-on.



(a) Turn-off step 1.



(b) Turn-off step 2.

Fig. 3: Schematics showing the turn-off behavior of the cascode GaN/SiC device in a Class E inverter. (a) The GaN FET will be turned off first while the SiC JFET is still on. (b) Once the source node of the JFET is charged to reach $V_{gs,JFET} = V_{threshold}$, the JFET is turned off.

the junction capacitor charge. The voltage blocking capability of the cascode GaN/SiC device is similar to that of the SiC JFET, which is measured to be higher than 1.2 kV.

In an event of hard-switching turn-on (Figure 2a), we apply the gate signal at t_4, and the GaN FET will be turned on first while the SiC JFET remains off (t_5). Once the GaN FET is on, all of the capacitors at its drain node (which is also the source node of the SiC JFET) will start discharging through the channel of the GaN FET (Figure 4a). The SiC JFET will be turned on when its V_{gs} is greater than the threshold voltage. Then the source node of SiC JFET will continue to discharge until it reaches 0 V (Figure 4b).

If I_D in Figure 4 is negative, it is possible to turn on the cascode device by ZVS (Figure 2b). The negative I_D helps to discharge the capacitors at the drain node of the GaN FET before we apply the gate signal. At t_4, $V_{ds,GaN}$ decreases to the threshold voltage of the SiC JFET, and the JFET will be turned on by ZVS. We will then turn on the GaN FET at t_5. However, since SiC JFETs usually have very small C_{ds} (on the order of a few pF), it can be hard to discharge the capacitors $C_{oss,GaN}$ and $C_{gs,Jfet}$ completely by the negative I_D. If reducing the gate loss is the primary goal, we could add external capacitors in parallel to the SiC JFET to achieve ZVS turn-on. However, one disadvantage of doing so is that the maximum drain voltage of the GaN FET will be higher. In addition, we need to make sure that the total C_{ds} of the SiC JFET (including the added capacitors) is completely discharged before the SiC JFET is turned on to avoid any power dissipation through the SiC JFET channel during the turn-on process [19].

In Section II-B, we discuss the gate loss of the SiC JFET in the cascode device for both hard-switching and soft-switching cases.

B. Gate Loss of the SiC JFET in the Cascode GaN/SiC Device

Generally, gate loss of a SiC device is quite high (tens of watts) in HF and VHF power circuits, and it is determined by device gate charge and gate voltage. However, the gate loss mechanism in the cascode GaN/SiC device is different. Theoretically, the SiC JFET in the cascode device can have zero gate loss in a soft-switching case.

As illustrated in Figure 3, during the turn-off process, C_{oss} of the GaN FET and all of the SiC JFET capacitors are charged by I_D. In an ideal case of zero $R_{g,Jfet}$, there will be no gate power loss in the turn-off process. With a non-zero $R_{g,Jfet}$, the gate power loss of the SiC JFET is

$$P_{JFETgate,turn-off} = P_{R_{g,Jfet}} = |i_{R_{g,Jfet}}(t)|^2_{RMS} \cdot R_{g,Jfet} \quad (1)$$

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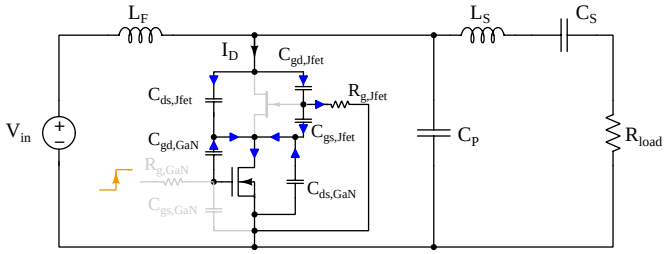
The current through $R_{g,Jfet}$ is

$$I_{R_{g,Jfet}} = I_D \cdot \frac{\frac{1}{jwC_{oss,GaN}}}{\frac{1}{jwC_{oss,GaN}} + \frac{1}{jwC_{iss,Jfet}} + R_{g,Jfet}} \tag{2}$$

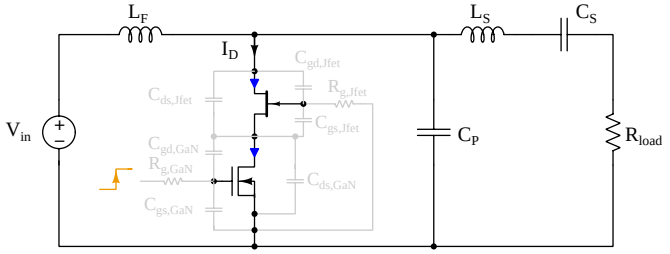
The power dissipation of $R_{g,Jfet}$ is

$$P_{R_{g,Jfet}} = R_{g,Jfet} \cdot \left| I_{D,rms} \cdot \frac{\frac{1}{jwC_{oss,GaN}}}{\frac{1}{jwC_{oss,GaN}} + \frac{1}{jwC_{iss,Jfet}} + R_{g,Jfet}} \right|^2 \tag{3}$$

$$P_{R_{g,Jfet}} = \frac{I_{D,rms}^2 R_{g,Jfet}}{\left(1 + \frac{C_{oss,GaN}}{C_{iss,Jfet}}\right)^2 + (wC_{oss,GaN}R_{g,Jfet})^2} \tag{4}$$



(a) Turn-on step 1.



(b) Turn-on step 2.

Fig. 4: Schematics showing the turn-on behavior of the cascode GaN/SiC device in a Class E inverter. (a) The GaN FET will be turned on first while the SiC JFET is still off. (b) Once the capacitors at the source node of the JFET are discharged to reach $V_{gs,JFET} = V_{threshold}$, the JFET is turned on.

Therefore, to minimize the gate power loss of the SiC JFET, we should minimize $R_{g,Jfet}$, reduce $C_{iss,Jfet}$, while increasing $C_{oss,GaN}$.

When the cascode device is turned on by hard-switching (I_D is positive), all of the charges at the drain node of the GaN FET ($Q_{drain,GaN}$, which includes charge stored in $C_{gs,JFET}$ and $C_{oss,GaN}$) will be dumped through the GaN FET channel (Figure 4a). Therefore, the SiC JFET will have gate loss of

$$P_{JFETgate,turn-on} = \frac{1}{2} Q_{drain,GaN} \cdot V_{drain,GaN} \cdot f_s + |i_{R_{g,Jfet}}(t)|^2_{RMS} \cdot R_{g,Jfet} \tag{5}$$

If the cascode device were turned on by ZVS (I_D is negative, and $C_{ds,Jfet}$ is sufficient), the capacitors at the drain node of the GaN FET could be discharged by I_D before the device is turned on. As a result, there will be no gate power loss for the SiC JFET with a zero $R_{g,Jfet}$. When $R_{g,Jfet}$ is non-zero, the SiC JFET will have a turn-on loss similar to Equation 1. However, if the negative current I_D does not discharge the drain node of the GaN FET ($Q_{drain,GaN}$) completely, the remaining charge will still be lost through the channel of the GaN FET and results in a turn-on loss similar to Equation 5. Therefore, in a soft-switching case, we can potentially eliminate all of the SiC JFET gating loss in the cascode device if $R_{g,Jfet}$ is negligible, while in a hard-switching case, we can reduce the SiC JFET gating loss by half.

C. Small Signal C_{oss} and Large Signal C_{oss} Energy Loss

Before using the cascode GaN/SiC device in power converters, we also measured its output capacitance (C_{oss}). Small signal C_{oss} is an important parameter when designing HF and VHF inverters, because the total drain-to-source capacitance (including both the device C_{oss} and the external capacitor C_p) determines the ranges of possible operating frequencies and power levels for an inverter. The total charge computed by integrating the small signal CV curve is also important to design for ZVS operations.

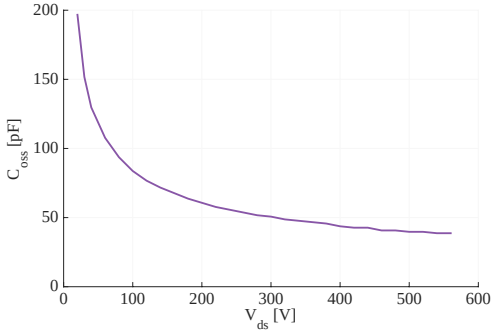


Fig. 5: Measured small signal C_{oss} of the cascode GaN/SiC device at 1 MHz from 0 V to 560 V.

Figure 5 shows the small signal C_{oss} of the cascode GaN/SiC device measured using an impedance analyzer (E5061B from Keysight Technologies). We measured C_{oss} at 1 MHz and swept the bias voltage from 0 V to 560 V. We did not take measurements above 560 V due to limitation of the available DC power supply. The C_{oss} of the cascode device

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is similar to the $C_{oss,Jfet}$ in series with $C_{oss,GaN}$. When the applied DC drain voltage across the cascode device is lower than -$V_{th,Jfet}$, the SiC JFET is on, and the measured effective C_{oss} is similar to that of the GaN FET. Once the applied voltage exceeds -$V_{th,Jfet}$, most of the drain voltage is then blocked by the SiC JFET. The effective C_{oss} of the cascode device then becomes $C_{oss,Jfet}$ in series with $C_{oss,GaN}$. When we swept the total V_{ds} from 10 V to 500 V, the measured $V_{ds,GaN}$ changed from 7 V to 17 V. From Figure 5, We see that the small signal C_{oss} of this cascode device is 40 pF at 500 V.

As mentioned in Section I, large sigal C_{oss} energy loss is not part of simulation models provided by manufacturers, but it contributes a significant portion to the total device switching loss in high-frequency and high-voltage applications. Using the Sawyer-Tower test [20], [21], we measured C_{oss} energy loss of the GaN FET (EPC2045) and SiC JFET (UJN1208K) separately at 13.56 MHz. We did not measure the C_{oss} energy loss of the cascode GaN/SiC device in a single test, because in that case, thermal measurements could also capture the gating loss of the SiC JFET. To ensure the SiC JFET is kept off during the test, we used batteries to apply a constant voltage of -20 V to its V_{GS} (Figure 6). Figure 7 shows the measured C_{oss} energy loss for EPC2045 and UJN1208K. In Figure 7b, we extrapolated the measured data using Equation 6, which is similar to the Steinmetz equation [22], to predict energy loss across all device operating voltages:

$$E_{diss} = k \cdot V_{ds}^{\alpha} \tag{6}$$

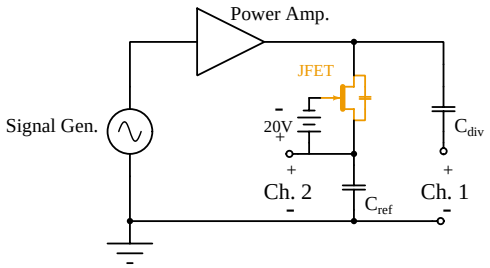


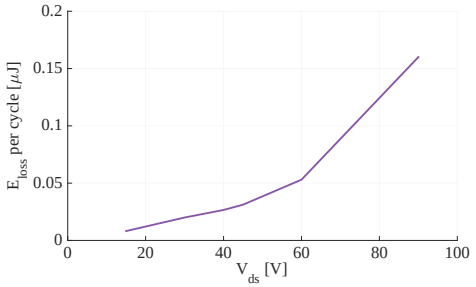
Fig. 6: Sawyer-Tower test circuit for measuring the C_{oss} energy loss of the SiC JFET. We used batteries to apply a constant voltage of -20 V to V_{GS} of the JFET to keep it off.

From Figure 7, we estimate the C_{oss} power dissipation of the cascode GaN/SiC device at 13.56 MHz with V_{DS} = 1000 V is 15 W.

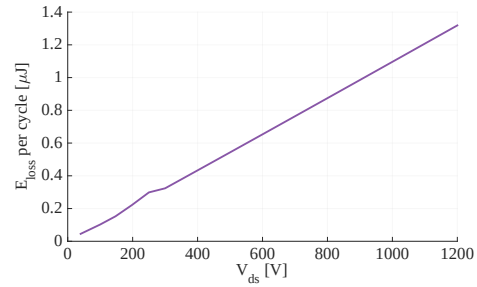
III. Using the Cascode GaN/SiC Power Device in a Class E Inverter

After analyzing the cascode GaN/SiC power device, we tested its performance in a Class E inverter. We designed and implemented a 13.56 MHz 700 W Class E inverter [23], [24] that has a maximum drain voltage of about 1 kV. The schematic and PCB of the Class E inverter are shown in Figure 8. The measured output power is 718 W with 91.1% efficiency at 200 V input.

Figure 9 shows the measured waveforms of the drain voltage and gate-to-source voltage $V_{gs}(t)$ of the SiC JFET in the



(a) EPC2045.



(b) UJN1208K.

Fig. 7: Measured C_{oss} energy loss per cycle at 13.56 MHz of the (a) GaN FET and (b) SiC JFET using Sawyer Tower Tests.

cascode device. $V_{gs}(t)$ of the SiC JFET is also the inverse of $V_{ds}(t)$ of the GaN FET. The measured maximum of the SiC JFET drain voltage is 998 V and $V_{gs}(t)$ is 0 V to -40 V. The oscillations in $V_{gs}(t)$ at each turn-off transition are caused by the parasitic inductance of the SiC JFET and PCB. The measured V_{gs} exceeds gate voltage rating of the SiC JFET (-20 V). However, we will show in Section IV that it is actually beneficial to drive the SiC JFET using a larger swing of gate voltage. The gate-to-source voltage of the SiC JFET depends on the junction capacitor charge during the turn-off transition [19] and the RC constant at the gate of the SiC JFET. From the waveforms in Figure 9, we also see that the JFET is turned on (V_{gs} = 0 V) when V_{Drain} is approximately 0 V. This means that the SiC JFET is operating under ZVS. In this circuit, we used a 5 V low-power gate driver (LM5114) to drive the cascode GaN/SiC device. The gate driver consumes only 558 mW at 13.56 MHz.

IV. Comparison of a SiC MOSFET, SiC JFET, and the Cascode GaN/SiC Device Used in a Class E Inverter

To demonstrate the advantages of the cascode GaN/SiC device, we built another two Class E inverters using a SiC MOSFET and a SiC JFET as the switching device and compared their performances. We chose the SiC MOSFET and SiC JFET that have similar voltage ratings and $R_{ds,on}$ values as the cascode device to make the comparison fair. We did not compare with GaN devices because of the limitations on their voltage ratings. Table II lists the parameters of these three switches based on device datasheets.

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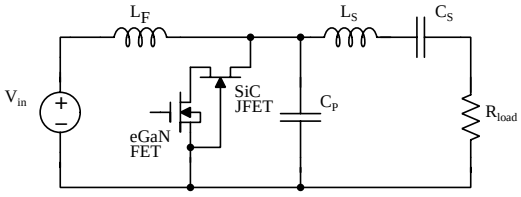
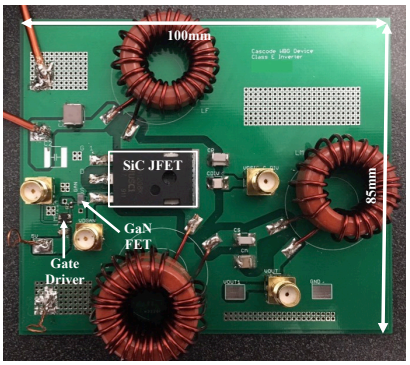
TABLE II: Device Parameters of SiC MOSFET, SiC JFET, and Cascode GaN/SiC Device.

Device	Part Number	V_{ds} [V]	$R_{ds,on}$ [mΩ]	C_{iss} [pF]	C_{oss} at V_{ds}=500 V [pF]	V_{gs} [V]
SiC MOSFET	C2M0080120D	1200	80	950	85	0 to 20
SiC JFET	UJN1208K	1200	77	450	42	-20 to 0
Cascode GaN/SiC Device	EPC2045 + UJN1208K	1350	84	570	40	0 to 5



(a) Class E Inverter Schematic.



(b) Class E Inverter PCB.

Fig. 8: Schematic and PCB of the Class E inverter using the cascode GaN/SiC device.

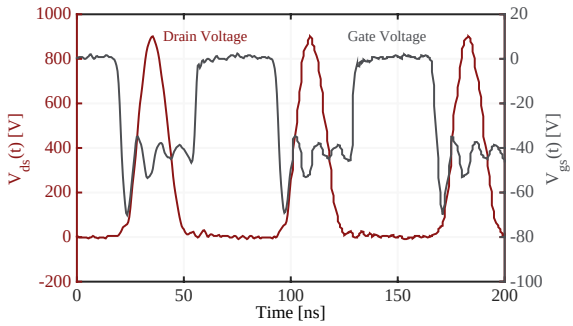


Fig. 9: Measured drain voltage and gate-to-source voltage waveforms of the SiC JFET in the cascode device. $V_{gs}(t)$ of the SiC JFET is also the inverse of $V_{ds}(t)$ of the GaN FET. The duty cycle is 50%.

We measured the breakdown voltage of the cascode GaN/SiC device to be 1350 V by sweeping its V_{ds} and measuring its leakage current using a curve tracer (Tektronix 576). The C_{oss} value of the cascode device in the table is based on the small signal measurement in Section II-C. In real circuit operations, most of the drain voltage is across the SiC JFET, which means most of the C_{oss} loss comes from the cascoded SiC JFET. The C_{iss} of the cascode device listed in the table is the C_{iss} of the GaN FET. Since the GaN FET has such low gate drive voltage, the gate loss of the cascode device is very low compared to the other two devices. However, as mentioned in Section II-B, the SiC JFET in the cascode device can still have gate loss. Besides the potential reduction of SiC JFET gate loss in the cascode device, there is a significant difference in the source of the SiC JFET gating power. When using a SiC JFET alone, the gate driver needs to provide sufficient power to drive the JFET. When using a cascode device, the gate driver only needs to drive the GaN FET, while the circuit's main supply is providing power to drive the SiC JFET because the gate of the SiC JFET is connected to the circuit's main ground. Since we do not need a high-power gate driver for the cascode device, the auxiliary gate drive circuitry will be much easier to design and occupies less board area.

After selecting the devices to compare, we built another two Class E inverters using the same specifications. Although the sizes of all passive components and active switches are quite similar in all three inverters, the complexity of their auxiliary gate drive circuits differ significantly. Figure 10 shows the shematics of the three gate drive circuits for the cascode GaN/SiC device, SiC MOSFET, and SiC JFET. To generate the supply voltage for the gate driver, we need to use a dc-dc regulator to convert the circuit's input voltage to the corresponding gate voltage in each case. The cascode GaN/SiC device only requires less than 1 W from a 5 V gate driver, while the SiC MOSFET and SiC JFET need 40 W from a 20 V gate driver and 20 W from a -20 V gate driver, respectively. As a result, the auxiliary gate drive circuit for the cascode device is the simplest and smallest among the three. Although both of the gate drive circuits for the SiC MOSFET and SiC JFET need to provide tens of watts, the one for the SiC MOSFET is much simpler because it does not require negative gate voltage. As shown in Figure 10c, when driving a SiC JFET, we need to use an isolated DC-DC converter to output -20 V and a level shifter to generate -20 V to -15 V gate signal feeding into its gate driver.

Figure 11 shows the PCB of the Class E inverter using the SiC JFET. Comparing with the inverter using the cascode GaN/SiC device in Figure 8b, we find that not only the gate driver IC for SiC JFET is larger than the total volume of the GaN FET and the gate driver IC in the cascode device, but its gate drive circuit is much more complicated and occupies larger board area. To quantify the benefits in gate drive circuitry of the cascode GaN/SiC device, Table III compares gate drive cost and weight of the SiC JFET with those of the cascode device. It is clear that both the weight and cost of the gate drive for the cascode device is much lower than that of the SiC JFET. Even if we consider the GaN FET as part of the gate drive for the cascode device, the total weight is still

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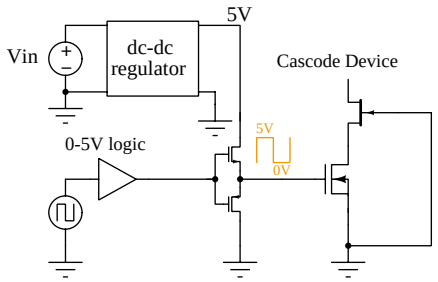
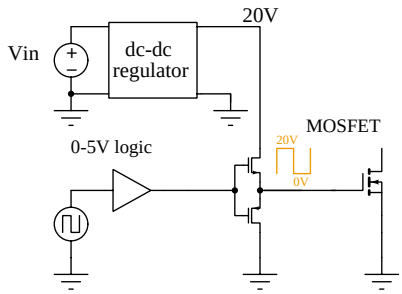
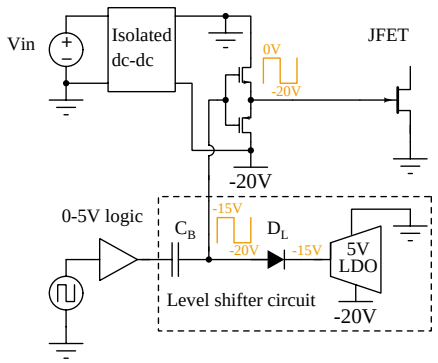


(a) Cascode GaN/SiC device.



(b) SiC MOSFET.



(c) SiC JFET.

Fig. 10: Auxiliary gate drive circuitry of (a) cascode GaN/SiC device (b) SiC MOSFET, (c) SiC JFET.

less than 0.1 g and the total cost (digikey low volume prices as of February 2019) is $7.7.

TABLE III: Comparison of the Gate Drive Weight and Cost for SiC JFET and the cascode GaN/SiC device.

Switch	Gate Drive Weight [g]	Gate Drive Cost [$]
SiC JFET	12.56	23.71
Cascode GaN/SiC Device	0.038	1.7

Table IV shows the efficiency comparison of the SiC JFET Class E inverters with different gate voltages. The inverter efficiency is 10% higher when the gate signal swings from -30 V to 0 V compared to from -20 V to 0 V. Although larger gate signal swing causes higher gating loss, it reduces switch transition time and results in lower leakage power. The combined effect is higher inverter efficiency. It is difficult for commercially available gate driver ICs to provide gate signals $\geq$30 V swing. However, when used in the cascode GaN/SiC device, the SiC JFET achieves a 40 V gate swing easily (Figure 9).

TABLE IV: Efficiency Comparison of the SiC JFET Class E Inverter (V_{in} = 200 V) with Different Gate Voltages.

Gate Voltage [V]	$\mathbf{I}_{in}$ [A]	$\mathbf{V}_{drain,max}$ [V]	$\mathbf{P}_{out}$ [W]	$\mathbf{P}_{gate}$ [W]	η_{total}
-20 to 0	3.66	1074	588	8.1	79.6%
-25 to 0	3.49	1127	616	17	86.2%
-30 to 0	3.44	1165	640	20	90.4%

Table V shows the performance comparison of the three inverters. We tested the Class E inverters using the SiC MOSFET, SiC JFET, and casocde GaN/SiC device at V_{in} = 200 V. In addition, we also tested the inverter using the cascode GaN/SiC device at V_{in} = 180 V to make a fair comparison with the other two inverters at a similar output power level. For efficiency calculations, we considered the power consumption in gate drive circuits in all three cases. To ensure a fair comparison with the cascode device, we drive the SiC JFET using a -30 V to 0 V gate signal.

From the table, we see that the inverters using the SiC JFET and cascode device have higher efficiencies than the inverter using SiC MOSFET. One reason is that the SiC MOSFET has both higher C_{iss} and C_{oss}, which leads to both higher gating loss and higher C_{oss} loss at high dV/dt. Another reason is that the inverter using the SiC MOSFET cannot achieve perfect ZVS due to large package parasitics and long delay time inside the MOSFET. Figure 12 shows the measured waveforms of the Class E inverter using the SiC MOSFET. To achieve its best performance, we used a low duty cycle of 36% in this case to compensate for large capacitances and long propagation delay of the device. The inverter efficiency using the cascode GaN/SiC device is slightly higher than that of the SiC JFET. Figure 13 shows the measured waveforms of the Class E inverter using the SiC JFET. Similarly, the circuit is tuned to have a duty cycle of 44% to achieve the best performance. Comparing with the waveforms of the Class E inverter using the cascode device (Figure 9), we see that the cascode device has the best ZVS performance among the three switching devices.

As a result of comparing three switches, we find that the inverter using the cascode GaN/SiC device shows the highest efficiency and requires a much simpler and cheaper auxiliary gate drive circuitry.

V. Advantages of Integrating the Cascode GaN/SiC Power Device

After demonstrating the benefits of the cascode GaN/SiC device by using commercially available discrete parts, we plan to integrate this cascode device in the future. This section discusses potential advantages of integrating the cascode GaN/SiC power device.

Most GaN HEMTs used in power applications today are built on Si, SiC, and sapphire substrates. Among these three, Si is the most common one due to its low cost and high availability of large Si wafers. However, it has the highest lattice mismatch (-17%) and thermal expansion mismatch

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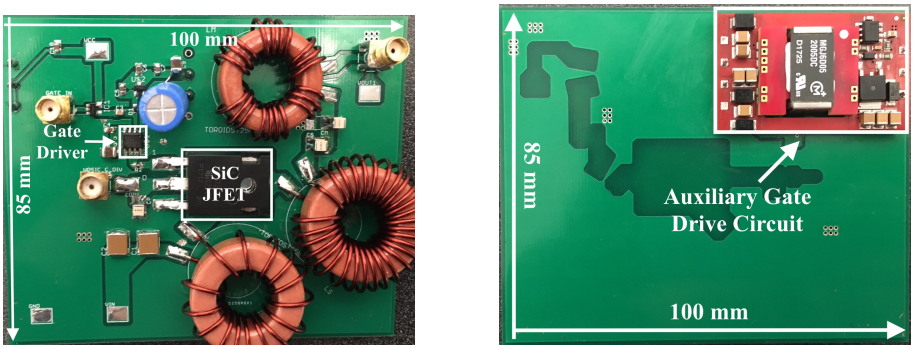

(a) PCB Top view. **(b)** PCB Bottom view.

Fig. 11: PCB of Class E inverter using the SiC JFET.

TABLE V: Comparison of Class E Inverters Using SiC MOSFET, SiC JFET, and Cascode GaN/SiC Device.

Switch	V_{in} [V]	I_{in} [A]	$V_{drain,max}$ [V]	P_{out} [W]	P_{gate} [W]	η_{total}
SiC MOSFET	200	3.73	1184	637	39	81.1%
SiC JFET	200	3.44	1165	640	20	90.4%
Cascode GaN/SiC Device	200	3.94	998	718	0.56	91.1%
Cascode GaN/SiC Device	180	3.68	828	619	0.56	93.4%

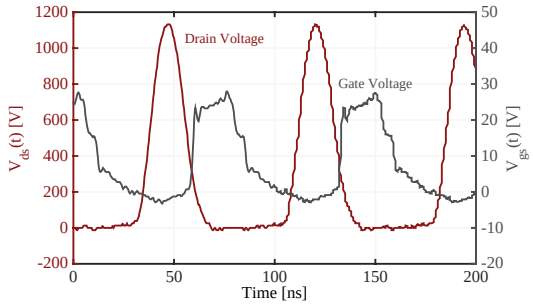

Fig. 12: Measured $V_{ds}(t)$ and $V_{gs}(t)$ waveforms of the SiC MOSFET in the Class E inverter. The duty cycle is tuned to be 36% to have the best performance.

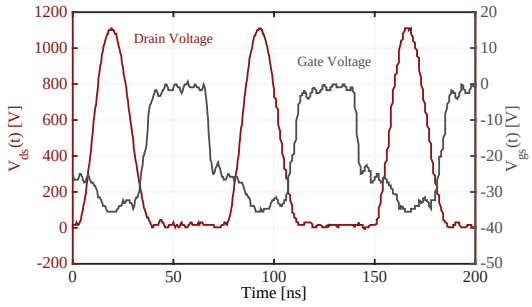

Fig. 13: Measured $V_{ds}(t)$ and $V_{gs}(t)$ waveforms of the SiC JFET in the Class E inverter. The duty cycle is tuned to be 44% to have the best performance.

(+116%) to GaN [25]. These mismatches make direct epitaxial growth of GaN/AlN layers on Si substrate difficult, and it is therefore necessary to include a buffer layer in the structure [26]. However, growth of the buffer layer introduces deep traps through foreign dopants, which leads to C_{oss} losses in the GaN-on-Si HEMTs [27]. On the other hand, SiC has much lower substrate lattice mismatch (+3.5%) and thermal expansion mismatch (+33%), with the trade-off of higher cost. Because of the low mismatch in material properties, there are fewer trapped charges in the buffer layer of the GaN-on-SiC devices. Therefore, GaN-on-SiC devices can have smaller C_{oss} losses than their GaN-on-Si counterparts. Differences in the substrate types also result in different current ratings of the devices. [28] shows that the maximum drain current of GaN-on-Si devices is only 68% of that of GaN-on-SiC devices. In addition, SiC has 3× higher thermal conductivity than Si, which makes heat removal much easier for GaN-on-SiC devices than for GaN-on-Si devices.

Integrating the cascode GaN/SiC power device also allows us to reduce device parasitics, design for smaller $R_{ds,ON}$, and minimize $R_{g,Jfet}$ to reduce SiC JFET gate power loss. Comparing with SiC MOSFETs of similar voltage rating, the integrated cascode GaN/SiC device will have smaller $R_{ds,ON}$ because of high electron mobility in the channel [29]. As discussed in Section II-B, minimizing gate resistance can save all of JFET gate power in a soft-switching case, and half of the JFET gate power in a hard-switching case. $R_{g,Jfet}$ depends on doping concentration in the p+ gate region. Since the ionization energy of SiC is high, dopants may not be fully ionized at room temperature, which may result in a high gate resistance. In the next step of integrating the cascode GaN/SiC device, we can minimize the gate resistance by redesigning the device structure and reducing the effective length of the p+ gate region.

To summarize, integrating the cascode GaN/SiC device has potential benefits of achieving lower C_{oss} losses, higher device ratings, and better thermal conductivity. Integration also provides flexibility of optimizing device parameters to improve efficiency.

VI. Conclusion

As more applications require high-frequency power converters, there is an increasing need for higher-power and faster-switching devices. In this paper, we propose and demonstrate a cascode GaN/SiC power device, which combines the benefits of both a GaN and a SiC device: simple gate drive circuitry, smaller C_{oss} losses at high frequencies, and relatively high voltage blocking capability. This cascode device has potential to save all of the SiC JFET gating power in a soft-switching case. We demonstrated that the cascode GaN/SiC device is able to block 1.2 kV, consumes only 558 mW in the gate driver at 13.56 MHz, and achieves 91% efficiency in a 13.56 MHz, 700 W Class E inverter. After comparing the performances of the Class E inverters using a SiC MOSFET, SiC JFET and cascode GaN/SiC device, we found that the inverter using the cascode device achieves the highest efficiency among all and requires a much simpler, cheaper, and smaller auxiliary gate drive circuitry. In the future, we will integrate this cascode GaN/SiC power device and optimize it for high-frequency and high-power circuits.

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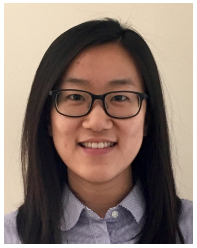
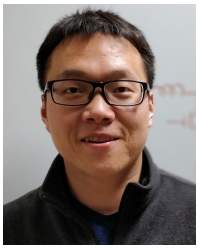


Jiale Xu (S'17) received the B.A.Sc degree in electrical engineering from University of Toronto, Toronto, Canada, in 2015, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2017. She is currently working toward the Ph.D. degree in electrical engineering in the Stanford University Power Electronics Research Lab, Stanford University, Stanford, CA, USA. Her research interests include high-frequency resonant converters.



Lei Gu (S'14) received the B.Eng. degree from Harbin Institute of Technology, Harbin, China, in 2013, and the M.S. degree from Stanford University, Stanford, CA, USA, in 2015. He is currently working towards the Ph.D. degree at the Stanford University Power Electronics Research Laboratory, Stanford University, Stanford, CA, USA. His research interests include high-frequency power electronics and RF power amplifiers.

Zhechi Ye (S'19) received the B.Eng. degree from the Tsinghua University, Beijing, China, in 2019. His research interests include high-frequency power converters, power semiconductor devices and their applications.

Saleh Kargarrazi (M'10) is a postdoctoral research scholar in the Department of Aeronautics and Astronautics at Stanford University. He holds a Ph.D. degree from KTH Royal Institute of Technology in Sweden, in 2017. His research has been focused on wide-bandgap (including Silicon Carbide and Gallium Nitride) devices and circuits for emerging applications.

Juan Rivas-Davila (S'01-M'06-SM'17) was born in Mexico City, Mexico. He received the B.A.Sc. degree from the Monterrey Institute of Technology, Monterrey, Mexico, in 1998, and the S.M. and Sc.D. degrees from the Laboratory of Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA, USA, in 2003 and 2006, respectively.

From 2007 to 2011, he was a Power Electronics Engineer with the High-Frequency Power Electronics Group at the General Electric Global Research Center, Niskayuna, NY, USA. From 2011 to 2013, he was an Assistant Professor at the University of Michigan, Ann Arbor, MI, USA. In 2014, he joined Stanford University, Stanford, CA, USA, as an Assistant Professor in the Electrical Engineering Department. His research interests include power electronics, RF power amplifiers, resonant converters, soft-switching topologies, and the design of air-core passive components for VHF power conversion.