

# Origins of Soft-switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications

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This paper has been accepted for publication by

**IEEE Journal of Emerging and Selected Topics in Power Electronics.**

## DOI

10.1109/JESTPE.2020.3034345

## Citation

Z. Tong, J. Roig-Guitart, T. Neyer, J. D. Plummer and J. M. Rivas-Davila, "Origins of Soft-switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2020.3034345.

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# Origins of Soft-switching $C_{oss}$ Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications

Zikang Tong, *Student Member, IEEE*, Jaume Roig-Guitart, Thomas Neyer, James D. Plummer, *Fellow, IEEE*, and Juan M. Rivas-Davila, *Senior Member, IEEE*

**Abstract**—The recent development and commercialization of wide bandgap (WBG) power semiconductors, specifically gallium nitride (GaN) and silicon carbide (SiC), has driven the increase in switching frequency for soft-switching power converters like the Class E, Class  $\Phi_2$ , and Class DE resonant inverters and rectifiers. However, prior literature has characterized numerous commercial GaN and SiC devices using the Sawyer-Tower circuit and discovered significant large-signal charge-voltage hysteresis of the  $C_{oss}$ . This  $C_{oss}$  hysteresis, equivalent to off-state energy loss, is highly dependent on the frequency and voltage across the device, hindering the efficiency and performance of MHz-range soft-switched converters. This paper is the first to explain the origin of the  $C_{oss}$  loss in SiC power devices as charging and discharging conduction loss at the termination of the device. The loss characteristics relative to operating voltage, frequency,  $dV/dt$ , and temperature are dictated by incomplete ionization. Incomplete ionization also highlights a significant inconsistency between the large-signal  $C_{oss}$  behavior and small-signal behavior, which is often the model used in manufacturers' datasheets and SPICE simulations. The large-signal charge-voltage behavior is transient, where the charge in the  $C_{oss}$  depends on the rate of the voltage swing across the device. We validate these hypotheses through mixed-mode simulations using Sentaurus® Technology Computer-Aided Design (TCAD) and experimentally using commercial and custom SiC devices.

**Index Terms**—Silicon carbide, Power semiconductor devices, Loss-measurement, Capacitance-voltage characteristics, Semiconductor device modeling

## I. INTRODUCTION

Silicon carbide (SiC) is a wide bandgap (WBG) material with promises to surpass the silicon (Si) power device limit by achieving orders of magnitude lower specific on-resistances for similar breakdown voltages [1]–[3]. These new device technologies allow power converters to achieve higher voltages, power levels, and frequencies, enabling the reduction of passive component sizes [4]. In the high-frequency (HF) 3 MHz – 30 MHz range, numerous studies and demonstrations on soft-switched power converters using SiC devices exist in the literature, targeting applications such as inductive wireless power transfer and high-power semiconductor plasma processing [5]–[13]. Despite this, many of these papers present converters with either (a) lower (< 80%) efficiencies, (b)

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reasonable efficiencies at high power levels but with large absolute semiconductor losses (> 50 W), or (c) good efficiencies and low semiconductor losses but with parts derated to under 50% of the maximum breakdown voltage and some even below 20%. Even though the devices in these systems are clearly operating under zero voltage switching (ZVS) conditions, energy stored in the device drain-source output capacitance ( $C_{oss}$ ) is still lost. The  $C_{oss}$  losses can be especially high at increased frequencies and voltages, which are regimes where these devices tend to operate.

The root causes for the anomalous  $C_{oss}$  losses in power devices have only been recently studied in the literature. The earliest investigations were on Si superjunction (SJ) MOSFETs switching in the kHz range [14]–[16]. Even at slower switching speeds, Si SJ MOSFETs exhibit significant charge-voltage hysteresis, making them unusable at higher frequencies. Since then, several reports have pinpointed the loss mechanism as a result of charge stranding between the superjunction pillars as the depletion region expands during off-state operation [15], [17]–[19]. For GaN high-electron-mobility transistors (HEMTs), a few papers have characterized and identified the  $C_{oss}$  loss mechanism as a result of a combination of leakage current through the silicon substrate and trapping in the buffer region stack [20], [21]. For SiC, some literature has measured  $C_{oss}$  losses in diodes and MOSFETs [22]–[27]. Compared to GaN, these devices exhibit a frequency independent loss trend in the MHz range [26]. However, previous work has not pinpointed the physical loss mechanism in these devices.

In addition to the  $C_{oss}$  losses, recent papers have observed a large discrepancy between  $C_{oss}$  energy storage from large-signal switching behavior and small-signal extrapolation [18], [19], [28]–[30]. In general, manufacturers' SPICE models utilize small-signal  $C_{oss}$  data to obtain energy and charge related values for circuit design. Therefore, it is crucial in soft-switching topologies to accurately and properly capture the  $C_{oss}$  behavior, since many resonant circuit topologies incorporate the device's output capacitance as snubbers in order to achieve ZVS. Many design techniques for these resonant converters involve the passive components having accurate values and predictable behavior, but currently, datasheets and SPICE models neither capture the  $C_{oss}$  losses nor the actual large-signal behavior. Prior art such as [31]–[33] has focused much attention on developing analytical and physics-based models to accurately capture the dynamics of hard-switching losses in SiC MOSFETs. Thus, the understanding of the device physics

in high-frequency and high- $dV/dt$  soft-switched regimes is just as vital in order to update these models and datasheets.

The mitigation of  $C_{oss}$  losses is significant for both the dominant applications, such as hundreds of kHz to a few MHz resonant converters, where  $dV/dt$ 's can be high in common topologies such as the LLC or dual active bridge (DAB) converters as well as emerging applications, such as 6.78 MHz or 13.56 MHz wireless power transfer. Therefore, the contribution of this paper is to provide the first reported explanation behind the origins of where in the device structure and what physical mechanisms influence the  $C_{oss}$  losses in SiC unipolar devices for high-frequency power applications. Based upon Sentaurus® TCAD simulations and experimental evidence, we identify the cause as resistive power dissipation mainly in the termination region, with frequency dependency and charge-voltage behavior dictated by incomplete ionization. The organization of this paper is as follows: Section II provides the necessary background information. Section III presents the experimental measurement procedures. Sections IV and V discuss, compare, and explain the measurement results with the TCAD simulations for the  $C_{oss}$  losses and the large-signal charge-voltage behavior respectively. Lastly, Section VI summarizes and concludes this work.

## II. DEVICE TECHNOLOGY AND PHYSICAL CONCEPTS

In this section, we provide a short review of semiconductor technology terminologies critical for the comprehension of the remainder of this paper. Specifically, we discuss the static and transient behavior of incomplete ionization and the structure of a vertical SiC power device.

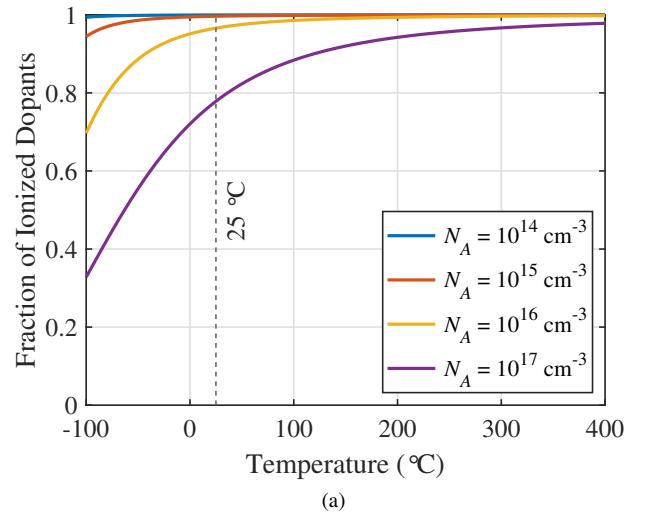
### A. Incomplete Ionization

For doped semiconductor materials, the concentration of free electrons and holes determine various electrical properties such as conductivity and junction capacitance. Introducing dopants into intrinsic semiconductors creates intermediate donor and acceptor energy levels, where electrons and holes can be easily thermally excited from these levels into the conduction or valence bands respectively. Because the donor and acceptor levels are close to the conduction and valence bands, Si at room temperature ( $\sim 25^\circ\text{C}$ ) is often assumed to be completely ionized, where, to first order, all of the electrons and holes in the donor and acceptor levels are excited into the conduction and valence bands, and the free electron and hole concentrations can be approximated as the doping concentrations ( $n \approx N_D$ ,  $p \approx N_A$ ). Equation (1) calculates the number of free carriers  $n$  and  $p$ , which is equivalent to the concentration of ionized donors and acceptors ( $N_D^+$  and  $N_A^-$ ).  $N_D$  and  $N_A$  are the concentration of donors and acceptors;  $E_F$  is the Fermi level;  $E_D$  and  $E_A$  are the donor and acceptor energy levels;  $kT$  is the Boltzmann constant-temperature product;  $g_A$  and  $g_D$  are the degeneracy factors [34].

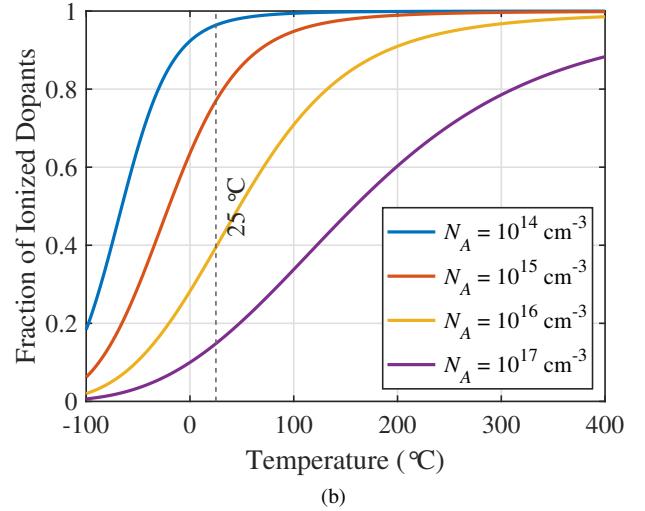
$$n = N_D^+ = \frac{N_D}{1 + g_D \times e^{\frac{E_F - E_D}{kT}} \times e^{\frac{-q\Psi}{kT}}}, \quad (1)$$

$$p = N_A^- = \frac{N_A}{1 + g_A \times e^{\frac{E_A - E_F}{kT}} \times e^{\frac{-q\Psi}{kT}}}$$

In WBG materials such as SiC, the donor and acceptor levels are much deeper within the bandgap. For 4H-SiC with a bandgap of 3.26 eV, acceptor ionization levels can be on the order of 200 meV to 350 meV above the valence band, requiring greater thermal energy for holes to transition to the valence band [34]. For example, in Fig. 1, when SiC is doped with a concentration of  $1 \times 10^{16} \text{ cm}^{-3}$  of Al, only 40% of the Al dopants are ionized at room temperature, while over 90% are ionized in Si. This effect is known as incomplete



(a)



(b)

Fig. 1. Fraction of ionized dopants for (a) Si and (b) 4H-SiC from  $-100^\circ\text{C}$  to  $400^\circ\text{C}$  for acceptor concentrations of  $1 \times 10^{14} \text{ cm}^{-3}$  (blue),  $1 \times 10^{15} \text{ cm}^{-3}$  (red),  $1 \times 10^{16} \text{ cm}^{-3}$  (yellow), and  $1 \times 10^{17} \text{ cm}^{-3}$  (purple). Both Si and SiC are doped with Al. For Si, the acceptor level is 72 meV above the valence band, and for SiC, the acceptor level is 200 meV above the valence band.

ionization. The term  $e^{-q\Psi/kT}$  is non-unity in the case where the electrostatic potential is non-zero, such as in the depletion region of a PN diode. In this case, the term becomes large enough that the denominator of Equation (1) approaches 1, and the dopants in the depletion region can be assumed to be fully ionized.

Furthermore, while the above analysis can determine the free carrier concentration, it is only valid in steady-state. As

discussed in [35], [36], quasi-static analysis is invalid if the excitation is on the order of the ionization time constant  $\tau$ , in which case a dynamic model is required. According to [36], the donors and acceptors are viewed as traps, where the rate of the capture and emission of electrons and holes can be represented by  $\tau$  and calculated by Equation (2), where  $e_p$  is the emission coefficient,  $N_v$  is the effective density of states in the valence band,  $v_{th}$  is the hole thermal velocity, and  $\sigma_p$  is the acceptor cross-section.

$$\tau_p = \frac{1}{e_p}, e_p = \frac{\sigma_p v_{th} N_v}{g_A} e^{-\frac{E_A - E_V}{kT}} \quad (2)$$

A simplified way of viewing  $\tau$  is the relaxation time constant for a dopant to ionize and release a free carrier in response to an excitation. For a complete ionization case such as room temperature Si, the ionization time constant is equal to 0.

In the example in Fig. 2, which depicts a PN junction excited by a reverse-biased pulse, the depletion region expands as the voltage increases. When considering transient

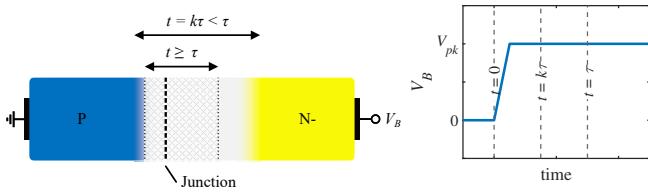


Fig. 2. Schematic of a PN junction depletion width over time when a reverse-bias step voltage is applied and incomplete ionization is considered. For the period less than the ionization time constant, the depletion region expands to a width greater than the steady-state value, as the dopants are not fully ionized to support the electric field.  $k$  is an arbitrary constant less than 1.  $\tau$  is the ionization time constant.

incomplete ionization, the depletion region starts at a greater width since the dopants cannot ionize in time to provide the charge to support the electric field. As the time approaches the ionization time constant, the depletion region shrinks to its steady-state width. This effect is crucial when considering junction capacitance and energy-related characteristics that heavily depend on depletion width, as quasi-static analysis of these values is no longer valid if the switching frequency is faster than the ionization time constant.

### B. SiC Device Structure

Vertical SiC power devices are composed of parallelized and repeated active cells, each of which can be viewed as a single switching device. Fig. 3 shows artist renderings of active cell cross-sections of a DMOS and a mixed PN-Schottky (MPS) diode. While the active region supports the electric field vertically, lateral support, especially along the edges of the die, is crucial as well. Hence, for vertical devices, a termination region surrounds the active cells. The termination gradually reduces the electric field towards the edges through an elongated PN junction. Two common types of termination structures in commercial SiC devices are the junction termination extension (JTE) and the floating guard ring (FGR) as shown in Fig. 3. In regards to switching behavior, the termination provides additional drain-to-source capacitance, and reports have shown

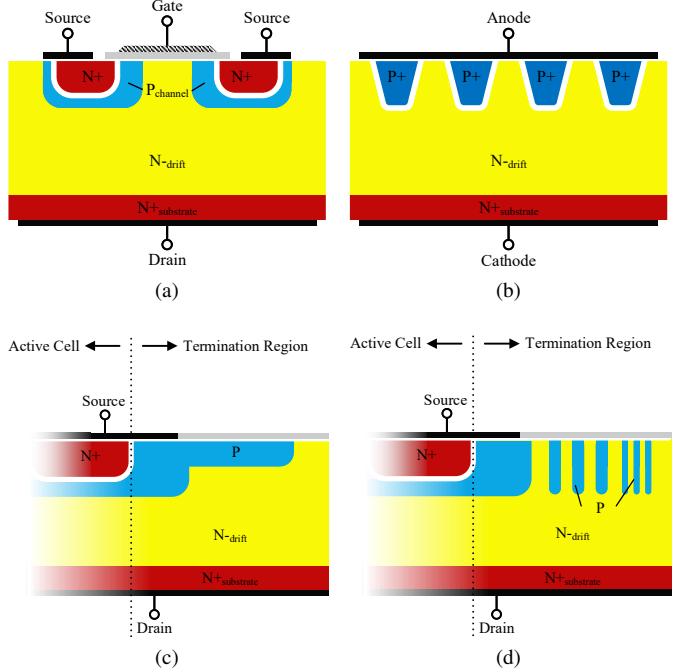


Fig. 3. (a) Cross-section of a vertical DMOSFET active cell. (b) Cross-section of an MPS diode active cell. (c) Cross-section of a generalized junction termination extension (JTE) structure. (d) Cross-section of a floating guard rings (FGR) termination structure.

that the termination contributes to additional current paths that increase turn-on losses by as much as 50% [37].

## III. METHODOLOGIES

This section discusses the simulation and measurement procedures, which include the small-signal measurement technique and various Sawyer-Tower measurement schemes used to capture large-signal charge-voltage behavior.

### A. Mixed-Mode Simulation

Mixed-Mode simulations consistently solve physical and circuit equations in a system combining SPICE elements and finite-element SiC structures. We employ Sentaurus®, a commercial technology computer-aided design (TCAD) software tool, for this purpose, where finite-element structures for the active cells and termination are generated by process simulation from ON Semiconductor. We utilize the default simulation parameters in Sentaurus® and Table I lists the detailed simulation parameters. Furthermore, [38] presents the cross-sections of the active region and termination of the 1200 V SiC device used in the simulation model for this work and notes the activated physical models, including electron mobility according to the Arora model, Fermi-Dirac statistics, and channel-mobility degradation. The transient mode solver deploys a coupled solution of Poisson's and electron and hole current continuity equations, excluding device self-heating. SPICE elements are also used to connect active cells and termination structures defined by their corresponding scaling factor, and excitations are provided by an ideal voltage source. Finally, the electrical waveforms and dissipated energies are

TABLE I  
LIST OF PHYSICAL SIMULATION PARAMETERS OF THE SiC DEVICE USED IN SENTAURUS<sup>®</sup> TCAD SIMULATIONS.

Parameter	Value
Temperature	300 K
$\epsilon_r$ (Relative Permittivity)	9.76
$E_g$ (300 K) (Bandgap at 300 K)	3.24 eV
$\mu_e$ (300 K) (Electron Low-Field Mobility at 300 K)	$\mu_e(300\text{ K}) = \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N_A + N_D}{N_v^{ref}})^{\alpha_v^\mu}},$ $\mu_{max} = 950 \text{ cm}^2/\text{Vs}, \mu_{min} = 40 \text{ cm}^2/\text{Vs},$ $N_v^{ref} = 1.94 \times 10^{17} \text{ cm}^{-3}, \alpha_v^\mu = 0.61$
$\mu_h$ (300 K) (Hole Low-Field Mobility at 300 K)	$\mu_h(300\text{ K}) = \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N_A + N_D}{N_v^{ref}})^{\alpha_v^\mu}},$ $\mu_{max} = 125 \text{ cm}^2/\text{Vs}, \mu_{min} = 15.9 \text{ cm}^2/\text{Vs},$ $N_v^{ref} = 1.76 \times 10^{19} \text{ cm}^{-3}, \alpha_v^\mu = 0.34$
P-Type Dopants	Aluminum
$\Delta E_A$ (P-Type Dopant Energy Level)	$\Delta E_A = \Delta E_0 - \alpha_A N_A^{1/3},$ $\Delta E_0 = 0.265 \text{ eV}, \alpha_A = 3.6 \times 10^{-8} \text{ eV cm}$
N-Type Dopants	Nitrogen on Hexagonal Site
$\Delta E_D$ (N-Type Dopant Energy Level)	$\Delta E_D = \Delta E_0 - \alpha_D N_D^{1/3},$ $\Delta E_0 = 0.0709 \text{ eV}, \alpha_D = 3.38 \times 10^{-8} \text{ eV cm}$

captured after a few cycles in order to avoid error induced by initial convergence issues.

### B. Small-signal $C_{oss}$ Measurement

The small-signal  $C_{oss}$  can be obtained from a network analyzer, which injects a small ac perturbation and obtains the device's equivalent impedance using voltage-current measurements. For this experiment, we utilized a Keysight E5061B network analyzer, which measures the small-signal impedance across a frequency bandwidth using the 1-port reflection method with calibrations of open, short, and  $50 \Omega$ . The measurement setup is schematized in Fig. 4a.  $V_{ac}$  represents the ac perturbation provided by the impedance analyzer and  $V_{dc}$  is the externally applied dc bias. Additionally,  $R_{block}$  serves to block  $i_{ac}$  from flowing to  $V_{dc}$ , preventing  $V_{dc}$  from affecting the ac small-signal measurement. We select  $R_{block}$  to be  $100 \text{ k}\Omega$ , which is three orders of magnitude larger than the impedance of a  $1 \text{ nF}$  capacitor at  $1 \text{ MHz}$ . For common commercial SiC devices, the  $C_{oss}$  typically can range from tens of pF to a few nF. Also, selecting  $R_{block}$  as  $100 \text{ k}\Omega$  does not limit the dc voltage sweep rate since the RC time constant for a  $1 \text{ nF}$   $C_{oss}$  is  $0.1 \text{ ms}$ . For our experiment, the dc voltage steps at an increment of  $0.1 \text{ V/s}$ . Since both  $C_{block}$  and the DUT restrict dc current from  $V_{dc}$ , any conduction loss through  $R_{block}$  is negligible as well.  $C_{block}$  serves as a dc block to protect the impedance analyzer from the large dc voltage across the  $C_{oss}$ . Fig. 4b shows an image of the testing setup and Table II lists the components used in the measurement setup.

### C. Conventional Sawyer-Tower Measurement

The Sawyer-Tower circuit obtains a charge-voltage curve of a capacitor for a charging half-cycle and a discharging half-cycle. The circuit has been utilized in [16], [17], [39] to characterize capacitor hysteresis in a variety of devices such

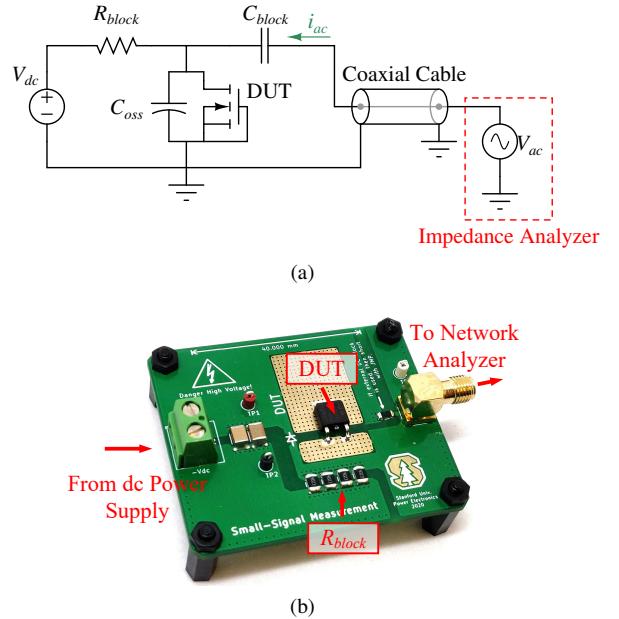


Fig. 4. (a) Schematic of the small-signal  $C_{oss}$  measurement circuit. (b) Photograph of small-signal measurement setup.

as Si SJ MOSFETs, GaN HEMTs, and SiC MOSFETs and diodes. As shown in Fig. 5, the Sawyer-Tower circuit utilizes a power amplifier to apply a large sinusoidal voltage across the series combination of the DUT and  $C_r$ . Because the DUT remains always off, the branch is equivalent to the  $C_{oss}$  in series with  $C_r$ . The anti-parallel diode only conducts for the first few cycles such that the minimum of  $V_d$  is  $0 \text{ V}$  in steady-state.  $C_d$  serves as a capacitor divider between the probe's internal capacitance such that the probe can be protected from measuring a large voltage. The value of  $C_d$  is  $1 \text{ pF}$  so that the power amplifier output is approximately ten times the mea-

TABLE II  
BILL OF MATERIALS FOR THE SMALL-SIGNAL MEASUREMENT CIRCUIT.

Component	P/N
dc Power Supply	TDK-Lambda GenH600-1.3
Network Analyzer	Keysight E5061B ENA Vector Network Analyzer
$R_{block}$	1 MΩ 0805 SMD Resistor
$C_{block}$	PE8250 Pasternack high-voltage dc block
Calibration Kit	Keysight 85052D Calibration Kit

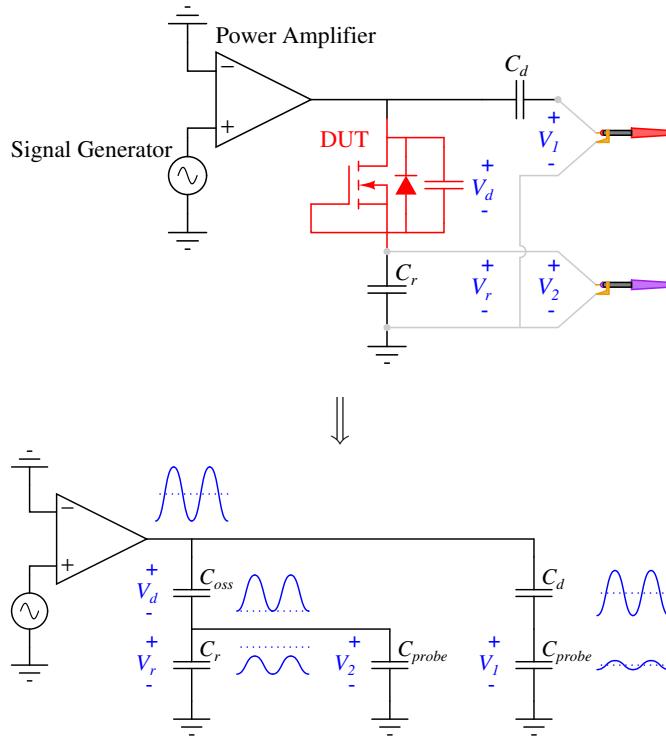


Fig. 5. Schematic of the Sawyer-Tower circuit showing the transformation to the equivalent circuit.

sured signal, as the probes' internal capacitance  $C_{probe}$  is on the order of 10 pF.  $C_r$  is a low-loss linear reference capacitor that is approximately five to ten times the value of the  $C_{oss}$  at 0 V. The reference capacitor tracks the instantaneous charge stored in the DUT through  $Q_d = C_r \times V_r$ , where  $V_r$  is directly measured by the second probe. The voltage across the DUT is extracted by  $V_d = V_1 \times (C_{probe} + C_d)/C_d - V_2$ . Fig. 6 shows an example charge-voltage curve extracted from the Sawyer-Tower circuit, where the area between the charging half-cycle and discharging half-cycle represents per cycle energy dissipation labeled as  $E_{diss}$ . As shown in Fig. 6, a capacitor with a parasitic resistor produces a charge-voltage hysteresis. For constant resistances, the hysteresis and equivalently the dissipated energy increases linearly with frequency [25], [40]. Accordingly, [18] is able to use simple RC networks to model the hysteresis behavior in Si SJ MOSFETs. Tab. III lists the equipment utilized in our setup as shown in Fig. 7.

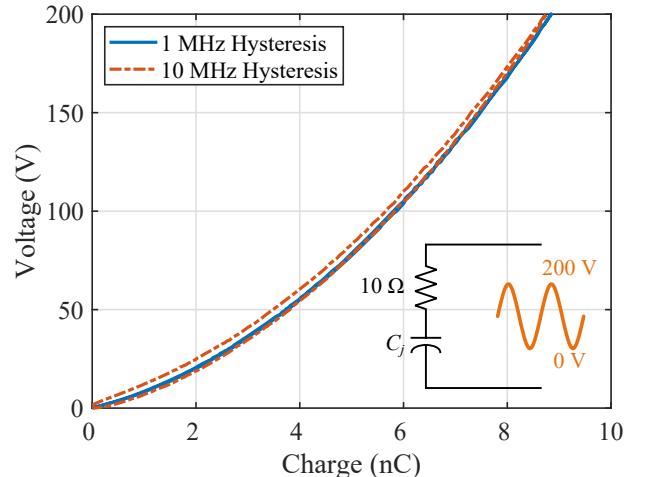


Fig. 6. QV hysteresis of an example RC structure at 1 MHz and 10 MHz as measured in the Sawyer-Tower circuit. As shown, the hysteresis increases with frequency and results from the  $RI^2$  dissipation.

TABLE III  
BILL OF MATERIALS FOR THE SAWYER-TOWER MEASUREMENT CIRCUIT

Component	P/N
Power Amplifier	ENI/E&I A1000 RF Power Amplifier (300 kHz to 35 MHz, 1 kW)
Oscilloscope	MSO9404A Mixed Signal Oscilloscope (4 GHz)
Oscilloscope Probes	Keysight N2875A 20 : 1, 500 MHz Passive Probe
Signal Generator	Keysight 81150A Pulse Function Arbitrary Noise Generator
$C_d$	1 pF, C0G capacitor

#### D. Half-Bridge Sawyer-Tower Measurement

The limitation with the original Sawyer-Tower measurement is that it can only obtain loss measurements for sinusoidal excitations. However, by replacing the power amplifier stage with a half-bridge network, similar data can be acquired for periodic trapezoidal voltages, which is more representative of waveforms in real converter applications such as the Class D power amplifier, resonant buck converter, or LLC converter. Bura et al. originally implemented this method to characterize hysteresis losses in GaN, SiC and Si SJ power devices.

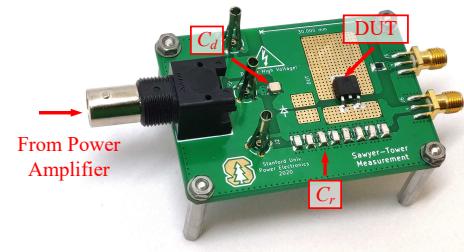


Fig. 7. Photograph of the experimental setup using the Sawyer-Tower circuit to measure charge-voltage hysteresis.

Fig. III-D illustrates the schematic of the half-bridge Sawyer-Tower measurement circuit.

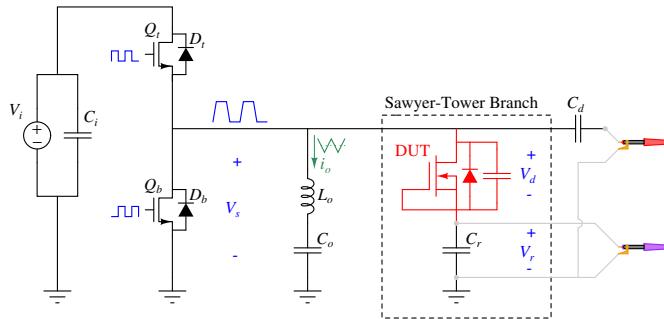


Fig. 8. Schematic of the half-bridge Sawyer-Tower circuit.

The half-bridge FETs drive the Sawyer-Tower branch which is in parallel with the resonant network containing  $L_o$  and  $C_o$ .  $L_o$  serves to control the peak-to-peak current  $i_o$ , which determines the  $dV/dt$  of the trapezoidal waveform. Equation (3) estimates the waveform's  $dV/dt$  based on the inductor value, where  $C_{eq}$  is the equivalent capacitance of the half-bridge FETs and the  $C_{oss}$  of the DUT.

$$\begin{aligned} dV/dt &= \frac{V_i}{\sqrt{L_o C_{eq}}} \times \left[ \sin^{-1} \left( \frac{V_i}{2\sqrt{\frac{L_o}{C_{eq}} I_o^2 + \frac{V_i^2}{4}}} \right) - \alpha + \frac{\pi}{2} \right], \\ \alpha &= \tan^{-1} \left( \frac{2I_o \sqrt{\frac{L_o}{C_{eq}}}}{V_i} \right), \\ I_o &\approx \frac{V_i}{8L_o f}, \\ C_{eq} &= 2C_{oss,HB} + C_{oss,DUT} \end{aligned} \quad (3)$$

An approximation can be made for  $I_o$  if the switch conduction time is close to half of the period. To set the dead-time of the half-bridge devices, we utilize an adjustable RCD dead-time circuit, using a trimmer potentiometer to tune the resistance. Since we operate the circuit at MHz frequencies,  $L_o$  is an air-core-wound inductor for inductance values under 20  $\mu$ H. For values above, the inductor is wound around a high-frequency ferrite toroid of 68 material from Fair-rite. Additionally,  $C_o$  is a large dc capacitor in order to maintain volt-second balance across  $L_o$  with the resonant frequency far below the switching frequency. Similar to the traditional Sawyer-Tower circuit, the series capacitance  $C_r$  tracks the instantaneous charge stored in the  $C_{oss}$ , and we probe the voltage across  $C_r$  and the  $C_{oss}$  to obtain the charge-voltage hysteresis. Fig. 9 shows an image of the testing setup and Table IV lists the part information of the components.

#### IV. $C_{oss}$ LOSSES RESULTS AND DISCUSSION

This section discusses the hypothesis and results from the measurements and pinpoints the behavior and origin of the soft-switching  $C_{oss}$  losses in SiC power devices. Table V lists the devices tested in this experiment. All measured and simulated devices in Table V are commercially-available.

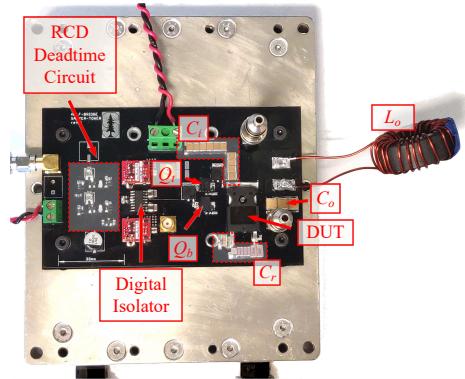


Fig. 9. Photograph of the half-bridge Sawyer-Tower setup.

TABLE IV  
BILL OF MATERIALS FOR THE HALF-BRIDGE SAWYER-TOWER MEASUREMENT CIRCUIT

Component	P/N
$Q_t, Q_b$	NV6117, 650 V, 120 m $\Omega$ GaN IC with integrated gate driver
$D_t, D_b$	STPSC406B, 650 V, 4 A SiC Schottky diode
$C_i$	C1812C104KDRAC7800, 0.1 $\mu$ F X7R capacitor $\times 30$
$L_o$	Air-core or 68 material toroidal inductor
$C_o$	2220Y1K00474KETWS2, 0.47 $\mu$ F X7R capacitor $\times 3$
dc-dc Supplies	NXE2S1215MC-R7, 15 V, 2 W isolated dc-dc converter
Digital Isolator	SI8275GB-IS1, 2.5 kV digital isolator

#### A. Variation with Voltage and Frequency

We begin by investigating the scaling of  $C_{oss}$  losses with frequency and voltage of a sinusoidal excitation. Previous works [25], [26] performed Sawyer-Tower measurements above 5 MHz for various commercial SiC devices and observed insignificant differences in energy dissipation across frequencies. However, these results are not studied outside

TABLE V  
LIST OF DEVICES MEASURED AND SIMULATED IN THIS EXPERIMENT

Properties	
Device A	SiC MOSFET, $R_{on} = 80 \text{ m}\Omega$ , $V_{bv} = 1200 \text{ V}$ , JTE termination
Device B	SiC MOSFET, $R_{on} = 80 \text{ m}\Omega$ , $V_{bv} = 1200 \text{ V}$ , FGR termination
Device C	Si PN Diode, $V_{fwd} = 1.15 \text{ V}$ , $V_{bv} = 1200 \text{ V}$ , JTE termination
Device D	SiC MPS Diode, $V_{fwd} = 1.45 \text{ V}$ , $V_{bv} = 650 \text{ V}$ , JTE termination
Device E	SiC MPS Diode, $V_{fwd} = 1.50 \text{ V}$ , $V_{bv} = 1700 \text{ V}$ , JTE termination

of the MHz regime. In this investigation, we measure and simulate the  $C_{oss}$  losses across a wider frequency range in the Sawyer-Tower circuit, extending to the kHz range as well. We analyze Device A, which is an  $80\text{ m}\Omega$ ,  $1200\text{ V}$  SiC MOSFET from ON Semiconductor with a JTE structure. For the frequency scaling, losses are measured and simulated from  $300\text{ kHz}$  to  $30\text{ MHz}$  in the Sawyer-Tower circuit with a  $400\text{ V}$  peak voltage. For the voltage scaling, the peak voltage of the sinusoidal waveform is stepped from  $50\text{ V}$  to  $600\text{ V}$  in  $50\text{ V}$  increments.

Fig. 10 displays the results from the experimental Sawyer-Tower measurements and TCAD simulations of Device A applied with similar voltage waveforms as in the Sawyer-Tower circuit. The TCAD simulations provide crucial insight into the loss mechanisms that the experiment is unable to capture. First, the Sawyer-Tower measurement only obtains the total losses in the device while TCAD can discern between the losses contributed by the termination and the active cells. Second, the simulation allows control over physical effects, where we can observe the loss behavior in the instance of ignoring incomplete ionization. It is also noteworthy that in Fig. 10, the loss trends match very well between simulation and experiment, with slight differences and offsets contributed by imperfect calibration of the TCAD model. Thus, the origins of the  $C_{oss}$  losses can be explained with an established understanding of device physics.

Based on Fig. 10, with incomplete ionization physics activated, the magnitude of the losses can be up to six times greater than the case of complete ionization. This behavior agrees with the theory discussed in Section II since it is well understood that in incomplete ionization, it is possible for fractional dopant activation to be as low as 10%. Since conductivity is proportional to ionized dopant concentration, the resistivity in the P-doped structures, such as the termination, will be higher as well.

Secondly, the frequency scaling of the losses is significantly different between the case of complete and incomplete ionization. For the complete ionization scenario, the  $C_{oss}$  losses increase linearly with both frequency and voltage. However, for incomplete ionization, the energy dissipation is nonlinear, where the loss saturates beyond  $5\text{ MHz}$ . The reason for this difference in behavior is attributed to the transient effects of incomplete ionization, where the rate of ionization cannot respond quickly to voltage excitations faster than the ionization time constant. Above  $5\text{ MHz}$ , it is highly likely that the ramp rate ( $1/2f$ ) of the Sawyer-Tower voltage swing is faster than the ionization time constant. This also indicates that the ionization time constant for this specific device in room temperature would be on the order of  $0.1\text{ ms}$ , which is a reasonable value for 4H-SiC with  $\sigma_p = 1 \times 10^{-15} \text{ cm}^2$  [36]. Furthermore, when analyzing the  $C_{oss}$  loss contribution from the termination and the active region, it is evident from Fig. 10 that the active region dissipates energy linearly across all frequencies while the termination energy loss decreases with frequency past  $5\text{ MHz}$ . The explanation for this behavior is the difference in structure and doping of the P-region. For the active area, the P-region is the P-channel of the DMOS, which is one hundred times greater doped than the

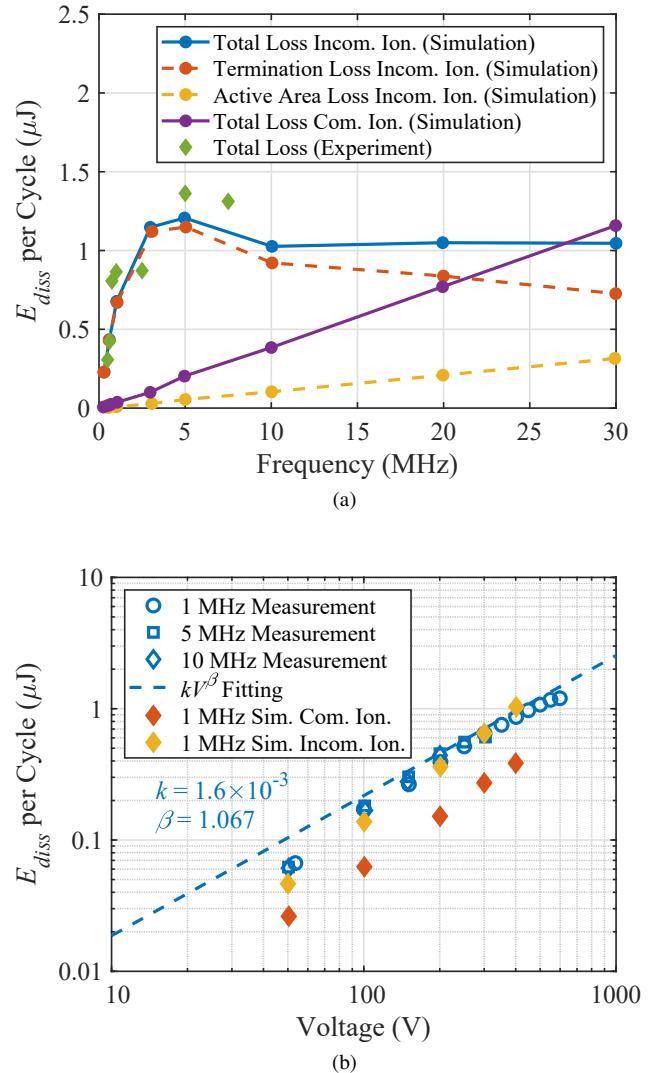


Fig. 10. (a) Energy dissipated per cycle versus frequency from simulation for the case of incomplete (blue) and complete ionization (purple). In the legend, Incom. Ion. stands for the incomplete ionization simulation condition and Com. Ion. stands for the complete ionization simulation condition. Experimentally measured  $E_{diss}$  is shown in green and is comparable to the incomplete ionization results. Additionally, for the case of incomplete ionization in the TCAD simulation, the losses are separated by the termination and active region contributions shown by the dashed lines. (b)  $E_{diss}$  vs. voltage in simulation and experiment. The results are fitted with an exponential function, where  $k$  and  $\beta$  are constants. The red and yellow diamonds correspond to the simulation results with incomplete ionization on and off respectively.

JTE's P-region and much thinner as well. This helps negate the effect of transient incomplete ionization in the active area as the probability of hole trapping decreases. For the termination, the  $C_{oss}$  losses decrease with frequency past the ionization time constant because the peak  $Q_{oss}$  decreases with frequency as will be explained in Section V. A reduction in  $Q_{oss}$  consequently lowers the charging and discharging current through the termination and, as a result, the conduction loss at the termination.

To compare with complete ionization, we experimentally measure the  $C_{oss}$  losses of a Si device. The device we select is Device C which is a  $1200\text{ V}$  standard recovery Si diode from ON Semiconductor. It is significant for the

Si device to be standard recovery rather than fast recovery since recombination centers are added in fast recovery diodes. Traditionally, recombination centers such as gold and platinum are incorporated into high-voltage devices in order to improve switching behavior and reduce reverse-recovery charge [41]. However, introducing these recombination centers also adds additional trapping energy states, which can produce the same effects as incomplete ionization [42]. Fig. 11 shows the measurement results for the Si diodes versus voltage and frequency and validates our explanation due to the approximate linear scaling of the energy dissipation with frequency.

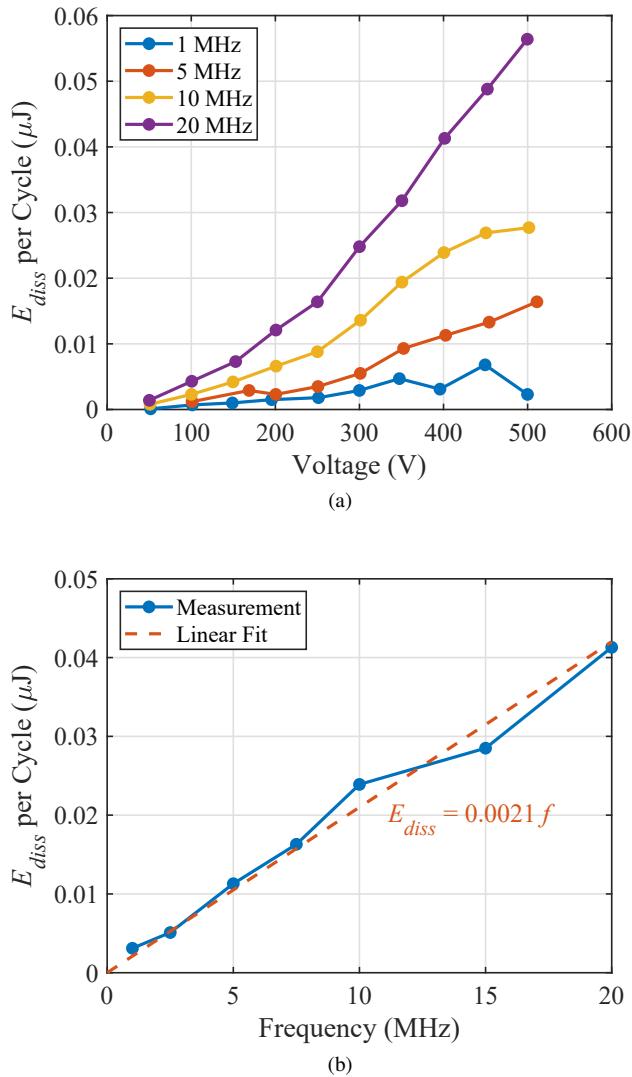


Fig. 11. (a) Measured energy dissipated per cycle vs. voltage for a Si diode (Device C) operating in the Sawyer-Tower circuit at 1, 5, 10, and 20 MHz. (b) Measured energy dissipated per cycle vs. frequency with a 400 V peak sinusoidal excitation.

The  $C_{oss}$  hysteresis for situations of complete ionization can be elucidated by a simple resistor-capacitor model. Shown in Fig. 12, the power device in off-state soft-switching conditions is equivalent to the  $C_{oss}$  in series with a constant resistor  $R_{oss}$ . The voltage excitation from the Sawyer-Tower circuit corresponds to an ac voltage source with value  $\frac{1}{2}V_{pk}(1 + \sin(2\pi ft))$ . While the actual Sawyer-Tower circuit contains a

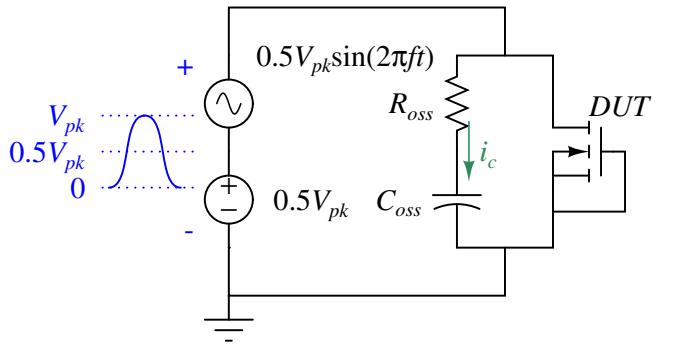


Fig. 12. Basic RC model of the  $C_{oss}$  loss in the Sawyer-Tower circuit. The power amplifier can be modeled as a sinusoidal voltage source swinging from 0 to  $V_{pk}$ . The device output capacitance is modeled as a single  $C_{oss}$  in series with an ESR labeled as  $R_{oss}$ .

series reference capacitor  $C_{ref}$ , we can consider it as a short as the value of  $C_{ref}$  is significantly larger than the  $C_{oss}$ .

To calculate the energy dissipated per cycle, we begin with two assumptions:

- 1) The voltage across the  $C_{oss}$ , which is  $V_c(t)$ , can be approximated as the voltage of the driving source as shown in Equation (4). This is valid if the impedance of  $R_{oss}$  is much smaller than the impedance of  $C_{oss}$ . For many power devices, the  $C_{oss}$  value typically ranges from 10 to 1000 pF, meaning that the impedance of the  $C_{oss}$  at 1 MHz would be on the order of 100  $\Omega$  to 10 k $\Omega$ . It is unreasonable for an  $R_{oss}$  value to be of the same order, since having parasitic resistances of this magnitude would make the devices unusable.
- 2) The nonlinear  $C_{oss}$  can be approximated using Equation (5), which is an equation for a voltage dependent junction capacitance.  $V_j$  is the built-in potential, which is typically around 1 V and is much smaller than  $V_R$  for high-voltage devices.  $C_{oss,0}$  is the capacitance value with no applied bias voltage.

$$V_c(t) \approx \frac{1}{2}V_{pk}\sin(2\pi ft) + \frac{1}{2}V_{pk} \quad (4)$$

$$C_{oss}(V_R) = \frac{C_{oss,0}}{\sqrt{V_R + V_j}} \approx \frac{C_{oss,0}}{\sqrt{V}} \quad (5)$$

$$i_c = C_{oss}(V_c) \times \frac{dV_c}{dt} \quad (6)$$

$$E_{diss} = \int_0^{\frac{1}{f}} R_{oss} \times i_c^2 dt \approx 2\pi^2 R_{oss} C_{oss,0}^2 V_{pk} f \quad (7)$$

We derive a formula for  $E_{diss}$  using Equation (7) by substituting  $i_c$  with Equation (6). To first-degree in the case of complete ionization, the losses for JTE-structured devices are linear with frequency and peak voltage, which matches the complete ionization and Si case. Furthermore,  $E_{diss}$  is proportional to  $R_{oss} C_{oss}^2$ , meaning that the  $E_{diss}$  of the active area is linear with the die area ( $A$ ) as well, since  $R_{oss} \propto 1/A$  and  $C_{oss} \propto A$ . The  $E_{diss}$  contribution from the termination is proportional to  $\sqrt{A}$ , since  $R_{oss} \propto 1/\sqrt{A}$  and  $C_{oss} \propto \sqrt{A}$  for the termination ring. These dependencies are explained in Fig. 13 which shows the physical representations of  $R_{oss}$  and  $C_{oss}$ . For the case

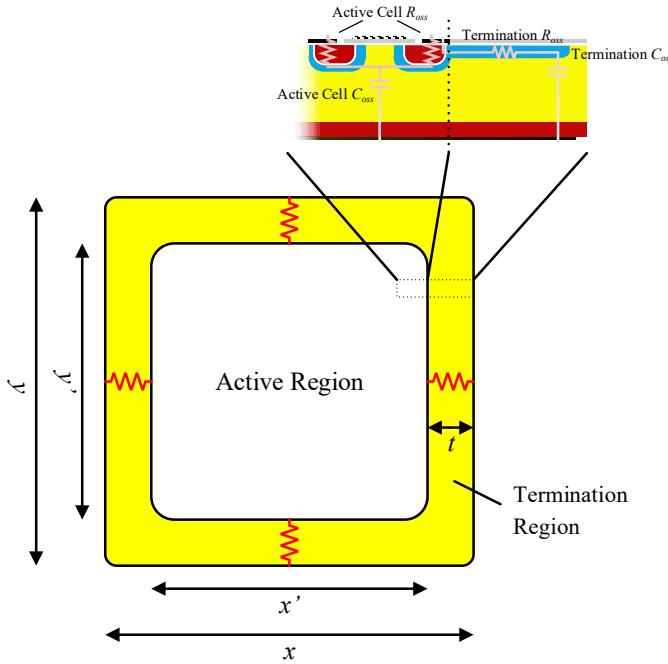


Fig. 13. Top-view of a power device die depicting the location of the equivalent  $R_{oss}$  and  $C_{oss}$ .  $x$ ,  $x'$ ,  $y$ , and  $y'$  are proportional to the square-root of the die area. Therefore, for the active region,  $R_{oss}$  and  $C_{oss}$  are related to the die area ( $A$ ). Since the termination current path is lateral,  $R_{oss}$  is dependent on the perimeter  $2(x+y)$  and roughly proportional to  $\sqrt{A}$ . The termination length  $t$  depends on the voltage rating of the device.

of incomplete ionization, the formula can be more difficult to analyze as  $R_{oss}$  and  $C_{oss}$  are both voltage and time-dependent, and transient effects need to be considered.

#### B. Variation with Active Cell and Termination Structure

As shown in Fig. 10, the loss in the termination dominates the loss from the active cell. This signifies that improvement and optimization of the termination structure are critical for the minimization of the  $C_{oss}$  losses. The previous results also suggest that the design of the active cell should not significantly alter the losses. To test this hypothesis, we measure Device D which is a SiC MPS diode from ON Semiconductor. ON Semiconductor has custom-fabricated variations of Device

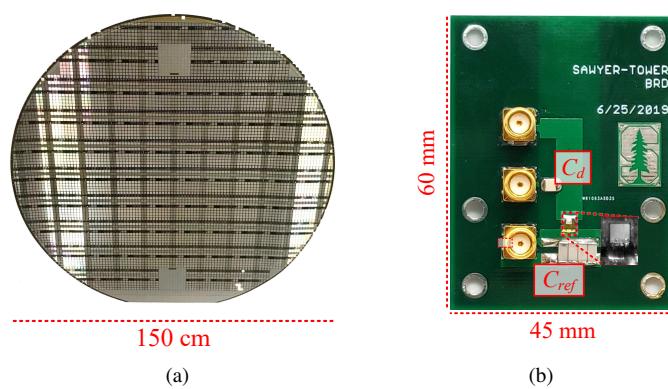


Fig. 14. (a) Image of the wafer with SiC diodes of various patterns. (b) Image of the Sawyer-Tower board containing the die and wire-bonds.

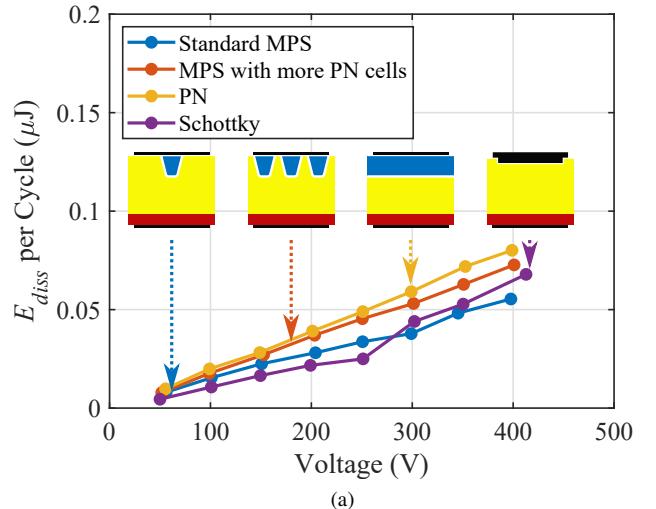


Fig. 15. (a)  $E_{diss}$  vs. voltage at 1 MHz for four different devices with the same termination structure and size but with differing active cell structures. (b)  $E_{diss}$  vs. voltage at 1 MHz for a PN diode with different termination lengths.

D with different active cell structures and JTE termination lengths. Fig. 14a shows the wafer which includes thirteen different combinations of cell structures and termination sizes. Since these devices are unpackaged, we measure them as bare dies in the Sawyer-Tower setup with the cathode side soldered onto the fixture PCB using a low temperature 180 °C solder paste and the anode wire-bonded to the board. Each gold wire bond is 1 mil in diameter and ten bonds are used per device to minimize the interconnect parasitics as shown in Fig. 14b.

To consider the loss behavior of the active cell, we test four dies having the same die area and termination lengths, but with different active cell types. In addition, we test three PN diodes with different termination sizes. The results in Fig. 15 show that the  $C_{oss}$  losses do not vary significantly with the active cell patterns but do greatly increase as the JTE termination lengthens. Thus, it is clear from simulation and experiment that the termination contributes to the majority portion of the energy dissipation.

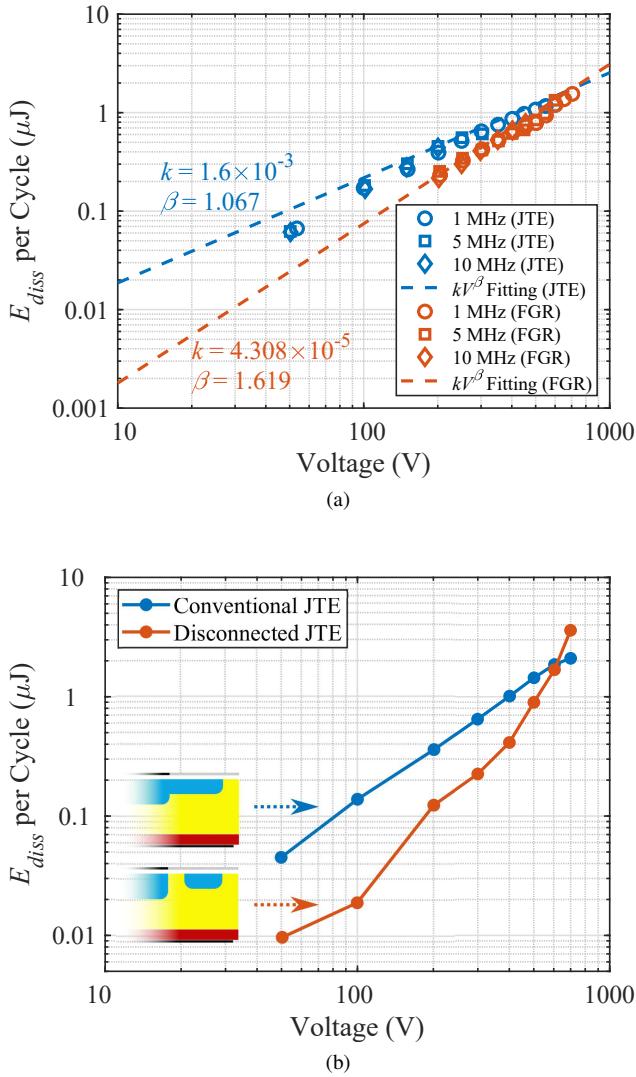


Fig. 16. (a) Comparison of measured energy dissipation vs. voltage between Device A and Device B. (b) Comparison of simulated energy dissipation vs. voltage between a Device A with JTE termination structure and Device A with a disconnected JTE structure, which is equivalent to an FGR termination with a single ring.

Secondly, we compare the scaling of the losses with different termination structures. Device B is a similarly rated SiC MOSFET compared to Device A, but with an FGR termination structure instead of JTE. The measurement results from the Sawyer-Tower circuit are shown in Fig. 16 including a frequency-independent Steinmetz fitting ( $kV^\beta$ ). Fig. 16b also compares in simulation the JTE and a disconnected JTE structure, which mimics a single-ring FGR termination. The results demonstrate the same trend as the measurement. At lower voltages, the JTE structure exhibits greater losses compared to the FGR structure, while the opposite occurs above 700 V. An explanation for this behavior is illustrated in Fig. 17. Considering the case of low voltage excitations, in the FGR cross-section, the depletion front extends only to the source implant, meaning that the current path for holes is shorter than that of the JTE, where holes must travel to and from the right-most edge of the JTE. However, when the

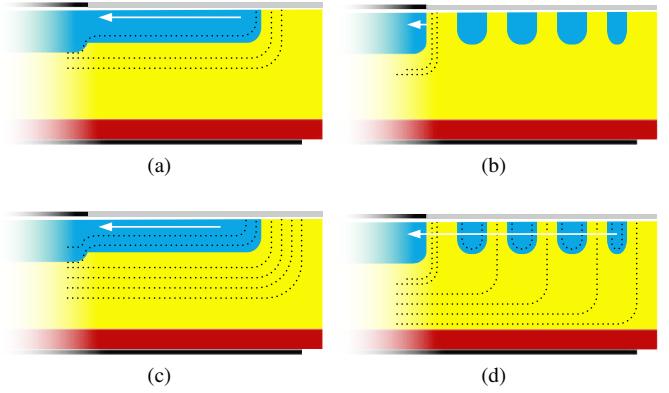


Fig. 17. (a) JTE termination with depletion front under low-voltage reverse-bias. The white arrow highlights the current path during discharging of the termination junction capacitance. (b) FGR termination with depletion front under low-voltage reverse-bias. (c) JTE termination under high-voltage reverse-bias. (d) FGR termination under high-voltage reverse-bias.

peak voltage increases, the depletion front extends through the guard rings, meaning the holes must travel the full distance to reach the farthest guard ring from the source, generating greater conduction losses.

### C. Variation with Waveform

There exists debate in the literature if the Sawyer-Tower circuit is a suitable measurement procedure to accurately characterize  $C_{oss}$  losses, with papers such as [20], [43] utilizing calorimetric soft-switching characterizations and claiming that the traditional Sawyer-Tower method does not accurately model soft-switching operation in a converter since the waveform imposed on the DUT is sinusoidal. While we agree that the traditional Sawyer-Tower circuit can be limited, a few converter topologies such as the Class E power amplifier establish half-sine waveforms across the switching device, in which case the Sawyer-Tower circuit can appropriately approximate the soft-switching  $C_{oss}$  losses in the device as demonstrated by [44]. For other converter topologies such as the Class D where waveforms are trapezoidal, the traditional Sawyer-Tower method is not applicable.

To investigate the impact of the waveform on the  $C_{oss}$  losses, we utilize the half-bridge Sawyer-Tower testing scheme which can control the  $dV/dt$  of the applied voltage. For this experiment, the peak voltage of the trapezoidal waveform is fixed, with one measurement set at 170 V and a second set at 600 V. The frequency of the trapezoidal waveform is 1 MHz and the  $dV/dt$  ranges from 1 V/ns to 30 V/ns. Fig. 18 presents the results which shows a close match between the experiment and TCAD simulation. The key aspect to note from Fig. 18 is that the  $E_{diss}$  saturates when the  $dV/dt$  increases beyond 20 V/ns. In the case of complete ionization, it is expected that an increase in  $dV/dt$  also increases the charging and discharging current through the  $C_{oss}$ , so the energy dissipation would scale with  $dV/dt$ . For incomplete ionization, the saturation of the  $E_{diss}$  with respect to  $dV/dt$  is equivalent to the  $E_{diss}$  saturation with respect to frequency in Subsection 10b. As the ramp rate of the electrical stimulus

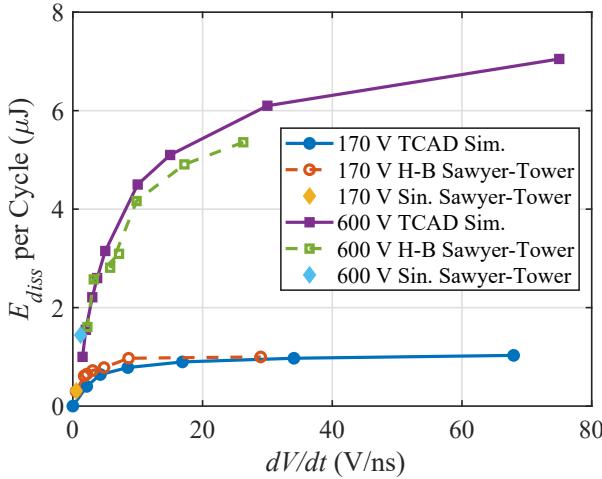
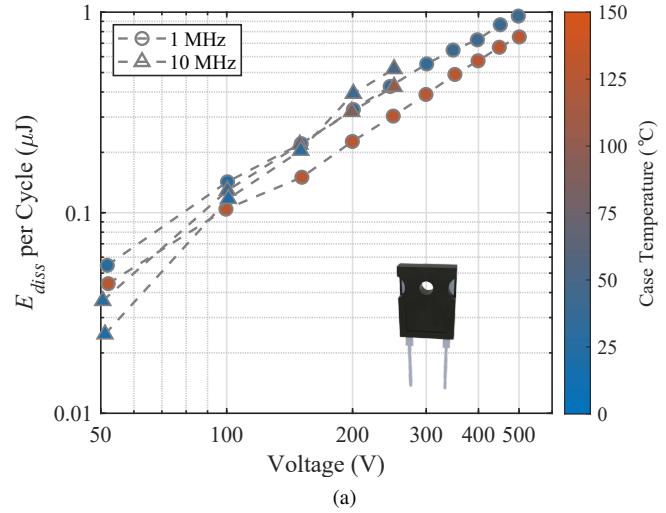


Fig. 18. Measured energy dissipation per cycle vs.  $dV/dt$  using the half-bridge Sawyer-Tower circuit using Device A. A periodic trapezoidal waveform of 1 MHz is applied across the device-under-test with a voltage amplitude of 170 V and 600 V.

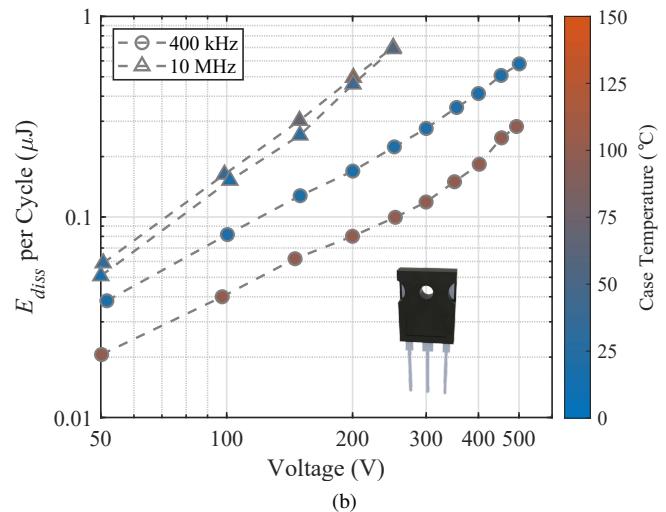
approaches and exceeds the ionization time constant  $\tau_p$ , the ionization and release of free carriers cannot follow the applied signal in time.

#### D. Variation with Temperature

Since the fraction of dopant ionization strongly depends on temperature, we study the  $C_{oss}$  losses of Device A and Device E at various temperature conditions. In our measurements, we can only obtain the case temperature since the devices are packaged. For standard Sawyer-Tower measurements, the device is placed in a room temperature environment, where no external heating or cooling elements affect the DUT and any additional temperature rise results from self-heating as  $E_{diss}$  increases. To increase the device temperature, a heat gun directs 100 °C air towards the DUT. To lower the temperature, the device is directly mounted onto a liquid-cooled cold plate set at 10 °C. All recorded temperatures are obtained using a FLIR A655SC thermal camera. For this experiment, we examine the temperature scaling at high frequencies beyond the ionization time-constant and low frequencies below the ionization time-constant with the results shown in Fig. 19. For both devices, at high frequencies, the  $C_{oss}$  losses are the same across temperatures. However, at low frequencies, the losses decrease with temperature. To explain this behavior, as the temperature increases, a larger concentration of dopants become ionized, resulting in increased conductivity throughout the P-regions in the JTE termination. Therefore, at low frequencies which resemble steady-state behavior, the conduction losses through the termination are lower at high temperatures. However, at high frequencies, when the frequency exceeds the ionization time constant, raising the temperature does not activate a greater concentration of dopants since ionization cannot occur quickly enough compared to the voltage perturbation. Hence, the  $C_{oss}$  and  $R_{oss}$  do not vary significantly with temperature.



(a)



(b)

Fig. 19. (a)  $E_{diss}$  vs. voltage at 1 MHz and 10 MHz for Device E in different temperature conditions. (b)  $E_{diss}$  vs. voltage at 400 kHz and 10 MHz for Device A in different temperature conditions.

## V. LARGE-SIGNAL AND SMALL-SIGNAL ANOMALIES

As previously stated, manufacturers' datasheets and SPICE models extract energy and charge storage in the  $C_{oss}$  based on small-signal parameters, which is only valid in circuit operation if transient and steady-state conditions are similar. When comparing the charge-voltage figures extracted from the Sawyer-Tower measurement, we observe that, other than the hysteresis, there exists a distinctive decrease in charge storage as the frequency of the sinusoidal excitation increases. In Fig. 20a, the charge in Device A's  $C_{oss}$  at 200 V is 53 nC for the 1 MHz measurement. However, at 5 MHz, the peak charge reduces to 49 nC and to 46 nC at 10 MHz. Moreover, we obtain the small-signal  $C_{oss}$  and integrate the result using Equation (8) to obtain the equivalent charge in quasi-static conditions.

$$Q_{oss} = \int_0^{V_{pk}} C_{oss} dV \quad (8)$$

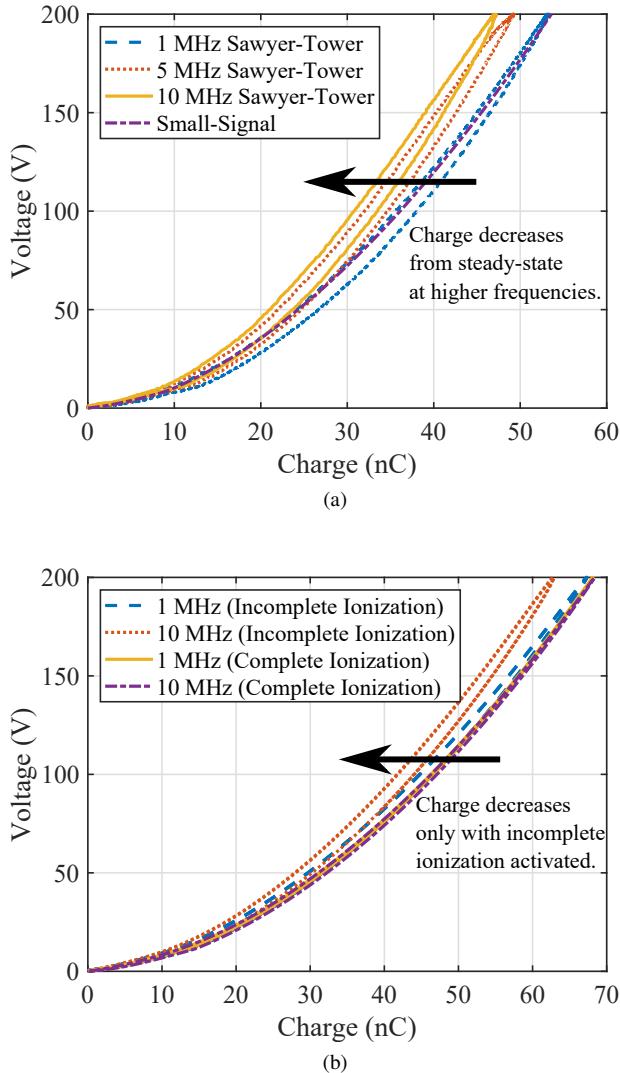


Fig. 20. (a) Comparison of charge-voltage behavior for a single cycle extracted from the Sawyer-Tower circuit at 1, 5, and 10 MHz and the small-signal measurement for Device A. (b) Simulated charge-voltage behavior at 1 MHz and 10 MHz for Device A with incomplete ionization and complete ionization.

This equivalent small-signal charge is also displayed in Fig. 20a. We observe that only the 1 MHz charge-voltage curve aligns with the small-signal measurement. To explain this behavior, in Section II for the case of a reverse-biased PN junction, the depletion region expands by ionizing neighboring layers of dopants. In the fast-charging case, when the frequency of the sinusoidal excitation is beyond the ionization time-constant, the P-dopants cannot ionize in time, leading to less free holes and causing the depletion width to spread wider as shown in Fig. 21a. However, when the charging process is slow (the voltage ramp rate is slower than the ionization time constant), the amount of ionized P-dopants is similar to the quasi-static scenario, and a thinner depletion width is achieved as shown in Fig. 21b. Thus, the difference in depletion widths results in a difference in equivalent  $C_{oss}$  capacitance in the termination and charge storage for the fast-charging and slow-charging cases. This explains why the stored charge is lower

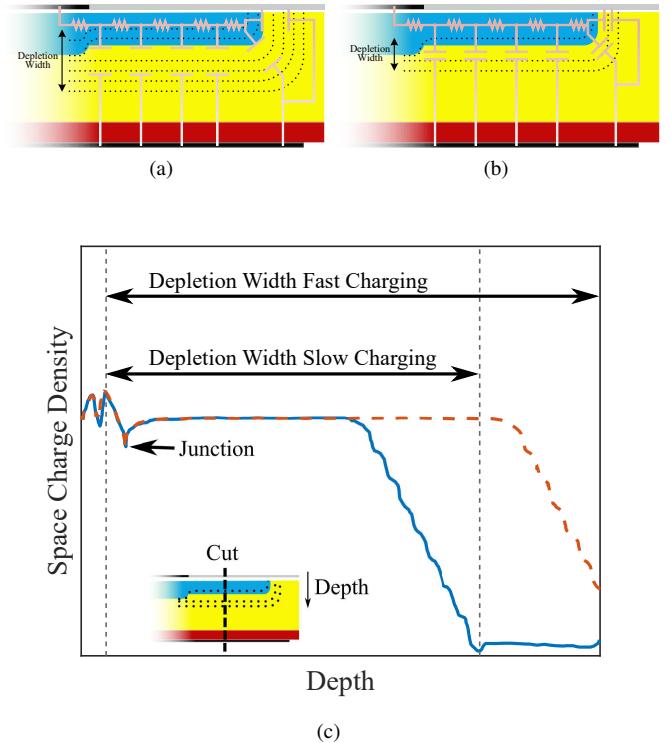


Fig. 21. (a) Diagram of the depletion region and equivalent circuit of the JTE termination in a fast-charging scenario. (b) Diagram of the depletion region and equivalent circuit of the JTE termination in a slow-charging scenario. (c) Space charge density vs. depth in a 1-D cut of the JTE termination for the slow-charging case (blue) and fast-charging case (dashed red). Specific values are not included in this figure due to proprietary information from ON Semiconductor.

at increased frequencies.

This presumption is further supported in mixed-mode TCAD simulations where we simulate Device A in a 200 V Sawyer-Tower circuit with both incomplete ionization physics activated and turned off. For the case of complete ionization as shown in Fig. 20b, both charge-voltage curves of 1 MHz and 10 MHz overlap. When incomplete ionization is activated in the model, we notice a significant shift in the charge, which matches the experimental measurements of Device A. Furthermore, Fig. 21c shows the space charge density of the 1-D cut-position in the middle of the JTE termination extracted from the incomplete ionization TCAD simulation. When comparing between fast-charging (10 MHz) and slow-charging (1 MHz) simulations, it is evident that the depletion width in the fast-charging condition is wider, justifying our hypothesis and explanation.

## VI. CONCLUSION

To summarize the findings in this paper, through Sentaurus<sup>®</sup> TCAD simulations supported by experimental measurements from the Sawyer-Tower circuit, the  $C_{oss}$  losses in SiC MOSFETs and diodes occur due to resistive power dissipation in the termination region. The variation of the losses with the excitation frequency,  $dV/dt$ , and device temperature results from incomplete ionization where experimental and simulation results are compared with and without incomplete ionization physics

activated in TCAD. Furthermore, incomplete ionization causes time-dependent charge storage in the device's output capacitance, which is a phenomenon unreported in datasheets and not modeled in SPICE models. We believe this work is the first to pinpoint the origins of the soft-switching  $C_{oss}$  losses in SiC power devices. Understanding and minimizing device losses is crucial for optimizing efficiency especially for popular applications using resonant bridge topologies around the 1 MHz regime as well as high-frequency applications such as 6.78 MHz wireless power transfer, where SiC diodes are often used in kW-level rectifiers. Additionally, we believe that this study can stimulate new and further research in device optimization, where potentially manufacturers can develop low  $C_{oss}$  loss termination structures. Lastly, this report highlights the value and need for improved analytical and SPICE models that capture the nonlinear behavior from incomplete ionization in the termination region during soft-switching operation.

#### ACKNOWLEDGMENT

This work is supported through the Stanford SystemX Alliance with ON Semiconductor. Zikang Tong is supported through the National Science Foundation Graduate Research Fellowship Program (NSF GRFP) and the Stanford Graduate Fellowship (SGF) as an Alcatel-Lucent fellow. In addition, we would like to thank Edith Pauline Prather for her assistance in wirebonding the test structure dies, Dennis Bura for discussion in the implementation of the half-bridge Sawyer-Tower measurement technique, Jia Zhuang for assistance on the small-signal measurement, and Grayson Zulauf for setting up the testing framework.

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