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Effect of Class 2 Ceramic Capacitor Variations on Switched Capacitor and Resonant Switched Capacitor Converters

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Abstract: **Class 2 ceramic capacitors, such as X7R, have relatively high energy density compared to Class 1 ceramic capacitors. However, they experience changes due to aging, temperature, and electric field. The measured X7R capacitance drop is 1-2% per decade hour due to aging, 18% due to a temperature change from 25°C to 125°C, and 75% due to an applied voltage that is 80% of the rated voltage. The measured equivalent series resistance (ESR) of the X7R capacitors show an increase of 20% to 70% due to aging of 1680 hours, and a 50% fluctuation in value when we apply 20% to 80% of the rated voltage. In switched capacitor (SC) and resonant switched capacitor (ReSC) converters, these variations can shift a converter's operating point and result in higher equivalent output resistance and lower efficiency. We quantified the converter performance degradation caused by capacitor variations in simulation and demonstrated the results by implementing a 1 MHz 25 W 1:4 Dickson ReSC converter. The converter efficiency decreases from 93.1% to 90.7% as a result of capacitor variations mainly due to aging effect.**

I. Introduction

Switched capacitor (SC) converters can achieve high power density in power electronics circuits because of their good utilization of high energy density capacitors. By adding a resonant inductor, resonant switched capacitor (ReSC) converters allow lossless charge transfer and operation with larger voltage swings across some of the capacitors [1]–[3]. As a result, ReSC converters achieve lower charge sharing loss and even higher power density than SC converters. The number of capacitors required in SC and ReSC converters depends on the voltage conversion ratio, and the performance of each capacitor in the circuit directly impacts the attainable efficiency of the entire converter. Therefore, to optimize the performance of these converters over their full life time, we need to have accurate predictions on the capacitor variations over time, temperature, and electric field.

Because of their high dielectric constant, Class 2 ceramic capacitors have high energy density, making them a popular choice for SC and ReSC converters [1]–[3]. In particular, X7R capacitors are often used due to their large nominal energy density, availability in a large capacitance range, and low cost. However, these capacitors are made of ferroelectric ceramic materials that are susceptible to aging, temperature dependencies, and electric field variations [4], [5]. These variations degrade SC and ReSC converter performance and change converter operating points over their lifetime, which presents a problem for applications where converters are expected to perform efficiently for many years. For example, converters used in photovoltaic applications are expected to remain operable for at least 10 years [6]. In practice, maintaining high efficiencies over the full converter lifetime may not be attainable due to many factors including degradation or failure of devices due to electrical and thermal stress, and variations in passives over long-term operation, such as capacitance variations.

To fully understand the effect of capacitor variations on SC and ReSC converter performance, we measured and modeled capacitor variation due to aging, temperature changes, and electric field and quantified their combined effects. Our findings show that existing capacitor models provided by manufacturers do not accurately predict measured results, and these capacitor variations result in an average of 5% and 20% more loss in an SC and ReSC converter, respectively.

This paper is based on our previous conference paper [7]. In addition, we present the equivalent series resistance (ESR) variation to incorporate the comments and feedback from the conference. Section II shows the measured capacitance and ESR variations. Section III presents a simulation model to predict capacitance variations based on the measured data. Section IV discusses the effect of capacitor variations on SC and ReSC converters and Section V demonstrates the effect using experimental results. Finally, Section VI concludes the paper.

II. Study on Capacitance and Equivalent Series Resistance Variation

In this section, we explore capacitance and ESR variations in Class 2 ceramic capacitors due to aging, temperature changes, and electric field. To understand the effect of aging on capacitors, we selected three sets of ten identical X7R capacitors in the same batch from different manufacturers (Table I). The aging effects in Class 2 ceramic capacitors can be reset if the capacitor is exposed to a temperature above the material's Curie point for an extended period [4]. To achieve adequate de-aging, capacitor manufacturers suggest to heat Class 2 ceramic capacitors to 150°C for more than one

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hour [8], [9]. Hence, we placed the capacitors we studied in a temperature controlled electric oven at 150°C for 1.5 hours to reset the aging effects. We then measured their capacitance values using an impedance analyzer (E5061B from Keysight Technologies, 10% accuracy [10]) twice every decade-hour for 3,000 hours.

Table I: List of capacitors used in this study. All capacitors are 100 nF, X7R in a SMD 1812 package.

Part #	Mfr.
18121C104KAT2A	AVX
VJ1812Y104KBBAT4X	Vishay
C1812C104K1RACTU	KEMET

Figure 1 shows that the average capacitance decrease per decade hour we measured is 1-2% regardless of manufacturer. Although all the components measured were nominally 100 nF, we observed a 12% difference in initial capacitance independent of aging effects. This result emphasizes the need for better capacitor models, since a single datasheet curve cannot accurately capture capacitor behavior. Figure 2 shows the predicted X7R aging effect from various manufacturers [9], [11]–[15]. The average capacitance drop per decade hour is 1-3%, but the data vary significantly by manufacturer. Using the photovotaic application mentioned in Section I as an example of how capacitor aging affects a system, we predict that all X7R capacitors used in the circuit will decrease by 5-15% [9], [11]–[15] over a 100,000-hour operation. Unlike capacitance, ESR of these X7R capacitors does not show a linear decrease per decade hour. Instead, we observed an average increase of 40% in ESR values over the measured period (Figure 3).

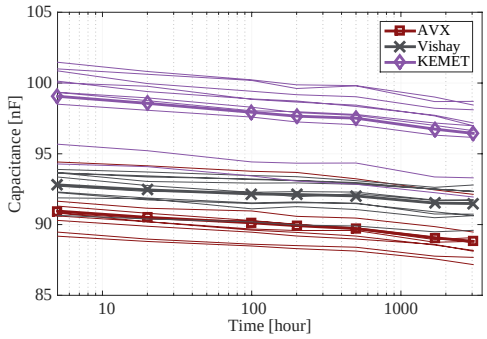

Figure 1: Measured X7R capacitance change over time from AVX, Vishay and KEMET. Average X7R capacitance decrease is 1-2% per decade hour. We measured 10 capacitors from each manufacturer at 1 MHz.

In addition to aging effects, capacitances of Class 2 ceramic capacitors have a nonlinear relationship with temperature and the well-known variation with applied voltage [4], [5]. Using the same X7R capacitors as in the aging study, we measured the capacitor variations due to changes in temperature and applied voltage. By sweeping the terminal dc voltage from 0 V to 80 V and measuring the capacitance from 25°C up to 125°C, we recorded variations and compared them with manufacturer-provided information (Figure 5, Figure 6, and

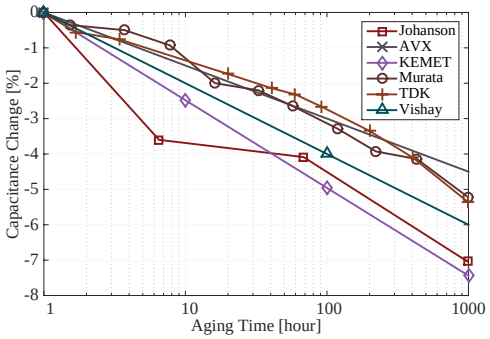

Figure 2: X7R capacitance change over time based on manufacturers' data. X7R capacitance drops 1-3% per decade hour according to these models.

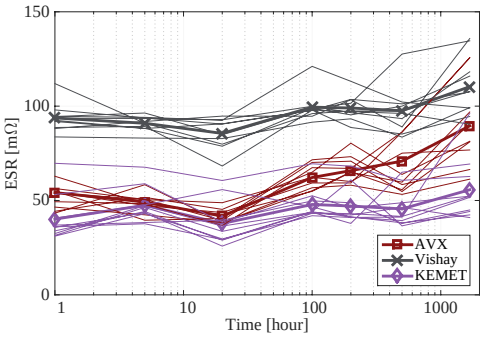

Figure 3: Measured X7R capacitor ESR change over time from AVX, Vishay, and KEMET. We measured 10 capacitors from each manufacturer at 1 MHz.

Figure 7). The test setup for measuring capacitor variation due to applied dc voltage is shown in Figure 4. Before measuring the capacitors (C_{DUT}), we first calibrated the impedance analyzer (E5061B) with the dc block attached (PE8250). After calibration, we connected the dc power supply across the capacitor through a 1 MΩ resistor. Then we increased the dc voltage and measured the corresponding capacitor values. The measured decrease in capacitance due to applied dc

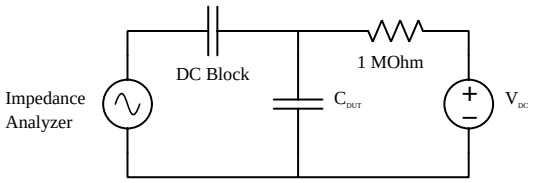

Figure 4: Circuit setup for measuring capacitance change with DC voltage.

voltage from 0 V to 80 V at room temperature is up to five times higher than the manufacturers report. When no dc voltage is applied, the maximum capacitance decrease due to a change in temperature from 25°C to 125°C is 18%. As the applied voltage increases, the effect of temperature on capacitance variations becomes less significant compared to the capacitance drop due to dc voltage.

Similarly, we measured ESR variations due to temperature

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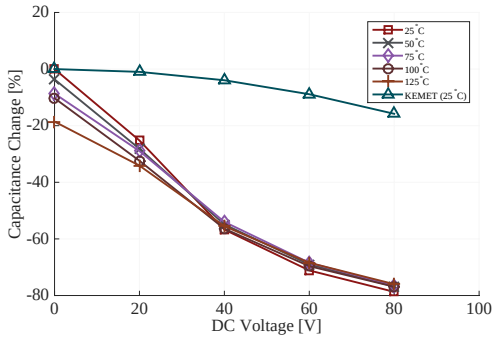

Figure 5: Measured KEMET X7R capacitance change at 1 MHz with applied DC voltage at 25°C steps from 25°C to 125°C compared to KEMET data at 25°C. The measured capacitors are C1812C104K1RACTU, which are 100 nF and rated for 100 V in SMD 1812 packages.

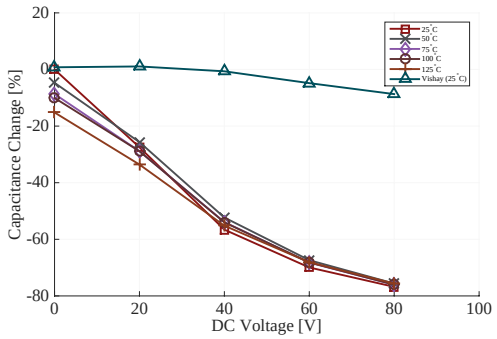

Figure 6: Measured Vishay X7R capacitance change at 1 MHz with applied DC voltage at 25°C steps from 25°C to 125°C compared to Vishay data at 25°C. The measured capacitors are VJ1812Y104KBBAT4X, which are 100 nF and rated for 100 V in SMD 1812 packages.

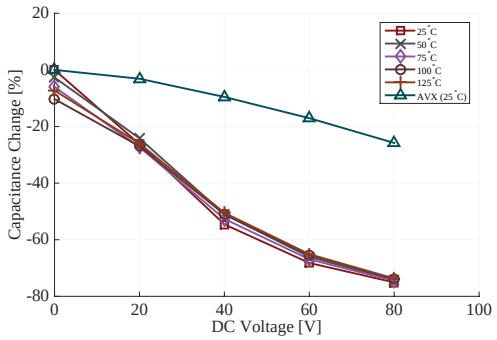

Figure 7: Measured AVX X7R capacitance change at 1 MHz with applied DC voltage at 25°C steps from 25°C to 125°C compared to AVX data at 25°C. The measured capacitors are 18121C104KAT2A, which are 100 nF and rated for 100 V in SMD 1812 packages.

and voltage (Figure 8). There are not many data from manufacturers on variations of capacitor ESR, although these variations can result in different power losses under different operating conditions. From Figure 8, we see that as the applied DC voltage increases from 0 V to 80 V, the average capacitor ESR fluctuates within 50% of its nominal value regardless of the temperature.

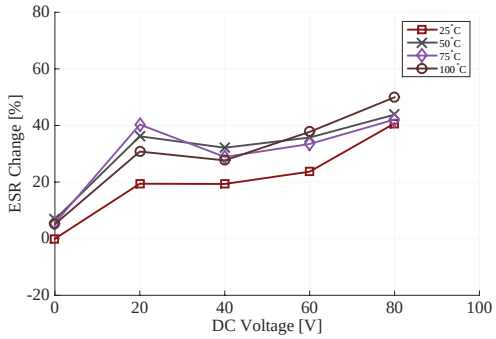

Figure 8: Measured average ESR change of X7R capacitors from all three manufacturers with applied DC voltage at 25°C steps from 25°C to 100°C at 1 MHz.

III. Capacitance Variation Modeling

To accurately predict capacitance variations due to aging, temperature, and voltage, we set up Monte Carlo simulations to model capacitance differences in discrete components based on the measured data from Section II. To use this simulation model, users must input the nominal capacitor value, voltage rating, length of operation (for aging), and operating temperature for each capacitor. Based on these inputs, the model computes the expected range of capacitance for each part, allowing for best and worst case converter performance predictions. Figure 9 illustrates the steps of generating this LTSpice simulation model using the measured capacitor data. The method we used to compute the possible capacitance range has two steps. First, we used Monte Carlo simulations based on uniform probability distribution to select initial capacitance values within 12% range around the user-defined capacitor value. This starting range is based on differences in the initial X7R capacitance measured in Section II (Figure 1). Next, a three dimensional look-up table takes the specified operating conditions (operation time, temperature, and applied voltage) and determines coefficients for each parameter.

To obtain the three dimensional look-up table, we used the measurement data to calculate the following coefficients: $Coeff_{Aging} = \frac{C_{Aging}}{C_{nom}}$, $Coeff_{Temperature} = \frac{C_{Temperature}}{C_{nom}}$, and $Coeff_{Voltage} = \frac{C_{Voltage}}{C_{nom}}$, where C_{nom} is the nominal capacitance value of all the capacitors, C_{Aging}, $C_{Temperature}$, and $C_{Voltage}$ are the average capacitance values under certain aging time, temperature, and applied voltage, respectively. Based on the measurement data for all three manufacturers, we found

$$Coeff_{Aging} = -0.003 \cdot ln(Hrs) + 0.9978,$$
$$Coeff_{Temperature} = 1 + Tc_1 \cdot (T-25) + Tc_2 \cdot (T-25)^2 + Tc_3 \cdot (T-25)^3 + Tc_4 \cdot (T-25)^4,$$

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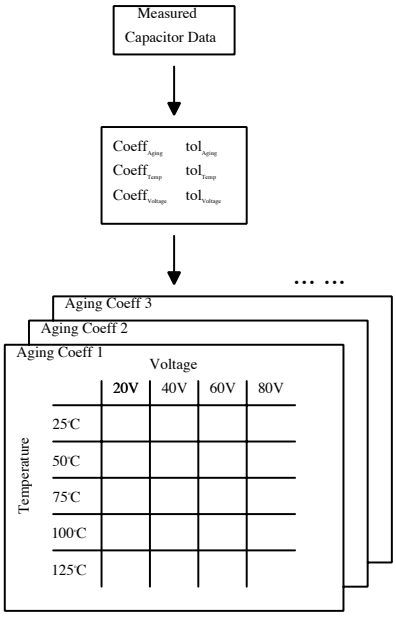

Figure 9: Flow chart describing the steps of obtaining the LTSpice simulation model. In each cell of the look-up table, we have a corresponding coefficient computed from the measured capacitor data, and a tolerance to represent the discrepancy among measured capacitors under the same condition.

where Tc_1 = 2.53e-3, Tc_2 = -1.94e-4, Tc_3 = 3.26e-6, Tc_4 = -1.76e-8, and T is temperature in °C.

To model the capacitance variation due to applied voltage, we calculated $Coeff_{Voltage}$ for 20 V, 40 V, 60 V, and 80 V separately and use interpolation to estimate capacitance values over the whole range of rated voltage. Based on the measurements, we get $Coeff_{20V}$ = 0.7411, $Coeff_{40V}$ = 0.4446, $Coeff_{60V}$ = 0.3037, $Coeff_{80V}$ = 0.2301.

Next, we calculated the ranges of possible capacitor values under each condition. tol_{Part} = 12% represents the differences in capacitor values at nominal conditions (room temperature when no voltage is applied). tol_{50C} = 2.897%, tol_{75C} = 4.303%, tol_{100C} = 3.756%, tol_{125C} = 12.13% represent possible discrepancies of capacitor values at different temperatures. tol_{20V} = 7.92%, tol_{40V} = 6.418%, tol_{60V} = 3.73%, tol_{80V} = 2.519% represent possible discrepancies of capacitor values under different voltages.

Finally, we set up the capacitor model in LTSpice using a behavioral source: *BIC N1 N2 i=ddt(V(N1)-V(N2))×Table(V(N1,N2))*, where Table(V(N1, N2) is generated based on the coefficients and tolerances calculated above. Under a certain operating condition (aging time, temperature, and voltage), the model finds the corresponding coefficients and tolerances and then uses Monte Carlo simulations to generate all possible capacitor values.

Figure 10 shows the range of capacitance values for discrete aging times. In the absence of temperature and dc voltage information, the simulation model could select any capacitance within the filled area that corresponds to a particular aging time. Similarly, Figure 11 shows the possible capacitance ranges for varying dc voltage and temperature. When all variations are considered for, the model computes the corresponding capacitance range based on all the user-defined parameters.

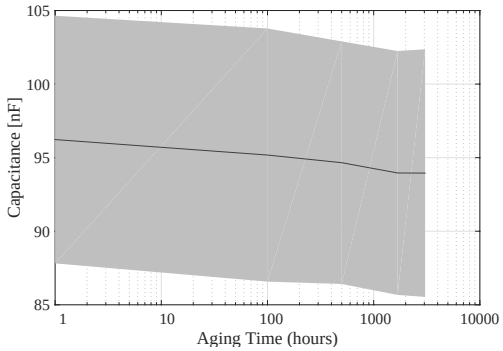

Figure 10: Possible capacitance ranges due to aging effects. The simulation model outputs ranges that correspond to the filled area for specific aging times.

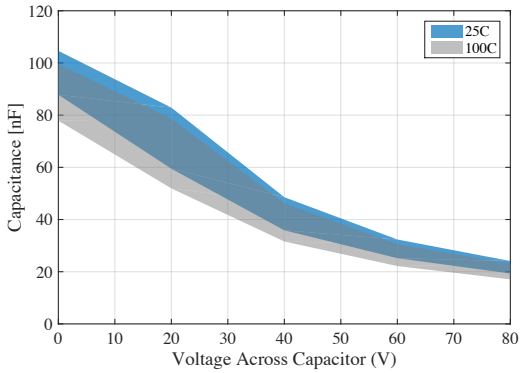

Figure 11: Modeled capacitance ranges at different DC voltages and temperatures. The filled areas show the ranges of all possible capacitor values at given voltage and temperature conditions.

IV. Effect on Switched Capacitor and Resonant Switched Capacitor Converters

The dc equivalent circuit model of an SC/ReSC converter [16] is shown in Figure 12. As the figure indicates, the converter's efficiency is inversely proportional to the equivalent output resistance (R_{eq}).

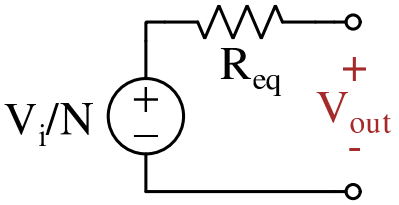

Figure 12: DC equivalent circuit model of an SC Converter. N is the nominal conversion ratio $\frac{V_{out}}{V_i}$ and R_{eq} is the equivalent output resistance.

An SC converter has two operating regimes: slow switching limit (SSL) and fast switching limit (FSL) [16]. When an SC converter is operating in SSL, its R_{eq} depends on capacitor values and the operating frequency [16]. Since converter efficiency is inversely proportional to R_{eq} (see the dc equivalent circuit model in Figure 12), maintaining a low R_{eq} is essential for high performance. However, the capacitance variations

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discussed in Section II have a detrimental effect on R_{eq} in the SSL. An alternative is to operate an SC converter in FSL. Figure 13 shows a plot of R_{eq} at different frequencies based on the circuit model from Figure 12. The plot indicates that R_{eq} of an SC converter can be minimized at high frequencies since it no longer depends on the capacitor values or operating frequency but instead on the switch on-resistance and ESR of the capacitors [16]. However, the circuit model shown in Figure 12 fails to account for switching and gating losses, which increase with frequency. As a result, many SC converters operate in SSL to obtain the best efficiency.

The addition of an inductor in ReSC converters allows for efficient charge re-distribution in the circuit. As a result, a ReSC converter achieves a low R_{eq}, which is comparable to an SC converter in FSL, but at a lower frequency to reduce switching and gating losses. Unlike an SC converter in FSL that has an R_{eq} independent of capacitance values, the minimum R_{eq} of a ReSC converter depends on the resonance created by the capacitors and the inductor, making it more sensitive to variations in frequency than an SC converter. Figure 13 shows the R_{eq} curve of both SC and ReSC converters. While the absolute minimum of the ReSC R_{eq} is due to the operation at resonant frequency, there are also local minima on the ReSC R_{eq} curve, which are caused by sub-harmonic operation at odd sub-multiples of the resonant frequency [17]. Figure 13 also shows an example of how a decrease in capacitance shifts the R_{eq} curves of both SC and ReSC converters to the right with respect to frequency, resulting in a larger R_{eq} and lower efficiency when operating at a fixed frequency.

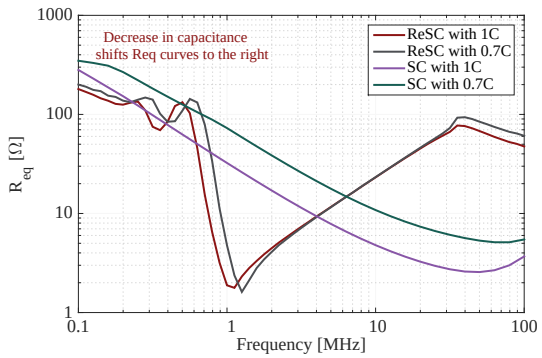

Figure 13: Equivalent output resistance (R_{eq}) of a 1:4 ReSC converter and a 1:4 SC converter. Reducing the capacitances by 30% results in a larger R_{eq} in both converters. Minimum R_{eq} of the ReSC converter is obtained at 1 MHz. Reducing the capacitances by 30% causes its Req to miss the minimum point at 1 MHz.

To quantify the effect of capacitance variations on SC and ReSC converter performance, we simulated a 1:4 Dickson SC (Figure 14) and a ReSC converter (Figure 15) using the capacitor model described in Section III. The nominal capacitor value is 100 nF and the rated voltage is 100 V for each resonant capacitor. As mentioned in Section II, capacitance variation due to temperature change is not significant when a dc voltage is applied. Therefore, we set the operating temperature to 25°C. Both converters have input voltages of 12.5 V and output power of 25 W. Table II lists the converter components used in the simulation. Both converters have the same components with the exception of the resonant inductor in the ReSC converter.

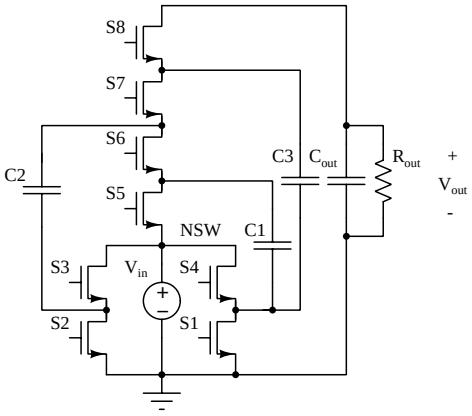

Figure 14: 1:4 Dickson SC converter.

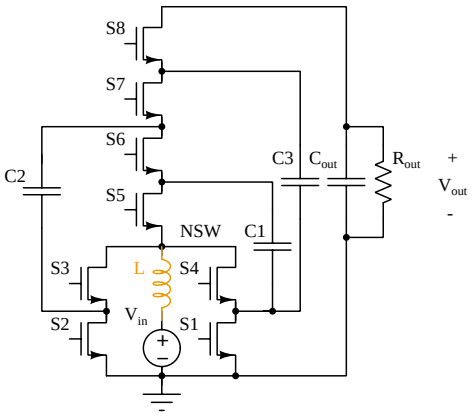

Figure 15: 1:4 Dickson ReSC converter.

Table II: Converter components

Component	Parameters
Resonant Inductor	200 nH (in ReSC converter only)
Resonant Capacitors	100 nF (×3)
Output Capacitor	100 nF
Output Resistor	100 Ω
Switches	EPC2010 & EPC2016
Gate Drivers	LM5113 & LM5114

Based on Figure 13 alone, the SC converter should be designed to operate at the boundary of SSL and FSL (30 MHz) to achieve maximum efficiency. However, as previously discussed, this high operating frequency leads to higher switching and gating losses in the switching devices. Figure 16 shows the efficiency plot of the SC converter using the EPC device models. Taking device switching losses into consideration, we see that as the frequency increases beyond 3 MHz, the efficiency drops significantly. Therefore, it is not practical to operate this SC converter at 30 MHz. Instead, we designed

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the SC converter to operate at 3 MHz, which results in the highest efficiency according to Figure 16. Using larger capacitors can lead to higher converter efficiency. However, since capacitance variations are related to capacitance densities [4], different capacitance values or package sizes result in different variations due to aging, temperature, and voltage. To make a fair comparison on the capacitance variation effect between an SC and a ReSC converter, we chose to use the same capacitors for both converters.

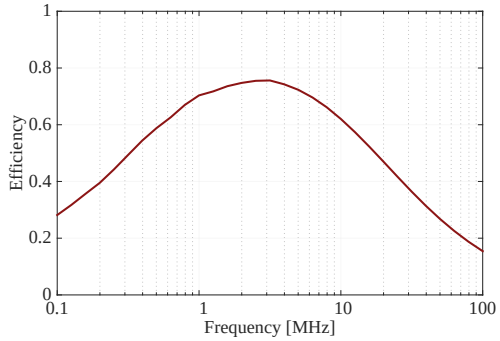

Figure 16: Efficiencies of the 1:4 Dickson SC converter at a range of operating frequencies. 3 MHz has the highest efficiency of 76%.

Since a ReSC converter achieves its lowest R_{eq} at a relatively low operating frequency, the converter operates most efficiently at this frequency even considering switching and gating losses. The efficiency plot of the ReSC converter in Figure 17 confirms that the converter achieves the maximum efficiency at 1 MHz, which is also the minimal R_{eq} point as shown in Figure 13.

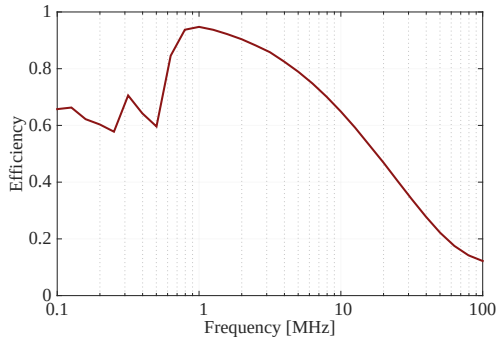

Figure 17: Efficiency plot of the 1:4 Dickson ReSC converter at a range of operating frequencies. The highest efficiency occurs at 1 MHz.

Using the capacitor model developed in Section III, we ran 100 Monte Carlo simulations of the SC/ReSC converters at different percentage capacitance drops due to combined effects of capacitance variations on a 100 nF nominal capacitor. Based on the simulation results, we compared the R_{eq} (Figure 18), efficiency and power loss (Figure 19) of the SC and ReSC converters including capacitance variations generated from the model at each operating point. The solid lines in the figures indicate the average converter performance and the filled areas show the entire performance ranges. From the figures, we see that the ReSC converter is more sensitive to capacitance variations, since these variations change the resonant frequency of the converter. As mentioned in Section II, converters used in photovoltaic applications should expect a capacitance drop of 5% to 15% in 100,000 hours. Figure 19 shows that a 5% to 15% capacitance drop in an SC converter leads to an average of 1% to 3% decrease in efficiency and 3% to 5% increase in total loss. In a ReSC converter, it results in an average of 1% to 4.5% decrease in converter efficiency and 7% to 20% increase in total loss.

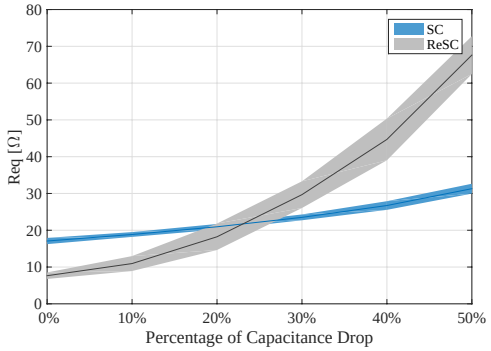

Figure 18: Simulated R_{eq} of the 1:4 Dickson SC and ReSC converters at different nominal capacitor values including capacitance variations. R_{eq} of the ReSC converter is more sensitive to capacitance changes than the SC converter.

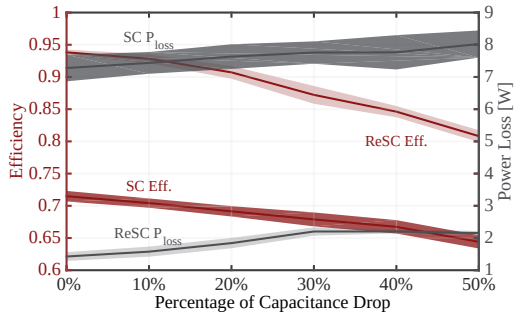

Figure 19: Simulated efficiency and total power loss of the 1:4 Dickson SC and ReSC converters at different nominal capacitor values including capacitance variations.

V. Experimental Results

Section IV revealed that ReSC converters show the most sensitivity to capacitance variations and are therefore the most relevant to study experimentally. To verify the performance degradation of a practical converter, we built the 1:4 Dickson ReSC converter designed in Section IV. We first tuned and tested the converter with KEMET capacitors (C1812C104K1RACTU) 10 hours after de-aging and re-tested 1,000 hours after de-aging. Figure 20 shows a picture of the PCB and Figure 21 shows the measured inductor current waveform at 1 MHz and 10 hours after de-aging. From Figure 21, we see that the inductor current has a shape of a rectified sine wave, which indicates that the ReSC converter is operating close to its resonant frequency.

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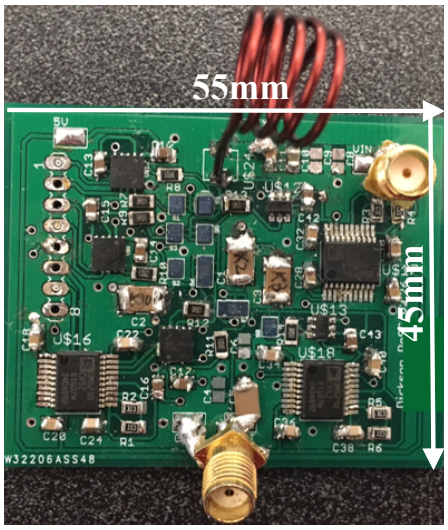

Figure 20: 1:4 Dickson ReSC converter PCB.

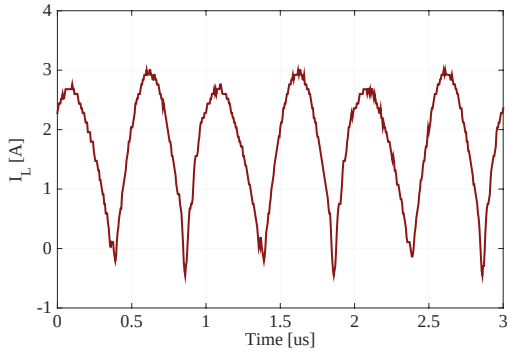

Figure 21: Measured inductor current waveform of the Dickson ReSC converter.

Table III shows the set of capacitance, efficiency, and total loss measurements taken on the converter. We observed a 2.4% drop in efficiency and 35% increase in total loss after 1,000 hours. These results indicate that even if the ReSC converter is tuned perfectly at the start of operation, considering the temperature and voltage effects on capacitance, the capacitors still experience variations due to aging that cause a significant drop in a converter's efficiency over its lifetime. Extrapolating the measured results, ReSC converters are predicted to have a 5% drop in efficiency and twice the total loss in a photovoltaic application at 100,000 hours. Besides aging effect, we mentioned in Section II that the capacitance variation due to applied dc voltage is much more significant than the manufacturers' models predict. Table IV compares the testing and simulation results on converter performance considering capacitance variation due to applied dc voltage using the manufacturer's capacitor model and the measured capacitance drop in Figure 5. From the table, we see that the simulation using the measured capacitor data leads to a better prediction of the actual converter performance.

Figure 22 shows the predictable range of converter efficiency and power loss using the simulation model, along with the measurement results. From the figure, we see that the model predicts the converter performance quite well but with slightly lower losses at 1000 hours. This is because the capacitor simulation model only captures the variations and losses of capacitors but not those of other circuit components.

Table III: Set of capacitance, efficiency, and total loss measurements at 10 and 1,000 hours.

Aging [hours]	$\mathbf{C_1}$ [nF]	$\mathbf{C_2}$ [nF]	$\mathbf{C_3}$ [nF]	$\mathbf{C_{out}}$ [nF]	η [%]	**Total Loss** [W]
10	101	98.8	94.6	100	93.1	1.59
1,000	98.7	96.3	92.3	97.7	90.7	2.15

Table IV: Comparison of the testing and simulation results on converter performance considering capacitance variation due to DC voltage using the manufacturer's capacitor model and the measured capacitor variation data

	η [%]	**Total Loss** [W]	$\mathbf{P_{out}}$ [W]
Testing Results	93.1	1.59	21.4
Sim - Manufacturer's Cap Model	94.7	1.37	24.4
Sim - Measured Cap Data	92.8	1.74	22.5

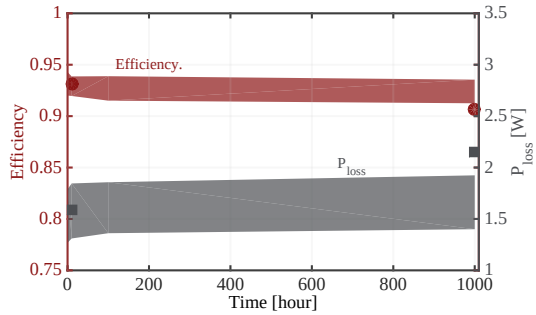

Figure 22: Simulated and measured efficiency and power loss of 1:4 Dickson ReSC converter. The red and grey areas show predicted range of efficiency and power loss using simulation models, respectively, at different capacitor aging time. The red dots and grey squares show measured efficiency and power loss, respectively, 10 hours and 1000 hours after de-aging the X7R capacitors.

One possible solution to minimize the effect of capacitor variation is to use Class 1 ceramic capacitors such as C0G. These capacitors have high stability over time, temperature, and electric field [18]. Figure 23 shows measured capacitance for ten C0G capacitors (KEMET C1812C104J1GACTU) over time after de-aging.

Compared to X7R capacitors, which have an average drop of 1-3% per decade hour, C0G capacitors remain nearly constant over time. However, one disadvantage of C0G capacitors is that they have significantly less capacitance per unit volume than X7R capacitors due to their low dielectric constant [19]. For example, the smallest commercially available packages for 100 nF X7R and C0G capacitors rated for 100 V are 0603 and 1206, respectively. Therefore, replacing X7R capacitors with C0G capacitors of the same capacitance values leads to a reduction in power density. On the other hand, in order to

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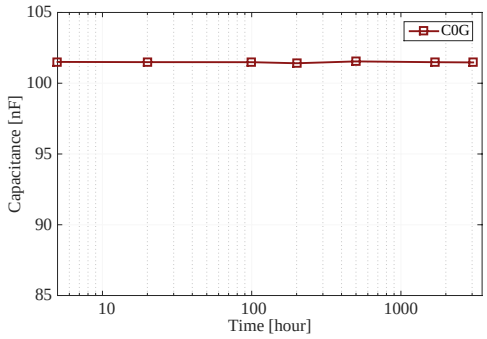

Figure 23: Measured average C0G capacitance change over time. We measured 10 capacitors at 1 MHz. These capacitors remain nearly constant.

achieve the same power density, C0G capacitors used in SC and ReSC converters have smaller capacitance values for the same package sizes as X7R capacitors. This leads to higher operating frequencies, and therefore, higher switching losses in converters. For example, if we replace 100 nF 0603 X7R capacitors with C0G capacitors of the same package size, the largest available capacitance value is 10 nF. Using the 10 nF C0G capacitors in the same ReSC converter results in a 3.6× larger switching frequency and an increase in gating loss from 0.82 W to 2.59 W.

VI. Conclusion

To achieve high power density in SC and ReSC converters, Class 2 ceramic capacitors are often used because of their high energy density. However, these capacitors suffer from capacitance and ESR variations due to aging, temperature, and electric field, which degrades converter performance. To quantify the effect of capacitor variations, we presented a simulation model to predict capacitor values under user-defined aging time, temperature, and applied voltage. Using this model in converter simulations, we were able to predict ranges of equivalent output resistance, efficiency, and total power loss accurately considering all causes for capacitance variations. Based on our findings, converter performance of a ReSC converter is more sensitive to capacitance variations than an SC converter. We demonstrated that the efficiency of a 1 MHz 25 W 1:4 Dickson ReSC converter drops from 93.1% to 90.7% due to capacitor variations.

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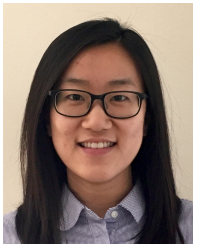

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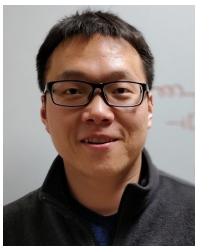

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