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A Wide-Input-Range High-Efficiency Step-down Power Factor Correction Converter Using Variable Frequency Multiplier Technique

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***Abstract*—This paper demonstrates a two-stage implementation of a step-down power factor preregulator design that achieves a high efficiency across the entire universal input voltage range ($85 - 265$ V_{rms}) for offline power supply application. In this implementation, a resonant LLC converter supplies power to a boost converter operating in continuous conduction mode. A variable frequency multiplier (VFX) technique is used in a resonant LLC converter stage to provide different dc gains and compress the effective input voltage range. The efficiency performance achieved is flatter and higher than other conventional off-line power converter design consisting of a boost power factor correction circuit followed by a resonant LLC converter, whose efficiency tends to drop significantly at low line input voltages. The proposed circuit allows MOSFETs with lower voltage ratings and better conduction/switching characteristics to be used in both converter stages. Both of the LLC stage and boost circuit can be better optimized due to the compressed operation range and better semiconductor switches. A scaling law of power losses versus breakdown voltage requirement for boost circuit under the condition of the same output power is presented. Experimental results demonstrated a flatter high efficiency performance across a wide input range.**

I. Introduction

Active power factor correction (PFC) along with the expectation of low distortion in the input ac-line is becoming more common in single-phase off-line power supply designs. Supplies operating with unity power factor utilize resources well, as no reactive power circulates through the power lines. In order to deliver power to the CPU, GPU, and other IC loads in telecommunication applications, a Distributed Power Architecture (DPA) is widely adopted in modern off-line supplies (Fig. 1).

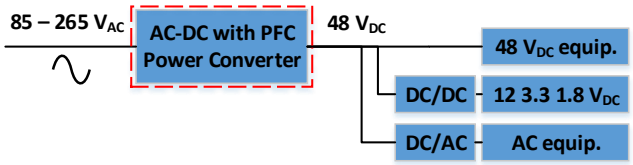

Fig. 1: Distributed power architecture

In most off-line DPA converters, the front end ac/dc stage transforms the typical 85-265 V_{rms}, 50/60 Hz single-phase input to a regulated, isolated dc bus voltage with nearly unity power factor. Fig. 2 shows a typical two-stage front-end ac/dc PFC supply which consists of a boost PFC circuit followed by an isolated series resonant dc-dc converter. This configuration is commonly used in various off-line power supplies [1]–[5]. A full bridge rectifier is placed at the front of the boost PFC stage to convert the 50/60 Hz input to rectified dc voltage. This assumption also holds for the rest of discussion in this paper. The universal ac line can vary in the range of 85 V_{rms} to 265 V_{rms}. As a result, the boost PFC circuit needs to convert the rectified sine wave to a dc voltage higher than the maximum input value, i. e., larger than 375 V. The capacitor C_{bulk} is placed at the boost output to smooth ac line power pulsations and to meet hold-up requirement specification. Moreover, a high frequency capacitor is connected in parallel to C_{bulk} to filter the high frequency ripple. This relative high dc-bus voltage leads to designs with silicon (Si) MOSFET and fast-recovery diode rated to a breakdown voltage $V_{BV} \geq 400$ V. In addition to the high V_{BV} requirement, the MOSFET and diode of the boost stage need a relatively large die area that can conduct a peak current (at low line) which can reach up to 3 times the peak of the high line current.

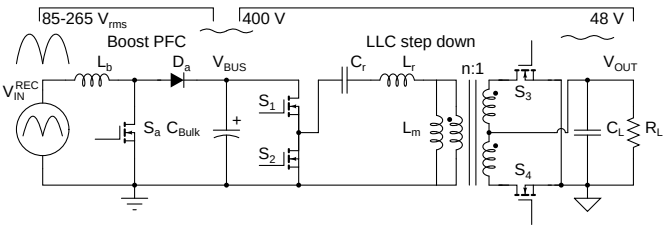

Fig. 2: Conventional two-stage step-down off-line supply design

At higher power levels, continuous conduction mode (CCM) operation is preferred in the boost circuit. However, at low line, the reverse-recovery loss of the diode as well as the MOSFET losses (both conduction and switching) increases with current. As a result, the low line efficiency tends to drop significantly compared to high line operation. Discontinuous conduction mode (DCM) can eliminate the reverse recovery charge in the diode as well as reduces MOSFET switching losses. However, this comes with increased core losses in the PFC inductor and current stresses on the MOSFET and diode. Hence, DCM PFC is preferred more at lower power levels. Nevertheless, the efficiency of a DCM PFC still drops significantly due to the increased conduction and core losses under low line

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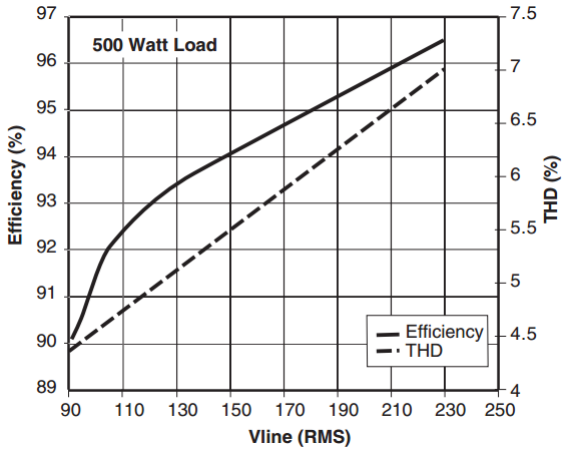
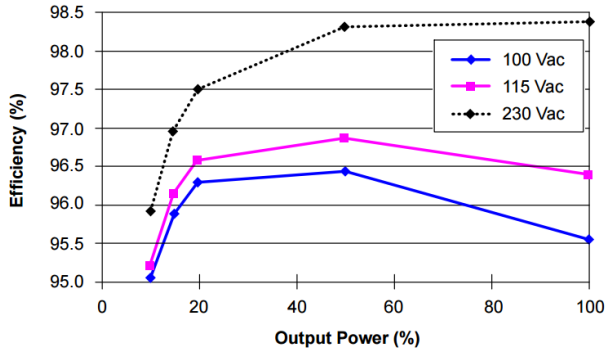


(a) Efficiency vs. V_{in} for a 500 W 400 V CCM boost PFC in [6]



(b) Efficiency vs. P_{out}, V_{in} for a 270 W 400 V FCCrM boost PFC in [7]

Fig. 3: Typical boost PFC efficiency performances, courtesy of On Semiconductor

conditions. Fig. 3 shows the typical efficiency of both a CCM and a Frequency Clamped Critical Conduction Mode (FCCrM) boost PFC converters [6], [7]. Notice the efficiency drops by 6% when V_{in} changes from 230 V_{rms} to 90 V_{rms} in the CCM case, and by 3% when V_{in} changes from 230 V_{rms} to 100 V_{rms} in the FCCrM case.

On the other hand, the low frequency capacitor, the PFC inductor, and the transformer are among the limiting factors to the volume reduction of converter shown in Fig 2. The buffer capacitor value C is determined by the energy pulsation ΔE and the specified voltage ripple ΔV. The relation is $\Delta E = CV_{\text{dc}} \cdot \Delta V$. Since the ripple voltage ΔV is typically limited to a few percent of the dc voltage V_{dc}, the bulky electrolytic capacitor is poorly utilized as only a fraction of the total energy $\frac{1}{2}CV_{\text{dc}}^2$ is utilized. Active Power Decoupling (APD) [8], [9] utilizes auxiliary circuit and extra buffer to store/release the low frequency energy and shift the power pulsations away from the dc bus. The capacitor volume can be reduced if significant ripple is allowed across its terminals.

A well-known way to reduce the size of the PFC inductor and isolation transformer is to increase the switching frequency of both the boost and the series resonant stages [10]–[12]. However, the large switching losses in Si MOSFETs and fast-recovery diodes are related to the need of devices with a high breakdown voltage that can also carry large currents in offline applications. This often limits the practical switching frequency to around 100 kHz at medium power levels.

Significant research efforts have been made to reduce the adverse effects of the MOSFET switching losses and diode reverse-recovery loss in boost rectifier during recent years. Many soft-switching boost circuits that use snubbers [13], [14] have been proposed to mitigate these losses and increase the switching frequency. Generally, an active snubber uses an auxiliary switch and other passive components to achieve soft switching on the boost MOSFET and diode. A passive snubber can also achieve soft switching but usually at a cost of increased voltage or current stress on the semiconductors [13]. The recent advances and commercial introduction of wide-band-gap (WBG) devices, e.g. GaN and SiC, are completely redefining the design and optimization of offline power supplies [15], [16]. The use of a SiC Schottky diode eliminates the reverse-recovery loss incurred by Si fast-recovery diode. GaN FETs have much lower gate charge and output charge compared with Si MOSFETs, which benefits high frequency operation significantly. However, the soft-switching achieved by the use of a passive/active snubber circuit is still necessary if the switching frequency needs to be increased furthermore to reduce the size of the boost inductor. Nevertheless, the cost and reliability figures of merit of WBG devices, including GaN and SiC, still need to be improved before they are widely adopted by all kinds of applications.

The techniques described above focus on mitigating the diode reverse-recovery loss as well as the MOSFET switching loss in the boost PFC circuit in Fig. 2. They either come with a higher cost, e.g., using WBG devices, or with an increase in design complexity, e.g., using active snubber to achieve soft switching. The fundamental reason behind these issues is that in the conventional ac/dc offline supply design in Fig. 2, due to the large variation of the $V_{\text{IN}}^{\text{REC}}$, the boost PFC circuit generates a dc bus voltage as high as 400 V. This gives a disadvantage in device stresses in both the boost stage and LLC primary side circuit, i.e., all the MOSFETs and diodes have to be rated for 400 V and able to accommodate the large current variation simultaneously.

This paper presents a different approach to solve the low-line efficiency drop in off-line supplies. The presented circuit is shown in Fig. 4. It does not comes with a much higher cost nor more complex circuit design. The proposed two-stage ac/dc supply consists of an LLC series resonant converter followed by a boost PFC circuit. The LLC series resonant converter uses the variable frequency multiplier (VFX) technique on the primary side to effectively compress the input voltage range by half [17]–[20]. Therefore, the efficiency of the entire converter would remain the same when the input voltage changes to half, as the loss components in two cases, for example $V_{\text{IN}} = 110$ V/220 V, are the same. By swapping the position of the LLC and boost stages, the LLC circuit first converts the rectified ac input to a smaller rectified sine wave $v_{\text{f}}(t) = V_{\text{f}}|\sin(\omega t)|$, then the boost converter provides PFC and regulation of the final output voltage V_{out}. V_{f} is regulated and smaller than V_{out} but close to it. Therefore, the switches in the boost circuit are only rated to V_{out} that is much smaller than 400 V and they do not require extra die area to accommodate

the large current variation occurred in conventional frond-end boost PFC in Fig. 2. With better conduction and switching characteristics of low-voltage semiconductor devices, the boost circuit in the proposed converter of Fig. 4 would be more efficient than the one in Fig. 2. In the end, the presented converter for off-line supplies in Fig. 4 can maintain higher efficiency over the entire universal input range than the conventional two-stage design in Fig. 2. This paper expands our work presented in [21] and presents an extended theoretical analysis and a more comprehensive set of experimental results.

The remainder of the paper is organized as follows. Section II introduces the operation of the presented converter. Section III explains the VFX technique used in the LLC circuit and how it adjusts the dc voltage conversion ratio depending on its input without affecting the efficiency. Section IV explains the constant power scaling law of boost circuit and the advantages of the proposed design over the conventional approach in details. Section V provides a simple control and regulation implementation. Experimental validations and details of a prototype converter appear in Section VI. Section VII concludes the paper.

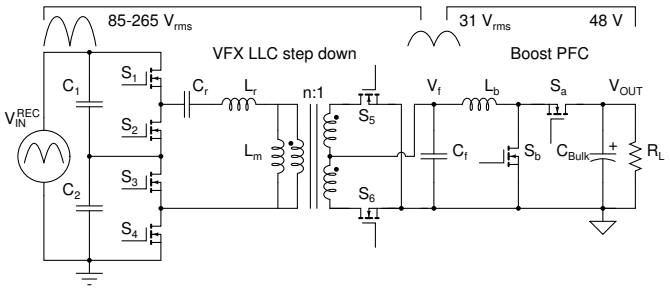


Fig. 4: Proposed two-stage ac/dc off-line converter with PFC

II. Converter Operation

The key idea of the proposed converter is to avoid the 400 $V_{\rm BUS}$ occurred in the conventional design. Instead of first boosting the rectified ac input $V_{\rm IN}^{\rm REC}$ to 400 $V_{\rm BUS}$ then down converting to final $V_{\rm OUT}$, the converter of Fig. 4 first converts the rectified sine input $V_{\rm IN}^{\rm REC}$ to a smaller ac voltage $v_{\rm f}(t) = V_{\rm f}|\sin(\omega t)|$ then boosts up to final $V_{\rm OUT}$. For example, if the desired $V_{\rm OUT}$ is 48 V, $V_{\rm f}$ should be smaller than this. The root-mean-square value of a sine wave with an amplitude of 48 V corresponds to 34 $\rm V_{rms}$. To leave a margin for the voltage ripple $\Delta V_{\rm OUT}$, $v_{\rm f}(t)$ can be regulated to 31 $\rm V_{rms}$ or lower.

In order to achieve PFC, the boost converter's current has to track the rectified sine wave $v_{\rm f}(t)$. By controlling the average boost inductor current, the boost converter will act as a fixed resistive load to the LLC stage during line cycle. Therefore, the average input current of the LLC stage will also resemble a rectified sine wave, which upon unfolding leads to a sinusoidal current at the input. Unlike the conventional design of Fig. 2, the LLC converter delivers a constant dc power $P_{\rm LLC}$, the LLC in the proposed converter delivers a pulsing power $2P_{\rm LLC}\sin^2(\omega t)$. Near the peak of the line input, the LLC delivers $2P_{\rm LLC}$ of instantaneous power, but delivering zero power when the input is at zero. The average power delivered over half of the line cycle by the LLC remains $P_{\rm LLC}$. $C_{\rm f}$ is a relatively small capacitor that only filters the high frequency ripple of the LLC and boost converters. The buffer capacitor $C_{\rm bulk}$ that smooths the low frequency power pulsations is connected at the output of the boost converter and provides filtering and hold-up.

In the conventional boost PFC front end, the input voltage $V_{\rm IN}^{\rm REC}$ can vary by 3 times within 85-265 $\rm V_{rms}$. Differently, the boost circuit in Fig. 4 is always driven by a constant voltage $v_{\rm f}(t) = V_{\rm f}|\sin(\omega t)|$, and the switching devices are rated for $V_{\rm OUT}$, which is much lower than 400 V. A Si Schottky diode that has no reverse recovery charge can be used to replace the fast-recovery diode. At certain power levels, a synchronous rectifier can also be implemented in order to reduce the conduction loss of a Schottky rectifier. The large variation of $V_{\rm IN}^{\rm REC}$ is shielded from this boost circuit and does not affect its efficiency. In the boost stage of the proposed circuit, the product of the switches' voltage and current rating only has to be a third of the value of a conventional front-end boost PFC converter.

However, now the LLC stage needs to convert a variable $V_{\rm IN}^{\rm REC}$ to a regulated $\rm V_f$. Generally, a LLC converter's efficiency would drop when the switching frequency is set far away from the resonant frequency. The switching losses would be insignificant in the circuit if ZVS is maintained across the whole input range. However, the efficiency will still drop as the conduction losses would increase with higher low-line current. The circulating losses would become larger as well when switching frequency moves away from the resonant point [22], [23]. If only the positions of boost and LLC circuits are swapped and the large input variation of the LLC stage is not taken care of, the efficiency of the presented off-line supply would still drop significantly under low line conditions. Therefore, to overcome this, a variable frequency multiplier (VFX) technique is applied to the primary inverter side of the LLC circuit.

III. Variable Frequency Multiplier

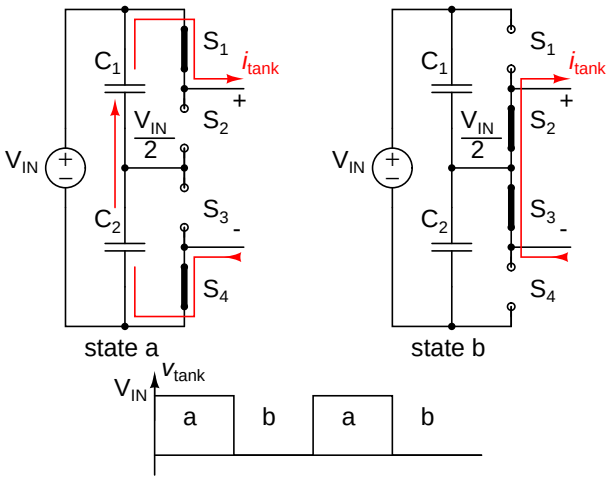
A frequency multiplier circuit is a dc-ac circuit where the frequency of the output signal is a harmonic component of the feed signal's frequency. For example, in a switched-mode RF power amplifier, if the gate-drive frequency is f_0, a resonant tank can be used to filter unwanted frequency components and only leave the signal component whose frequency is $\rm N$$f_0$ at the output [17], [18]. This technique is useful in a switched-mode RF power amplifier when the semiconductors' parasitics limit the maximum switching frequency of operation. In dc-dc resonant converters, this technique has been used to provide different operation modes and maintain a high efficiency performance over a wide operating range [19], [20]. Here, the limit in operating frequency is of no concern. The Variable Frequency Multiplier (VFX) technique is used to adjust the conversion ratio of the dc-dc converter depending on the input voltage. A 17 kW 750 V input LLC converter using this technique in [19] can generate three different output voltages (650 V, 325 V, and 163 V) with a similar efficiency.

[20] applies the VFX technique to a 20 V output dc-dc converter for an off-line power supply with no PFC. This 50 W off-line converter is able to maintain a flat efficiency across the entire universal line input range. We want to extend the VFX technique to a similar application but include capabilities of PFC for higher power level as shown in Fig. 4. Together with the advantages of using low-voltage devices, the efficiency of the presented two-stage PFC converter can be higher and flatter across the universal ac input range. This section explains the operation of VFX technique in a dc-dc converter.

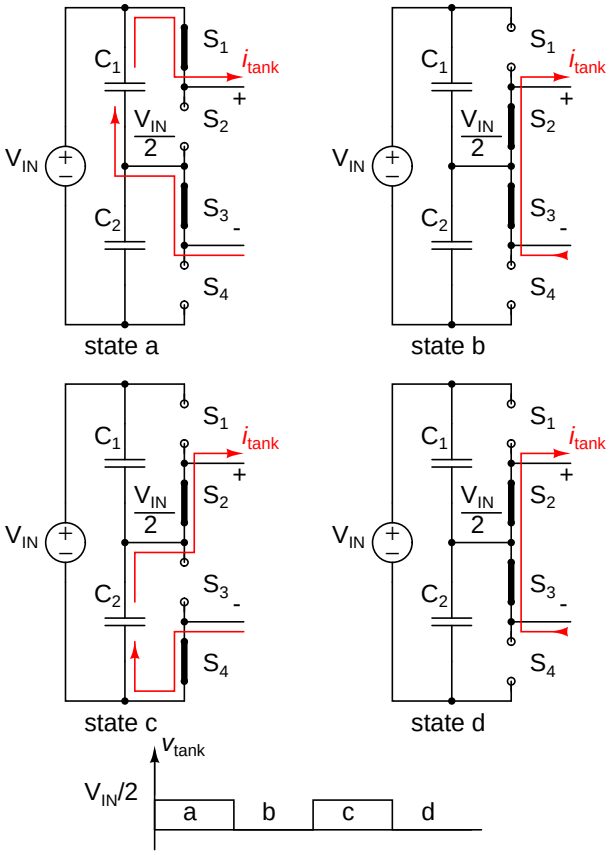
The key idea of this VFX technique is based on using a multi-level inverter circuit to generate the high frequency ac signal across the resonant tank in a dc-dc converter. The circuit shown in Fig. 4 uses a three-level inverter circuit with two operation modes. Possible switching states of this VFX LLC converter are shown in Fig. 5. However, unlike the conventional multilevel dc-ac converter [24] which uses all the different voltage levels simultaneously to reduce THD of ac output, the primary inverter of this VFX LLC converter operates with solely one of the two levels depending on the peak input voltage.

For example, when operating with the *full voltage swing mode* in Fig. 5a, the inverter will generates a square voltage swinging between 0 and 170 V, if V_{IN} is 170 V. On the other hand, if V_{IN} changes to 340 V, the system will use the *half voltage swing mode* instead. Under this condition (Fig. 5b), the voltages across C_1 and C_2 will be 170 V. Notice that the resulting square voltage in this mode will also have a 170 V swing. There are four switching states in the *half voltage swing mode*, the actual switching frequency of the MOSFET is half of the output frequency of $V_{\text{tank}}(t)$.

The advantage of using the VFX technique here is that when $\text{V}_{\text{IN}}^{\text{REC}}$ =110 V or 220 V_{rms}, by working under different modes, the LLC resonant tank operates with an almost constant voltage and current. Therefore, the losses in the LLC resonant tank, isolation transformer, and the diodes remain unchanged. Similarly, in both operating modes of the VFX converter, there are always two series connected switches carrying the tank current, and thus the losses in S_{1-4} remain the same either when $\text{V}_{\text{IN}}^{\text{REC}}$ = 110 V_{rms} or 220 V_{rms}. Therefore, the efficiency of the entire two-stage converter remains unchanged even though the input varies from $V_{\text{IN}}^{\text{REC}}$ to $2V_{\text{IN}}^{\text{REC}}$. This operating characteristic is beneficial in universal input off-line power converters that need to operate over an input voltage range that spans from 85 to 265 V_{rms}. Table I shows the operating conditions of the VFX converter over the universal input range. Furthermore, even the VFX LLC converter has to address the issues that come with an variable input voltage, the effective variation is compressed to half of the original case. The resonant tank only needs to provide an variable voltage gain from $\frac{95}{48} = 2$ to $\frac{190}{48} = 4$ rather than from $\frac{120}{48} = 2.5$ to $\frac{375}{48} = 7.8$. Two most common input voltages 120 V_{rms} and 230 V_{rms} ($\frac{230}{2} = 115$) can be both designed to be close to the optimum operating point near the resonant frequency.



(a) Full voltage swing mode



(b) Half voltage swing mode

Fig. 5: Switching states of a three-level half bridge inverter

IV. Constant Power Scaling of Boost Circuit

The other advantage of this proposed converter is allowing the usage of better semiconductor switches with lower voltage ratings. Table II compares the device stresses of the presented circuit of Fig. 4 and the conventional design of Fig 2 for off-line supplies in details. In a dc-dc converter, it has been demonstrated that using stacked or multi-level structures with low-voltage switching devices can improve the overall efficiency and power density performance [25]–

TABLE I: VFX MODE SELECTION

Mode	$V_{\text{IN}}^{\text{REC}}$	$V_{\text{IN,peak}}^{\text{REC}}$	$V_{\text{tank,peak}}$
Full voltage swing	85-134 V_{rms}	120-190 V	120-190 V
Half voltage swing	134-265 V_{rms}	190-375 V	95-188 V

[27]. For the LLC stage, as two stacked half bridge are used, S_{1-4} can use 200 V Si MOSFETs instead of 400 V in the conventional case. The specific on-resistance $R_{on,sp}$, which is the on-resistance per unit area, of high voltage ($\geq$ 100 V) Si MOSFET scales quadratically with breakdown voltage V_{BV} [28], i.e., $R_{on,sp} \propto V_{\text{BV}}^2$. Even though in the VFX LLC converter shown in Fig. 4, there are always two switches connected in series to carry the tank current, the total resistance are only $2 \times \left(\frac{200\text{ V}}{400\text{ V}}\right)^2 = \frac{1}{2}$ of the conventional case in Fig. 2, so is the total conduction loss.

TABLE II: DEVICE VOLTAGE STRESS COMPARISON

VFX LLC + Boost		
Device	**Voltage stress**	**Design value**
$S_{1,2,3,4}$	$V_{\text{IN,peak}}^{\text{REC}}$	200 V
$S_{5,6}$	$2V_{\text{f}}$	120 V
$S_{a,b}$	V_{OUT}	60 V
Boost + LLC		
Device	**Voltage stress**	**Design value**
S_a, D_a	V_{BUS}	400 V
$S_{1,2}$	V_{BUS}	400 V
$S_{3,4}$	$2V_{\text{OUT}}$	120 V

Comparing the boost PFC circuits in these two cases, if the final output voltage is 48 V, we can use 60 V MOSFETs and Schottky diodes in the proposed converter, while 400 V MOSFETs and fast-recovery diodes are required in the conventional design. However, the current increases proportionally as the voltage decreases in order to deliver constant output power. A detail discussion on the scaling of boost converter's efficiency versus the breakdown voltage of the Si uni-polar devices is presented as follows.

For a boost PFC circuit operating with voltage within 10s to 100s of volts, the dominant loss components in the circuit are shown in Fig. 6. Assuming the converter operates in CCM, the inductor current ripple is small, and magnetic core losses can be neglected. Here, the major loss in the inductor is due to conduction. The low-side switch has both conduction and switching losses. The high-side switch has natural zero voltage switching, so the conduction loss dominates. For a low-voltage-high-current boost circuit, using a synchronous rectifier could reduce the conduction losses compared with using a Schottky diode rectifier under certain conditions.

For this analysis of scaling of power losses versus switching devices' voltage rating, we first assume the same transistor structure is used for the MOSFET with different ratings. In reality, to get the best performance, different transistor structures are adopted in Si power MOSFET with different V_{BV} requirements. Later we will discuss what the practical

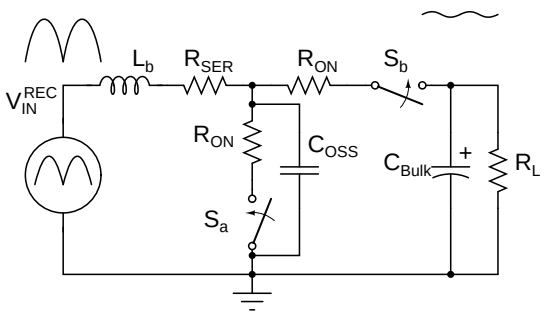


Fig. 6: Boost circuit loss model

dependence of $R_{on,sp}$ on V_{BV} is and how this affects the conclusion we can draw.

Assume the ideal on-resistance R_{on} scales linearly with breakdown voltage V_{BV}, and is inversely proportional to the die area A,

$$R_{on} = \frac{R_{on,sp}}{A} \propto \frac{V_{\text{BV}}}{A} \tag{1}$$

$R_{on,sp}$ is the unit area resistance for Si MOSFET.

The output capacitance C_{oss} is proportional to the die area A. To simplify the analysis, assume it is independent on V_{BV},

$$C_{oss} \propto A \tag{2}$$

If the output power of the boost circuit is kept constant, the voltage is scaled down by k times and the current is scaled up by k times,

$$V \to \frac{V}{k}, I \to kI \tag{3}$$

Then, MOSFET rated to $\frac{V_{\text{BV}}}{k}$ can be used in the low voltage case, but also larger die area is needed to carry the increased current. If the die area is increased by k times,

$$R_{on,sp} \to \frac{R_{on,sp}}{k}, A \to kA \tag{4}$$

Correspondingly, the on-resistance and output capacitance of the low voltage MOSFETs used are

$$\begin{aligned} R_{on} = \frac{R_{on,sp}}{A} \to & \frac{\frac{R_{on,sp}}{k}}{kA} = \frac{R_{on}}{k^2}, \\ C_{oss} \to & kC_{oss} \end{aligned} \tag{5}$$

The conduction loss is the same as high-voltage case,

$$I^2 R_{on} \to (kI)^2 \frac{R_{on}}{k^2} = I^2 R_{on} \tag{6}$$

The switching loss due to output capacitance becomes k times smaller,

$$f_s C_{oss} V^2 \to f_s (kC_{oss})(\frac{V}{k})^2 = \frac{1}{k} f_s C_{oss} V^2 \tag{7}$$

The switching loss due to MOSFET voltage and current overlap during turn-on/off transitions becomes

$$\frac{1}{2} VI(t_{rise} + t_{fall}) f_s \to \frac{1}{2} VI(t'_{rise} + t'_{fall}) f_s \tag{8}$$

If the new rise/fall time t'_{rise}, t'_{fall} are the same as the high-voltage case, the overlap loss does not change. To first order

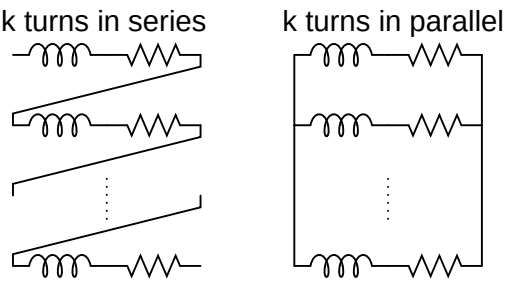


Fig. 7: Illustrative boost inductor winding structure for high-voltage (left) and low-voltage (right)

assumption, the rise/fall time is proportional to the product of gate charge and gate resistance,

$$t_{rise}^{(\prime)}, t_{fall}^{(\prime)} \propto \frac{Q_g R_g}{V_g} \tag{9}$$

Typically, for the same $V \cdot I$ rated Si MOSFET, when $V_{\rm BV}$ is reduced from 500 V to 60 V, the Q_g is indeed increased due to larger die size, but the internal gate resistance R_g is significantly larger in 500 V MOSFET than 60 V. Example state-of-the-art Si MOSFET parts are listed in Table III. Thus, for Si MOSFET with similar $V \cdot I$ rating, low votlage devices has faster rise/fall time than high-voltage devices and so less overlap loss.

Therefore, with the assumptions above and the condition that the output power and MOSFET $V \cdot I$ rating in a CCM boost converter are constant, as the voltage level is scaling down, the conduction loss in the switching devices remain constant, but the switching loss decreases. As a result, the total power losses of switching devices would decrease.

For the boost inductor, the inductor current ripple ratio $\mathcal{R}_L$ is given by,

$$\mathcal{R}_L = \frac{DD'^2 V_o}{2 f_s L I_o} = \frac{DD'^2 P_o^2}{2 f_s L I_o^2} \tag{10}$$

L is the inductance value, D ($D' = 1-D$) is the duty cycle. If $\mathcal{R}_L$, f_s, and P_o are constant, the energy stored in the inductor $E = \frac{1}{2} L I_i^2$ is independent of the voltage V_o.

$$E = \frac{1}{2} L I_i^2 \propto \frac{1}{2} L I_o^2 = \frac{DD'^2 P_o^2}{4 f_s \mathcal{R}_L} \tag{11}$$

I_i and I_o are input and output current. Therefore, we can select the magnetic core with the same geometry and permeability as well as the air gap distance when designing the inductor for the two cases. If the original inductor in the 400 V boost circuit has k turns in series as shown in Fig. 7, while in the low-voltage (48 V) high-current case, the series-connected winding can be changed to parallel connection. The current in each turn of the new inductor on the right is still I_i, as the total inductor current becomes kI_i. Therefore, the conduction loss in the inductor remains constant.

In conclusion, with constant switching frequency, output power, switching device $V \cdot I$ rating, and inductor size in a CCM boost converter, as the voltage is scaled down and the current is scaled up proportionally, the total losses in the switching devices would decrease, while the loss in the inductor is constant. The efficiency of the boost stage hence increases. The reason behind this comes from the better conduction and switching characteristics of low-voltage devices. The total efficiency of proposed two-stage ac/dc PFC converter of Fig. 4 can be higher and much flatter than the conventional design across the entire universal line input range.

However, this scaling law of efficiency versus $V_{\rm BV}$ for boost circuit has its own limited range. It is not accurate to assume that specific resistance $R_{on,sp}$ always scales linearly versus breakdown voltage $V_{\rm BV}$ for Si MOSFETs, i.e., $R_{on,sp} \propto V_{\rm BV}$. Many types of transistor structures were developed for Si MOSFETs used all kinds of application. Typical structures for Power MOSFETs include lateral double-diffused transistor (LDMOS) [29], vertical double-diffused transistor (VDMOS) [30], V-groove double-diffused transistor (VMOS) [31], and trench transistor (UMOS) [32], [33]. Among these structure, trench transistor has the lowest on-resistance due to the elimination of the JFET region and the small cell pitch, which reduces the corresponding channel resistance, accumulation resistances, and drift resistance [34], [35]. Super-junction deep-trench transistor introduced by Infineon Technologies with its CoolMOS products [36] can significantly reduce the on-resistance of Si MOSFET with $V_{\rm BV} \geq 500$ V by a factor of five compared with trench MOSFET.

To block high-voltage, the vertical Si power MOSFET contains a lightly doped N-drift region, shown in Fig. 8. For Si power MOSFET $\geq$ 100 V, this drift resistance per unit area $R_{{\rm D},sp}$ dominates the total on resistance $R_{on,sp}$ [28], given by

$$R_{{\rm D},sp} = \frac{4 V_{BV}^2}{\varepsilon_s \mu_n E_C^3} \tag{12}$$

ε_s is the dielectric constant of Si, μ_n is the mobility, and E_C is the critical electric field. The effective scaling law of $R_{on,sp}$ versus $V_{\rm BV}$ for Si Power MOSFET $\geq$ 100 V is roughly the power of 2.4$\sim$2.6 [37].

$$R_{on,sp} \propto V_{\rm BV}^{\alpha}, \quad \alpha = 2.4 \sim 2.6 \tag{13}$$

If $\alpha = 2.5$, this is a stronger argument than the linear assumption in (1). By this, the new on-resistance and conduction loss are,

$$\begin{aligned} R_{on} = \frac{R_{on,sp}}{A} \rightarrow \frac{\frac{R_{on,sp}}{k^{2.5}}}{kA} = \frac{R_{on}}{k^{3.5}}, \\ I^2 R_{on} \rightarrow (kI)^2 \frac{R_{on}}{k^{3.5}} = \frac{1}{k^{1.5}} I^2 R_{on} \end{aligned} \tag{14}$$

Thus, the conduction loss would also decrease along with the switching loss in a low-voltage-high-current boost converter.

The structure of a trench MOSFET with all the internal resistance components is shown in Fig. 8. However, when the breakdown voltage is further scaled down $<$ 100 V, the channel resistance $R_{\rm CH}$ and contact resistances $R_{\rm CS}$, $R_{\rm CD}$ that do not have strong dependence on $V_{\rm BV}$ become more dominant over drift resistance $R_{\rm D}$. This applies to all the different power MOSFET structures. The reduction of $R_{on,sp}$ versus $V_{\rm BV}$ of Si power MOSFET usually saturates around 20 V as shown in Fig. 9.

On the other hand, as the output voltage V_o, which is also the drain voltage, goes under 20 V approaching the typical

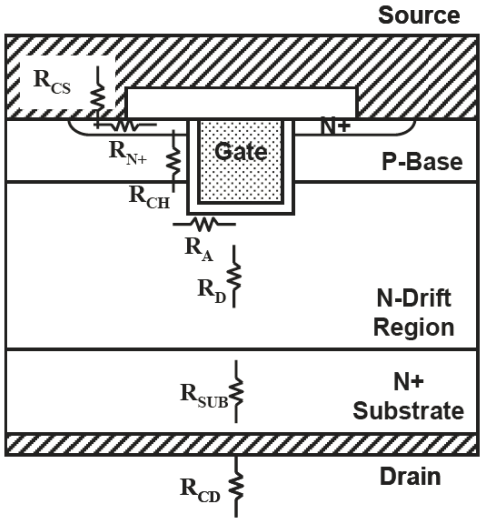


Fig. 8: Trench power MOSFET structure with its internal resistances, figure taken from [28]

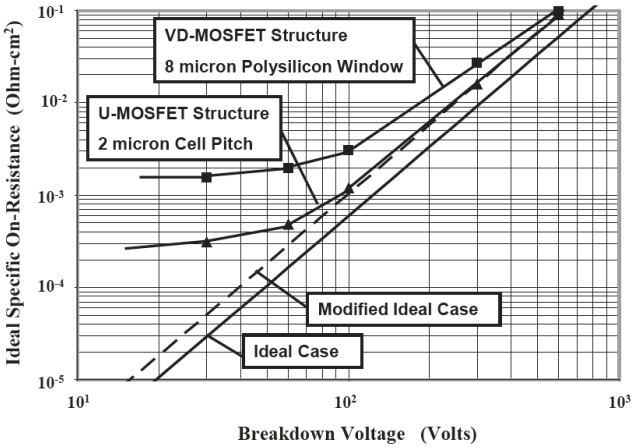


Fig. 9: Specific on-resistance of UMOS and VDMOS linear cell structure, figure taken from [28]

gate voltage $V_g = 10$ V, the gate driving loss $f_s Q_g V_g$ becomes dominant over output charge switching loss $f_s Q_{oss} V_o$. Therefore, as the voltage of the boost circuit is further scaling down under 20 V, the conduction loss $I^2 R_{on}$ and the gate driving loss $f_s Q_g V_g$ could both become larger than the high-voltage case and defect the efficiency. Table III lists several state-of-the-art 500 V and 60 V Si power MOSFETs. These devices can be used to design the boost PFC converters with output voltage $V_o = 400$ V and 48 V respectively. It shows that the output charge switching loss $f_s Q_{oss} V_o$ still dominates over the gate driving loss $f_s Q_g V_g$ in the specific cases above. The effective scaling power on $R_{on,sp}$ from 500 V to 60 V of the best Si power MOSFET is between 1 and 2. Therefore, for boost PFC converters with the same output power, 48 V_o case would have higher efficiency than 400 V_o case as all the conduction loss and switching loss are decreasing due to the scaling is stronger than linear.

V. Design Guideline and Control Implementation

A guideline to design an example off-line PFC converter in Fig. 4 with $V_{\rm OUT} = 48$ V, $P_{\rm OUT} = 250$ W is presented here. The block diagram of a simple control solution is shown in Fig. 10. The design starts with the boost converter. The low frequency buffer capacitance $C_{\rm Bluk}$ is determined by the ripple $\Delta V_{\rm OUT}$ on the output voltage $V_{\rm OUT}$,

$$\Delta V_{\rm OUT} \simeq \frac{V_{\rm OUT}}{2\omega R_L C_{\rm Bulk}} \tag{15}$$

Here, ω is the frequency of the ac input, R_L is the output load. The peak output voltage of the LLC stage, $V_{\rm f}$, has to be smaller than the instantaneous $v_{\rm OUT}(t)$. That is:

$$V_{\rm f} < V_{\rm OUT} - \frac{1}{2}\Delta V_{\rm OUT} \tag{16}$$

If the average output power is $P_{\rm OUT}$, the estimated boost converter efficiency is $\eta_{\rm boost}$, then after the selection of $V_{\rm f}$, the effective load resistance presented to LLC stage by the boost PFC circuit, R_e, is

$$R_e = \frac{V_{\rm f}^2 \times \eta_{\rm boost}}{2P_{\rm OUT}} \tag{17}$$

The boost converter operates in CCM. As shown in Fig. 10, a fast feedback loop controls the average boost inductor current $i_{\rm g}(t)$ to be proportional to $v_{\rm f}(t)$.

Detail analysis and design guidelines of the LLC circuit are well presented in [22], [23]. Methods of designing and utilizing the leakage inductance of the transformer as the resonant inductor L_r in LLC converters in order to reduce the volume are discussed in [38], [39]. [40], [41] describe ways of using synchronous rectification to improve the efficiency of LLC circuits. During half of an ac cycle, the VFX LLC converter delivers a pulsing power,

$$P_{\rm LLC} = 2\frac{P_{\rm OUT}}{\eta_{\rm boost}}\sin^2(\omega t) \tag{18}$$

To design the resonant components L_r, C_r, and L_m, the operating condition at the peak of a line cycle should be used. Based on the VFX mode selection of Table I, Table IV summarizes the design parameters of the VFX LLC DCX stage. C_1 and C_2 are small-value high frequency filter capacitor at the LLC stage's input. Under *full voltage swing mode*, C_1 and C_2 are effectively connected in series for filtering, while in parallel under *half voltage swing mode*. Assuming all the high frequency current goes through C_1 and C_2, the value of $C_{1,2}$ can be determined by $\Delta V_{in} = \Delta I_{in}\frac{1}{2\pi f_s C}$. ΔV_{in} is the total voltage ripple allowed on the capacitor, and ΔI_{in} is the high frequency current ripple, which rougly equals the current amplitude through C_r. This current in the resonant tank can be calculated using the peak voltage listed in Table I and effective ac loading resistance from the rectifier [22], [23]. Between the frequency range of 150 kHz-30 MHz, the impedance of $C_{1,2}$ is typically much smaller than the 50 Ω output impedance of a Line Impedance Stabilization Network (LISN). Therefore, the assumption that most of the high frequency current goes through C_1 and C_2 is valid enough to determine the required capacitance. However, similar to other ac/dc converters, in

TABLE III: STATE-OF-THE-ART SI POWER MOSFETS COMPARISON

500 V Si CoolMOS, V_o = 400 V, I_o = 1 A, V_g = 10 V, f_s = 500 kHz, $T_C = 25°$C								
Part	I_D	$V \cdot I$ rating	$R_{on,typ}$	Q_g	R_g	$I^2R_{on,typ}$	$f_sQ_{oss}V_o$	$f_sQ_gV_g$
IPD50R800CE	7.6 A	3.8 kVA	0.72 Ω	12.4 nC	3 Ω	0.72 W	1.45 W	0.062 W
IPD50R1K4CE	4.8 A	2.4 kVA	1.26 Ω	8.2 nC	7 Ω	1.26 W	0.80 W	0.041 W
IPD50R2K0CE	3.6 A	1.8 kVA	1.80 Ω	6 nC	7 Ω	1.80 W	0.64 W	0.030 W
60 V Si OptiMOS, V_o = 48 V, I_o = 8.33 A, V_g = 10 V, f_s = 500 kHz, $T_C = 25°$C								
Part	I_D	$V \cdot I$ rating	$R_{on,typ}$	Q_g	R_g	$I^2R_{on,typ}$	$f_sQ_{oss}V_o$	$f_sQ_gV_g$
BSC066N06NS	64 A	3.84 kVA	5.5 mΩ	17 nC	1.2 Ω	0.38 W	0.58 W	0.085 W
BSC097N06NS	46 A	2.76 kVA	8.0 mΩ	12 nC	1.1 Ω	0.56 W	0.42 W	0.060 W
Comparison of 500 V and 60 V Si MOSFET $R_{on,sp}$ with similar VA rating								
Part	V_{BV}	$V \cdot I$ rating	$R_{on,500\ V} \times (\frac{60}{500})^3$		$R_{on,typ}$	$R_{on,500\ V} \times (\frac{60}{500})^2$		$\frac{Q_g R_g}{V_g}$
IPD50R1K4CE	500 V	2.4 kVA	—		1260 mΩ	—		5.74 ns
BSC097N06NS	60 V	2.76 kVA	**2.2 mΩ**		8 mΩ	**18 mΩ**		1.32 ns
IPD50R800CE	500 V	3.8 kVA	—		720 mΩ	—		3.72 ns
BSC066N06NS	60 V	3.84 kVA	**1.2 mΩ**		5.5 mΩ	**10 mΩ**		2.04 ns

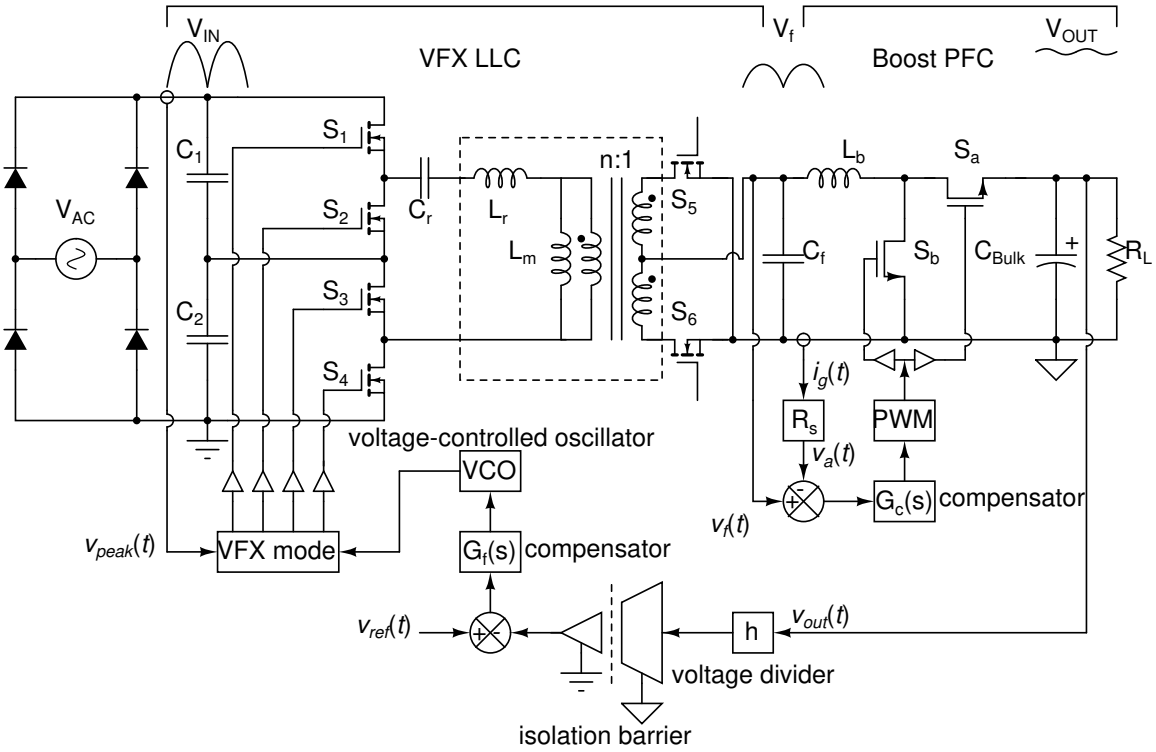


Fig. 10: VFX LLC and boost PFC with control

order to comply with conducted EMI regulations, such as the FCC Part 15 and CISPR 22, extra EMI filter circuit is still necessary. Adding an inductor between the full bridge rectifier and VFX LLC converter can potentially reduce the EMI noise to the ac source and also improve the quality of the input current. Methods of conducted EMI analysis and filter design for ac/dc converters are well studied in [42]–[46].

TABLE IV: VFX LLC DCX DESIGN PARAMETERS

Specification	Design	Value
Input voltage	$V_{\text{tank,peak}}$	95-190 V
Output voltage	V_{f}	43 V
Load resistance	$\frac{V_{\text{f}}^2 \times \eta_{\text{boost}}}{2P_{\text{OUT}}}$	3.5 Ω
Output power	$2\frac{P_{\text{OUT}}}{\eta_{\text{boost}}}$	$\frac{2\times250}{0.98}$ W
Resonant tank gain	$\frac{V_{\text{f}}}{V_{\text{tank,peak}}}$	2.2-4.4

To regulate V_{OUT}, another feedback loop outside the current control loop can be designed to adjust the gain of the resonant tank. Shown in Fig. 10, $v_{\text{OUT}}(t)$ is sensed through isolation barrier to control the frequency of $V_{\text{tank}}(t)$. The unity-gain bandwidth of this loop is small and placed before the dominant pole $\frac{1}{R_{\text{L}}C_{\text{Bulk}}}$. The peak of $V_{\text{IN}}^{\text{REC}}$ sets the VFX *full/half voltage swing mode* that the inverter will be operating with. V_{f} can

also be sensed to control the frequency, but another feedback loop is necessary to regulate V_{OUT}.

VI. Experimental Results

A prototype converter corresponding to the circuit in Fig. 4 and 10 was designed and implemented for an off-line PFC power supply application with $V_{\text{OUT}} = 48$ V, $P_{\text{OUT}} = 250$ W. The effective resonant inductor L_r consists of the leakage inductance of the transformer and an extra air-core inductor. The measured values of the gapped transformer circuit model is shown in Fig. 11. The cross coupling between the two secondary windings are assumed to be ideal.

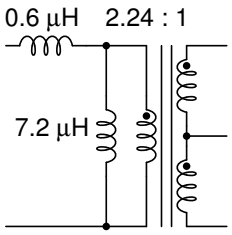
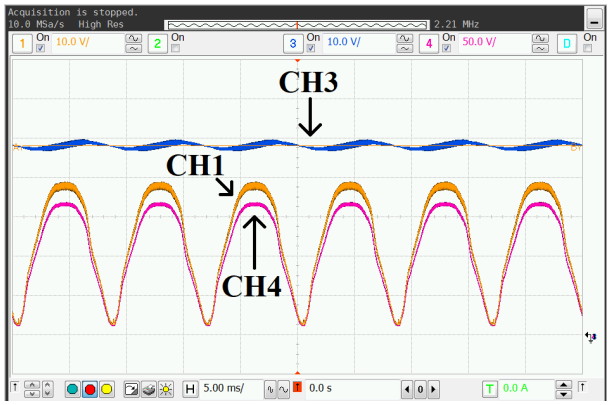


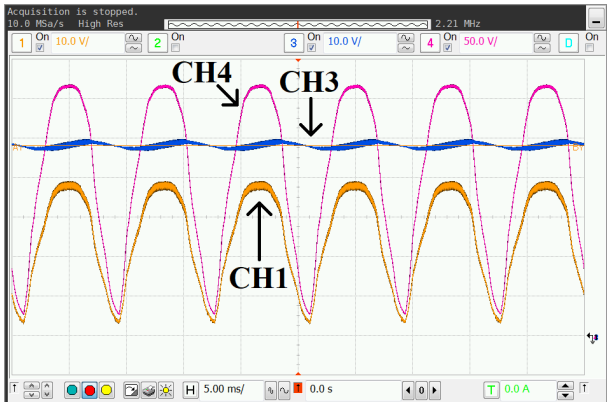
Fig. 11: Measured leakage and magnetizing inductance of gapped transformer

Table V summarizes the key components of the prototype converter. Fig. 19 shows the photograph of the converter. During the experimental test, a full bridge rectifier GBPC1506W is connected before the prototype converter. The measured voltage waveform across different nodes are shown in Fig. 12. It clearly shows that the LLC converter first converts the rectified sine wave to a smaller voltage which eliminates the high-voltage dc bus in the conventional boost PFC converters. The second stage boost circuit converts this smaller rectified ac to the final output voltage and provides power factor correction. As shown in Fig. 12b, the VFX *half voltage swing mode* provides extra 2-to-1 gain when operating with high line input ac voltage.

Fig. 13 shows the measured ac current waveform at different input voltages. Fig. 14 presents the measured efficiency performance from rectified ac input to 48 V_{out} at full output power 250 W. Across the entire universal line input range, the total efficiency of the proposed two-stage converter is between 93% and 95%, and the variation is $\leq 2\%$. Compared with the conventional two-stage design in Fig. 2, the efficiency of the boost stage alone typically drops by $4 \sim 6\%$ as shown in Fig. 3. The ac current Total Harmonic Distortion (THD) and power factor performance are shown in Fig. 15. At full load, the proposed converter is able to achieve high power factor and low distortion in the current across entire input range. Fig. 16 shows the efficiency versus output power at different voltage levels. At 120 V and 230 V input, the converter can maintain high efficiency across a large load range. The efficiency performance of two cases are almost the same due to the dynamic adjustment of dc-dc gain by using a VFX circuit. The THD and power factor performance versus output power are provided in Fig. 17 and Fig. 18, respectively. Fig. 20 shows a thermal image of the converter in operation captured using FLIR A655sc thermal camera. The block diagram and a photograph of the experimental test setup are shown in Fig. 21 and 22, respectively.



(a) VFX *full voltage swing mode*, $V_{\text{IN}}^{\text{REC}} = 120$ V_{rms}

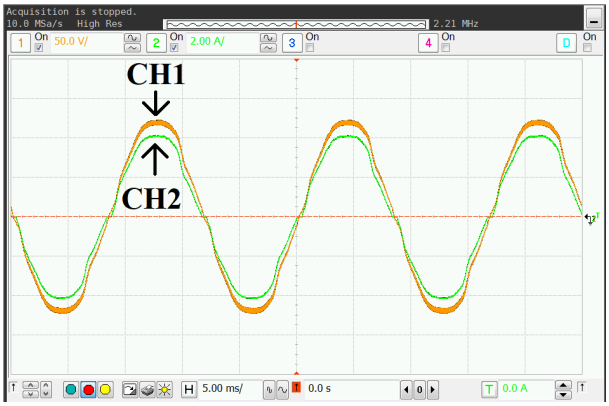


(b) VFX *half voltage swing mode*, $V_{\text{IN}}^{\text{REC}} = 230$ V_{rms}

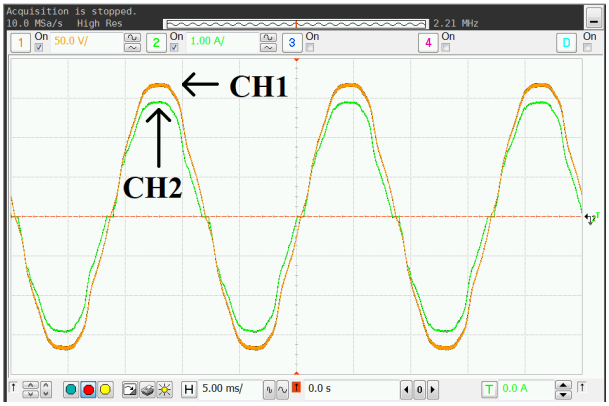
Fig. 12: Measured voltage waveforms of prototype converter at different nodes. CH4 in purple is the rectified input voltage $V_{\text{IN}}^{\text{REC}}(t)$, CH1 in yellow is the output voltage of the LLC converter $V_{\text{f}}(t)$, and CH3 in blue is the final output voltage $V_{\text{out}}(t)$.

VII. Conclusion

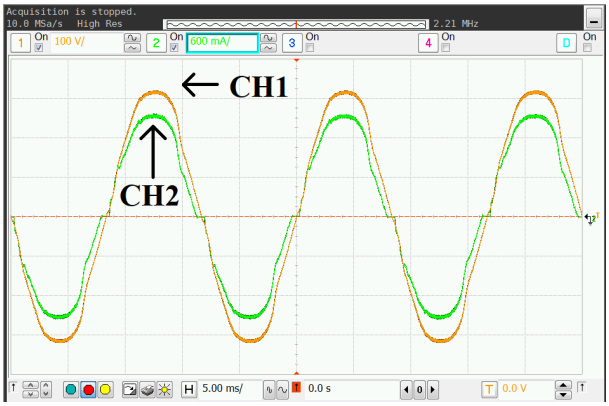
A two-stage step-down power factor pre-regulator topology that is suitable for designing a low-voltage off-line supply is presented in this paper. This circuit consists of a LLC converter followed by a boost PFC circuit and so eliminates the 400 V dc bus which is usually a tough obstacle for device selection in the conventional off-line power supply design. A variable frequency multiplier technique is used to provide different dc-dc conversion ratio depending on the input voltage and compress the effective voltage conversion range. This circuit configuration reduces the low line efficiency drop often encountered in many universal input off-line power supplies without increasing the cost and design complexity. The proposed design also allows better semiconductor switches with lower breakdown voltage ratings to be used in both of the LLC and boost circuit. Constant power scaling shows that a medium-voltage (48 V) boost converter can be designed to operate more efficiently than a high-voltage (400 V) converter, due to the inherent superiority of low-voltage power devices. Therefore, for off-line PFC power supply with low-to-medium output voltage (20∼100 V), the proposed circuit can provides higher and flatter efficiency performance compared with the conventional design which consists of a boost PFC stage followed by a LLC circuit. However, higher output power,



(a) VFX *full voltage swing mode*, V_{IN}^{REC} = 85 V_{rms}



(b) VFX *full voltage swing mode*, V_{IN}^{REC} = 120 V_{rms}



(c) VFX *half voltage swing mode*, V_{IN}^{REC} = 230 V_{rms}

Fig. 13: Measured ac input waveforms of prototype converter. CH1 in yellow is the input voltage, CH2 in green is the input current.

e.g., $\geq$ 500 W, also proposes design challenges in high-current boost inductor, current sense circuit, high frequency switching of large-die Si MOSFETs, etc. A 250 W prototype converter built using Si devices demonstrates the promised flat and high efficiency performance under both high line and low line input voltage conditions.

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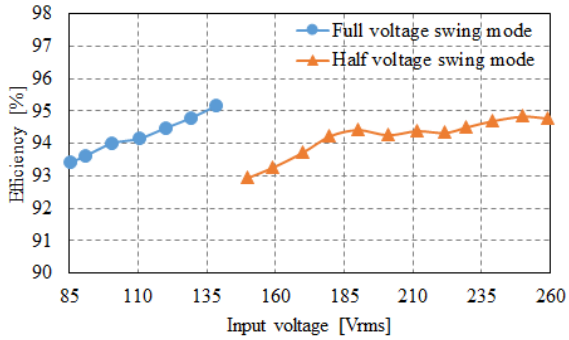

Fig. 14: Measured efficiency versus input voltage, P_{out} = 250 W, V_{out} = 48 V

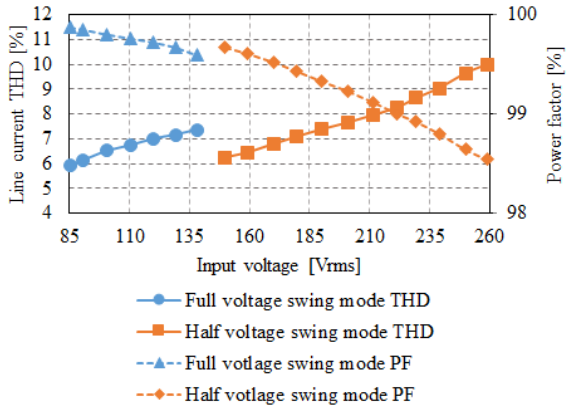

Fig. 15: Input current THD and power factor versus input voltage, solid line is the input current THD referred to left vertical axis, dashed line is the power factor referred to right vertical axis, P_{out} = 250 W, V_{out} = 48 V

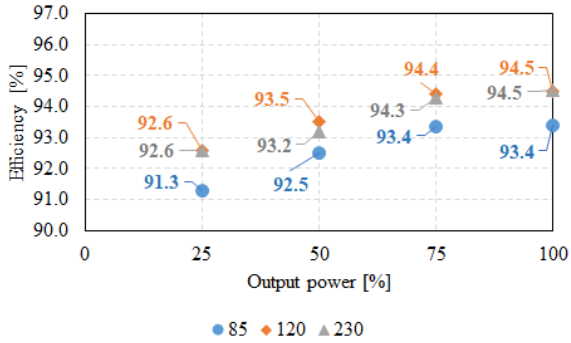

Fig. 16: Efficiency versus output power, V_{in} = 85 V, 120 V, and 230 V listed

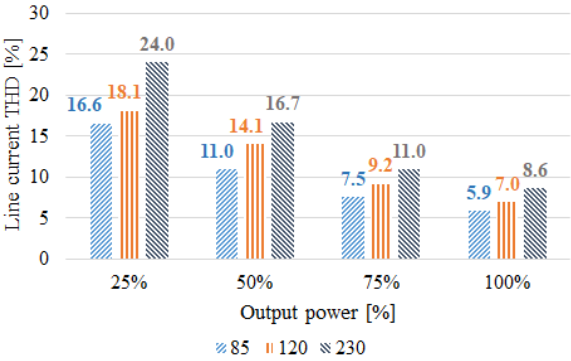

Fig. 17: AC line current THD versus output power, V_{in} = 85 V, 120 V, and 230 V listed

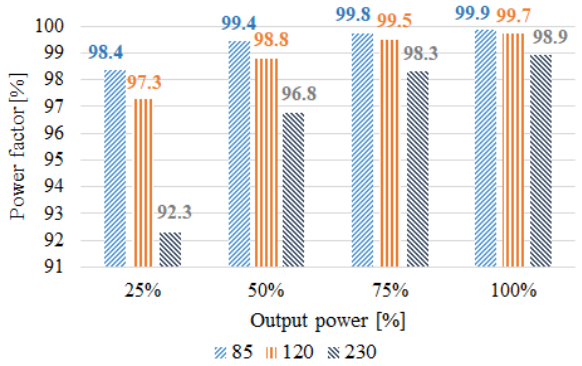

Fig. 18: Power factor versus output power, V_{in} = 85 V, 120 V, and 230 V listed

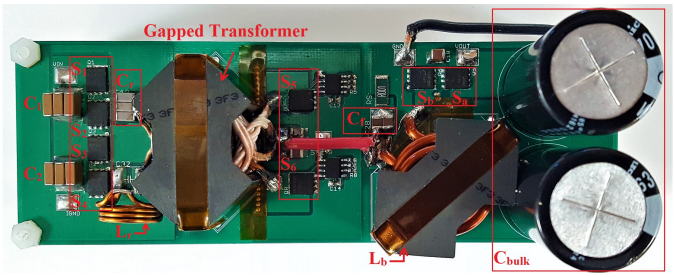

Fig. 19: Photograph of prototype converter, PCB dimension 145×50 mm

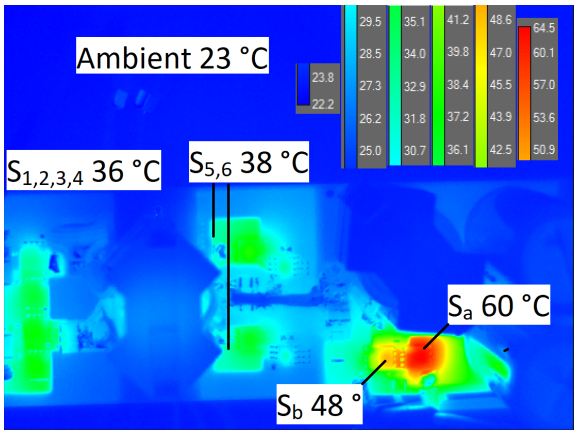

Fig. 20: Thermal image of the prototype converter in operation, $V_{\text{IN}}^{\text{REC}}$ = 130 V_{rms}, P_{out} = 250 W

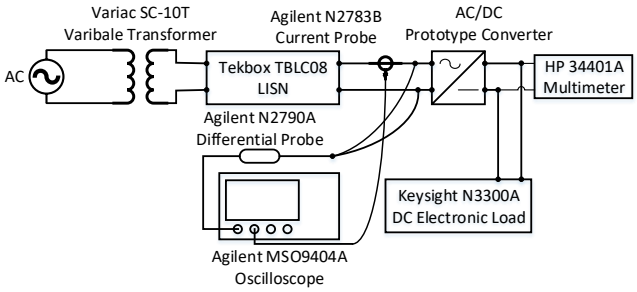

Fig. 21: Block diagram of key components in the experimental test setup

TABLE V: BILL-OF-MATERIALS (BOM) OF THE PROTOTYPE CONVERTER

VFX LLC	
Device	**Component Description**
$S_{1,2,3,4}$	Infineon BSC350N20NSFD 200 V/35 A Si OptiMOS
$S_{5,6}$	Infineon BSC093N15NS5 150 V/87 A Si OptiMOS
Transformer	Ferroxcube RM12-3F3 core, gap 1.28 mm, turns ratio 7:3:3, 2 AWG46/330 Litz wire in parallel
C_r	141 nF, NP0 Ceramic, 450 V, CGA8N4NP02W473J230KA × 3
L_r	710 nH, 600 nH leakage + 110 nH Coilcraft 1212VS-111ME
L_m	7.2 uH
$C_{1,2}$	6.6 uF, X6S Ceramic, 450 V, C5750X6S2W225K250KA × 3
Switching frequency	205-410 kHz for low line, 90-180 kHz for high line
Resonant frequency	500 kHz
$S_{1,2,3,4}$ driver	Silicon Labs SI8273GB-IS1
$S_{5,6}$ driver	ON Semi. NCP4305DDR2G
Microcontroller	STM32F411VE
Boost	
Device	**Component Description**
$S_{a,b}$	Infineon BSC066N06NS 60 V/64 A Si OptiMOS
L_b	7.8 uH, Ferroxcube RM12-3F3 core, gap 1.6 mm, 10 turns, AWG12 magnet wire
C_{Bulk}	4700uF × 2, 63V, UVR1J472MRD × 2
$S_{a,b}$ driver	TI half bridge driver LM5104
PWM IC	Linear Tech LTC6992-1
Opamps	Linear Tech LTC6360
Current Shunt	3 W R2512 1% 1 mΩ
Switching frequency	450 kHz

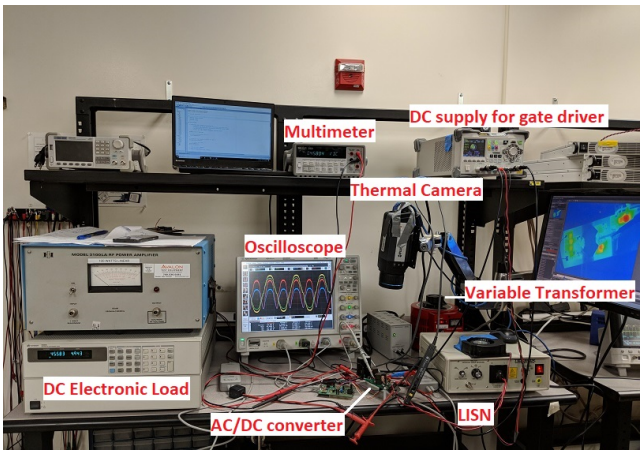

Fig. 22: Photograph of the experimental test setup

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