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On the Optimization of a Class-E Power Amplifier with GaN HEMTs at MHz Operation

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***Abstract*—Class-E power amplifiers have regained academic interest over the past decades due to the introduction of new high-performance wide-bandgap semiconductor devices and the increasing demand for high-efficiency power amplifiers. While these power devices, notably GaN HEMTs, have exceptional performance at megahertz operation, they also display an additional loss component due to the C_{oss} at this frequency. Unfortunately, the dependency of this loss term on the peak voltage and the device size is the opposite of that of the conduction loss.**

In this paper, we mathematically analyze the operation of a Class-E amplifier to find the optimal input voltage and device sizing where the sum of these two losses is minimized. From this analysis, we have found that the common design approach of maximizing device voltage rating and area to get the best efficiency no longer holds for some operating conditions. Furthermore, we examine the constraints that dictate when this optimization equations can and cannot be used, as well as propose a distributed loss model for the C_{oss} loss based on a generalized Steinmetz equation (GSE) to allow this new loss term to be easily simulated.

To verify our mathematical analysis and to demonstrate the applications of the proposed GSE-based C_{oss} loss model, two design examples are provided. They consist of a choke-input Class-E amplifier at 10 MHz and a variable-resistance Class-E amplifier at 40.68 MHz. The experimental results on these two design examples show good agreements with our analysis.

I. Introduction

The Class-E power amplifier concept was first introduced by Ewing in 1964 [1] and popularized by the Sokals in 1975 [2]. Since then, it has received an enormous amount of academic interest. Almost every aspect of the topology has been analyzed, whether it be the circuit tuning methods [3]–[7], effects of non-linear capacitance of the switch [8]–[10], power losses [11]–[13], circuit optimization [14]–[17], etc.

In term of the input voltage and the device selection, it has long been established that "[f]or the highest efficiency, the highest possible V_{CC} [input voltage] should be used, within the V_{CE} limitation of the transistor" [2, p. 174]. Moreover, "[t]he shunt capacitor can be implemented, either partially or entirely by C_{dd} [drain capacitance of the switch], since the impact of its nonlinearity on PA performance is weak" and "[t]he maximum device width [device size] minimizing the power loss due to r_{on} is found when the shunt capacitance is entirely made of the drain capacitance" [13, p. 1223].

Over the past decades, a number of new semiconductor devices specially designed and optimized for high-frequency operation have started coming into the market. The combination of these new devices and the increased demand for high-efficiency power amplifiers for wireless communication and wireless power transfer applications had consequently sparked a renew interest in the Class-E topology [18]–[26].

While these devices, notably GaN HEMTs, show superior performance, studies have found that they possess an undocumented loss mechanism not yet incorporated into the simulation models or manufacturer's datasheets [27]–[34]. This loss occurs when an ac voltage is applied across the device during its off-state and manifests itself as hysteresis in the Q-V plot of the semiconductors. Due to the hysteresis nature, this C_{oss}-related loss not only increases with both the frequency of operation and the peak voltage across the device but also with the die area. This positive dependency of the C_{oss} loss on the peak voltage and device size is precisely the opposite to how the conduction loss scale.

Due to its frequency dependency, when the operating frequency is high enough, this C_{oss} loss will surpass the conduction loss and become the main loss contributor. Once this happens, in contrast to the common design approach on the input voltage and device selection, reducing the input voltage and the device size will actually reduce the overall power loss, increasing the circuit efficiency.

In this paper, we will look in details at the design and optimization of a Class-E power amplifier when dealing with these two losses. In section II, we will mathematically calculate the minimum frequency where one needs to start considering the C_{oss} loss in their design, as well as the optimum input voltage and optimum device sizing to use when operating above this frequency. In section III, we will demonstrate a method to create a SPICE simulatable model for the C_{oss} loss to allow for an optimization of non-ideal Class-E amplifiers via simulation. In section IV, we will showcase two design examples utilizing the aforementioned analysis and loss model. Experimental result and its comparison with the simulation will be in section V and VI. Finally, section VII will conclude the paper.

While the bulk of this paper will discuss the effect of the C_{oss} loss on the optimization of a Class-E amplifier with GaN HEMTs, the mathematical equations and the proposed simulation model can be directly applied to amplifiers made with any transistors that have C_{oss} loss, including silicon (Si) and silicon carbide (SiC) devices. In fact, the important C_{oss} loss parameters used in all of the optimization equations in this paper for many SiC devices are already located in [31]. In the case that these loss parameters cannot be directly found, appendix A will present a method to derive them from another, more frequently reported, set of loss parameters. Appendix B will provide additional tables showing the optimum input

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voltage and device sizing for a number of devices at different frequencies and power levels. Lastly, appendix C will investigate the effect of the turn off loss on the optimization.

II. Mathematical Analysis and Optimization

In this section, we will mathematically analyze a semi-ideal Class-E power amplifier, considering only the conduction and the C_{oss} loss.

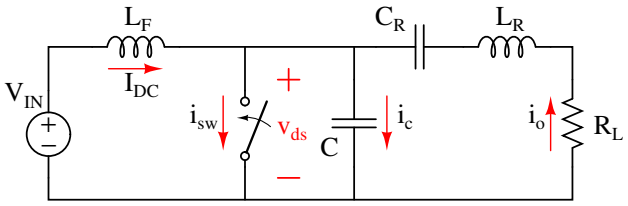

Fig. 1: The simplified schematic of a standard choke-input Class-E power amplifier. The capacitor, C, represents the junction capacitance of the switch, C_{oss}, lumped together with any added external capacitor.

A. Assumptions

The basic topology of a Class-E power amplifier is shown in figure 1. To simplify the analysis, we use the following assumptions.

- The input inductor, L_f, is very large, resulting in a dc input current, I_{dc}.
- The series output filter, C_r–L_r, has high Q factor resulting in a sinusoidal output current, $i_o(t) = I_m \sin(\omega t + \theta)$.
- All of the inductors and capacitors are loss-less.
- The loss in the switch is sufficiently small to have no effect on the circuit's operation resulting in $P_{in} = P_{out}$.
- The junction capacitance of the switch, C_{oss}, is linear.
- The switch operates at 50% duty cycle, has a constant on-resistance, R_{on}, and has sufficiently fast turn-on/off transitions.

By using zero-voltage-switching (ZVS) and zero-dv/dt-switching conditions (ZDS), along with the above assumptions, we can show that

$$i_{sw}(t) = \begin{cases} I_m \sin(\omega t + \theta) + I_{dc}, & 0 \le \omega t < \pi \\ 0, & \pi \le \omega t < 2\pi, \end{cases} \tag{1}$$

$$i_c(t) = \begin{cases} 0, & 0 \le \omega t < \pi \\ I_m \sin(\omega t + \theta) + I_{dc}, & \pi \le \omega t < 2\pi, \end{cases} \tag{2}$$

$$\begin{aligned} v_{ds}(t) &= \frac{1}{C}\int_0^t i_c \, dt \\ &= \begin{cases} 0, & 0 \le \omega t < \pi \\ \frac{1}{\omega C}\{I_{dc}(\omega t - \pi) - I_m(\cos(\theta) + \cos(\omega t + \theta))\}, \\ & \pi \le \omega t < 2\pi, \end{cases} \end{aligned} \tag{3}$$

where $\theta = -\operatorname{atan}\left(\frac{2}{\pi}\right)$, $I_m = \frac{4}{\sqrt{4+\pi^2}}\frac{V_{in}}{R_L}$, and $I_{dc} = \frac{8}{(4+\pi^2)}\frac{V_{in}}{R_L}$.

B. Loss components

The two loss components we will consider are the conduction and the C_{oss} loss. The total power loss, P_{loss}, is taken as the sum of these two losses.

Depending on the device characteristic and the operating condition, the gating and the turn-off loss can also be a significant part of the overall power dissipation. Nonetheless, they are ignored for simplicity of this analysis.

1) Conduction loss, P_{cond}

The conduction loss is the result of the current flowing through the channel of the switch during its on-time.

$$\begin{aligned} P_{cond} &= \frac{1}{\omega T}\int_0^{\omega T} (i_{sw}(t))^2 R_{on} dt \\ &= r R_{on}\left(\frac{P_{in}}{V_{in}}\right)^2, \qquad \left[r \equiv \frac{28+\pi^2}{16}\right] \end{aligned} \tag{4}$$

The value of R_{on} is the effective on-resistance during the on-time of the device. It can be approximated from the datasheet but should be altered to include the effect of finite gating time, the temperature dependency, and other dynamic effects such as dynamic on-resistance [35]–[43]. While reported dynamic-to-static on-resistance ratio for GaN devices varies greatly from as low as 1.08x in [37] to as high as 5x in [41], we choose to use $R_{on} = 2.5\times R_{datasheet}$ in this analysis. From our previous study in [39] along with our personal experience, we believe this to be a good approximation for the effect of dynamic on-resistance of the current generation of GaN HEMTs in soft-switching converters at MHz frequencies.

2) Junction capacitance (C_{oss}) loss, P_{coss}

The C_{oss} loss is the result of the hysteresis effect in the junction capacitance of the switch. For a Class-E waveform, it can be approximated with an equation that resembles the Steinmetz equation [29]–[31].

$$\begin{aligned} P_{coss} &= k_e f^{(\alpha+1)} V_p^{\beta} \\ &= k_e f^{(\alpha+1)} (p V_{in})^{\beta}, \qquad \left[p \equiv 2\pi \operatorname{atan}\left(\frac{2}{\pi}\right)\right] \end{aligned} \tag{5}$$

The variables f and V_p are the switching frequency and the peak drain voltage across the switch. The parameters k_e, α, and β are the Steinmetz-like C_{oss} loss parameters for the Class-E waveform which can be directly found on or derived from published papers, or calculated from a device measurement on a Sawyer-Tower circuit.

Table I shows such parameters taken from [31] for a 650 V GaN HEMT from GaNSystems, GS66504B, along with other important device parameters. We will use this device and others in the same GS6650xx series to demonstrate key concepts in the rest of this paper.

TABLE I: Steinmetz and other device parameters for the GS66504B.

k_e [W/V·Hz]	α	β	R_{on} [mΩ]	C_{oss} [pF]	$V_{ds,max}$ [V]	$I_{ds,max}$ [A]
7.1×10^{-16}	0.6	1.6	2.5×100	44	650	36

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C. Optimization

Here, we will find the design parameters that minimize the overall power loss for different design constraints and operating conditions.

1) Optimal input voltage, $V_{in,opt}$

For a given device, power level, and operating frequency, what is the input voltage that minimizes the overall power loss?

To find this $V_{in,opt}$, we set the derivative of the total power loss with respect to the input voltage to be equal to zero.

$$\frac{dP_{loss}}{dV_{in}} = \frac{d}{dV_{in}}\left(P_{cond} + P_{coss}\right) = 0$$

This yields

$$-2rR_{on}\frac{P_{in}^2}{V_{in}^3} + k_e f^{(\alpha+1)} p^\beta \beta V_{in}^{(\beta-1)} = 0.$$

Thus,

$$V_{in,opt} = \left(\frac{2r}{p^\beta}\frac{R_{on}P_{in}^2}{\beta k_e f^{(\alpha+1)}}\right)^{\frac{1}{\beta+2}}. \tag{6}$$

For example, a 200 W 40 MHz Class-E amplifier designed with the 650 V GS66504B GaN HEMT (parameters shown in table I) will have

$$V_{in,opt} = 67 \text{ V}.$$

2) Minimum frequency, f_{min}

For a given device and power level, what is the minimum frequency where using the highest input voltage possible no longer gives the best efficiency?

To find the f_{min}, we set the the maximum drain voltage of the device to be equal to $p \times V_{in,opt}$, where p is the ratio between the peak and the input voltage in a Class-E waveform.

$$V_{ds,max} = p\left(\frac{2r}{p^\beta}\frac{R_{on}P_{in}^2}{\beta k_e f_{min}^{(\alpha+1)}}\right)^{\frac{1}{\beta+2}}$$

This yields

$$f_{min} = \left(2rp^2\frac{R_{on}P_{in}^2}{\beta k_e V_{ds,max}^{(\beta+2)}}\right)^{\frac{1}{\alpha+1}}. \tag{7}$$

For example, a 500 W amplifier designed with GS66504B will have

$$f_{min} = 13.2 \text{ MHz}.$$

Above f_{min}, the overall power loss will be minimized if one were to use the input voltage in (6) instead of the highest V_{in} possible.

3) Optimal device size, m_{opt}

For a given power level, frequency, and input voltage, if we had access to a series of devices with scaling die sizes (e.g., GaNSystems GS66502B, GS66504B, GS66506T, GS66508T, etc.), which one of these devices should we use to minimize the overall power loss?

To find the optimal device size, we first define the scaling factor, m, to be the ratio between the die size of the selected device to that of the nominal device. While this information is usually not available in the datasheet, it can be approximated by

$$m = \frac{R_{ds(on),nom}}{R_{ds(on),sel}} = \frac{C_{oss,sel}}{C_{oss,nom}}.$$

For instance, if we define GS66504B to be the nominal device, then GS66506T will have $m = 1.5$ and GS66502B will have $m = 0.5$.

With this device scaling factor defined, the overall power loss of any device can then be expressed as

$$P_{loss} = \frac{rR_{on}}{m}\left(\frac{P_{in}}{V_{in}}\right)^2 + mk_e f^{(\alpha+1)}(pV_{in})^\beta, \tag{8}$$

where R_{on} and k_e are those of the nominal device.

To find the m_{opt}, we set the derivative of the total power loss with respect to the device scaling factor to be equal to zero.

$$\frac{dP_{loss}}{dm} = 0$$

This yields

$$-\frac{rR_{on}}{m^2}\frac{P_{in}^2}{V_{in}^2} + k_e f^{(\alpha+1)}(pV_{in})^\beta = 0.$$

Thus,

$$m_{opt} = \sqrt{\frac{rR_{on}}{k_e p^\beta f^{(\alpha+1)}}}\frac{P_{in}}{V_{in}^{\frac{(\beta+2)}{2}}}. \tag{9}$$

For example, in a 200 W 40 MHz amplifier with 100 V input designed with GaNSystems GS6650xx series, to get the best efficiency, one should use

$$m_{opt} = 0.43,$$

which corresponds to the GS66502B, the smallest device in the series.

4) Optimal input voltage and device size pair

So for, we have separately found the optimal input voltage (when the device size is fixed) and the optimal device size (when the input voltage is fixed). Next, we will investigate the case where neither the input voltage nor the device size is fixed.

Does an optimal input voltage and device size pair exists, for a particular power level and operating frequency?

To do that, we first put the m_{opt} back into the equation (8).

$$P'_{loss} = \frac{rR_{on}}{m_{opt}}\left(\frac{P_{in}}{V_{in}}\right)^2 + m_{opt}k_e f^{(\alpha+1)}(pV_{in})^\beta$$

In another word, we find what the total power loss will be once the optimal device size is used. This results in P'_{loss} that is a function of P_{in} and V_{in}, but not a function of m.

Next, we take the derivative of this P'_{loss} with respect to V_{in}.

$$\frac{dP'_{loss}}{dV_{in}} = -rR_{on}P_{in}^2\left(\frac{2}{m_{opt}Vin^3} + \frac{1}{m_{opt}^2V_{in}^2}\frac{dm_{opt}}{dV_{in}}\right) + k_e p^\beta f^{(\alpha+1)}\left(\beta m_{opt}V_{in}^{(\beta-1)} + V_{in}^\beta\frac{dm_{opt}}{dV_{in}}\right)$$

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By substituting in m_{opt} from equation (9) and its derivative, we get

$$\frac{dP'_{loss}}{dV_{in}} = (\beta-2)\sqrt{rR_{on}k_e p^\beta f^{(\alpha+1)}}P_{in}V_{in}^{\left(\frac{\beta}{2}-2\right)}.$$

Due to the $(\beta-2)$ multiplier, the dP'_{loss}/dV_{in} is always positive when $\beta > 2$, and always negative when $\beta < 2$. As a result, the P'_{loss} will monotonically increase as we increase the V_{in} when $\beta > 2$. On the other hand, the P'_{loss} will monotonically decrease as we increase the V_{in} when $\beta < 2$.

For most of the wide-bandgap devices tested in [29]–[31], the β term is less than 2. This means that we can keep reducing the P'_{loss} by increasing the V_{in}, given that we scale the device size down accordingly As a result, when there are no other constraints, using the highest input voltage possible and scaling the device size with m_{opt} will provide the best efficiency.

In general, this is not always the case. We might not have access to the device that is small enough (e.g., $m_{opt} = 0.2$ but the smallest commercially available device in the series is $m = 0.5$). Or, we do have access to that small device, but due to either its I-V curve or its thermal resistance, it cannot handle the power level we need. To get the best efficiency in both of these cases, we will have to use the bigger device and scale the input voltage according to the equation (6) instead.

D. Other constraints

Additionally, we have to verify that by using the m_{opt}, we do not exceed other constraints on the circuit. The two constraints we will consider are the required shunt capacitance and the maximum channel current.

1) Required shunt capacitance, C_{req}

First, we define a parameter C_{ratio} to be the ratio between the junction capacitance of our m_{opt} device to the required shunt capacitance of the Class-E amplifier. As long as the C_{ratio} is less than one, extra external capacitance can be added to achieve the value of the C_{req}, making the design possible.

$$C_{ratio} \equiv \frac{m_{opt}C_{oss}}{C_{req}},$$

where the C_{oss} is that of the nominal device.

The required shunt capacitance, C_{req}, of the Class-E amplifier can be calculated from

$$\frac{1}{\omega T}\int_0^{\omega T} v_{ds}d(\omega t) = V_{in}.$$

This yields

$$C_{req} = \frac{P_{in}}{2\pi^2 f V_{in}^2}.$$

By substituting in m_{opt} from equation (9), we get

$$C_{ratio} = 2\pi^2\sqrt{\frac{rR_{on}}{k_e p^\beta}}C_{oss}f^{\left(\frac{1-\alpha}{2}\right)}V_{in}^{\left(\frac{2-\beta}{2}\right)}. \qquad (10)$$

Notice that this C_{ratio} is not dependent on the power level. Moreover, its dependency on the frequency and the input voltage is also quite low. To illustrate, for the GS6650xx series, $C_{ratio} \propto f^{0.2}V_{in}^{0.2}$, and C_{ratio} at

$$\begin{aligned} 5\text{ MHz}/60\ V_{in} &= 0.45, & 5\text{ MHz}/150\ V_{in} &= 0.54,\\ 50\text{ MHz}/60\ V_{in} &= 0.71, & 50\text{ MHz}/150\ V_{in} &= 0.86. \end{aligned}$$

This means that for the GS6650xx series at 10s of MHz, we can achieve a close to optimal design by simply picking the device with a junction capacitance value between 1/2 to 3/4 of the required shunt capacitance without actually calculating the m_{opt}.

2) Maximum channel current, $I_{ds,max}$

Here, we define a parameter I_{ratio} to be the ratio between the maximum channel current the m_{opt} device can handle to the maximum current actually going through the device. This number must be more than one, and the larger this number is, the lower the current stress is on the device.

$$I_{ratio} \equiv \frac{m_{opt}I_{ds,max}}{I_{sw,max}},$$

where $I_{ds,max}$ is that of the nominal device.

The maximum current through the switch can be found from equation (1).

$$I_{sw,max} = \left(\sqrt{1+\frac{\pi^2}{4}}\right)\frac{P_{in}}{V_{in}}$$

Thus,

$$I_{ratio} = \frac{1}{1+\frac{\pi^2}{4}}\sqrt{\frac{rR_{on}}{k_e p^\beta}}\frac{I_{ds,max}}{\sqrt{f^{(\alpha+1)}V_{in}^\beta}}. \qquad (11)$$

Again, this I_{ratio} is not power dependent. For the GS6650xx series, I_{ratio} at

$$\begin{aligned} 5\text{ MHz}/60\ V_{in} &= 21.7, & 5\text{ MHz}/150\ V_{in} &= 10.4,\\ 50\text{ MHz}/60\ V_{in} &= 3.4, & 50\text{ MHz}/150\ V_{in} &= 1.7. \end{aligned}$$

III. Simulation Technique

While the mathematical analysis in section II is a good starting point in the design process of a Class-E power amplifier, there are still other factors we need to consider in a real practical design. Examples of such factors are

- The real input inductor is finite.
- The passive components are actually lossy and their losses do affect the circuit's operation.
- The junction capacitance, C_{oss}, is non-linear.
- The channel resistance, R_{on}, is not of a static value.
- The gate rise/fall time is not instantaneous, causing additional losses, etc.

Although we can try to mathematically model all of these to improve the accuracy of our hand-derived optimization equations, with such wide varieties in the methods to design and tune modern Class-E power amplifiers (e.g., [7], [12], [15], [22]–[24], [26], [44]–[48]), doing so is impractical. A better solution is to have a good and accurate simulation-ready model for all the loss components such that one can quickly optimize their design via a circuit simulation program.

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A. Distributed loss equation for the C_{oss} loss

While passive component losses, gating related losses (e.g., gating loss, turn off loss etc.), and conduction loss (sans dynamic $R_{ds,on}$) can all be easily modeled in a simulation software, the C_{oss} loss cannot yet be readily simulated. This is because the Steinmetz-like C_{oss} loss equation, equation (5), gives a value for the average loss, not an instantaneous one.

According to [29]–[31], the C_{oss} loss is due to the hysteresis effect of the junction capacitance, and its magnitude increases with both the peak voltage and the dv/dt. By the same reasoning used in the derivation of the generalized Steinmetz equation (GSE) which is used to model non-linear core losses in magnetic with a non-sinusoidal input [49], we propose an instantaneous power dissipation equation, $p(t)$, for the C_{oss} loss in a Class-E amplifier as

$$p(t) = k_1 \left| \frac{dv_{ds}(t)}{dt} \right|^{(\alpha+1)} v_{ds}(t)^{(\beta-\alpha-1)}. \tag{12}$$

Notice that we choose the power terms of this equation so that its frequency dependency, $1/dt^{(\alpha+1)}$, and its voltage dependency, $dv_{ds}^{(\alpha+1)} \cdot v_{ds}^{(\beta-\alpha-1)}$, default to those of the equation (5).

To find the value of k_1, we find the time average of this $p(t)$ equation for the Class-E waveform by substituting in the v_{ds} from the equation (3).

$$\begin{aligned}\langle p(t) \rangle =& \frac{1}{\omega T} \int_0^{\omega T} k_1 \left| \frac{dv_{ds}(t)}{dt} \right|^{(\alpha+1)} v_{ds}(t)^{(\beta-\alpha-1)} d(\omega t) \\ =& \frac{k_1 (2\pi)^{\alpha}}{\left(2 \operatorname{atan}\left(\frac{2}{\pi}\right)\right)^{\beta}} V_p^{\beta} f^{(\alpha+1)} \int_{\pi}^{2\pi} \left| \sqrt{1+\frac{\pi^2}{4}} \cdot \ldots \right. \\ & \left. \sin\left(\phi - \operatorname{atan}\left(\frac{2}{\pi}\right)\right) + 1 \right|^{(\alpha+1)} \left[\phi - \frac{3\pi}{2} - \ldots \right. \\ & \left. \sqrt{1+\frac{\pi^2}{4}} \cdot \cos\left(\phi - \operatorname{atan}\left(\frac{2}{\pi}\right)\right) \right]^{(\beta-\alpha-1)} d\phi \end{aligned}$$

Since this time average power dissipation must be equal to that of the equation (5), we get

$$\langle p(t) \rangle = k_e f^{(\alpha+1)} \ V_p^{\beta}.$$

Thus,

$$k_1 = \frac{\left(2 \operatorname{atan}\left(\frac{2}{\pi}\right)\right)^{\beta}}{(2\pi)^{\alpha}} \frac{k_e}{\displaystyle\int_{\pi}^{2\pi} \left| \ldots \right|^{(\alpha+1)} \left[\ldots \right]^{(\beta-\alpha-1)} d\phi}. \tag{13}$$

For GS66504B, $k_1 = 1.3 \times 10^{-16}$ W/Hz·V.

B. GSE-based C_{oss} loss model implementation in a circuit simulation

With the proposed instantaneous power dissipation equation, we can quickly create a loss model compatible with most simulation software. Below is one way to implement this C_{oss} loss as a sub-circuit in LTspice using the behavioral current source.

```
.subckt  G66504B_Pcoss  drain  source
  BI1  drain  source
  I = (time>9u)*((k1*pow((abs(ddt(V(drain)))), (alpha+1))*
      pow(V(drain), (beta-alpha-1))))/(V(drain) + 1000*
      (V(drain)<0.1*Vin))
.ends
```

In this sub-circuit, the multiplier term (time>9u) is used to increase the simulation speed by excluding the C_{oss} loss term from the start-up part of the simulation. Furthermore, the term 1000*(V(drain) < 0.1*Vin) is used to null the C_{oss} loss during the on-time of the switch.

IV. Design Examples

In this section, we will provide two design examples to demonstrate how the analytical equations and the distributed C_{oss} loss model can be used to optimize the design of Class-E amplifiers.

A. Design A: Choke-input Class-E

The first example we will look at is for a choke-input Class-E power amplifier. For this design example, we assume that the circuit is to operate at 10 MHz with 120 V input and nominal output power of 200 W to a 50 Ω load. Since the 50 Ω load is not the same as the nominal load needed by the Class-E circuit, a low-pass matching network is added to the output. Figure 2 shows its schematic.

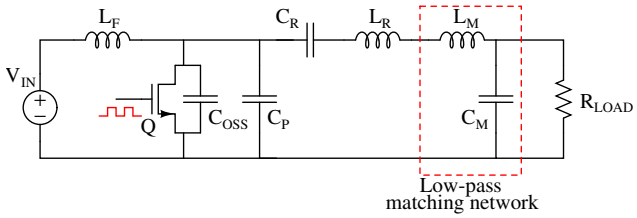

Fig. 2: The schematic of a standard choke-input Class-E power amplifier with a low-pass matching network at the output.

The question we would like to answer is, given these design specifications, what size of GS6650xx should we use as the main power switch to get the best efficiency?

1) Analytical calculation

To find the optimal device size, we can use the m_{opt} equation, equation (9). If we assume that GS66504B is the nominal ($m = 1$) device, by plugging in above design specifications along with parameters from table I, we get

$$m_{opt} = \sqrt{\frac{rR_{on}}{k_e p^{\beta} f^{(\alpha+1)}}} \frac{P_{in}}{V_{in}^{\frac{(\beta+2)}{2}}} = 0.95.$$

This means that the optimal device is the same as the nominal device (GS66504B).

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2) Optimization in simulation

To confirm our hand calculation, we simulate four different choke-input Class-E power amplifier circuits with four different devices from the GS6650xx series. The design procedure starts with the standard Class-E equations as outlined in [2]. Then, we adjust component values to take into account passive/active component losses and non-linearity of the C_{oss}. Finally, we add the low-pass matching network to match the output impedance to the required 50 Ω load.

The distributed loss model, shown in section III-B, and its scaled version are used to model the C_{oss} loss. The drain-to-source resistance of the GaN HEMTs models is adjusted to reflect the 2.5× dynamic on-resistance multiplier as discussed in section II-B1. Furthermore, the gate rise/fall time of 4 ns are also used to mimic the actual gate transitions. This allows us to capture both the extra loss due to the higher on-resistance during the gate transition periods, as well as the turn off loss due the the current fall time.

From our experience, this 4 ns time roughly approximates the best gate rise/fall time one can get with the currently commercially available gate driver and standard PCB layout technique for this frequency and power level. The actual gate rise/fall time of the tested devices will differ from this assumed value depending on the input capacitance of the device (e.g., GS66508T will have longer gate rise/fall time than GS66502B). However, the resulting difference in the power loss between each device due to this fall time disparity is small at this operating frequency and is neglected in this design step (more on this in appendix C).

To make a fair comparison and to simplify the experimental testing procedure, the same passive components are used in all four simulated circuits. This results in slight differences between the input/output powers among the amplifiers. Nonetheless, this will ensure that any efficiency differences we measure will come solely from the difference in the devices used. Table II shows the resulting component values which are shared by the four Class-E amplifiers.

TABLE II: Operating condition and shared passive component values for the simulated choke-input Class-E power amplifier circuits.

V_{in} [V]	$L_f(Q)$ [μH]	$L_r(Q)$ [μH]	$L_m(Q)$ [nH]	C_r [pF]	C_m [pF]	R_{load} [Ω]
120	10 (∞)	1.13 (300)	398 (300)	568	331	50

Table III presents the simulation results, the break down of the losses, along with the value of C_p used to achieve ZVS in each circuit. As can be seen, the simulation results match the hand calculation well, with GS66504B having the highest efficiency of 96.6%. While the overall efficiency difference seems small due to all four circuits having very high efficiency, the predicted power dissipation difference between the optimal device (GS66504B) and the biggest device (GS66508T) is more than 1.5 times larger.

B. Design B variable-resistance Class-E

The second example we will look at is for a variable-resistance Class-E power amplifier [46] shown in figure 3.

TABLE III: Simulation results for the four choke-input Class-E power amplifiers at 10 MHz and 200 W (nominal power) with different switching devices, from the smallest device (left) to the biggest device (right).

Q		GS66502B	**GS66504B**	GS66506T	GS66508T
V_{peak}	[V]	410	450	500	540
C_p	[pF]	130	88	45	15
P_{out}	[W]	179.0	192.1	205.8	210.5
P_{in}	[W]	186.1	198.9	214.0	220.3
P_{cond}	[W]	3.6	2.0	1.5	1.4
P_{coss}	[W]	0.7	1.7	3.3	5.0
$P_{fet,tot}$	[W]	4.3	**3.7**	4.8	6.4
$Eff.$	[%]	96.2	**96.6**	96.2	95.6

By forgoing the zero-dv/dt-switching condition, utilizing the input inductor, L_f as a resonating inductor, as well as adding series-parallel resonant filters at the output, Roslaniec et al. were able to tune the Class-E amplifier to maintain ZVS over a wide load range.

There are three main reasons we select this specific Class-E topology as the second example.

1) It is one of the modern Class-E tunings that has the potential to be adopted into many applications, making this a more realistic design example.
2) Its tuning differs greatly from the standard choke-input Class-E amplifier analyzed in section II.
3) Its load-independency allows us to easily compare circuits with the different input voltages at the same output power level.

For this design example, we assume that the circuit is to operate at 40.68 MHz with the maximum output power of 300 W and the nominal output power (where the circuit is to be optimized for) of 200 W. To simplify the comparison, the R_{load} is allowed to be of any value. Furthermore, due to thermal consideration, the GS66504B ($R_{\theta JC} = 1$ C/W) is chosen as the main power switch over its smaller cousin, the GS66502B ($R_{\theta JC} = 2$ C/W).

The question we would like to answer is, given these design specifications and the device choice, what input voltage should we use to get the best efficiency?

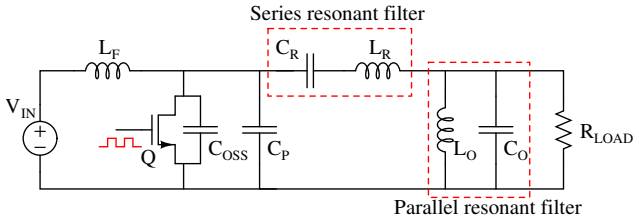

Fig. 3: The schematic of a variable-resistance Class-E power amplifier with a series-parallel resonant filter at the output.

1) Optimization in simulation

Since this variable-resistance tuning deviates heavily from the standard Class-E amplifier assumption, it is better to use the circuit simulation to optimize the design. To find the optimal input voltage, we simulate five different circuits with five input voltages from 85 V to 145 V. We follow the design

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TABLE IV: Operating conditions and shared passive component values for the simulated variable-resistance Class-E power amplifier circuits.

FET	$L_f(Q)$ [nH]	$L_r(Q)$ [nH]	$L_o(Q)$ [nH]	C_r [pF]	C_o [pF]
GS66504B	per tab. V (400)	386 (500)	78 (500)	39	196

procedure for the variable-resistance Class-E power amplifier as described in [46]. Specifically, $k_f = 0.5$ is used to select the value of the input inductor, L_f. Instead of tuning five separate output filters for the five circuits, one combined series-parallel resonant output filter covering the whole tested load range is used for the ease of the testing. The filter is designed such that it has the $Q_s = 4$ at $R_{min} = 25$, and $Q_p = 4$ at $R_{max} = 200$. Calculated parameters are then slightly adjusted on the simulation. Once again, the 2.5× dynamic on-resistance multiplier and 4 ns gate rise/fall time are used. Table IV shows the resulting component values which are shared by the five Class-E amplifiers.

Table V presents the simulation results, the break down of the losses, along with the value of L_f, C_p, and R_{load} used. In each case, the C_p is carefully adjusted to achieve ZVS, and R_{load} is selected to obtain approximately 200 W of output power. As expected, the conduction loss decreases as the input voltage gets higher, while the C_{oss} loss increases. The simulated efficiency is predicted to have the highest value of 88.2% at the input voltage of 100 V. Again, the predicted power dissipation difference in the switch, $P_{fet,tot}$, between the optimal case (100 V_{in}) and the highest input voltage case (145 V_{in}) is more than 1.5 times.

TABLE V: Simulation results for the five variable-resistance Class-E power amplifiers at 40.68 MHz and 200 W (nominal power) with different input voltages, from the lowest voltage (left) to the highest voltage (right).

V_{in}	[V]	85	**100**	115	130	145
V_{peak}	[V]	290	345	410	510	600
L_f	[nH]	42	57	76	97	121
C_p	[pF]	145	100	65	36	20
R_{load}	[Ω]	44	61	82	115	145
P_{out}	[W]	194.5	197.0	199.9	198.6	203.7
P_{in}	[W]	222.4	223.4	227.9	232.0	243.6
P_{cond}	[W]	15.1	11.1	8.8	6.3	5.1
P_{coss}	[W]	7.5	9.8	13.0	20.0	26.9
$P_{fet,tot}$	[W]	22.6	**20.9**	21.9	26.3	31.9
$P_{Lf} + P_{Lr} + P_{Lo}$	[W]	4.6	4.8	5.2	6.1	7.0
$Eff.$	[%]	87.5	**88.2**	87.7	85.6	83.6

V. Experimental Results

To verify our mathematical analysis and the proposed GSE-based loss modeling technique, two experiments following the design examples above are demonstrated in this section.

Experimental and measurement setups

To minimize the effect of the temperature dependency as much as possible, we use a 1/4-inch-thick copper heat spreader with a 3 mm-diameter-1.6 mm-tall copper post at its center to cool the device. This copper post goes through a drill hole on the printed circuit board, and is soldered directly to the thermal pad of the tested GaN HEMT providing a very low thermal resistance path. We then utilize a cold plate with a water cooling system to keep the copper bar at the room temperature.

To sufficiently drive the gate of the tested GaN HEMTs, a low-side gate driver, LM5114 from Texas Instruments, is used. We place the gate driver as close as possible to tested switch to minimize the loop inductance in the gate, as well as use a gate resistor of 2.4 Ω to minimize the ringing.

All inductors used in the experiments are of air-core type and are made with 12 AWG magnet wire. Their impedances and quality factors are measured with a network analyzer, Agilent E5061B. Each inductor is made as big as reasonably possible to obtain a high quality factor. To minimize any coupling between the inductors, adjacent inductors are positioned 90° from each other. All resonant capacitors used are of the C0G type with appropriate voltage rating, with quality factors of above 2000 at the operating frequency.

The input power is calculated from the input voltage and current, where the input voltage is measured with a digital multimeter, Agilent 34411A, and the input current is recorded from the readout of the dc power supply, Agilent N5771A. The output power is measured via a directional coupler/ power meter setup. The setup consists of a calibrated 4-port RF directional coupler, C5827-10, from Werlatone Inc., two N8482A thermocouple power sensors from Keysight Technologies, and an N1914A EPM series power meter from Keysight Technologies. The whole setup has an absolute accuracy (power linearity) of ±1%.

All measurements are done once the device has reached its thermal steady state. To minimize the random measurement error as much as possible, each circuit is tested five times. Their average measurement values are used. The case temperature of the switch is also recorded via a thermal camera and used to verify the electrical measurements.

A. Experiment A: Choke-input Class-E

In this experiment, we investigate what size of GS6650xx will give the best efficiency, given the specification as described in the design example IV-A.

TABLE VI: Operating conditions and shared passive component values for the tested choke-input Class-E power amplifier circuits.

V_{in} [V]	f [MHz]	$L_f(Q)$ [μH]	$L_r + L_m(Q)$ [μH]	C_r [pF]	C_m [pF]	R_{load} [Ω]
120	10	12.8 (630)	1.51 (310)	568	330	50

Four choke-input Class-E power amplifier circuits with four different devices are made and tuned. Their shared component values are shown in table VI. To maintain a fair comparison, all four circuits share these same physical components, which are moved from board to board throughout the testing process. Figure 4 shows one of the circuits mounted on the copper heat spreader.

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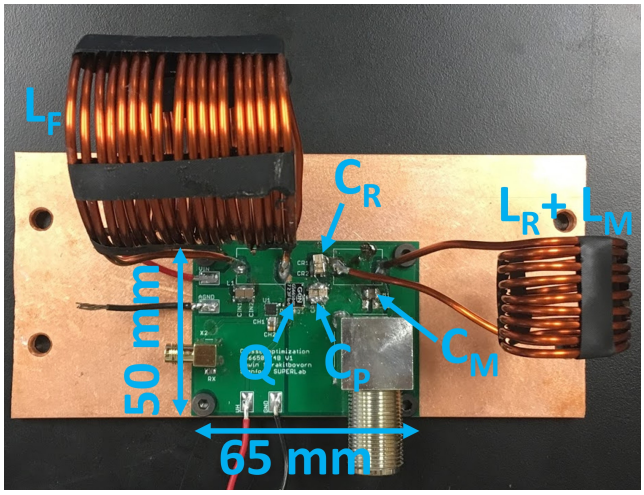

Fig. 4: One of the tested choke-input Class-E power amplifier circuit with the GS66504B HEMT.

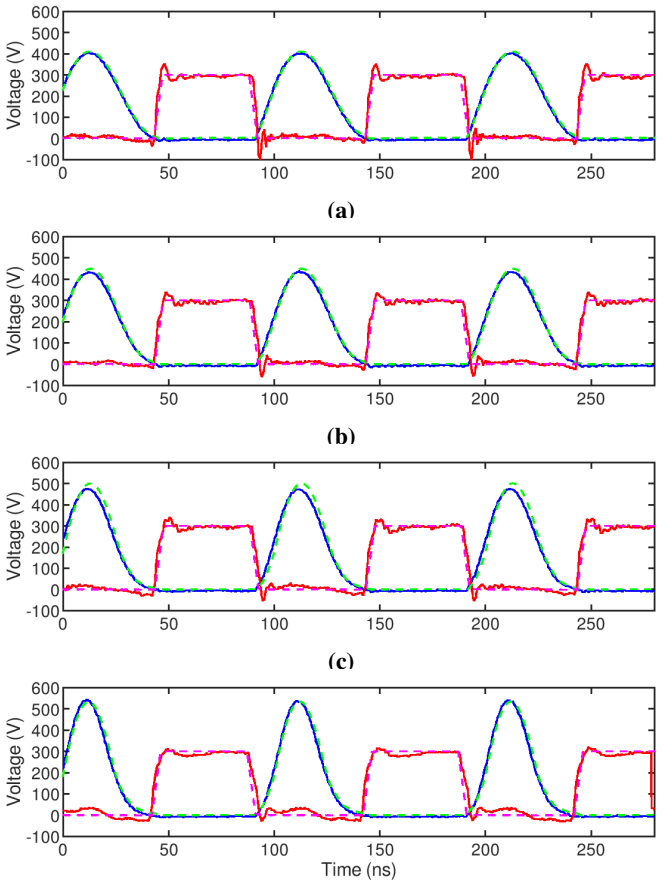

Fig. 5: Comparison between the measured and simulated drain voltage (blue and green - 1x) and gate voltage (red and pink - 50x) waveforms from the experiment A with choke-input Class-E power amplifiers. (a) GS66502B, (b) GS66504B, (c) GS66506T, (d) GS66508T.

Each circuit is carefully tuned by adjusting the value of C_p to achieve perfect ZVS. Figure 5 shows their measured drain and gate voltage waveforms and compare them to their simulated counterparts. Table VII shows the experimental results. The input and power powers, along with the device temperatures, are measured and recorded as described in the experimental and measurement setups section.

TABLE VII: Experimental results for the four choke-input Class-E power amplifiers at 10 MHz and 200 W (nominal power) with different switching devices, from the smallest device (left) to the biggest device (right).

DUT	GS66502B	**GS66504B**	GS66506T	GS66508T
V_{peak} [V]	410	430	480	530
C_p [pF]	133	86	49	12
P_{out} [W]	197.3	213.6	222.4	241.7
P_{in} [W]	204.6	220.6	230.4	251.4
P_{loss} [W]	7.3	7.0	8.0	9.7
P_{gate} [W]	0.24	0.3	0.3	0.36
T_{fet} [C]	25.7	**25.0**	26.0	27.1
Eff [%]	96.5	**96.8**	96.5	96.1

B. *Experiment B: Variable-resistance Class-E*

In this experiment, we investigate what input voltage will give the best efficiency, given the specification as described in the design example IV-B.

TABLE VIII: Operating conditions and shared passive component values for the tested variable-resistance Class-E power amplifier circuits.

f [MHz]	FET	$L_r(Q)$ [nH]	$L_o(Q)$ [nH]	C_r [pF]	C_o [pF]
40.68	GS66504B	386 (550)	77 (450)	39	196

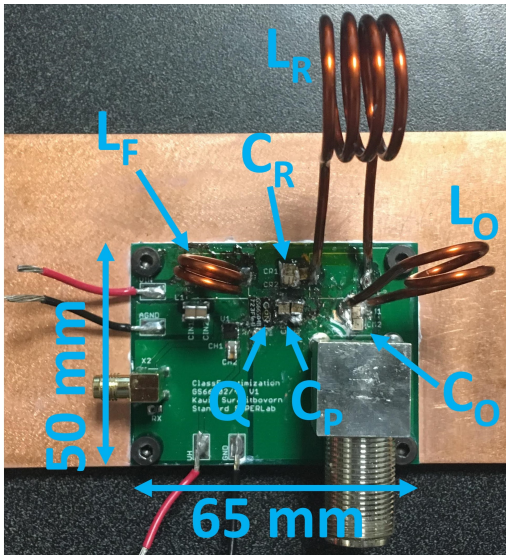

Fig. 6: One of the tested variable-resistance Class-E power amplifier circuit with L_f = 56.5 nH.

Five variable-resistance Class-E power amplifier circuits with five different input voltages are made and tuned. To maintain a fair comparison, all five circuits are made on the same board with the same switching device (GS66504B). The same series-parallel output filter with values described in table VIII are used throughout the testing. Figure 6 shows one of the circuits mounted on the copper heat spreader.

To precisely adjust the load resistance, R_{load}, such that 200 W of output power is achieved in each case, a separate

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automatic matching network is used. This matcher allows us to generate any resistance and reactance at the test frequency in a precise and controlled manner.

To eliminate extra loss contribution from the matching network, the output power measurement is taken as the out power from the amplifier going into the matching network.

$$P_{out} = P_{fwd} - P_{ref}$$

Each circuit is carefully tuned by adjusting the value of C_p to achieve perfect ZVS. Figure 7 shows their measured and simulated drain and gate voltage waveforms. Table IX shows the experimental results.

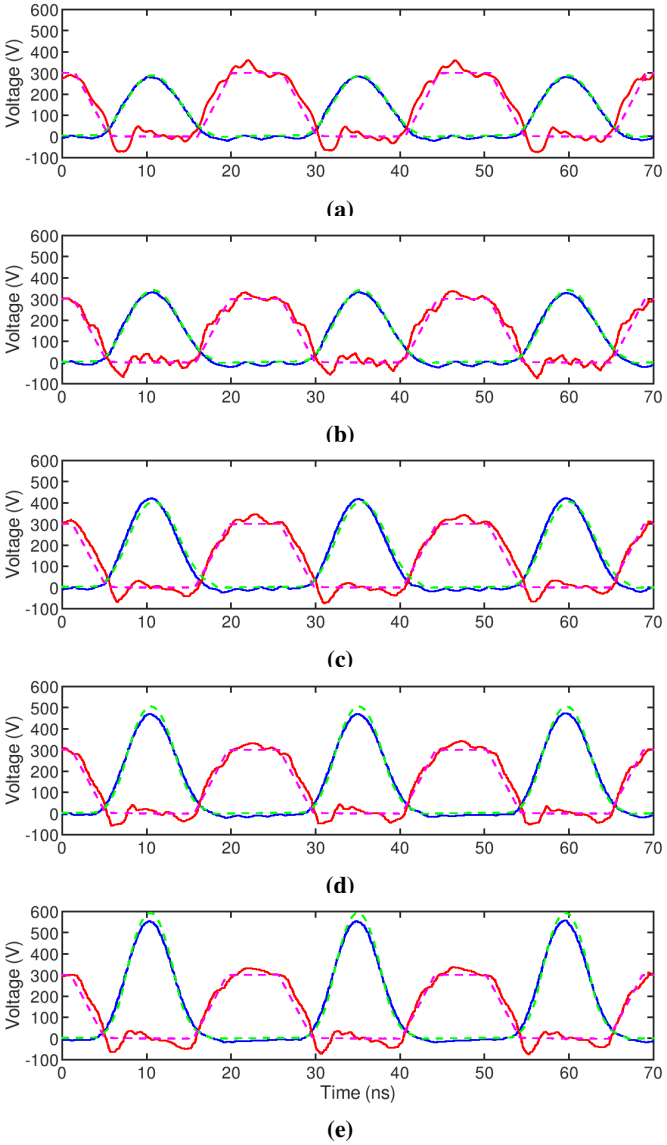

Fig. 7: Comparison between the measured and simulated drain voltage (blue and green - 1x) and gate voltage (red and pink - 50x) waveforms from the experiment B with variable-resistance Class-E power amplifiers. (a) 85 V, (b) 100 V, (c) 115 V, (d) 130 V. (e) 145 V.

TABLE IX: Experimental results for the 5 variable-resistance class-E power amplifiers at 40.68 MHz and 200 W (nominal power) with different input voltages, from the lowest voltage (left) to the highest voltage (right).

V_{in} [V]	85	100	**115**	130	145
V_{peak} [V]	290	330	420	470	560
L_f [nH]	41.5	56.5	76	96	120
C_p [pF]	160	101	57	39	15
R_{load} [Ω]	40	53	77.5	101	130
P_{out} [W]	199.5	198.6	198.5	195.6	195.6
P_{in} [W]	228.6	223.9	223.1	221	224.8
P_{loss} [W]	29.1	25.3	24.6	25.4	29.2
T_{fet} [C]	40.9	36.7	**36.4**	37.5	40.8
Eff [%]	87.3	88.7	**89.0**	88.5	87.0

VI. Comparison between the simulation and the experimental results

A. Case A: choke-input Class-E

The experimental results for the optimal device of a choke-input Class-E at 10 MHz in table VII match the analytical and simulation results well. All three pinpoint the GS66504B, which has half the die area of the biggest device that can be used, as the optimal device. With this device, the simulation predicts the efficiency of 96.6% and the experiment shows the efficiency of 96.8%.

As seen in figure 5, the measured waveforms also match the simulated waveforms well. When comparing the input/output power between the simulation and the experiment, however, a 10 - 15% difference in power is observed. We believe that this to be the result of the added output capacitance across the load due to the oscilloscope probe used to capture the output voltage waveforms (which are not shown in figure 5). Figure 8 shows the difference between the measured and simulated efficiency. For all tested devices, this difference is less than 0.6%.

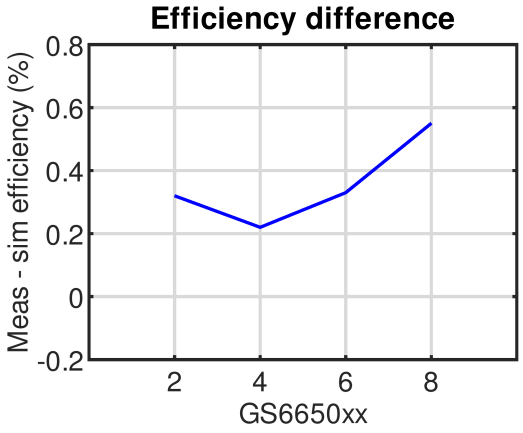

Fig. 8: The difference between the measured and simulated efficiency for the experiment A with choke-input Class-E at 10 MHz.

While the difference in the measured efficiency between the optimal device and the other tested devices is less than 1%, certainly within the error limit of the electrical measurement setups, we believe the relative values between measurements to be accurate. This is due to the fact that while the power meter/sensors setup has its absolute accuracy down to only

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1%, its inaccuracy comes mainly from the non-linearity of the sensors.

As a result, rather than having a random Gaussian distribution of error around its true value, the measured value differs from its true value by one non-random factor. And since all of the measurements are at the same power level and frequency, we believe that this error factor will be close to the same across all measurements. Thus, the relative values between measurements, which tell us which device performs the best, can still be trusted even though the absolute efficiency value is subjected to the 1% error.

The temperature measurement showing the electrically measured optimal device having the lowest case temperature further supports our belief.

B. Case B: variable-resistance Class-E at 40.68 MHz

The experimental results for the optimal input voltage of a variable-resistance Class-E at 40.68 MHz in table IX deviates slightly from the simulation results, showing the optimal input voltage of 115 V instead of the simulated value of 100 V. Nonetheless, the results clearly show that the circuit efficiency is improved by using an input voltage lower than the maximum voltage the device can withstand. In this case, the peak voltage of the optimal design is at only 65% of the maximum drain voltage.

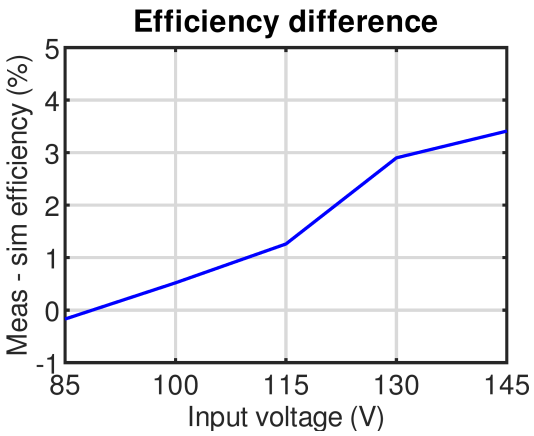

Fig. 9: The difference between the measured and simulated efficiency for the experiment A with variable-resistance Class-E at 40 MHz.

Figure 9 shows the difference between the measured and simulated efficiency. At all but the lowest input voltages, the experimental results show higher efficiency than the simulation, with the discrepancy growing larger (up to 3.4%) the higher input voltage becomes. We speculate that this might be caused by a combination of three factors.

1) The difference between the actual profile of the non-linear junction capacitance, C_{oss}, and that of the manufacturer provided device model causing the simulation to over-predict the peak voltage and C_{oss} loss.

2) The temperature dependency of the C_{oss} loss that was not accounted for in the original Sawyer-Tower testing in [29] causing the proposed Class-E C_{oss} loss equation in [31] to over-predict at the high frequency and high voltage end.

3) A possible interaction between the C_{oss} loss and the conduction loss when both occur on the same device instead of when they are separately measured one without the other.

Nonetheless, without further intensive testing, we cannot confirm that any of these hypotheses is correct.

VII. Conclusion

This paper analyzes the input voltage selection and device sizing procedure of a Class-E power amplifier when faced with a new loss term called C_{oss} loss. By assuming a semi-ideal Class-E operation, we analytically calculated the optimal input voltage and optimal device sizing equations, to achieve the highest efficiency for given design constraints. For the case of non-ideal class-E circuits as well as class-E variations, we proposed a distributed loss model for the C_{oss} loss, in analogy with the generalized Steinmetz equation, as a convenient way to input this new loss term into the circuit simulation. This method allowed the effect of the C_{oss} loss on the circuit waveform and efficiency to be observed, as well as an optimization via simulation to be done.

In the domain where this C_{oss} loss is a significant part of the overall power loss, the conventional practice of using the highest input voltage and biggest device possible to get the best efficiency is no longer valid. Our mathematical analysis has found that while the highest efficiency will still occur when the highest input voltage is selected, this is only on the condition that the optimal device size for that input voltage is used, not the biggest device possible.

In practice, we sometimes cannot actually use this optimal device size for the highest input voltage. A lot of the time, this optimal device size is smaller than the smallest device commercially available, or it has the maximum current capability that is lower than what is required by the rest of the circuit. In such cases, as we are limited by the device, a new optimal input voltage for that device will need to be calculated to obtain the best efficiency. In many cases, this optimal input voltage will be much lower than the maximum voltage the device can handle.

While the GSE-based C_{oss} loss model is accurate at predicting the C_{oss} loss for the Class-E waveform, we find that this model does not extend well to other resonant topology waveforms with higher harmonics, such as that of a Class-Φ_2. Moreover, while our mathematical analysis and simulation method provided good matches with the experimental results, disparities in the efficiencies were observed at the higher end of voltage and frequency. Therefore, in order to further improve the accuracy of the optimization, more studies into understanding, predicting, and modeling of the C_{oss} loss is still needed.

Appendix A

On a method to derive the Steinmetz C_{oss} loss parameter k_e for the Class-E waveform from the sinusoidal waveform parameter.

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For a given semiconductor device, its Steinmetz-like C_{oss} loss parameters for the Class-E waveform, k_e, α, and β, are essential to the optimization of a Class-E power amplifier. While the paper [31] has included these parameters for some of the commercially available devices, there are still many devices not accounted for.

For some of those devices, we can alternatively find their Steinmetz-like loss parameters for the sinusoidal excitation, k, α, and β, in [30], or extract them from the E_{diss} vs. V_{ds} and $freq.$ plots for sinusoidal excitations in [31]. As for any device not included in those studies, a simple Sawyer's tower measurement can be used to find the device's Steinmetz loss parameters for sinusoidal excitation.

Regardless of how these Steinmetz-like loss parameters for the sinusoidal excitation, k, α, and β, are obtained, here we will show one way to convert them to the Steinmetz loss parameters for the Class-E waveform.

First, let us assume that we have two waveforms with the same peak voltage, V_p, and maximum dv/dt.

One of them is a sinusoidal waveform at the frequency f_s.

$$\left(\frac{dv_{ds}}{dt}\right)_{max}^{sine} = \pi V_p f_s$$

The other one is a Class-E waveform at the frequency f_e.

$$\left(\frac{dv_{ds}}{dt}\right)_{max}^{class-e} = \frac{2\pi}{\operatorname{atan}\left(\frac{2}{\pi}\right)} V_p f_e$$

And since

$$\left(\frac{dv_{ds}}{dt}\right)_{max}^{sine} = \left(\frac{dv_{ds}}{dt}\right)_{max}^{class-e},$$

the two frequencies must relate by

$$f_s = \frac{2\pi}{\operatorname{atan}\left(\frac{2}{\pi}\right)} f_e.$$

Next, let us assume that the Steinmetz-like loss equation for both waveforms are

$$P_{coss,sine} = k f_s^{(\alpha+1)} V_p^{\beta}$$

and

$$P_{coss,e} = k_e f_e^{(\alpha+1)} V_p^{\beta}.$$

Then, their energy dissipation per cycle, E_{diss}, will have to be

$$E_{diss,sine} = k f_s^{\alpha} V_p^{\beta}$$

and

$$E_{diss,e} = k_e f_e^{\alpha} V_p^{\beta}.$$

Note that P_{coss} = E_{diss} per cycle $\times f$.

From the experimental data and normalized dv/dt concept proposed in [30], it can be shown that if two waveforms have the same $(dv/dt)_{max}$ and V_p, they will have the same energy dissipation, E_{diss}, per cycle.

$$E_{diss,e} = E_{diss,sine}$$

Then,

$$k_e f_e^{\alpha} V_p^{\beta} = k f_s^{\alpha} V_p^{\beta}$$

$$k_e f_e^{\alpha} V_p^{\beta} = k \left(\frac{2\pi}{\operatorname{atan}\left(\frac{2}{\pi}\right)} f_e\right)^{\alpha} V_p^{\beta}.$$

Thus,

$$k_e = k \frac{2^{\alpha}}{\operatorname{atan}\left(\frac{2}{\pi}\right)^{\alpha}}.$$

APPENDIX B

Extra examples for selected GaN, Si, and, SiC devices

The following set of tables show the device parameters, the optimal input voltage, the optimal device size, and the capacitance ratio over a range of design parameters for the GaN HEMT GS66504B from GaNSystems.

TABLE X: Steinmetz and other device parameters for the GS66504B.

k_e [W/V·Hz]	α	β	R_{on} [mΩ]	C_{oss} [pF]	$V_{ds,max}$ [V]	$I_{ds,max}$ [A]
7.1×10^{-16}	0.6	1.6	2.5×100	44	650	36

TABLE XI: Optimal input voltage, $V_{in,opt}$, for the GS66504B at different operating frequencies and power levels. Asterisks denote those above 180 V which would cause the peak voltage to exceed the $V_{ds,max}$ of the device.

P / f	25 [W]	50 [W]	100 [W]	200 [W]	350 [W]	500 [W]
1 [MHz]	109	160	*	*	*	*
2 [MHz]	80	117	173	*	*	*
5 [MHz]	53	78	115	169	*	*
10 [MHz]	39	57	84	124	169	*
20 [MHz]	29	42	62	91	124	152
40 [MHz]	21	31	46	67	91	111

TABLE XII: Optimal device size, m_{opt} for a 100 W design at different operating frequencies and input voltage levels. GS66504B is used as the nominal device ($m = 1$).

V_{in} / f	45 [V]	60 [V]	80 [V]	110 [V]	145 [V]	180 [V]
1 [MHz]	18	10	6.2	3.5	2.1	1.4
2 [MHz]	10	6	3.6	2	1.2	0.83
5 [MHz]	4.8	2.9	1.7	0.97	0.59	0.4
10 [MHz]	2.8	1.7	0.99	0.56	0.34	0.23
20 [MHz]	1.6	0.95	0.57	0.32	0.19	0.13
40 [MHz]	0.92	0.55	0.32	0.18	0.11	0.075

TABLE XIII: Capacitance ratio, C_{ratio}, of the optimal device at different operating frequencies and input voltage levels.

V_{in} / f	45 [V]	60 [V]	80 [V]	110 [V]	145 [V]	180 [V]
1 [MHz]	0.31	0.33	0.35	0.37	0.39	0.41
2 [MHz]	0.35	0.37	0.4	0.42	0.45	0.47
5 [MHz]	0.42	0.45	0.48	0.51	0.54	0.56
10 [MHz]	0.49	0.52	0.55	0.58	0.62	0.64
20 [MHz]	0.56	0.59	0.63	0.67	0.71	0.74
40 [MHz]	0.64	0.68	0.72	0.77	0.81	0.85

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The following set of tables show the device parameters, the optimal input voltage, the optimal device size, and the capacitance ratio over a range of design parameters for the GaN HEMT PGA26E19BA from Panasonic.

TABLE XIV: Steinmetz and other device parameters for the PGA26E19BA.

k_e [W/V·Hz]	α	β	R_{on} [mΩ]	C_{oss} [pF]	$V_{ds,max}$ [V]	$I_{ds,max}$ [A]
3.7×10^{-15}	0.5	1.76	2.5×140	33	600	23

TABLE XV: Optimal input voltage, $V_{in,opt}$, for the PGA26E19BA at different operating frequencies and power levels. Asterisks denote those above 165 V which would cause the peak voltage to exceed the $V_{ds,max}$ of the device.

P / f	25 [W]	50 [W]	100 [W]	200 [W]	350 [W]	500 [W]
1 [MHz]	84	121	*	*	*	*
2 [MHz]	64	92	133	*	*	*
5 [MHz]	44	64	92	133	*	*
10 [MHz]	34	48	70	101	136	165
20 [MHz]	25	37	53	77	103	125
40 [MHz]	19	28	40	58	78	95

TABLE XVI: Optimal device size, m_{opt} for a 100 W design at different operating frequencies and input voltage levels. PGA26E19BA is used as the nominal device ($m = 1$). Asterisks denote those where their maximum switch current exceeds the $I_{ds,max}$ of the device.

V_{in} / f	45 [V]	60 [V]	80 [V]	100 [V]	130 [V]	165 [V]
1 [MHz]	12	7	4.1	2.7	1.6	1.1
2 [MHz]	7.2	4.2	2.4	1.6	0.98	0.63
5 [MHz]	3.6	2.1	1.2	0.81	0.49	0.31
10 [MHz]	2.2	1.3	0.73	0.48	0.29	0.19
20 [MHz]	1.3	0.74	0.43	0.29	0.17	0.11
40 [MHz]	0.76	0.44	0.26	0.17	*	*

TABLE XVII: Capacitance ratio, C_{ratio}, of the optimal device at different operating frequencies and input voltage levels. Asterisks denote those where their maximum switch current exceeds the $I_{ds,max}$ of the device.

V_{in} / f	45 [V]	60 [V]	80 [V]	100 [V]	130 [V]	165 [V]
1 [MHz]	0.16	0.17	0.17	0.18	0.18	0.19
2 [MHz]	0.19	0.2	0.2	0.21	0.22	0.22
5 [MHz]	0.24	0.25	0.26	0.26	0.27	0.28
10 [MHz]	0.28	0.29	0.3	0.31	0.32	0.33
20 [MHz]	0.34	0.35	0.36	0.37	0.38	0.39
40 [MHz]	0.4	0.42	0.43	0.44	*	*

The following set of tables show the device parameters, the optimal input voltage, the optimal device size, and the capacitance ratio over a range of design parameters for the Si MOSFET STD3NK80ZT4 from STElectronic.

TABLE XVIII: Steinmetz and other device parameters for the STD3NK80ZT4.

k_e [W/V·Hz]	α	β	R_{on} [Ω]	C_{oss} [pF]	$V_{ds,max}$ [V]	$I_{ds,max}$ [A]
4.3×10^{-14}	0.6	0.95	3.8	22	800	10

TABLE XIX: Optimal input voltage, $V_{in,opt}$, for the STD3NK80ZT4 at different operating frequencies and power levels. Asterisks denote those above 225 V which would cause the peak voltage to exceed the $V_{ds,max}$ of the device.

P / f	25 [W]	50 [W]	100 [W]	200 [W]	350 [W]	500 [W]
1 [MHz]	*	*	*	*	*	*
2 [MHz]	208	*	*	*	*	*
5 [MHz]	126	202	*	*	*	*
10 [MHz]	87	139	222	*	*	*
20 [MHz]	60	95	153	*	*	*
40 [MHz]	41	66	105	168	*	*

TABLE XX: Optimal device size, m_{opt} for a 100 W design at different operating frequencies and input voltage levels. STD3NK80ZT4 is used as the nominal device ($m = 1$). Asterisks denote those where their junction capacitance exceeds the C_{req} of the circuit.

V_{in} / f	60 [V]	90 [V]	120 [V]	150 [V]	180 [V]	220 [V]
1 [MHz]	30	17	11	7.8	5.9	4.4
2 [MHz]	17	9.5	6.2	4.5	3.4	*
5 [MHz]	8.3	4.6	3	*	*	*
10 [MHz]	4.8	2.6	*	*	*	*
20 [MHz]	2.7	*	*	*	*	*
40 [MHz]	1.6	*	*	*	*	*

TABLE XXI: Capacitance ratio, C_{ratio}, of the optimal device at different operating frequencies and input voltage levels. Asterisks denote those where their junction capacitance exceeds the C_{req} of the circuit.

V_{in} / f	60 [V]	90 [V]	120 [V]	150 [V]	180 [V]	220 [V]
1 [MHz]	0.47	0.58	0.68	0.76	0.84	0.93
2 [MHz]	0.54	0.67	0.78	0.87	0.96	*
5 [MHz]	0.65	0.8	0.93	*	*	*
10 [MHz]	0.74	0.92	*	*	*	*
20 [MHz]	0.85	*	*	*	*	*
40 [MHz]	0.98	*	*	*	*	*

The following set of tables show the device parameters, the optimal input voltage, the optimal device size, and the capacitance ratio over a range of design parameters for the SiC MOSFET C3M0075120J from Wolfspeed.

TABLE XXII: Steinmetz and other device parameters for the C3M0075120J.

k_e [W/V·Hz]	α	β	R_{on} [mΩ]	C_{oss} [pF]	$V_{ds,max}$ [V]	$I_{ds,max}$ [A]
1.33×10^{-10}	0	1.32	75	66	1200	80

TABLE XXIII: Optimal input voltage, $V_{in,opt}$, for the C3M0075120J at different operating frequencies and power levels.

P / f	25 [W]	50 [W]	100 [W]	200 [W]	350 [W]	500 [W]
1 [MHz]	42	63	96	145	204	253
2 [MHz]	34	51	78	118	165	205
5 [MHz]	26	39	59	90	125	156
10 [MHz]	21	32	48	73	102	126
20 [MHz]	17	26	39	59	83	102
40 [MHz]	14	21	32	48	67	83

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TABLE XXIV: Optimal device size, m_{opt} for a 100 W design at different operating frequencies and input voltage levels. C3M0075120J is used as the nominal device ($m = 1$).

V_{in} / f	50 [V]	100 [V]	150 [V]	200 [V]	250 [V]	300 [V]
1 [MHz]	2.4	0.76	0.39	0.24	0.17	0.12
2 [MHz]	1.7	0.53	0.27	0.17	0.12	0.086
5 [MHz]	1.1	0.34	0.17	0.11	0.074	0.055
10 [MHz]	0.76	0.24	0.12	0.076	0.052	0.039
20 [MHz]	0.53	0.17	0.086	0.053	0.037	0.027
40 [MHz]	0.38	0.12	0.061	0.038	0.026	0.019

TABLE XXV: Capacitance ratio, C_{ratio}, of the optimal device at different operating frequencies and input voltage levels.

V_{in} / f	50 [V]	100 [V]	150 [V]	200 [V]	250 [V]	300 [V]
1 [MHz]	0.078	0.099	0.11	0.12	0.13	0.14
2 [MHz]	0.11	0.14	0.16	0.18	0.19	0.2
5 [MHz]	0.17	0.22	0.25	0.28	0.3	0.32
10 [MHz]	0.25	0.31	0.36	0.39	0.43	0.45
20 [MHz]	0.35	0.44	0.51	0.56	0.6	0.64
40 [MHz]	0.49	0.62	0.72	0.79	0.85	0.91

APPENDIX C

A. The effect of the turn off (current fall time) loss on on the experiment A.

To make sure that the efficiency difference between the optimal device (GS66504B) and the larger devices (GS66506T and GS66508T) in the experiment A is not coming from the difference in the turn off loss due to the slower gate fall time in the larger devices, we perform an extra experiment. Here, we increase the gate resistance of the circuit in figure 4 to artificially increase the gate fall time of the choke-input class-E circuit with the GS66504B GaN HEMT. Seven different resistance from 2.4 Ω to 12 Ω are used. All the other component values are kept the same as in table VI and VII.

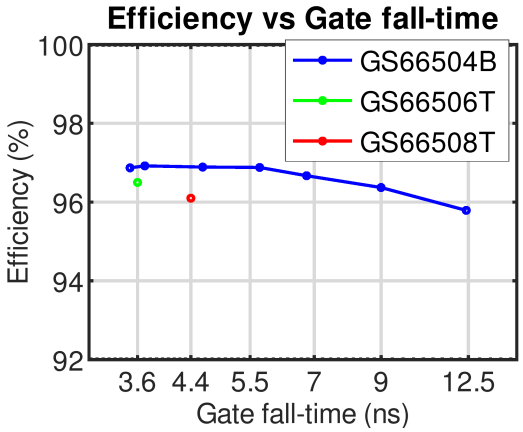
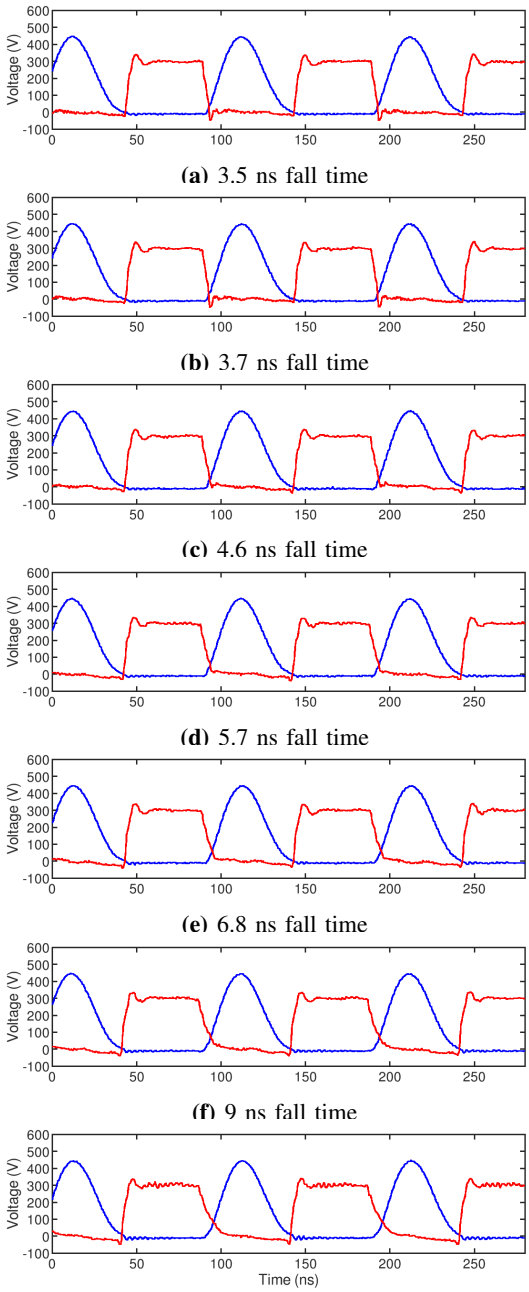


Fig. 10: The measured efficiency vs gate fall time of the choke-input class-E circuit at 10 MHz and 200 W.

The resulting fall time of the gate voltage (90% to 10%) varies from 3.5 ns to 12.4 ns. Figure 10 shows the measured efficiency of the circuit with GS66504B at the different gate fall time and compares them with the efficiency of the circuit with GS66506T and GS66508T from section V-A. Figure 11 shows the measured drain and gate waveforms of the 7 circuits.

As seen from the plot, even when the gate fall time of the GS66504B circuit are increased to equal and even higher to that of the GS66506T (t_{fg} = 3.6 ns) and GS66508T (t_{fg} = 4.4 ns) circuit, the GS66504B efficiency still remains higher than that of the other two. This proves that the superior efficiency of the GS66504B in the experiment A stems from the difference in the C_{oss} loss and not difference in the turn off loss due to the gate fall time.



(a) 3.5 ns fall time

(b) 3.7 ns fall time

(c) 4.6 ns fall time

(d) 5.7 ns fall time

(e) 6.8 ns fall time

(f) 9 ns fall time

(g) 12.4 ns fall time

Fig. 11: The measured drain voltage (blue - 1x) and gate voltage (red - 50x) waveforms from the extra experiment to study the effect of slow gate fall time with choke Class-E power amplifiers.

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Using this data, we can also estimate the magnitude of the turn off loss in the experiment A. Figure 12 plots the overall power loss of the circuit ($P_{in} - P_{out}$) versus the gate fall time. Since the loss in all the other parts of this circuit remains the same, we can curve fit this data to calculate the turn off loss.

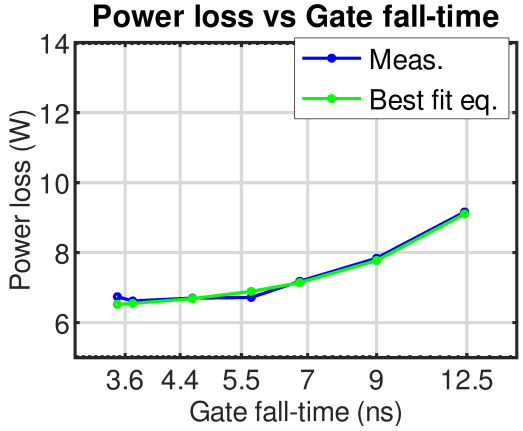

Fig. 12: The measured overall power loss (blue) and the best fit curve (green) vs the gate fall time of the choke-input class-E circuit at 10 MHz and 200 W.

$$P_{loss} = 6.3 + \frac{(2\pi \cdot 10 \times 10^6 \cdot t_{fg}/1.9)^2}{12} \times 200$$

By subtracting away the static part ($t_{fg} = 0\ ns$, we find that

$$P_{tf} = \frac{(2\pi \cdot 10 \times 10^6 \cdot t_{fg}/1.9)^2}{12} \times 200,$$

where t_{fg} is the 90% to 10% gate voltage fall time.

For instance, for the gate fall time of 3.5 ns (the original GS66504B circuit with $R_g = 2.4\ \Omega$), the turn off (fall time) loss is approximately $P_{tf} = 0.22\ W$. Likewise, for the gate fall time of 4.4 ns (the gate fall time of the GS66508T circuit), the turn off (fall time) loss is approximately $P_{tf} = 0.35\ W$.

B. The effect of the turn off (current fall time) loss on on the optimization equations.

While the optimization equations in section II-C works well when the current fall time is small (such as in the experiment A), there are times where this is not the case. To incorporate the fall time loss, P_{tf} into the optimization equations, we can approximate the fall time loss by the equation [50]

$$P_{tf} = \frac{(\omega t_f)^2}{12} P_{in},$$

where t_f is the fall time of the drain current. (This drain current fall time is related but not equal to the fall time of the gate voltage.) Notice that since this fall time loss is independent of the input voltage, it has no effect on the optimal input voltage (eq. 6) and minimum frequency (eq. 7) equations.

To find its effect on the optimal device size equation, we assume that the drain current fall time of the different size device scales linearly with the gate input capacitance. This is the case when the gate voltage fall time is limited by the input capacitance of the device.

With this assumption, we can find that the fall time loss for any device is

$$P_{tf} = m^2 \frac{(\omega t_f)^2}{12} P_{in},$$

where t_f is the fall time of the nominal device and m is the scaling factor used in section II-C.

By adding this term to the overall power loss equation, we find that the optimal device size, m_{opt}, can be calculated by

$$-\frac{rR_{on}}{m_{opt}^2}\frac{P_{in}^2}{V_{in}^2} + k_e f^{(\alpha+1)}(pV_{in})^\beta + m_{opt}\frac{2}{3}\pi^2 f^2 t_f^2 P_{in} = 0.$$

Unfortunately, this is a 3rd degree polynomial equation with no concise solution.

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