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This paper has been accepted for publication by

IEEE Journal of Emerging and Selected Topics in Power Electronics.

DOI
10.1109/JESTPE.2020.3011658

Citation
K. Surakitbovorn and J. Rivas-Davila, "A Simple Method to Combine the Output Power from Multiple Class-E Power Amplifiers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2020.3011658.

IEEE Xplore URL
https://ieeexplore.ieee.org/document/9146859

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A Simple Method to Combine the Output Power from Multiple Class-E Power Amplifiers

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***Abstract*—Radio frequency (RF) power amplifiers are an integral part of many academic, medical, and industrial applications. For many of these applications, the required power level is high enough such that a single amplifier circuit cannot provide enough power, and multiple amplifiers are needed. Conventionally, a power combiner network is used to isolate any mismatch between the multiple power amplifiers combining their output powers. However, these power combiner networks have their disadvantages, including additional loss and an increase in overall system size.**

In this paper, we present an alternative approach to designing a high-efficiency high power RF amplifier system. Here, we offer a simple tuning method that allows output powers from multiple power amplifiers to be combined directly without the need for an extra combiner network, given that the mismatches between the amplifiers are sufficiently small. The method is specifically developed for class-E power amplifiers at kilowatts power level and is demonstrated with a 1500 W 40.68 MHz power amplifier design utilizing six sub-circuits directly combining power.

***Index Terms*—Power combining, class-E amplifier, RF power amplifier, RF generator, gallium nitride (GaN)**

I. Introduction

Radio frequency (RF) power amplifiers (PAs) are employed in a multitude of applications ranging from RF communication, medical imaging, industrial plasma generation and processing, etc. Traditionally, linear amplifiers such as class-A, class-B, or class-AB are used because of their design simplicity and linearity. However, as the need for higher efficiency arises, switched-mode designs such as class-D [1]–[3], E [4], [5], F [6]–[8], E/F [9], Φ [10]–[12], etc. have risen in popularity. Unlike a linear PA, switched-mode design can reach very high efficiency but falls short with regards to input/output linearity [13].

Depending on the operating frequency and the amplifier design, a single power amplifier will always be bounded in output power by various limiting processes that include thermal design, package parasitics, device current/voltage capability, etc. When the power required in the system exceeds that which a single power amplifier circuit can generate, multiple power amplifiers are needed [14], [15]. To create a single output port, the output powers from these amplifiers have to be electrically combined. When the amplifiers are identical and driven with exactly the same inputs, it is possible to combine their output powers directly without the need for any added combiner network. At low enough frequency ($<$ 5 MHz), this is achievable with a good layout and a tight component variation control. However, at higher frequency (10+ MHz), any slight mismatch between the amplifiers, either due to variation in the component values or the input signal timing, can cause serious problems to direct connection.

To avoid problems that come from this mismatch, a separate power combiner network is typically employed to combine the output powers from two or more power amplifiers. There are many ways to create a power combiner network. The most conventional approach is to use an isolating combiner [16]. In its most common form, an isolating power combiner network consists of two input ports, one output port, and one isolated port, as shown in fig. 1. The matched portions of the input powers are combined and sent to the output port. The mismatched portions of the input powers are isolated out and sent to the isolated port. Conventionally, this is then dissipated away as heat on an isolation resistor; however, it can also be recovered back through a rectifier to improve the overall system efficiency [17]–[19].

Another approach to power combining is to use a lossless non-isolating combiner network where the isolation port is not needed. The most well-known circuit for this type of combiner is the classic Chireix combiner [16], [20], [21], but other non-isolating combiner typologies with improved performance have also been proposed [13], [22]–[24].

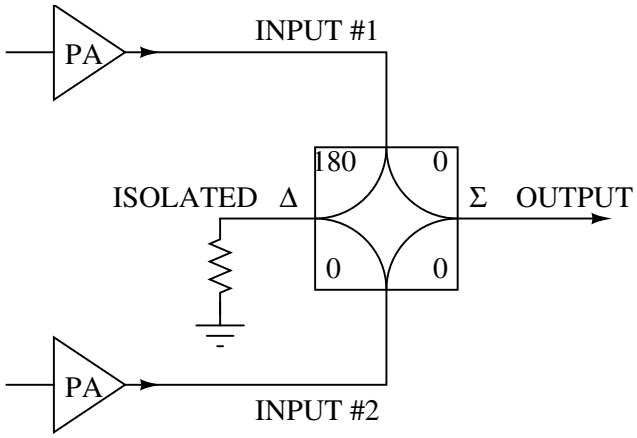

Fig. 1: A typical power combiner circuit consists of 2 input ports, 1 output port, and 1 isolated port.

While using power combiner networks is a good solution to the mismatch problem when one needs to combine the power from multiple amplifiers, they do present their own disadvantages. Regardless of the type, a combiner network consists of inductors, capacitors, or transmission lines. Under operation, each of these components will present their associating loss due to their parasitic resistances. Thus, even with perfectly

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matched inputs, a "lossless" combiner network is never truly lossless, causing the efficiency at the combined output to always be slightly lower than the original efficiency of each power amplifier. Furthermore, for applications where space is limited or where weight is critical (e.g., RF communication for cell-phones and micro-satellite propulsion), these components do take up extra valuable space and add excess weight to the system. For certain types of combiner networks, the number of combinable power amplifiers must also follow a binary sequence ($2^N = 2, 4, 8, 16...$), limiting the design freedom.

In this work, we present an alternative approach to the problem of power combining. Here, we offer a simple methodology to tune and operate individual PA stages that allows their output powers to be combined directly without the need for additional power combiner networks. This method eliminates the extra loss associated with the combiner network, reduce the system size and weight, as well as allowing the circuit designer freedom to connect any number of power amplifiers together given that their mismatch is sufficiently small.

Section II of this paper mathematically derives the necessary condition for direct power combining in the proposed tuning method, as well as describes the steps to convert a standard class-E amplifier into a "power-combinable" class-E amplifier. Utilizing this tuning technique, section III demonstrates a continuous wave (CW) 1500 W 40.68 MHz power amplifier design with six class-E amplifiers directly combining power. The system achieves a high dc-to-rf efficiency of 89% and is intended for plasma generation applications. While the equations and method developed in this paper mainly target class-E power amplifiers used in high power (kilowatts level) applications, they can be easily modified to be used with other types of amplifiers at other power levels. Finally, section IV concludes the paper.

II. Power Combining without a Power Combiner

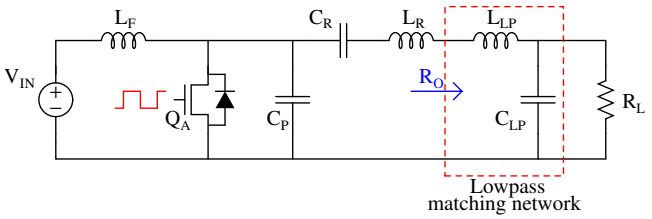

Fig. 2: A typical class-E power amplifier circuit for high power applications utilizing a low-pass matching network at the output.

Fig. 2 shows the schematic of a typical class-E power amplifier circuit for high power applications. Because a class-E amplifier appears as a voltage source, in order to output high power, the output resistance that the amplifier sees, R_O, need to be of a small value. However, in RF applications, the actual load of the circuit, R_L, is commonly a 50 Ω impedance [25]–[27].

As a result, a low-to-high matching network is usually needed to match these two impedances. In this paper, we will demonstrate the case where a low-pass LC matching network is utilized; however, the derived equations can be easily modified for when other types of matching networks are used.

For a low-pass low-to-high LC matching network, the following textbook equations calculate the capacitor and inductor value needed for proper impedance matching [28].

$$C_{LP} = \frac{1}{\omega R_L}\sqrt{\frac{R_L}{R_O} - 1} \tag{1}$$

$$L_{LP} = \frac{R_O}{\omega}\sqrt{\frac{R_L}{R_O} - 1} \tag{2}$$

Instead of tuning the matching network to simply match the load to the optimum impedance the PA can drive as per (1) and (2), here we present an alternative way to pick the inductor and capacitor values. On top of performing impedance matching, this alternative network makes direct power combining possible even when there is a timing mismatch between the power amplifiers. The following sections will explain the derivation of this modified low-pass matching network and how it can be used in a class-E amplifier circuit.

A. Modified Low-Pass Matching Network

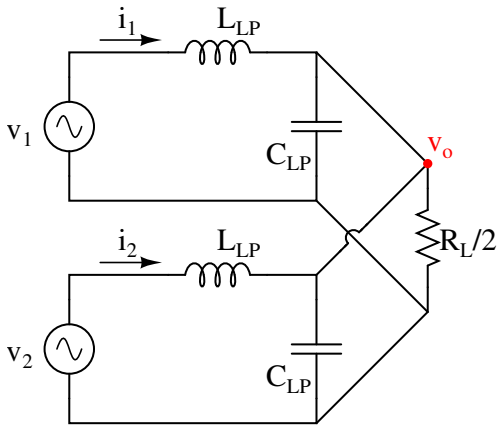

Fig. 3: A simplified circuit representing two amplifiers with LC low-pass networks combining power at the output.

In this section, we will analyze the case with two amplifier circuits combining power; however, the result can be directly applied to any number (2+) of circuits combining power. Fig. 3 shows the simplified circuit with v_o being the output voltage across the combined load, $R_L/2$. To simplify the problem, we will approximate the output of each amplifier as a sinusoidal voltage source with the same amplitude, V. Furthermore, we will assume that due to a small timing mismatch between the gate driving signals of the two class-E circuits, the two voltage sources have a small phase difference, δ.

$$v_1 = Ve^{j(\omega t + \phi_1)}$$

$$v_2 = Ve^{j(\omega t + \phi_2)}$$

$$\delta = \phi_2 - \phi_1 << 1$$

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To minimize the effect of this timing mismatch on the amplifiers, we want to find the L_{LP} and C_{LP} values that allow the output power from each voltage source to remain the same regardless of the change in δ.

To find the output power from the top voltage source, P_1, we first find the output voltage, v_o, by using super-position.

$$v_o = Ve^{j\omega t}(e^{j\phi_1}+e^{j\phi_2})\frac{R_L/2}{(-\omega^2 R_L L_{LP} C_{LP}+R_L+j\omega L_{LP})} \quad (3)$$

Then, we can calculate the top source current, i_1 from

$$i_1 = \frac{v_1 - v_o}{j\omega L_{LP}}.$$

Substituting in v_o from (3) gives

$$i_1 = \frac{Ve^{j(\omega t+\phi_1)}}{j\omega L_{LP}}\left(1-\frac{(1+e^{j(\phi_2-\phi_1)})R_L/2}{(-\omega^2 R_L L_{LP} C_{LP}+R_L+j\omega L_{LP})}\right).$$

The output power from the top source, P_1, can be calculated from

$$P_1 = \mathbf{Re}\left[\frac{v_1 i_1^*}{2}\right].$$

Hence,

$$P_1 = \mathbf{Re}\left[-\frac{V^2}{2j\omega L_{LP}}\left(1-\frac{(1+e^{-j(\phi_2-\phi_1)})R_L/2}{(-\omega^2 R_L L_{LP} C_{LP}+R_L-j\omega L_{LP})}\right)\right].$$

By using a small phase difference approximation, we get

$$P_1 = \mathbf{Re}\left[-\frac{V^2}{2j\omega L_{LP}}\left(1-\frac{(2-j\delta)R_L/2}{(-\omega^2 R_L L_{LP} C_{LP}+R_L-j\omega L_{LP})}\right)\right].$$

Thus,

$$P_1 = \frac{V^2}{2}\frac{\left(R_L+\frac{\delta R_L^2\omega C_{LP}}{2}-\frac{\delta R_L^2}{2\omega L_{LP}}\right)}{(\omega L_{LP})^2+(-\omega^2 R_L L_{LP} C_{LP}+R_L)^2}. \quad (4)$$

To find the condition where P_1 does not change in relative to δ, we set

$$\frac{d}{d\delta}P_1 = 0.$$

As a result, we find that

$$\omega^2 L_{LP} C_{LP} = 1 \quad (5)$$

and

$$P_1 = \frac{V^2}{2}\frac{R_L}{(\omega L_{LP})^2}. \quad (6)$$

By symmetry, the same also applies to the output power from the bottom source, P_2.

Equation (5) means that if we pick the C_{LP} and L_{LP} such that they resonate at the switching frequency, then they will "shield" the circuits from the small timing mismatch between power amplifiers, enabling output power from multiple PAs to be directly combined. Furthermore, (6) also dictates that when C_{LP} and L_{LP} are tuned this way, the output power will be linearly proportional to the load resistance. Essentially, this tuning makes the voltage source appears to the load as a current source.

While this condition on C_{LP} and L_{LP} enables direct power combining, there are infinitely many possible combinations of them. To maintain the impedance matching functionality that the original low-pass matching circuit provides, we have to find the values of C_{LP} and L_{LP} such that the output powers from the two voltage sources, v_1 and v_2, are equal to the original output powers from the conventional matching network in (1) and (2).

In the original case, the impedance looking into the low-pass matching network is R_O. Thus, the original output power from each source is

$$P_{1,ori} = P_{2,ori} = \frac{V^2}{2}\frac{1}{R_O}.$$

By setting $P_{1,ori} = P_1$ from (6), we find that in order to maintain the same power the modified low-pass network must have

$$C_{LP} = \frac{1}{\omega\sqrt{R_L R_O}} \quad (7)$$

$$L_{LP} = \frac{\sqrt{R_L R_O}}{\omega}. \quad (8)$$

Naturally, this choice of C_{LP} and L_{LP} does not guarantee that the input impedance looking into this modified low-pass network will be resistive. In fact, the impedance looking into this network is slightly inductive.

$$Z_{IN} = \frac{R_L}{(1+\omega^2 C_{LP}^2 R_L^2)}+\frac{j\omega(L_{LP}(1+\omega^2 C_{LP}^2 R_L^2)-C_{LP}R_L^2)}{1+\omega^2 C_{LP}^2 R_L^2}$$

$$Z_{IN} = \frac{R_O}{1+\frac{R_O}{R_L}}\left(1+j\sqrt{\frac{R_O}{R_L}}\right) \quad (9)$$

To maintain zero-voltage-switching (ZVS) condition in a class-E amplifier, an extra capacitance should then be added to the C_P to counteract this inductive component.

B. Power-Combinable Class-E Amplifier

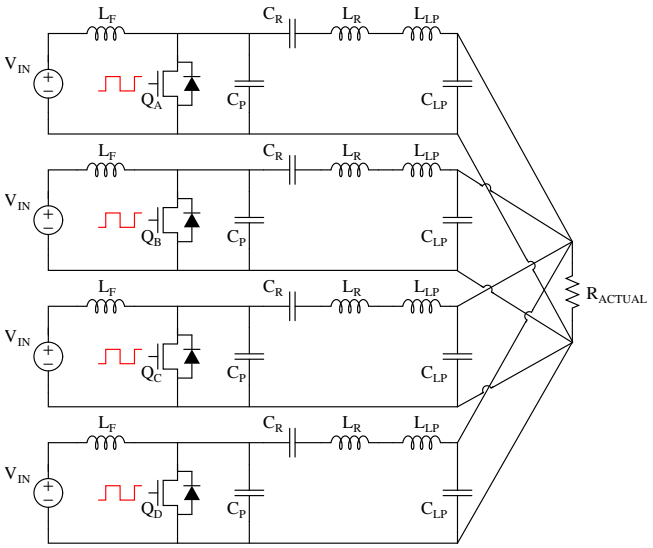

Fig. 4: A system consists of 4 class-E amplifiers combining power at the output.

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In this section, we will describe the tuning steps to create power-combinable class-E amplifiers by utilizing the derived modified matching network. As an example, fig. 4 depicts a system with four power-combinable class-E amplifiers directly combining their power at the output.

The tuning of power-combinable class-E amplifiers starts by selecting the component values, L_F, C_P, L_R, and C_R, as well as the output impedance, R_O, following standard class-E design equations according to the desired operation regime and power level. For example, according to Acar et al., if one wishes to attain the maximum output power from a given switching device, one should use the following component values:

$$\begin{gathered} R_O = \frac{k_P V_{in}^2}{P},\ C_P = \frac{k_C}{\omega R_O},\ L_F = \frac{k_L R_O}{\omega}, \\ L_R = \frac{Q R_O}{\omega},\ C_R = \frac{1}{\omega Q R_O}, \\ (k_P = 1.365,\ k_C = 0.685,\ k_L = 0.732) \end{gathered} \tag{10}$$

where Q is the desired loaded quality factor of the series output filter [29].

Depending on the required actual load impedance, R_{actual}, and the number of circuits to be combined, N, the load impedance each circuit has to be tuned for, R_L, can be calculated from

$$R_L = N \times R_{actual}. \tag{11}$$

Using both the calculated R_O and R_L, we can calculate the modified low-pass component values from (7) and (8).

$$C_{LP} = \frac{1}{\omega\sqrt{R_L R_O}},\ L_{LP} = \frac{\sqrt{R_L R_O}}{\omega}$$

As previously stated, in order to compensate for the added inductive loading due to the modified low-pass network, an extra capacitance, C_{extra}, should be added to the C_P such that ZVS condition is attained. The value of this C_{extra} depends on the type and operation regime of the selected class-E amplifier. However, because ZVS condition in a class-E circuit depends not only on its fundamental contents but also on the exact shape of the drain voltage and current waveforms, the exact value of C_{extra} is best obtained via circuit simulation. Nonetheless, we have empirically found that for a class-E amplifier tuned according to the (10), the following C_{extra} value will result in a very near ZVS condition.

$$C_{extra} \approx C_P \sqrt{\frac{R_O}{R_L}} \tag{12}$$

Thus, the total value of the required parallel capacitance for each maximum output power class-E circuit becomes

$$C_{P,tot.} \approx \frac{k_C}{\omega R_O}\left(1 + \sqrt{\frac{R_O}{R_L}}\right). \tag{13}$$

III. Experimental Demonstration

In this section, we will experimentally demonstrate the design of a 40.68 MHz 1500 W RF amplifier utilizing the proposed power-combinable class-E amplifier circuit. The intended application for this RF amplifier is for plasma generation used in semiconductor processing industries for etching and deposition [30]. In order to reach the desired 1500 W power level while keeping the circuit temperature sufficiently low, we choose to use six identical class-E circuits combining the power to spread out the heat generation due to the loss on the switches. To get the best performance at this high frequency, 650 V GaN transistors, GS66506T(s), from GaNSystems are used as the main power switches.

A. Circuit Design and Simulation

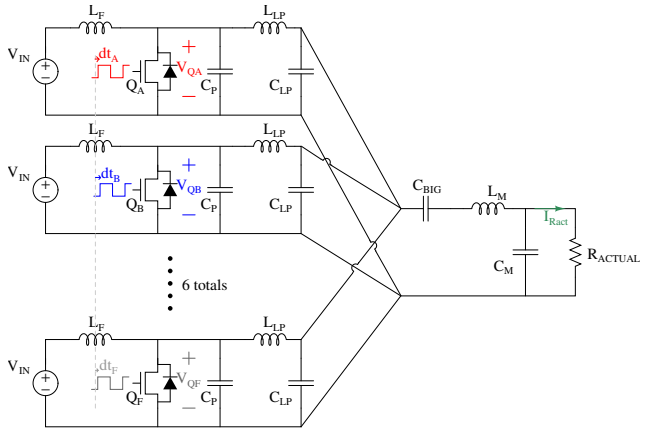

Fig. 5: Six class-E amplifier circuits with double stage low-pass matching networks combining power.

Fig. 5 shows the schematic of the circuit used in this prototype. Here, the terms dt_X(s) represent the timing mismatch/delay between the gating signals of the different amplifiers. There are many causes of this timing mismatch, with the variation of the propagation delays in logic gate and gate driver chips being the most common source. Unlike in section II, here we choose to use two-stage low-pass matching networks in order to keep the quality factors of the matching networks low, making them less sensitive to component variation in an actual circuit. The first stage (L_{LP} and C_{LP}) is tuned according to the proposed modified low-pass network, while the second stage (L_M and C_M) is tuned as a conventional matching network. Furthermore, unlike in the previous section where series LC filters are used to filter out the other harmonic contents, a single large capacitor, C_{BIG}, is used here for dc-blocking. Since the two-stage low-pass network provides adequate filtering, the removal of this series resonant filter serves to further increase the efficiency and reduce the overall size/volume of the circuit.

The general design step follows that which is outlined in section II. However, to take into account losses in the switches and passive components as well as the non-linearity of the junction capacitance of the transistor, we over-design

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the circuit by tuning it with the equation for power level $P = 2000\ W$ instead of 1500 W. This results in the L_F and C_P values that are roughly 30% lower/higher, as well as the L_{LP} and C_{LP} values that are roughly 15% lower/higher than those of an ideal circuit.

We pick the input voltage of the circuit to optimize the circuit efficiency in the face of "off-state" C_{OSS} loss in GaN devices according to [31]–[33]. With 60 V input voltage and 2000 W power, we can calculate from (10)

$$R_O = \frac{k_P V_{in}^2}{P} = \frac{1.365 \cdot 60^2}{2000/6} = 14.7\ \Omega$$

$$L_F = \frac{k_L R_O}{\omega} = \frac{0.732 \cdot 14.7}{2\pi \cdot 40.68 \cdot 10^6} = 42.3\ \text{nH}.$$

In order to keep similar matching ratio (quality factor) of both matching stages, the first stage matching network is tuned to match the 14.7 Ω output impedance of the amplifier (R_O), to a 75 Ω impedance (R_L). Then, the second stage matching network is tuned to match the combined impedance of six 75 Ω in parallel (75/6 = 12.5 Ω) to the actual load impedance of 50 Ω.

Following (7), (8) and (13), we find

$$C_{LP} = \frac{1}{2\pi \cdot 40.68 \cdot 10^6 \sqrt{75 \cdot 14.7}} = 118\ \text{pF}$$

$$L_{LP} = \frac{\sqrt{75 \cdot 14.7}}{2\pi \cdot 40.68 \cdot 10^6} = 130\ \text{nH}$$

$$C_{P,tot.} = \frac{0.685}{2\pi \cdot 40.68 \cdot 10^6 \cdot 14.7}\left(1+\sqrt{\frac{14.7}{75}}\right) = 262\ \text{pF}.$$

TABLE I: Operating condition and component values of the simulated power-combinable class-E amplifier circuits in fig. 5.

V_{IN} [V]	FET	L_F [nH]	C_P [pF]	L_{LP} [nH]	C_{LP} [pF]	L_M [nH]	C_M [pF]	C_{BIG} [nF]	$R_{act.}$ [Ω]
60	GS66506T	42	150	130	115	85	135	4	50

Then, minor adjustment is then made on simulation to achieve the best performance and to take into account the junction capacitance of the switches. Table I summaries the component values used in the simulation. For this simulation, a quality factor of 150 is used for all inductors, while a quality factor of 1000 is used for all capacitors.

To achieve a realistic simulation, we randomly insert a 5% variation in the component values into different passive components. Variation of the gate timing, dt_A - dt_F, of up to 1 ns is also randomly added to the different gate signals to simulate timing mismatch. From our experience and in consistent with device datasheets [34], [35], this number is a good approximation for typical variation in gate timings due to the propagation delays in the discrete ICs unless intensive component matching is performed.

Fig. 6 shows the simulated drain waveforms across the six switches, as well as the sinusoidal output current across the 50 Ω load. Notice that due to the introduced component value and timing variation, the drain waveforms from each of the

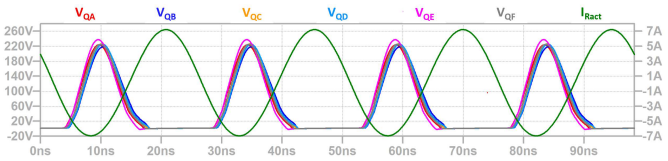

Fig. 6: The drain waveforms (red/blue/orange/sky-blue/magenta/grey) and output currents (green) of the simulated power-combinable class-E amplifier circuits.

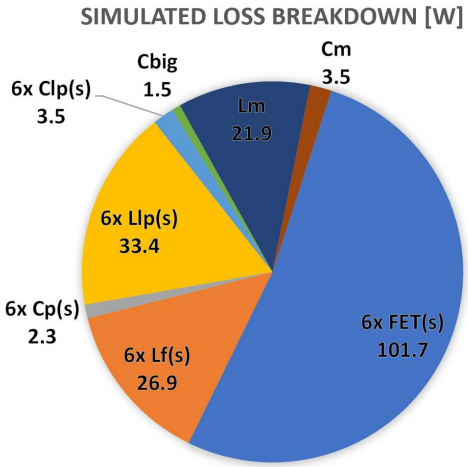

Fig. 7: The simulated loss breakdown of the amplifier shown in fig. 5.

six sub-circuits slightly differ. Fig. 7 shows the simulated loss breakdown across the different components. The simulated output power is 1533 W, and the simulated drain efficiency is 88.5%. Fig. 8 and 9 show the simulated output power distribution and transistor loss distribution across the six circuits (A to F). Even with both the component value variation and the timing mismatch, the output power and the transistor loss values are still maintained to within less than 10% of each other.

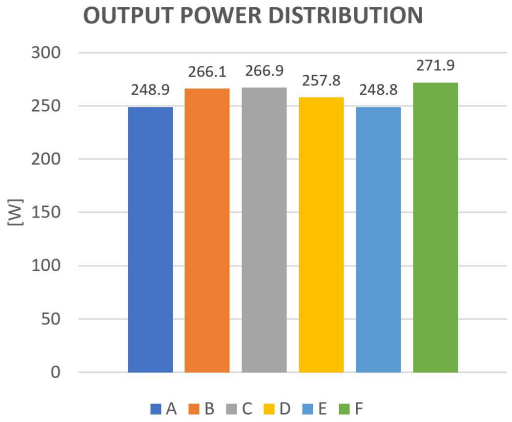

Fig. 8: The simulated output power distribution of the amplifier shown in fig. 5.

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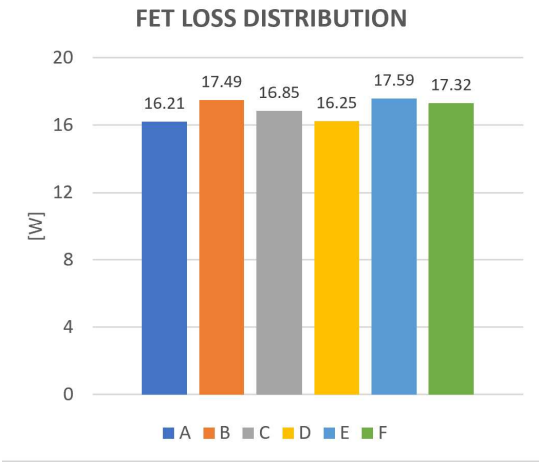
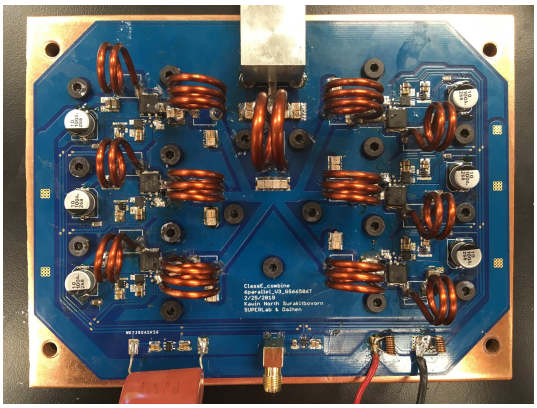
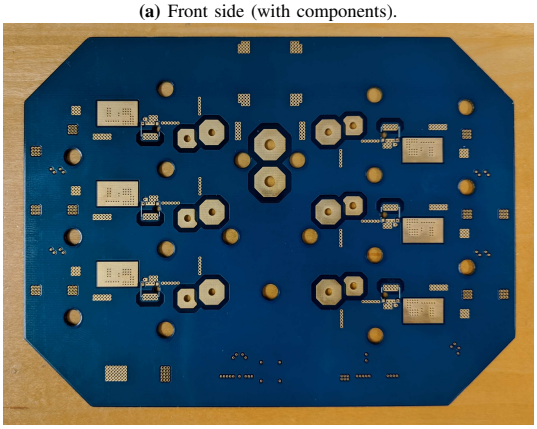


Fig. 9: The simulated transistor loss distribution of the amplifier shown in fig. 5.



(a) Front side (with components).



(b) Back side (bare board).

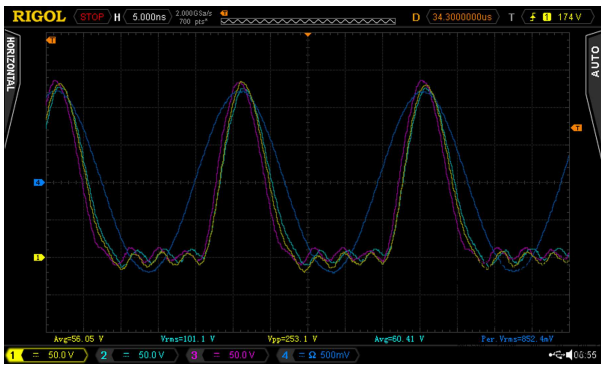
Fig. 10: The 1500 W 40.68 MHz amplifier circuit. The board dimension is 160 x 120 mm.

B. Experimental Result

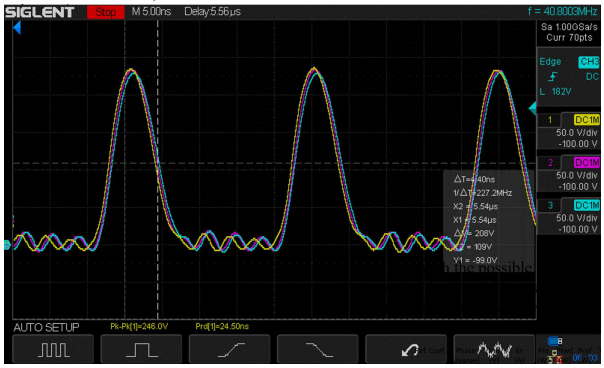
The actual circuit, shown in fig. 10, is implemented on a standard 2-layer FR-4 PCB using the component values from the simulation. All six sub-circuits share the same gating signal, with six non-inverting logic gate IC(s) used to buffer the signals. All of the inductors are air-cored and hand-wound. TEMCo 10 AWG copper magnet wires are used for the L_F(s) and L_{LP}(s), and TEMCo 8 AWG copper magnet wire is used for the L_M. Low loss C0G ceramic capacitor from American Technical Ceramic (ATC) are used for C_P(s) C_{LP}(s) and C_M. Due to the high operating frequency, parasitic inductance and capacitance of the PCB traces also affect the tuning and are taken into account.

To sufficiently drive the gate of the tested GaN HEMTs, a low-side gate driver, LM5114 from Texas Instruments, is used. We place the gate drivers as close as possible to the GaN switches to minimize the loop inductance in the gate, as well as use a gate resistor of 2.4 Ω to dampen any ringing in the gate voltage. Additionally, SiC Schottky diodes STPSC406 from ST Microelectronics, seen on the top of the board, are added in parallel to the switches to reduce the loss associated with reverse conduction in GaN transistor [36].

To facilitate the cooling of the switching devices, we mount the GaN transistors, GS66506T from GaNSystems, on the bottom side of the board so that they can be directly connected to the copper heat spreader. Additionally, some inductors are also mounted as “through-holes” so that they can be in direct thermal contact with the thermal pad underneath the PCB. Water cooling, which is standard for commercial RF systems at this power level, is also used.



(a) Measured drain waveforms on unit A, B and C (yellow, sky-blue and pink) on the left side of the board, as well as the output voltage (blue - measured across an attenuator).



(b) Measured drain waveforms on unit D, E and F (yellow, pink and sky-blue) on the right side of the board.

Fig. 11: The experimentally measured waveforms - two separate oscilloscopes are used to capture all of the waveforms.

The input power is calculated from the dc input voltage and current under continuous operation. The input voltage is

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3011658, IEEE Journal of Emerging and Selected Topics in Power Electronics

measured with a digital multimeter, Agilent 34411A, and the input current is recorded from the readout of the dc power supply, Agilent N5767A. The output power into the 50 Ω load is measured with a directional coupler/ power meter setup. The setup consists of a calibrated 4-port RF directional coupler, C5827-10, from Werlatone Inc., two N8482A thermocouple power sensors from Keysight Technologies, and an N1914A EPM series power meter from Keysight Technologies.

Fig. 11 shows the measured drain waveforms on all six sub-circuits, as well as the output voltage waveform across an attenuator. While all of the drain voltages show the characteristic soft-switching class-E waveforms, they differ slightly from each other due to the intrinsic mismatch/variation in the system. Nonetheless, with the proposed modified matching network, the circuit is able to attain a high dc-to-rf efficiency of 89 $\pm$ 2% with 1560 W output power.

Fig. 12 shows the surface temperature of the passive components on top of the board under the steady-state operation. From the thermal image, the inductors of the units near the center of the board appear hotter than those on the outside. We believe that this is due to the natural temperature gradient on the printed circuit board, with the center area being hotter than the area on the outer edges, and not from uneven power distribution between units. To measure the temperature of the switches which are mounted on the bottom side of the board, thermocouples are be inserted through small drill holes on the PCB. This thermal measurement shows all six FETs having their case temperature within 40 $\pm$ 3 C, suggesting balanced power sharing between the six circuits.

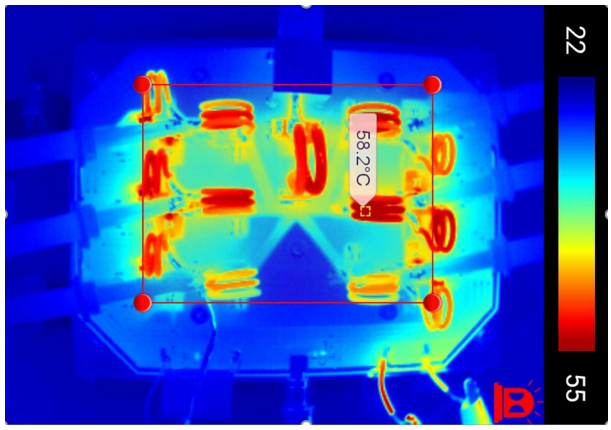


Fig. 12: Thermal image of the top side of the circuit under steady state operation at full power.

C. Power Sharing Verification

To verify that the power is indeed equally shared amount the six stages, we perform an additional experiment where the dc input power into each unit is measured. Small modifications to the circuit are made to allow for this measurement without changing the operation of the original circuit. Specifically, the dc-blocking capacitor, C_{BIG}, is split into each branch of the circuit to dc-isolate the units from each other. Furthermore, the dc input trace on each unit is also modified so that a digital multimeter (DMM) can be inserted inline to measure the input current into each unit.

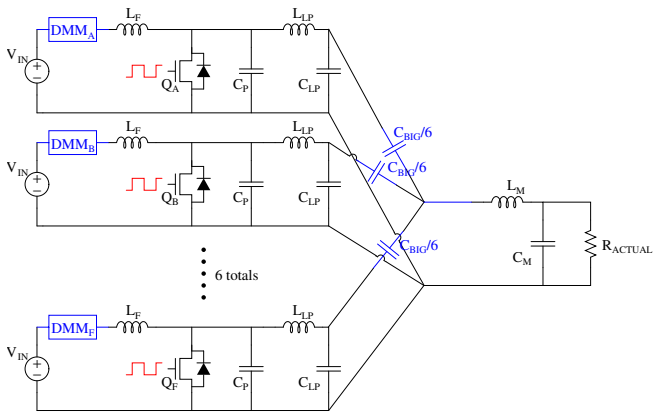


Fig. 13: Schematic of the circuit modified for individual dc-input power measurement.

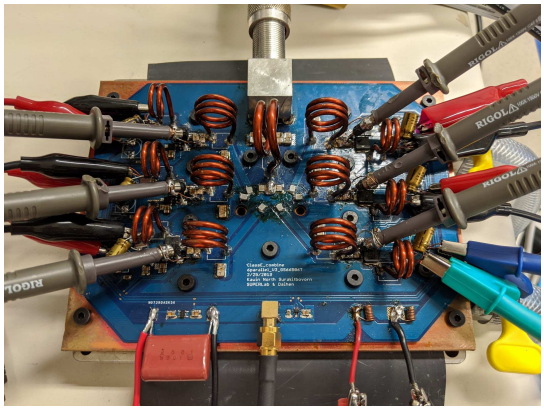


Fig. 14: The modified board used for the power sharing verification experiment.

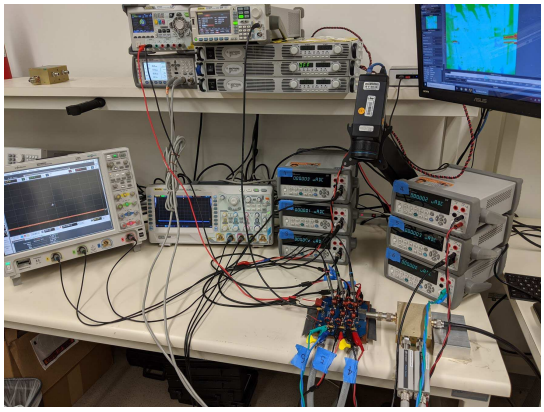


Fig. 15: The experimental setup for power sharing verification.

Fig. 13 shows the schematics of the modified circuit, while fig. 14 shows the physical modification made to the PCB itself. Shown in fig. 15, six digital multimeters, Agilent 34411A, are used to measure the input current into each unit. The dc input power into each unit is calculated from this current multiplied

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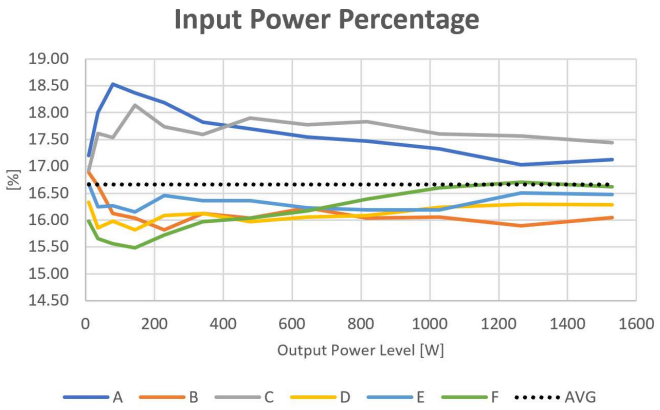

Fig. 16: The experimentally measured input power percentage of each unit (y-axis) vs output power level (x-axis).

by the dc input voltage taken from the readout of the dc power supply. Twelve data points are collected as we raise the input voltage from 5 V to 60 V to increase the output power. The plot in fig. 16 shows how the input power percentage (input power into each unit divided by the total input power) changes as the power level is varied. The power sharing capability appears to become more even as the power level increases. Once again, the highest and lowest measured input power percentage at full power fall within 10% of each other, confirming balanced power sharing between the six circuits.

IV. Conclusion

This paper describes a new tuning method that allows output power from multiple amplifiers to be directly connected without the need for any additional power combiner networks. In contrast with conventional high power RF amplifier systems where separate power combiner circuits are used to combine the output powers, the method introduced here relies on changing the way the components already existed in the high power amplifiers are tuned without adding any extra components.

Major benefits of this tuning method are the simplicity of the design and the reduction in the number of components needed to achieve power combining capability. This results in circuits that are easy to design and scale, small in size and low in component counts, and can achieve much higher efficiency than conventional amplifiers.

The application of this modified matching network is demonstrated on class-E power amplifiers to create power-combinable class-E amplifiers. The circuit is tested under continuous operation and shows a stable operation both thermally and electrically. In particular, we demonstrated a 1500 W RF amplifier with 89% efficiency and 25 W/in^3 power density at 40.68 MHz utilizing six class-E power amplifiers combining power. This achieved efficiency is much higher than other studies at similar frequency and power level (79% - 100 W - 27.12 MHz [37], 83% - 490 W - 27.12 MHz [38], 83% - 1150 W - 40.68 MHz [39]). Moreover, the achieved power density is also more than three times higher than the most power-dense RF generator commercially available, APEX RF Generator (7.4 W/in^3 - 5500 W - 13.56 MHz [40]). While this paper only provides explicit design equations for the low-pass matching network and class-E power amplifier combination, the methodology derived here can be directly applied to other types of matching networks and other classes of amplifiers.

References

[1] S. Zhukov and V. Kozyrev, "Push-pull switching generator without switching loss," *Poluprovodnikovye Pribory v Tekhnike Elektrosvyazi*, vol. 15, pp. 95–107, 1975.

[2] D. C. Hamill, "Impedance plane analysis of class DE amplifier," *Electronics Letters*, vol. 30, no. 23, pp. 1905–1906, 1994.

[3] S.-A. El-Hamamsy, "Design of high-efficiency rf class-D power amplifier," *IEEE Transactions on Power Electronics*, vol. 9, no. 3, pp. 297–308, 1994.

[4] N. O. Sokal and A. D. Sokal, "Class E-a new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun 1975.

[5] N. O. Sokal and A. Mediano, "Redefining the optimum rf class-E switch-voltage waveform, to correct a long-used incorrect waveform," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, June 2013, pp. 1–3.

[6] V. Tyler, "A new high-efficiency high-power amplifier," *Marconi Rev.*, vol. 21, no. 130, pp. 96–109, 1958.

[7] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 11, pp. 2007–2012, 1997.

[8] K. Honjo, "A simple circuit synthesis method for microwave class-F ultra-high-efficiency amplifiers with reactance-compensation circuits," *Solid-State Electronics*, vol. 44, no. 8, pp. 1477–1482, 2000.

[9] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1677–1690, 2003.

[10] J. W. Phinney, D. J. Perreault, and J. H. Lang, "Radio-frequency inverters with transmission-line input networks," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1154–1161, 2007.

[11] J. M. Rivas, Y. Han, O. Leitermann, A. Sagneri, and D. J. Perreault, "A high-frequency resonant inverter topology with low voltage stress," in *2007 IEEE Power Electronics Specialists Conference*. IEEE, 2007, pp. 2705–2717.

[12] L. Gu, G. Zulauf, Z. Zhang, S. Chakraborty, and J. Rivas Davila, "Push-pull class Φ_2 rf power amplifier," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.

[13] D. J. Perreault, "A new power combining and outphasing modulation system for high-efficiency power amplification," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1713–1726, Aug 2011.

[14] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for rf and microwave," *IEEE transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814–826, 2002.

[15] S. C. Cripps, *RF power amplifiers for wireless communications*. Artech house Norwood, MA, 1999.

[16] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Rf and microwave power amplifier and transmitter technologies-part 1," *high frequency electronics*, vol. 2, no. 3, pp. 22–36, 2003.

[17] R. Langridge, T. Thornton, P. M. Asbeck, and L. E. Larson, "A power re-use technique for improved efficiency of outphasing microwave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 8, pp. 1467–1470, 1999.

[18] X. Zhang, L. E. Larson, P. M. Asbeck, and R. A. Langridge, "Analysis of power recycling techniques for rf and microwave outphasing power amplifiers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 5, pp. 312–320, 2002.

[19] P. A. Godoy, D. J. Perreault, and J. L. Dawson, "Outphasing energy recovery amplifier with resistance compression for improved efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 2895–2906, 2009.

[20] H. Chireix, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, 1935.

[21] I. Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto, "A 2.14-GHz Chireix outphasing transmitter," *IEEE transactions on Microwave Theory and Techniques*, vol. 53, no. 6, pp. 2129–2138, 2005.

[22] W. Gerhard and R. Knoechel, "Improved design of outphasing power amplifier combiners," in *2009 German Microwave Conference*. IEEE, 2009, pp. 1–4.

[23] R. Beltran, F. H. Raab, and A. Velazquez, "HF outphasing transmitter using class-E power amplifiers," in *2009 IEEE MTT-S International Microwave Symposium Digest*. IEEE, 2009, pp. 757–760.

[24] T. Ni and F. Liu, "A new impedance match method in serial Chireix combiner," in *2008 Asia-Pacific Microwave Conference*. IEEE, 2008, pp. 1–4.

[25] S. Cripps, *Advanced Techniques in RF Power Amplifier Design*, ser. Artech House microwave library. Artech House, 2002. [Online]. Available: https://books.google.com/books?id=8KhANPEO88UC

[26] C. Weisman, *The Essential Guide to RF and Wireless*. Pearson Education, 2002. [Online]. Available: https://books.google.com/books?id=pVuFDNfEcVUC

[27] M. Golio, *The RF and Microwave Handbook*, ser. Electrical Engineering Handbook. CRC Press, 2000. [Online]. Available: https://books.google.com/books?id=UIHMnx0k9oAC

[28] L. Besser and R. Gilmore, *Practical RF Circuit Design for Modern Wireless Systems: Passive Circuits and Systems Passive Circuits and Systems, Volume 1*, ser. Artech House microwave library. Artech House, 2002. [Online]. Available: https://books.google.com/books?id=-GC9n2UDvEEC

[29] M. Acar, A. J. Annema, and B. Nauta, "Analytical design equations for class-E power amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 12, pp. 2706–2717, Dec 2007.

[30] R. Heckman, G. Roche, and J. R. Usher, "The evolution of rf power delivery in plasma processing," *Advanced Energy Industries, Inc*, pp. 1–8, 1998.

[31] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[32] K. Surakitbovorn and J. R. Davila, "Evaluation of GaN transistor losses at MHz frequencies in soft switching converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–6.

[33] K. N. Surakitbovorn and J. M. Rivas-Davila, "On the optimization of a class-E power amplifier with GaN HEMTs at megahertz operation," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4009–4023, April 2020.

[34] Texas Instruments. Lm5114 single 7.6-a peak current low-side gate driver. [Online]. Available: https://www.ti.com/product/LM5114

[35] ——. Sn74lvc1g17-q1 single schmitt-trigger buffer. [Online]. Available: https://www.ti.com/product/SN74LVC1G17-Q1

[36] S. Park and J. Rivas-Davila, "Power loss of GaN transistor reverse diodes in a high frequency high voltage resonant rectifier," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1942–1945.

[37] A. S. Jurkov, L. Roslaniec, and D. J. Perreault, "Lossless multiway power combining and outphasing for high-frequency resonant inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1894–1908, 2013.

[38] R. Frey, "500 W, class E 27.12 MHz amplifier using a single plastic MOSFET," in *1999 IEEE MTT-S International Microwave Symposium Digest (Cat. No. 99CH36282)*, vol. 1. IEEE, 1999, pp. 359–362.

[39] J. Choi, Y. Ooue, N. Furukawa, and J. Rivas, "Designing a 40.68 MHz power-combining resonant inverter with eGaN FETs for plasma generation," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2018, pp. 1322–1327.

[40] Advanced Energy. Apex RF generators and power-delivery systems. [Online]. Available: https://www.advancedenergy.com/globalassets/resources-root/data-sheets/apex-rf-generators-data-sheet.pdf