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On the Techniques to Utilize SiC Power Devices in High- and Very High-Frequency Power Converters

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Abstract—In this paper, we explore the challenges of implementing resonant converters using silicon carbide (SiC) power devices at high-frequency: namely, the issue of high parasitic inductance packages and the ability to drive and enhance the MOSFET at these frequencies. Although power circuit designers have many alternative device technologies to choose from such as silicon (Si) and gallium nitride materials (GaN), SiC devices have several advantageous attributes especially in high power applications. As a solution, we study the device performance and parasitics of SiC MOSFETs in different packaging schemes. We further offer a solution to the challenges of driving SiC devices by demonstrating a multi-resonant gate driver and use this scheme to drive a SiC MOSFET at 30 MHz and a SiC JFET at 13.56 MHz in a class-E inverter, achieving 85.7% drain efficiency for the MOSFET and 93.8% for the JFET.

I. INTRODUCTION

As an aim to miniaturize the passive storage elements of power converters, circuit designers increase the switching frequency of the power device in their systems, while utilizing resonant topologies to mitigate the switching losses of the device. Published results [1]–[4] have demonstrated resonant converters with devices operating at 10’s and even 100’s of MHz, much faster than pulse-width modulated (PWM) converters and with capabilities to achieve higher power densities and high efficiencies. From these papers, it is evident that gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have become popular options for the active-controlled switching device in high-frequency (HF) and very high-frequency (VHF) systems due to their lower on-resistance ($R_{ds,on}$), lower enhancement gate voltage, and low inductance and compact packages.

However, GaN devices cannot easily be adaptable for all types of systems and present inherent disadvantages compared to silicon carbide (SiC) alternatives. Namely, lateral GaN transistors are often unsuitable for high voltage applications since commercial SiC devices offer much higher blocking voltages and generally have avalanche protection due to their intrinsic body diode, preventing voltage overshoots [5]. Secondly, GaN transistors experience abnormal transient behavior not reported in datasheets such as current collapse, where the drain current is reduced after a large voltage is applied across the drain-source of the device [6]. Along with current collapse, GaN devices also reportedly experience charge trapping, causing what is known as dynamic $R_{ds,on}$ [7], [8]. Thirdly, silicon carbide has better thermal properties than gallium nitride, with

over three times higher thermal conductivity [9], allowing for better heat transfer and more compact thermal designs. In addition, GaN transistors exhibit conduction losses with two times the thermal dependency compared to SiC MOSFETs [10], meaning that GaN devices need to be sufficiently cooled to achieve high system efficiency.

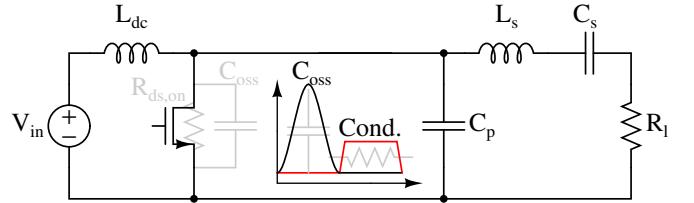


Figure 1. An example of a class-E inverter highlighting the conduction loss during the on-time of the switch and the charging-discharging C_{oss} loss during the off-time.

On top of these advantages, recent publications such as [11]–[15] have characterized trends of the losses in the output capacitance of various commercially-available wide-bandgap devices. In an example class-E inverter as shown in Figure 1, during the on-time of the switch, the device experiences loss from channel conduction, while during the off-time, the device loses a fraction of its energy during the charge-discharge cycle of the C_{oss} . The previous cited papers have demonstrated GaN and SiC devices have C_{oss} power dissipation that scales differently based on voltage swing, switching frequency, and dV/dt , where SiC has a linear power loss frequency dependency and GaN depends on $f^{1.6}$. Therefore, the authors of [12] state that there are certain frequency and power level regimes where SiC devices can perform with lower losses than GaN devices in soft-switching applications.

Despite these advantages, SiC devices are often unfavorable in HF/VHF converters regardless of the application due to a few reasons. Firstly, SiC MOSFETs have smaller transconductances due to lower electron mobility [16], meaning that a larger gate voltage is required to achieve a certain channel current. Furthermore, manufacturers, such as Wolfspeed/Cree and Rohm Semiconductor, recommend 15–20 V peak gate-to-source voltages due to threshold voltage instabilities from poor oxide-bulk interface, temperature, age, and bias voltage dependencies [17], [18]. In comparison, GaN HEMTs from companies such as EPC and GaN Systems require only 5–7 V peak gate voltage, while also having small gate capacitances (on the order of 50 pF). This results in SiC devices

experiencing larger gating losses and requiring gate drivers to output higher voltages while still maintaining short rise and fall times to operate at high-frequencies. This is the main reason why papers like [19] have difficulty maintaining high efficiencies in converters switching SiC MOSFETs past 10 MHz. Furthermore, manufacturers currently package SiC devices in high inductance packages making them unsuitable for high-frequency converters. In this study, we investigate alternative packaging schemes and resonant gate driving methods that can save gating power compared to a hard-switched gate driver. We then present the results of a resonant class-E inverter using a flip-chip packaged SiC MOSFET, switching at 30 MHz with 85.7% drain efficiency. In addition, we also demonstrate similar gate driving schemes for a class-E inverter using a SiC JFET operating at 13.56 MHz.

II. SiC DEVICE PACKAGING

Parasitic inductances resulting from semiconductor device packaging can prevent designers from successfully operating the device in higher frequency applications. For resonant inverter topologies like class-E and class- Φ_2 , parasitic drain-source inductances add ringing to the drain voltage which increases the semiconductor stress. [20] shows that the extended leads of a TO-247 package can increase the switching energy by 32%. Additionally, the ringing can also superimpose during the on-state of the device, adding to the conduction loss. It is evident why papers such as [21]–[24] propose inductance cancellation methods, as a means to alleviate this issue. However, such techniques are best to avoid in practical circuit design because they require accurate modeling of the parasitics within the device and the board layout. The fact that GaN switches are packaged in cases with low lead inductances is one reason why designers favor them for high-frequency applications. In this section, we discuss the packaging method-

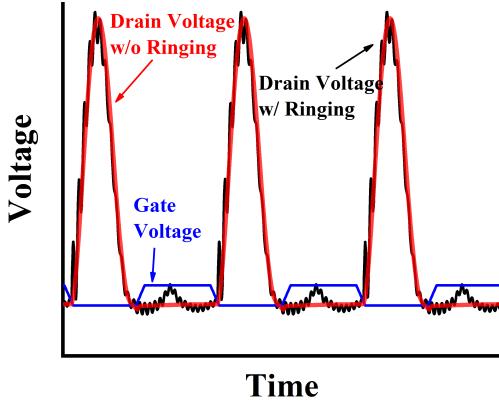


Figure 2. An example of the ringing in the drain voltage that high inductance leads in packages can cause in a class-E inverter.

ology for the custom packaged devices, measure the parasitic inductances for commercially available SiC devices and the custom packaged devices, and compare with commercial GaN packages.

A. Custom Packaging Methodologies

Generally, manufacturers package SiC MOSFETs in large TO-247 packages with long leads because the large base plate

attached to the drain increases the thermal mass of the device. To avoid large parasitic packages, manufacturers also distribute bare die versions of the device. An additional step in custom packaging the die must be taken because often times, they cannot be directly soldered onto circuits board due to having aluminum (Al) bond pads. For this study, we custom packaged a GE1700903A1 SiC MOSFET die from General Electric, rated at 1700 V breakdown and with $380 \text{ m}\Omega R_{ds,on}$, in both a surface mount device (SMD) ceramic case and a flip-chip package.

The SMD package was manufactured and assembled by SMART Microsystems. The SiC MOSFET die was bonded on the drain side to Pad 1 of the package using high lead (5% Sn and 95% Pb) solder, referencing Figure 3. The gate is wire bonded to Pad 3 with a 1 mil Al wire bond and the source is bonded to Pad 2 with three 5 mil Al wire bonds.

An additional packaging scheme suitable for high-frequency applications is flip-chip, where the source and gate pads are soldered onto the PCB and a copper connector is attached from the back-side drain to another PCB pad. Similar to [25], [26], we utilize an electroless remetallization procedure to plate nickel on top of the aluminum bond pads to allow solderable contacts to a circuit board.

The following procedure describes the development of the flip-chip package:

- 1) Etch the native oxide of the aluminum bond pads.
- 2) Dip the dies in a zincate solution to grow a zinc adhesion layer.
- 3) Electroless plate the zinc layer with nickel in a chemical bath to grow $5 \mu\text{m}$ thickness of nickel plating.
- 4) Attach solder spheres to the pads using a low temperature solder as a glue.
- 5) Solder the die to the board.
- 6) Solder the copper tab to the drain side and the PCB.

B. Analysis of Packaging Parasitics

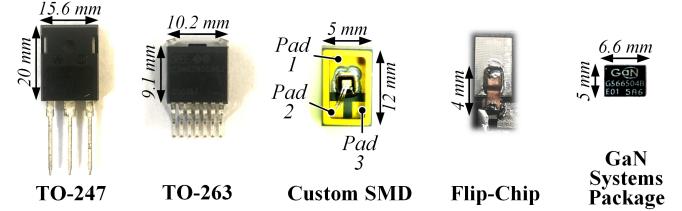


Figure 3. Two common packages (TO-247 and TO-263) for SiC devices as well as custom packaged SiC device and a GaN Systems package for reference

To compare the various packages, we measure the series inductances at the drain, gate, and source nodes. We assume a simplified model where the package parasitics are modeled as three lumped inductors in series with the gate, source, and drain. We measured two commercial SiC MOSFETs (C2M0080120D in a TO-247 and C2M1000170J in a TO-263) from Cree, our two custom packaged devices, and a GaN Systems GS66504B.

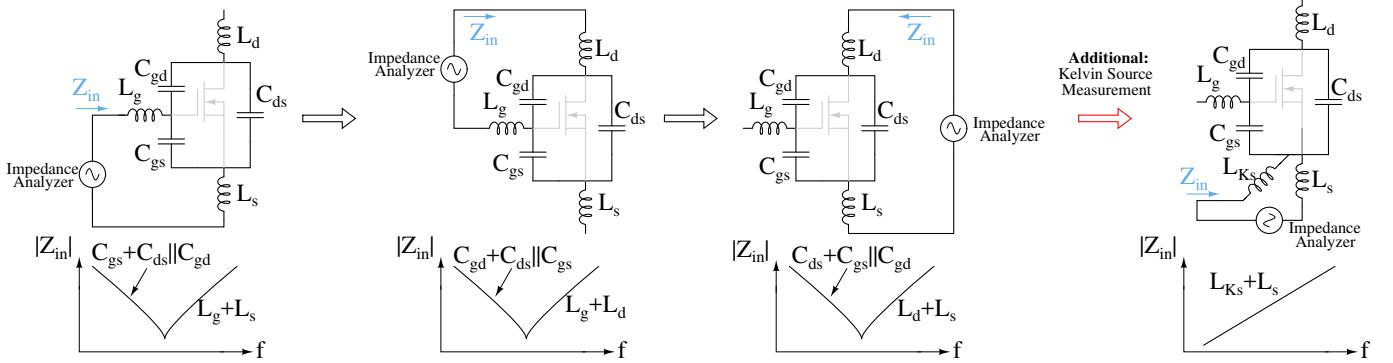


Figure 4. Measurement procedure to obtain the series parasitic inductance of the package. The fourth measurement step is only for devices with an additional Kelvin source pin, such as the TO-263 7 pin, with parasitic inductance L_{Ks} .

1) Measurement Procedure: To measure the inductances, we used a Keysight E5061B network analyzer to measure the series inductance of the gate-source, gate-drain, and drain-source terminals while leaving the third terminal open. We set the network analyzer to impedance measurement mode and used the Keysight 16201A and 16092A test fixtures. Then, we set the frequency sweep range from 1 to 100 MHz and calibrated using open, short, and $50\ \Omega$ load with the Keysight 16195B calibration kit. In the impedance measurement mode, the instrument models the device under test (DUT) as a series RLC network, in which it can display the series inductance value. From the inductance measurements, we obtain a system of equations shown by Equation 1, and can solve for L_d , L_g , and L_s . Figure 4 shows the measurement procedure. We repeated the measurement for three devices per package.

$$\begin{aligned} 1 \cdot L_g + 0 \cdot L_d + 1 \cdot L_s &= L_{meas,1} \\ 1 \cdot L_g + 1 \cdot L_d + 0 \cdot L_s &= L_{meas,2} \\ 0 \cdot L_g + 1 \cdot L_d + 1 \cdot L_s &= L_{meas,3} \end{aligned} \quad \downarrow \quad (1)$$

$$\begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} L_g \\ L_d \\ L_s \end{bmatrix} = \begin{bmatrix} L_{meas,1} \\ L_{meas,2} \\ L_{meas,3} \end{bmatrix}$$

Some device manufacturers are implementing dies packaged in 4 terminal cases, where the fourth terminal serves as a Kelvin source to reference the gate voltage. The purpose of the Kelvin source is to separate the main power path from the driving path, allowing for improved noise immunity at the gate when large currents flow through the power path [27]. Publications such as [28] demonstrate smoother turn-on and turn-off transients and a reduction in overall device power dissipation. In this study, the TO-263 7 pin package from Cree features a Kelvin source pin (second pin from the left). Therefore, we added an additional inductance to characterize as shown in Figure 4. To obtain the 4 inductance values, the same procedure as described previously still stands to obtain L_g , L_d , and L_s . An additional fourth measurement between the two sources is required, and subtracting L_s from the measurement results in the Kelvin source parasitic inductance L_{Ks} .

2) Results: Figure 5 shows the obvious result that the TO-247 has the largest amount of parasitic inductance, with 2

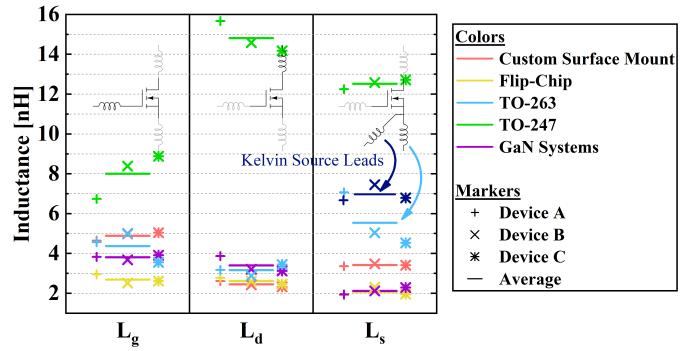


Figure 5. Measured L_g , L_d , and L_s for each of the three devices for all five packages. The lines mark the average of the three device measurements.

to 8 times more inductance than the other packages. On the other side of the spectrum, the flip-chip package has the lowest inductance due to direct contact from die to PCB. The flip-chip package is similar to the GaN devices from EPC, which are commercially available in die form with solder bumps attached during the fabrication process [29]. What is interesting to note is that the commercial SiC TO-263 package has similar values to that of the custom SMD and the GaN Systems package. Moreover, their inductances are only slightly higher than that of the flip-chip package. This shows that manufacturers currently have available packages for SiC devices suitable for high-frequency applications. Regardless of the packaging parasitics, the gate switching speed is fundamentally limited by the RC time constant of the gate loop, meaning if the gate resistance and/or C_{iss} are too large, the device cannot switch faster than the limiting frequency. For a 50% duty cycle gate waveform, the max switching frequency limited by the gate is given by $\frac{1}{4R_g C_{iss}}$. From Figure 6, the main roadblock that limits circuit designers from replacing GaN with SiC devices in high-frequency converters is the significant gate RC time constant. Therefore, the reduction of gate resistance is the critical factor for manufacturers to tap into the HF/VHF market with SiC devices, which can be critical for accessing both a high voltage and high speed regime.

III. GATE DRIVING TECHNIQUE FOR SiC MOSFETs

Conventionally, designers drive MOSFET gates using a hard-switched totem-pole gate driver, schematized in Fig-

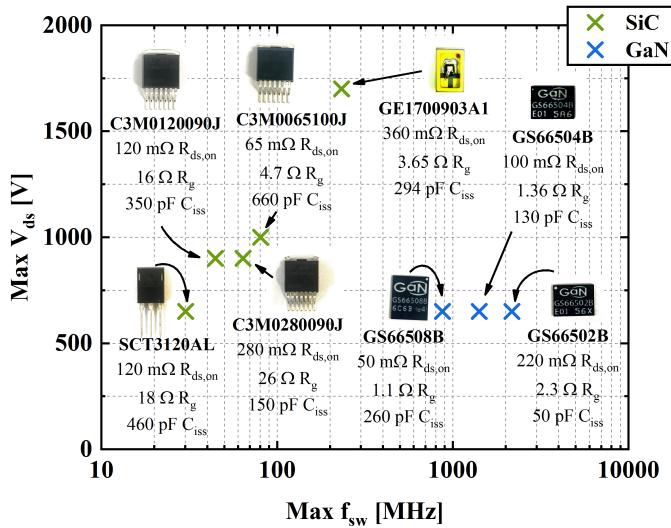


Figure 6. Figure displaying the maximum rated drain-source voltage (derived from datasheet) and the maximum operating frequency based upon $\frac{1}{4R_g C_{iss}}$ for 8 different GaN and SiC devices. We observe from this Figure that SiC devices are suitable for high voltage applications but to compete with GaN in terms of switching speed, manufacturers should offer lower R_g devices.

ure 7a, with power dissipation calculated by Equation 2.

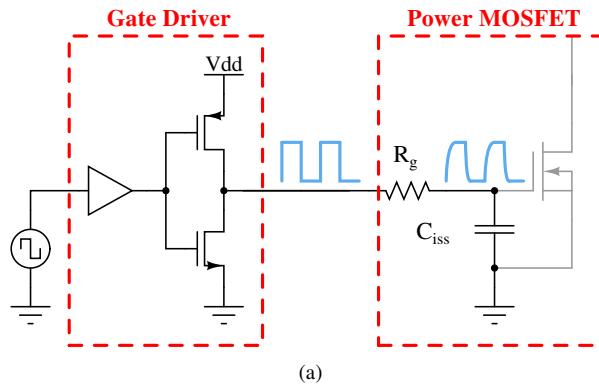
$$P_{gate} = f_{sw} C_{iss} V_g^2 \quad (2)$$

Every cycle, an energy $C_{iss} V_g^2$ is supplied by the gate driver and dissipated at the turn-off. Figure 7b lists the gate power dissipation using a hard-switching gate driver for two SiC MOSFETs, a GaN HEMT, and a Si superjunction FET with similar $R_{ds, on}$ at three ISM (industrial, scientific and medical) band frequencies. It is evident that the advantage of WBG devices is the much lower C_{iss} input capacitance required to charge the gate. However, since the gate energy scales with V_g^2 , the much higher enhancement voltages greatly worsens the gating loss for SiC devices. Another issue is that currently, very few commercial gate drivers can operate with supply voltages above 15 V with output signals that have fast rise and fall time transitions (<4 ns). To resolve these challenges, we propose to resonantly drive the gate of the MOSFET, in order to partially recycle the energy transmitted from the gate driver to the gate, as well as provide a large gate voltage that commercial gate drive ICs cannot provide.

Table I
KEY PARAMETERS OF DIFFERENT POWER DEVICES WITH SIMILAR $R_{ds, on}$.

Device	Manufacturer	Material	$V_{ds,max}$	$R_{ds, on}$	$V_{g, on}$	C_{iss}
GE1700903A1	General Electric	SiC	1700 V	360 mΩ	20 V	300 pF
C3M0280090J	Cree Semiconductor	SiC	900 V	280 mΩ	15 V	150 pF
GS66502B	GaN Systems	GaN	650 V	220 mΩ	7 V	50 pF
R6015KNJTL	Rohm Semiconductor	Si	600 V	290 mΩ	10 V	1050 pF

Previous papers such as [30]–[32] demonstrate a few different resonant gating topologies with the capability to conserve gate power in silicon devices as switching speeds scale beyond 100 MHz. While these topologies can work for SiC devices, for this paper we choose a multi-resonant gate driving circuit based from [33] and schematized in Figure 8. The operation of this circuit is to pass the dc component, amplify the



(a)

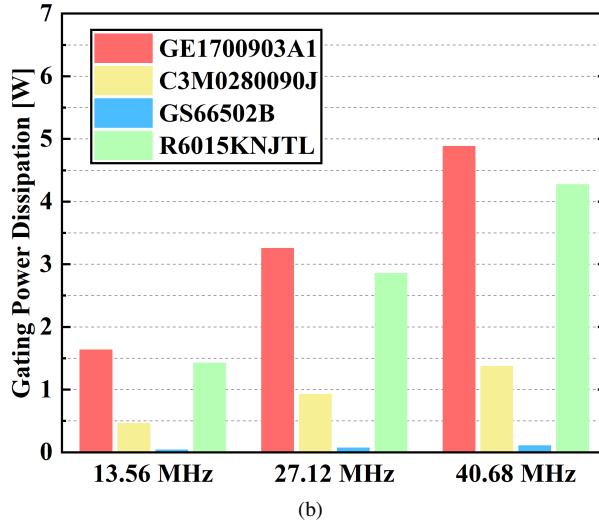


Figure 7. (a) Schematic of a hard-switched gate drive. (b) Calculated hard-switched gating loss of 4 different high-voltage power devices from Table I at three ISM bands. Note that SiC devices have much higher gating losses, making it harder to drive at high-frequency.

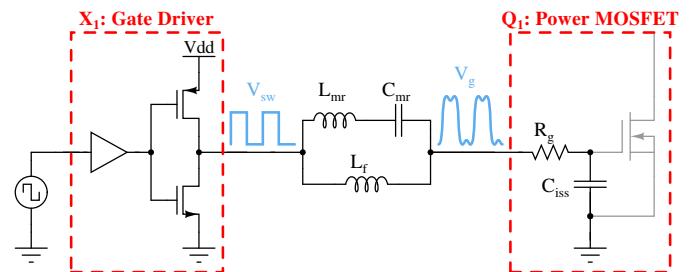


Figure 8. Simplified schematic of the multi-resonant gate driver for SiC MOSFETs. The gate of the power MOSFET is modeled as a series RC circuit with gate resistance R_g and an input capacitance C_{iss} . The gate driver chip is modeled as a totem-pole network.

first harmonic and third harmonics, and filter the remaining harmonics of a 50% duty cycle square wave. Thus, this gate drive topology is suitable for driving MOSFETs in resonant inverters, such as a class-E inverter, that require a 50% duty cycle trapezoidal-shaped gate waveform. The same resonant gate drive topology is demonstrated in [34] using a 13.56 MHz class-E inverter with a GaN device. However, the gating power conservation is low for GaN. Compared to a conventional gate driver, the resonant gate driver in their case conserves only 70 mW of power (under 10%). In this section, we present

the tuning criteria and procedure for the gate drive, a design example, a comparison with a commercial hard-switching gate drive, and a demonstration using a resonant converter.

A. Tuning Procedure

We modify the tuning procedure from [33] to account for an ample gain at the first and third harmonics of V_{sw} , where [33] targets unity gain. Additionally, we impose these conditions for the design criteria:

- 1) Design the input impedance $Z_{sw}(s)$ to be inductive at f_{sw} and $3f_{sw}$ in order to minimize the switching losses of the two devices in the totem-pole gate driver. This is due the finite C_{oss} of the FETs.
- 2) The amplitudes of the first and third harmonics of V_g should have an approximate ratio of 3:1 in order to maintain the trapezoidal shape. Additionally, the phases of the first and third harmonic should be defined by Equation 3.

$$\phi_1 = \frac{\phi_3 + 2k\pi}{3}, k = 0, \pm 1, \pm 2, \dots \quad (3)$$

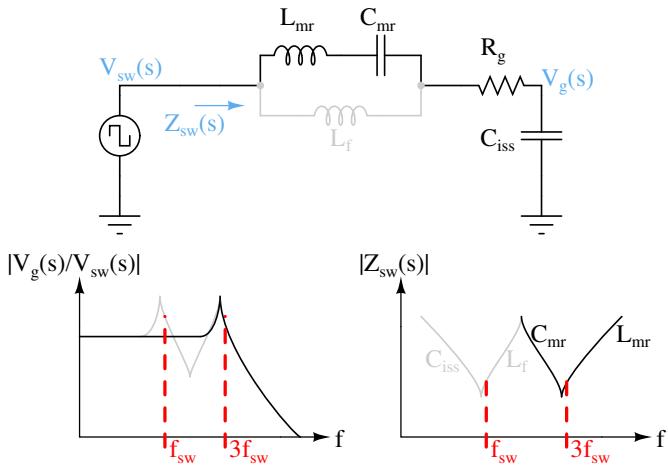


Figure 9. Equivalent approximated network when calculating the gain at the first harmonic. Note that this approximation has less error when operating at higher switching frequencies.

We begin the procedure by selecting the value of L_f , which is used to amplify the fundamental component of $V_{sw}(s)$. To simplify calculations, we ignore C_{mr} and L_{mr} when calculating $Z_{sw}(s)$, since they will present a large parallel impedance compared to L_f at f_{sw} . Thus, the circuit at f_{sw} can be approximated as a low-pass RLC filter, where Equation 4 describes the magnitude of the transfer function of the filter at f_{sw} .

$$\left| \frac{V_g(j\omega_{sw})}{V_{sw}(j\omega_{sw})} \right| \approx \frac{\omega_0^2}{\sqrt{(\omega_0^2 - \omega_{sw}^2)^2 + (\frac{\omega_{sw}R_g}{L_f})^2}}, \quad (4)$$

$$\omega_0 = \frac{1}{\sqrt{L_f C_{iss}}}$$

Since R_g and C_{iss} are fixed by the power MOSFET, we can use Equation 4 to solve for L_f . Generally, Equation 4 will result with 2 possible solutions for L_f . We select the

larger solution because this allows $Z_{sw}(s)$ to have an inductive impedance at f_{sw} .

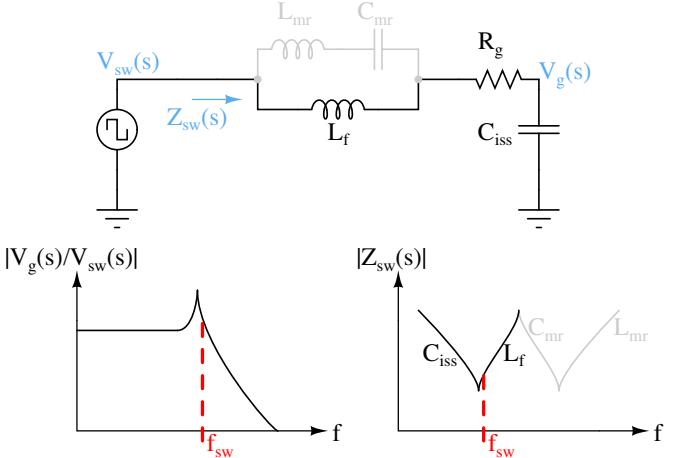


Figure 10. Equivalent approximated network when calculating the gain at the third harmonic.

The remaining values to select are C_{mr} and L_{mr} , which are used to pass the 3rd harmonic of $V_{sw}(s)$. Likewise, at $3f_{sw}$ we can neglect C_{iss} and L_f and consider $Z_{sw}(s)$ as another RLC network.

$$\left| \frac{V_g(j3\omega_{sw})}{V_{sw}(j3\omega_{sw})} \right| \approx \frac{\omega_1^2}{\sqrt{(\omega_2^2 - (3\omega_{sw})^2)^2 + (\frac{3\omega_{sw}R_g}{L_{mr}})^2}}, \quad (5)$$

$$\omega_1 = \frac{1}{\sqrt{L_{mr}C_{iss}}}, \quad \omega_2 = \frac{1}{\sqrt{L_{mr}C_{mr}}}$$

Equation 5, which computes an approximate transfer function at $3f_{sw}$, gives a relationship between C_{mr} and L_{mr} based upon the desired 3rd harmonic gain. We recommend to select an initial value of C_{mr} as $C_{iss}/5$ and solve for L_{mr} using Equation 5.

Lastly, because we neglect the phase criterion from Equation 3 in the previous steps of the tuning procedure, we then make slight adjustments from the initial values to satisfy this criterion and increase the gain if necessary.

It is important to note that this resonant gate drive method will not achieve the targeted gain for all SiC MOSFETs at certain frequencies. Some MOSFETs have gate resistances and/or capacitances that are too large that degrade the Q factor. Therefore, we also advise the designer to take careful considerations in selecting the MOSFET.

B. Design Example

As an example, we demonstrate the multi-resonant gate driver at 30 MHz using a 1700 V rated GE1700903A1 SiC MOSFET from General Electric. We model the gate of the MOSFET as an RC tank with R_g as 3.65 Ω and C_{iss} as 400 pF measured at 30 MHz. We also select an LM5114 low-side gate drive chip from Texas Instruments to serve as the totem-pole of the resonant gate driver. We supply the V_{dd} with 11 V, and aim to achieve a gate voltage with an 18 to 20 V peak in order to fully enhance the FET. Thus, our targeted gain is between 1.6 to 1.7 (4.1 to 4.6 dB). From Equation 4, we substitute R_g

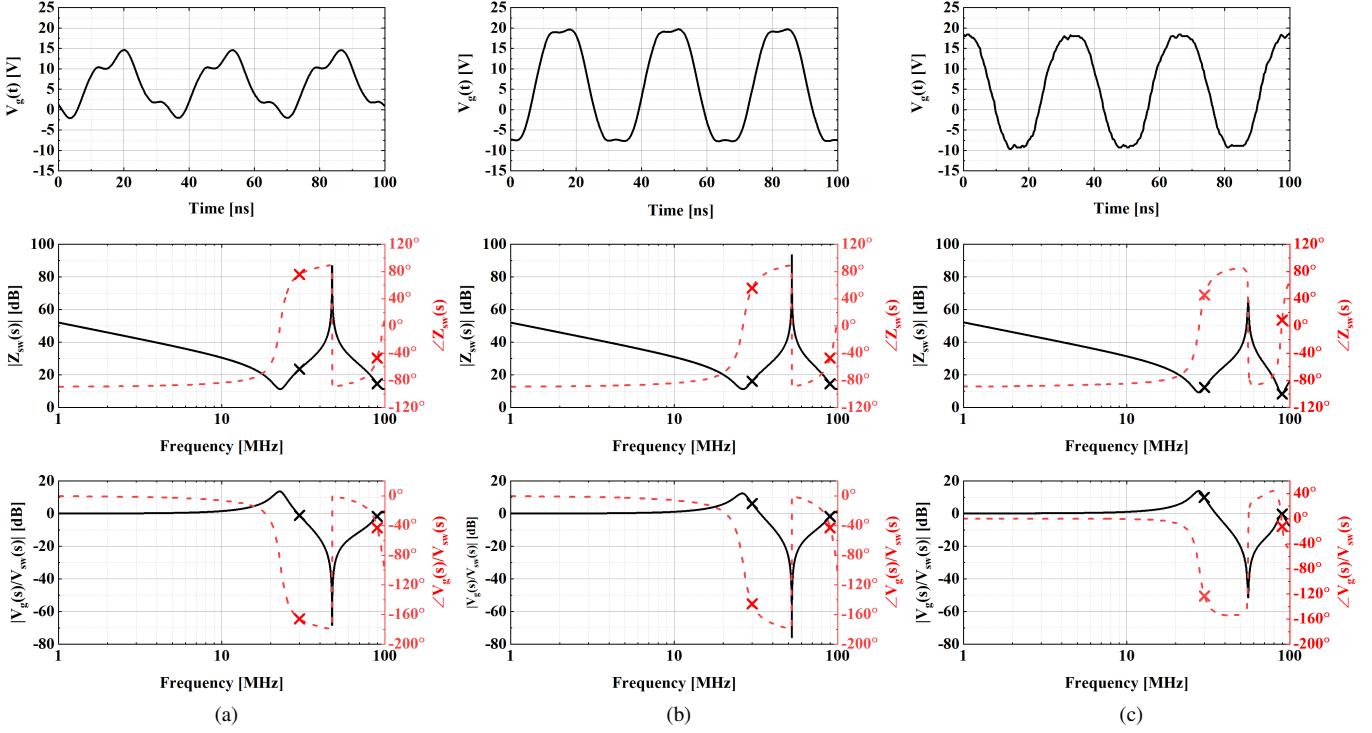


Figure 11. Transient gate voltage $V_g(t)$, small-signal input impedance $Z_{sw}(s)$, and gain of the initial tuned values of the multi-resonant gate drive from (a) simulation and (b) experimental measurement of the circuit shown in Figure 12.

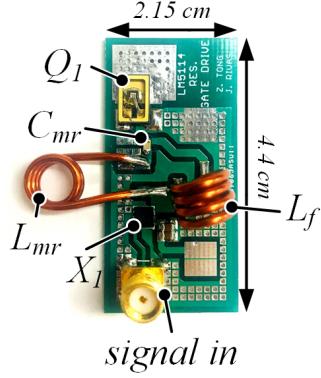


Figure 12. Photograph of multi-resonant gate driver PCB.

and C_{iss} to obtain a relationship between the first harmonic gain and L_f , plotted in Figure 13. We select initial values for L_f and C_{mr} to be 100 nH and 80 pF ($C_{iss}/5$) respectively. From Equation 5 we obtain a relationship between the third harmonic gain and L_{mr} shown in Figure 13, and select L_{mr} to be 40 nH to achieve the largest third harmonic gain. Figure 11a displays the simulated transient waveform as well as the small-signal input impedance and gain from the initial values of L_{mr} , C_{mr} , and L_f . It is evident that the first harmonic gain and phase are slightly lower than the targeted values. Both issues can be resolved by lowering the value of L_f , resulting in an L_f value of 75 nH. Figure 11b displays the transient waveform, small-signal input impedance, and gain from the final values based on simulation and Figure 11c displays the measured waveforms using the circuit in Figure 12.

Table II
MULTI-RESONANT GATE DRIVER PARAMETERS AND VALUES.

Parameter	Value
f_{sw}	30 MHz
Q_1	GE1700903A1
R_g of Q_1	3.65 Ω
C_{iss} of Q_1	400 pF at 30 MHz (measured)
X_1	LM5114
L_{mr}	38 nH
C_{mr}	82 pF
L_f	73 nH

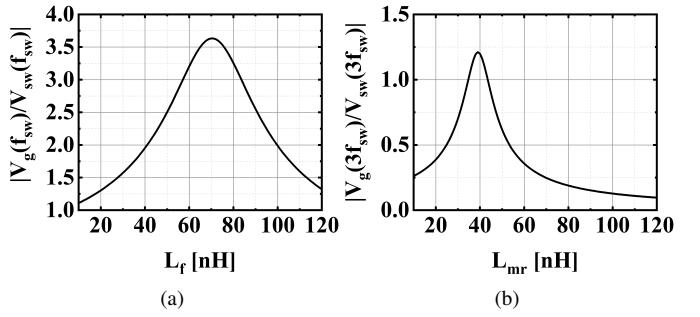


Figure 13. (a) First harmonic gain versus the variation in L_f . (b) Third harmonic gain versus the variation in L_{mr} for a C_{mr} fixed at $C_{iss}/5$.

C. Power Dissipation

Additionally, we compare the gating power between the multi-resonant gate drive with a conventional hard-switching

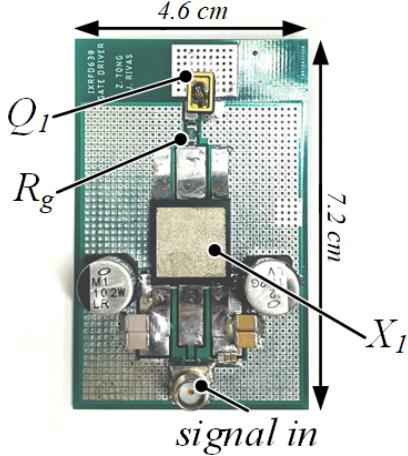


Figure 14. Photograph of hard-switching gate driver PCB.

the additional power dissipation is a result of the additional resistances of the totem-pole switches generating extra losses and the fact that we are not operating at complete zero voltage switching (ZVS). For the hard-switching gate driver, the losses in the experiment are over 10 times the calculated losses. This is due to the non-idealities in the IXRFD630 gate drive chip. From Figure 15a which is derived from the manufacturer's datasheet, the gate drive IC draws several amps of current when switching at 30 MHz, equating to tens of watts of power loss since the supply voltage is 18 V. In addition to saving power, the resonant gate drive provides a negative turn-off gate voltage, which is beneficial for faster turn-on and turn-off transitions. The reason is because the rise and fall times are fixed regardless of the amplitude of the voltage swing of the gate waveform. When comparing a gate waveform that swings from 0 to 18 V to a gate waveform that swings from -10 to 18 V, the -10 to 18 V waveform transitions from V_{th}

Table III
LIST OF PARAMETERS AND VALUES FOR HARD-SWITCHING DRIVER.

Parameter	Value
f_{sw}	30 MHz
Q_1	GE1700903A1
X_1	IXRFD630
R_g	3 Ω

gate drive. For the hard-switching gate drive, we select an IXRFD630 gate driver chip from IXYS, capable of operating up to 30 V with 4 ns rise and fall times. Figure 14 displays the test circuit where we supplied 18 V on the gate driver V_{dd} to drive the GE1700903A1. Table IV compares the gating losses between the resonant gate drive and the hard-switching IXRFD630. [33] presents a detailed analysis of the gating

Table IV
COMPARISON BETWEEN HARD-SWITCHED GATE DRIVER AND RESONANT GATE DRIVER AT 30 MHZ SWITCHING FREQUENCY.

Parameter	Hard-Switching	Resonant
V_{dd}	18 V	11 V
I_{in}	1.82 A	0.51 A
P_{gate}	32.8 W	5.6 W
P_{gate} (Equations 2 and 6)	3.6 W	1.9 W

power dissipation for the multi-resonant gate driver. For our case, we follow Equation 6 to calculate the gating loss derived from [33].

$$P_{QW} = \frac{V_g^2}{2R_g} \times \left(\frac{A_1^2}{q_s^2 + 1} + \frac{A_3^2}{\frac{1}{9}q_s^2 + 1} \right), \quad (6)$$

$$q_s = \frac{1}{\omega_s C_{iss} R_g}, \quad A_1 = \frac{2}{\pi}, \quad A_3 = \frac{2}{\pi} \times \frac{1}{3}$$

From Table IV, compared to the hard-switching IXYS gate driver, resonant gating has over 5 times less gate power dissipation from experiment and 89% less gate power dissipation from using Equations 2 and 6. For the resonant gate driver,

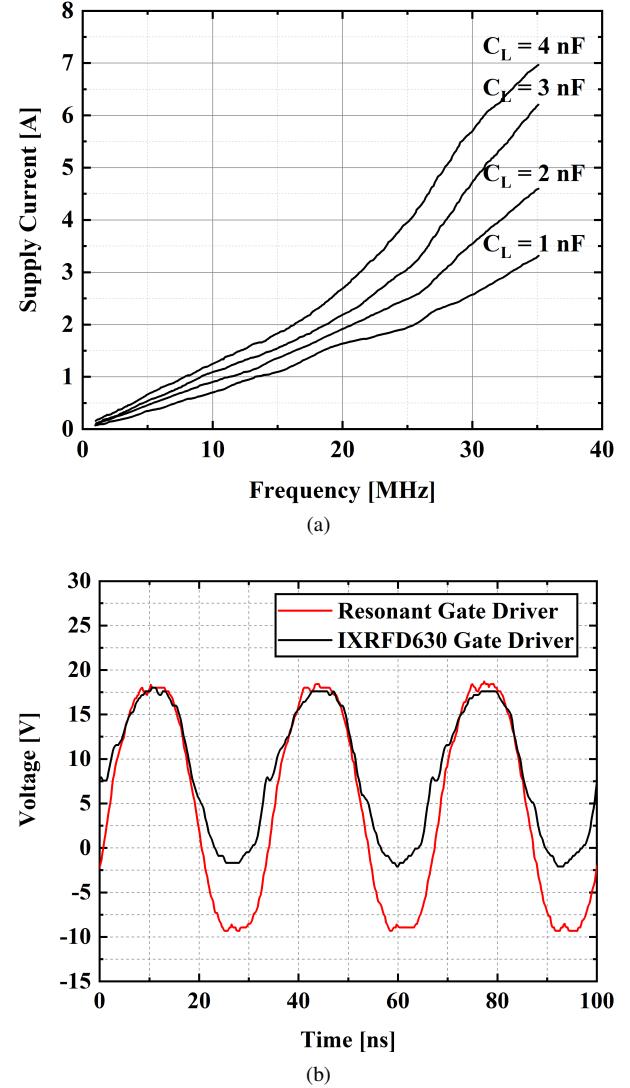


Figure 15. (a) A plot of the IXRFD630 Supply Current vs. Switching Frequency derived from the manufacturer datasheet [35]. (b) A comparison of the gate signals provided by the resonant gate driver in red and the hard-switching gate driver in black. Note the resonant gate driver has a slew rate of 2.5 V/ns, where the hard-switched has 1.8 V/ns.

to the peak voltage and vice versa faster than the 0 to 18 V waveform.

D. Converter Demonstration

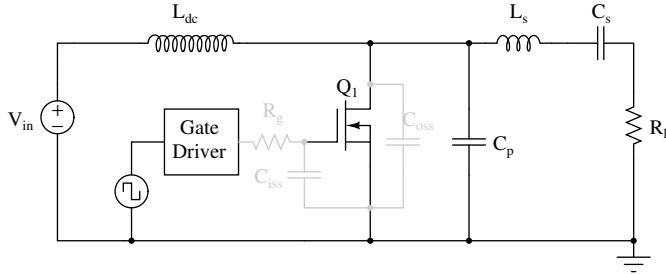


Figure 16. Schematic of a class-E resonant inverter used in this experiment.

Lastly, we demonstrate the operation of our gate driver in a large choke inductance class-E inverter switching at 30 MHz. Figure 16 illustrates the schematic for the inverter. [36] outlines the design procedure utilized in our experiment and Table V lists the values of the components.

Table V
KEY COMPONENTS OF THE CLASS-E AMPLIFIER AND RESONANT GATE DRIVER.

Part	Description
R_l	12.5 Ω RF Dummy Load
L_{dc}	1.38 μ H, Q factor 140, AWG 18, 34 turns
L_s	320 nH, Q factor 138.6, AWG 18, 15 turns
L_f	75 nH, Solenoid
L_{mr}	40 nH, Solenoid
C_p	N/A
C_{in}	100 μ F, 200 V Electrolytic
C_s	230 pF, 500 V C0G Ceramic
C_{mr}	80 pF, 100 V C0G Ceramic
Q_1	GE1700903A1, 1700 V SiC MOSFET
X_1	LM5114, Texas Instruments, gate drive IC

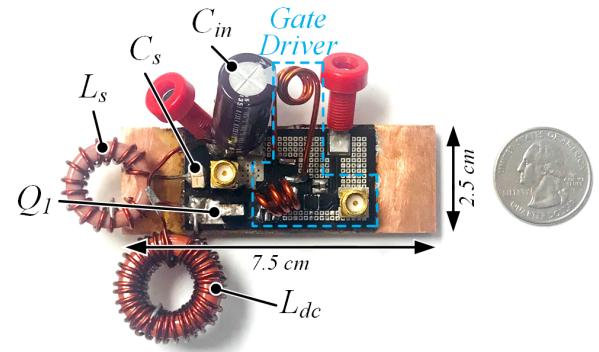
Our inverter operates to deliver 50 W of power to a 12.5 RF load at 85.7% drain efficiency, with performance metrics listed in Table VI. Finally, Figure 17b displays the V_{ds} , V_{gs} , and V_{out} over a few cycles of operation.

IV. GATE DRIVER FOR SiC JFETs

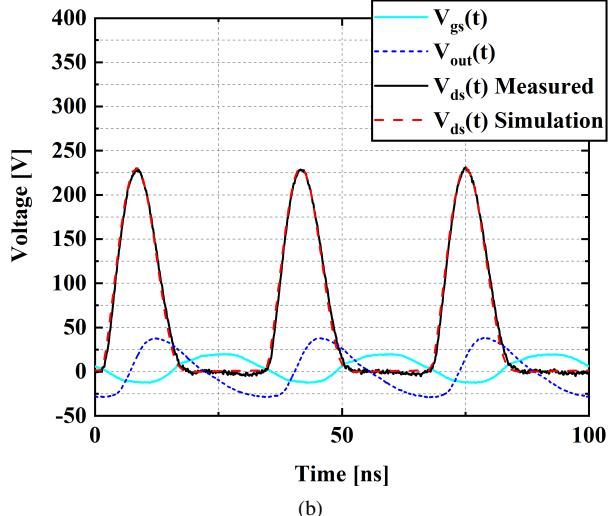
Traditionally, switch-mode converters are often implemented using the normally-off enhancement mode devices such as MOSFETs, IGBTs, and HEMTs. Enhancement mode devices are favorable for resonant conversion systems because they offer safer start-up and power down transients and provide simpler gate driving circuitry. Depletion mode devices like JFETs are normally-on and can only turn off with a negative gate-to-source voltage (if the JFET is n-type). While papers like [37], [38] demonstrate converters using SiC JFETs switching in the kHz range, not much literature exists for MHz converters implementing JFETs. Despite this, SiC JFETs present key benefits over SiC MOSFETs. Namely, the presence

Table VI
PERFORMANCE METRICS OF THE CLASS-E AMPLIFIER USING THE RESONANT GATE DRIVER.

Part	Description
V_{in}	60 V
I_{in}	0.86 A
P_{in}	51.6 W
V_{out}	23.5 V _{rms}
I_{out}	1.88 A _{rms}
P_{out}	44.2 W
P_{gate}	5.6 W
η w/o gating loss	85.7%
η w/ gating loss	74.8%



(a)



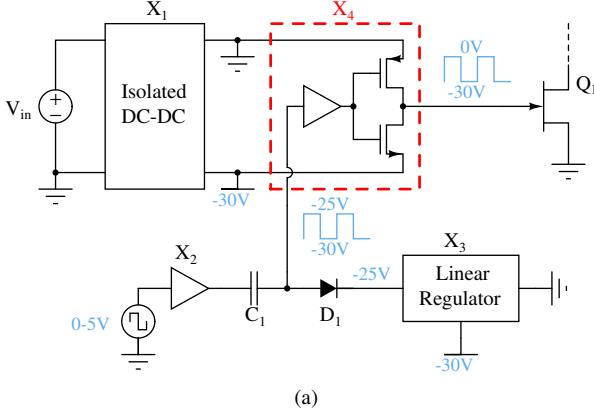
(b)

Figure 17. (a) Photograph of class-E resonant converter using a flip-chip packaged MOSFET and switching at 30 MHz with the resonant gate drive. (b) Drain, gate, and output waveforms of the class-E inverter.

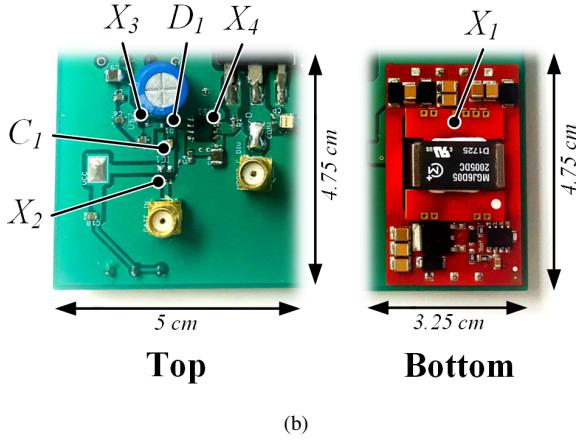
of oxide traps and defects degrade the channel mobility of SiC MOSFETs causing the threshold voltage and on-resistance to be dependent on temperature and age [17]. Additionally, [39] reports that SiC JFETs have lower C_{oss} losses than SiC MOSFETs. Both facts hint that SiC JFETs have capabilities to achieve higher efficiency than SiC MOSFETs. In this section, we present a JFET resonant gate drive scheme, similar to the one developed for the MOSFET and compare the performance

with a hard-switched version.

A. Hard-Switching Gate Driver



(a)



(b)

Figure 18. (a) Schematic for a hard-switched JFET gate driver. (b) Photograph of the gate driver on a PCB.

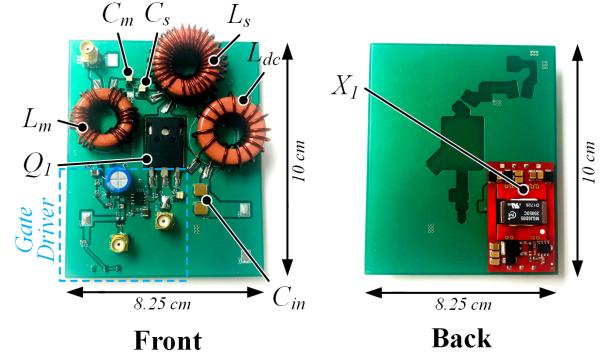
Figure 18a displays the hard-switched gate drive topology. The JFET is driven by X_4 , a commercial totem-pole gate drive IC, which is referenced to a minus voltage provided by the isolated dc-dc X_1 . The PWM input to X_4 is supplied from a signal generator cascaded with a level shifter to provide a dc offset to the signal generator's waveform. Figure 18b shows the board containing the gate drive circuit.

Table VII
PERFORMANCE METRICS OF THE CLASS-E AMPLIFIER USING A HARD-SWITCHED DRIVER FOR THE SiC JFET.

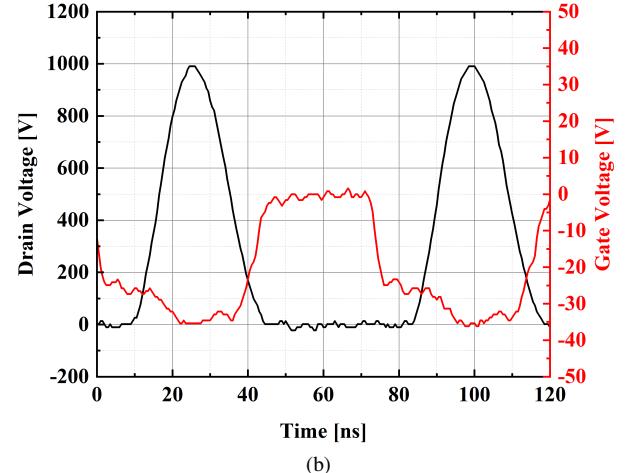
Part	Description
V_{in}	200 V
I_{in}	3.44 A
P_{in}	687.3 W
P_{out}	640 W
P_{gate}	20.3 W
η w/o gating loss	93.1%
η w/ gating loss	90.4%

Furthermore, we provide an example of a class-E inverter switching at 13.56 MHz using a UJC1208K 1700 V SiC JFET

from UnitedSiC. The converter delivers 640 W of output power with 93.1% drain efficiency and 90.4% total efficiency. Tables VIII and VII list the converter's components and performance metrics respectively, while Figures 19a and 19b show the PCB and converter's waveform.



(a)



(b)

Figure 19. (a) Photograph of the class-E inverter using a SiC JFET driven by a hard-switched gate driver. (b) Drain and gate waveforms of the converter.

B. Resonant Gate Driver

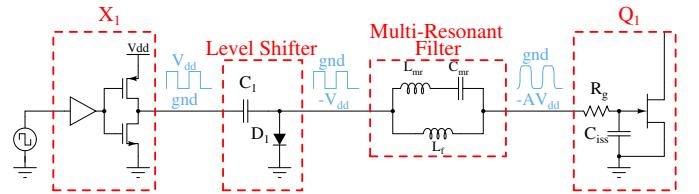


Figure 20. Schematic of multi-resonant gate driver for SiC JFET.

One of the main disadvantages of driving the JFET hard-switched is that the gating power is quite large, approximately 20 W according to Table VII. Another more subtle downside is the hardware implementation can be expensive and complex, requiring an additional dc-dc converter to provide a negative reference voltage. To reduce gating loss, we propose the resonant gate drive configuration investigated in the previous section to partially recover the energy used to charge the gate

Table VIII
KEY COMPONENTS OF THE CLASS-E AMPLIFIER USING A HARD-SWITCHED GATE DRIVER FOR THE SiC JFET.

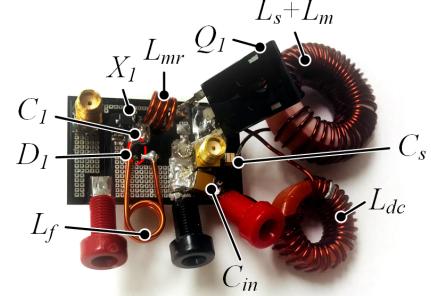
Part	Description
R_l	50 Ω RF Dummy Load
L_{dc}	767 nH, Q factor 128, AWG 18, 14 turns
L_s	2.04 μH, Q factor 180, AWG 18, 30 turns
L_m	575 nH, Q factor 163, AWG 18, 20 turns
C_1	10 μF, X7R Ceramic
C_p	30 pF, C0G Ceramic
C_s	67 pF, C0G Ceramic
C_m	117 pF, C0G Ceramic
Q_1	UJC1208K, UnitedSiC, 1700 V SiC JFET
X_1	MGJ6D05 Isolated DC-DC Converter
X_2	SN7404 5 V Logic Inverter
X_3	LM348 5 V Linear Regulator
X_4	IXDD614SI Gate Drive IC
D_1	1N4001

of the JFET. To account for the negative voltage to deplete the JFET, we cascade the level shifting circuit in front of the multi-resonant filter to create the dc offset. Figure 20 displays the schematic for the gate drive circuit.

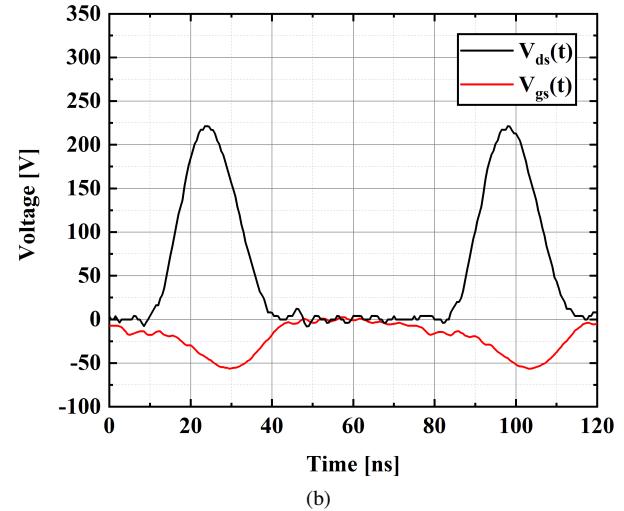
Table IX
PERFORMANCE METRICS OF THE CLASS-E AMPLIFIER USING A RESONANT GATE DRIVER FOR THE SiC JFET.

Part	Description
V_{in}	50 V
I_{in}	1.6 A
P_{in}	80 W
P_{out}	75.2 W
P_{gate}	4.8 W
η w/o gating loss	93.8%
η w/ gating loss	88%

Since the only addition to the JFET gate drive circuit compared to the MOSFET case is the addition of the level shifter, the tuning procedure and gating power dissipation are the same. Likewise, we implement a 13.56 MHz class-E inverter using the resonant gate drive method for the JFET. Table X and IX list the components and performance respectively and Figures 21a and 21b display the PCB and waveforms of the inverter. We note that our results demonstrate that SiC JFETs can in fact achieve high efficiencies at high switching frequencies. Both the hard-switched gated converter and the resonant gated converter display around 90% efficiency, but the performances are incomparable because the previous converter operates at a 640 W power level while the resonant gated converter operates at 75 W. (The two converters were designed for different applications.) Regardless, the significance is that the resonant gate driver converses over 15 W of gating power compared to the hard-switched gate driver, which is fair to compare since the two converters both switch at 13.56 MHz. Lastly, we push manufacturers to develop SiC devices with smaller



(a)



(b)

Figure 21. (a) Photograph of the class-E inverter using a SiC JFET driven resonantly with C_{mr} and C_p not shown. (b) Drain and gate voltage waveforms of the converter.

gate resistances. The large gate resistance of the UJC1208K, along with the high inductance packaging, prevented us from operating the device at VHF despite the high efficiency.

Table X
KEY COMPONENTS OF THE CLASS-E AMPLIFIER USING A RESONANT GATE DRIVER FOR THE SiC JFET.

Part	Description
R_l	50 Ω RF Dummy Load
L_{dc}	750 nH, Q factor 139, AWG 18, 23 turns
$L_s + L_m$	2.75 nH, Q factor 161, AWG 18, 40 turns
L_f	81 nH, Solenoid
L_{mr}	79 nH, Solenoid
C_p	N/A
C_{in}	20 uF, X7R Ceramic
C_s	62 pF, C0G Ceramic
C_m	118 pF, C0G Ceramic
C_{mr}	82 pF, C0G Ceramic
Q_1	UJC1208K, UnitedSiC, 1700 V SiC JFET
X_1	LM5114, Texas Instruments, gate drive IC

V. CONCLUSION

Silicon carbide power devices present numerous advantages compared to GaN and Si in high power systems with higher voltage ratings and dV/dt independent C_{oss} losses. In current applications, these devices are not widely used in HF/VHF resonant converters because of the challenges of driving these devices, as well as manufacturers not actively marketing SiC devices for the high-frequency regime with large inductance packages and gate resistances. In this report, we propose and demonstrate techniques to overcome these challenges. First, we discuss a flip-chip packaging scheme to allow commercial SiC dies to be solder-mounted onto a PCB with 50% reductance in parasitic inductances. Then, we present a multi-resonant gate driver that can fully enhance the gate while using low voltage gate driver chips and can greatly reduce gating power. We demonstrate this with a VHF 30 MHz class-E inverter with 85.7% drain efficiency. Lastly, we adapt this gate drive strategy for a SiC JFET, where we demonstrate a 13.56 MHz class-E inverter with above 90% efficiency. Overall, the market for SiC devices can shift towards to high-frequency regime and compete with GaN devices. The techniques presented in this paper, in conjunction to manufacturers producing new devices suitable for this regime, can further this trend.

VI. ACKNOWLEDGEMENTS

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