

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

This paper has been accepted for publication by

**IEEE Transactions on Power Electronics.**

**DOI**

10.1109/TPEL.2017.2693271

**Citation**

S. Park and J. Rivas-Davila, "Design of a Class-DE Rectifier with Shunt Inductance and Nonlinear Capacitance for High Voltage Conversion," *IEEE Trans. Power Electronics*, pp. 2282-2294, Mar. 2018.

**IEEE Xplore URL**

<http://ieeexplore.ieee.org/document/7896644>

More papers from Juan Rivas's group at Stanford University can be found here:

<http://superlab.stanford.edu/publications.html>

# Design of a Class-DE Rectifier with Shunt Inductance and Nonlinear Capacitance for High Voltage Conversion

Sanghyeon Park and Juan M. Rivas, *Member, IEEE*

**Abstract** – This paper presents a design method for a resonant class-DE rectifier with a shunt inductance input network. The Class-DE resonant rectifier offers numerous advantages at high operating frequencies and high output voltages. For a high-voltage design, the limiting factor has been the absence of a design process incorporating shunt inductance for low-to-high impedance matching as well as nonlinear capacitance from semiconductor devices. To design a rectifier with a specific input impedance at the fundamental frequency of operation, designers have been relying on either parametric variation in iterative simulations which often takes a long time to complete, or simple equations without considering nonlinear capacitances which renders the analysis inaccurate at high frequencies. In this paper, we propose a design procedure that begins with universal design curves which are applicable regardless of the capacitance nonlinearity. This is followed by parameter selection and a convergence check to ensure the rectifier operates at the desired output voltage. Based on the outlined procedure, we design and experimentally verify a 27 MHz 350 V current-driven rectifier, a 25 MHz 500 V voltage-driven rectifier, and a 27.12 MHz 2 kV 4-stage rectifier, all of which the resonant capacitor is nonlinear and the input impedance is resistive at the switching frequency.

**Index Terms**—Resonant power conversion, Rectifiers, AC-DC power conversion.

Part of this work has been presented at the 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, Norway, 2016 [1].

## I. INTRODUCTION

Class-DE resonant rectifier [2]–[7] is suitable for high-voltage conversion (100s of V or higher) at high switching frequencies (faster than 10 MHz). This rectifier achieves zero-voltage switching across the diodes [8] for high efficiency operation. Regarding the high-voltage conversion, class-DE rectifier topology has several advantages over class-E and  $\Phi_2$  topologies [9]. First, the voltage stress on switches is a few times lower than that in class-E or  $\Phi_2$ . This allows us to use better semiconductor devices. Second, the equivalent input impedance at the switching frequency is lower. This lower input impedance relaxes the quality factor requirement for the preceding matching network that bridges the low-voltage inverter output and the high-voltage rectifier input. Moreover, high output voltage makes the diode voltage drop negligible, rendering passive rectification a viable option. Using a pair of diodes instead of active switches eliminates the need to build a floating gate drive and to synchronously control multiple switches. Table I summarizes the pros and cons of the class-DE topology compared to other resonant converter topologies.

Another advantage of the class-DE rectifier is that it is possible to capacitively isolate multiple rectifiers and connect

them in series [10], [11] to achieve a large voltage gain, fast rise time, high efficiency and small size. For example, [11] experimentally demonstrates a dc-dc converter with a gain of 50, a risetime shorter than 10  $\mu$ s from 0 to 2 kV and 84% dc-dc efficiency. Such stacked rectifiers can be used to generate several to tens of kV dc voltage that finds its use in advanced space applications [12] and medical applications including electroporation sterilizers [13], [14] and X-ray generators [15].

Design guidelines for the class-DE topology have been provided for both inverters [16]–[23] and rectifiers [2]–[7], but they all miss one or two essential elements of a high-frequency high-voltage design. First, for low-to-high dc-dc voltage conversion it is necessary to analyze the effect of adding a shunt inductor as part of a low-to-high impedance matching network [24]. The shunt inductor changes the circuit operation in a way that makes published analyses inaccurate and calls for a dedicated investigation. Moreover, design methods with nonlinear capacitance are either missing or unsatisfactory for high voltage conversion. The undesirable effect of nonlinear capacitance manifests itself at high frequencies because semiconductor junction capacitances become comparable to necessary resonant capacitance values and thus cannot be ignored. [23], [25], [26] include nonlinear capacitance into the design process, but the proposed method requires that the designer can freely adjust the semiconductor size, which is a good assumption in integrated circuits but often not the case in discrete circuit designs. Also, [21], [23] assumes a duty ratio of 25% which is often too high for low-current high-voltage applications [12]–[15]. More importantly, analyses in previous publications such as [21], [23] are limited to only one particular value of the switch duty cycle. [8], [19], [27] address this problem by evaluating parameters at multiple duty cycles and summarizing them into a table or a plot. However, such plot or table may be difficult to use when the designer selects a duty ratio that is in between sampled values or out of the evaluation range. As a result of the aforementioned drawbacks of conventional methods, the analysis has been inaccurate, the tuning process has been lengthy and has not guaranteed the

TABLE I: Comparison of rectifier topologies for a multi-MHz frequency operation. Evaluations are made in reference to each other.  $V_o$  denotes the rectifier output voltage.

Topology	Class-E	Class-DE	Class- $\Phi_2$
<b>Input Impedance</b>	High	Low	Middle
<b>Voltage Stress on Switch</b>	$\approx 4V_o$	$= V_o$	$\approx 2V_o$
<b>Design Complexity</b>	Low	Low	High
<b>Difficulty of Sync. Rect.</b>	Low	High	Low

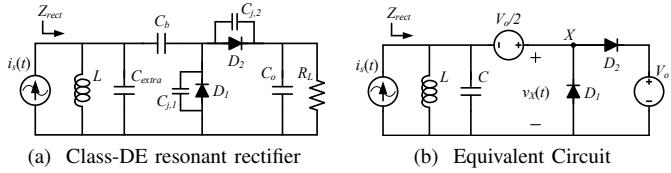


Fig. 1: (a) Class-DE resonant rectifier.  $C_b$  and  $C_o$  are large enough to present negligible impedance at the switching frequency; therefore, they can be modelled as a dc voltage source of  $V_o/2$  and  $V_o$ , respectively. (b) The equivalent circuit of the rectifier:  $C_b$  and  $C_o$  are replaced with voltage sources for the aforementioned reason;  $C_{extra}$ ,  $C_{j,1}$  and  $C_{j,2}$  are combined to form  $C$ .

convergence of the output voltage to the intended value under realistic load conditions.

We propose a class-DE rectifier design method [1] with following advantages. First, this design method incorporates nonlinear capacitance of a wide range of  $C - V$  profiles. The method is applicable to nonlinear capacitances with any grading coefficient as defined in [28]. Second, the proposed methodology includes a convergence analysis that reveals whether the circuit will initially converge to the desired steady state at rectifier startup. The analysis also identifies the range of the output voltage and load range in which the on-off control scheme [29]–[31] is available. Lastly, the method exploits a pair of design curves which are obtained from the compression of complete two-dimensional design spaces. The compression of the design space not only provides a simple yet accurate parameter selection process but also gives us an easy way to fully explore two degrees of design freedom in search of an optimum design point.

This paper is organized as follows. Section II provides the analysis on the rectifier operation and the theoretical background of the proposed design methodology. Section III presents experimental results to validate the proposed design curves. Section IV illustrates the design procedure by designing a 350 V 27 MHz current-driven rectifier and a 500 V 25 MHz voltage-driven rectifier. As a practical example, we also design a 2 kV 300 W four-stage rectifier with 15  $\mu$ s rise time that can be used in real-world applications [13], [14].

Section V concludes the paper.

## II. ANALYSIS ON THE CLASS-DE RECTIFIER

The schematic of the class-DE resonant rectifier is shown in Fig. 1a along with its simplified equivalent circuit in Fig. 1b. Notice that the diode's junction capacitance  $C_{j,1}$  and  $C_{j,2}$  can be combined with  $C_{extra}$  to create an effective resonant capacitance  $C$ . During operation of the rectifier, the sinusoidal input current  $i_s(t)$  resonates with the parallel  $LC$  tank of Fig. 1 and clamps  $v_X(t)$ , the voltage across diode  $D_1$ , either to zero or to the output voltage  $V_o$ . Current flows from ground to the node  $X$  when  $D_1$  is ON, and from node  $X$  to the output when  $D_2$  is ON. Provided that  $C_b$  and  $C_o$  are large enough to present negligible impedance at the switching frequency, their steady-state behavior can be modelled as a dc voltage source of  $V_o/2$  and  $V_o$ , respectively.

### A. Rectifier Input Impedance

Fig. 2 shows the waveforms of the inductor voltage  $v_L(t)$ , the input current  $i_s(t)$  and the output current  $i_o(t)$  of the class DE resonant rectifier of Fig. 1a as well as the equivalent circuits during the various commutation intervals within the switching cycle.

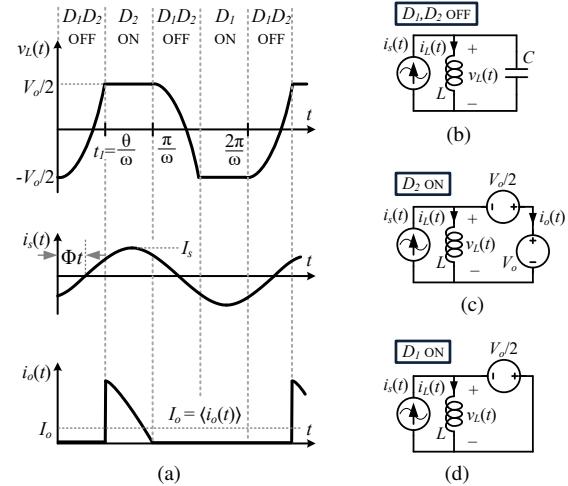


Fig. 2: Analysis of rectifier operation. (a) Waveforms of the inductor voltage  $v_L(t)$ , the input current  $i_s(t)$  and the output current  $i_o(t)$ . (b-d) Equivalent circuits according to which diode is conducting.

Here we approximate the fundamental component of the inductor voltage  $v_L(t)$  waveform in Fig. 2a as a sine wave with  $V_o/2$  amplitude and  $\theta/2$  phase offset. To justify this approximation, let us look at two extreme cases of the rectifier operating states. At one extreme, the resonant current in the  $LC$  tank is large and the capacitor  $C$  is charged and discharged very quickly. In this case,  $v_L(t)$  takes the form of a square wave and the fundamental component of  $v_L(t)$  is a sine wave having the amplitude of  $\frac{4}{\pi} \cdot (V_o/2) = 1.27(V_o/2)$ . At the other extreme where the resonant current is small, the capacitor is charged slowly such that  $v_L(t)$  barely reaches  $V_o/2$  (or  $-V_o/2$ ) before it starts to decrease (or increase). Here  $v_L(t)$  waveform is close to a triangle wave of which the fundamental component is a sine wave with the amplitude of  $\frac{8}{\pi^2} \cdot (V_o/2) = 0.81(V_o/2)$ . The analysis on those two cases reveals that in all the possible operating states between the two extremes the amplitude of the fundamental component of  $v_L(t)$  can be approximated to  $V_o/2$  with equal to or less than 27% error. Also, in either cases the phase offset of the fundamental component sine wave is roughly  $\theta/2$  where  $\theta$  represents the phase interval where both  $D_1$  and  $D_2$  are off. For that reason we approximate the phase offset of the fundamental component of  $v_L(t)$  by  $\theta/2$ .

$Z_{rect}$  is defined as the input impedance of the rectifier at the switching frequency. By the approximation above, the magnitude of the impedance  $|Z_{rect}|$  is expressed as

$$|Z_{rect}| \approx \frac{V_o}{2I_s} \quad (1)$$

where  $I_s$  is the amplitude of the sinusoidal input current  $i_s(t)$ . Also, the phase of the impedance  $\angle Z_{rect}$  can be approximated

by

$$\underline{Z}_{rect} \approx \frac{\theta}{2} - \Phi \quad (2)$$

where  $\Phi$  is the phase offset of  $i_s(t)$ .

### B. Universal Design Curves

Fig. 3 shows a plot of the analytical solutions of the input-to-output current gain ( $I_o/I_s$ ) (Fig. 3a) and the input impedance phase ( $\underline{Z}_{rect}$ ) (Fig. 3b), plotted against  $\theta$  and  $\omega\sqrt{LC}$ .

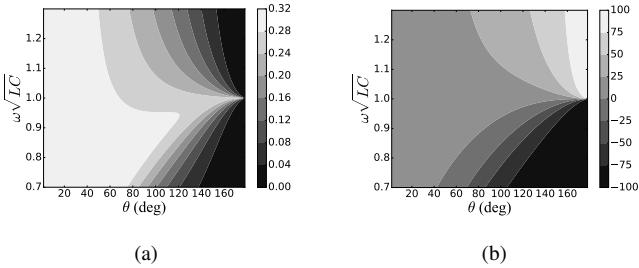


Fig. 3: Analytical solution of the class-DE resonant rectifier. (a)  $I_o/I_s$  (b)  $\underline{Z}_{rect}$

$(I_o/I_s)$  and  $\underline{Z}_{rect}$  are found by imposing the following four conditions on the circuit of Fig. 1b: a) When  $D_1$  switches from the ON-state to the OFF-state (at  $\phi = 0$  in Fig. 2), the current through  $D_1$  is zero, and b) the voltage across the inductor is  $-V_o/2$ ; c) when  $D_2$  switches from the OFF-state to the ON-state (at  $\phi = \theta$  in Fig. 2), the voltage across the inductor is  $V_o/2$ ; and d) Half a cycle after  $D_1$  turns OFF (at  $\phi = \pi$  in Fig. 2), the current through  $D_2$  reduces to zero and turns  $D_2$  OFF for periodicity. The detailed derivation is presented in Appendix.

Fig. 4 shows the analytical solution of  $(I_o/I_s)$  and  $\underline{Z}_{rect}$  that are plotted against a new design parameter  $u$  defined as

$$u := (\omega\sqrt{LC} - 1) \frac{V_o}{I_s\sqrt{L/C}} \quad (3)$$

The definition of  $u$  is constructed such that  $(I_o/I_s)$  and  $\underline{Z}_{rect}$  plotted against  $u$  remain almost constant with respect to the vertical axis variable  $\omega\sqrt{LC}$ .

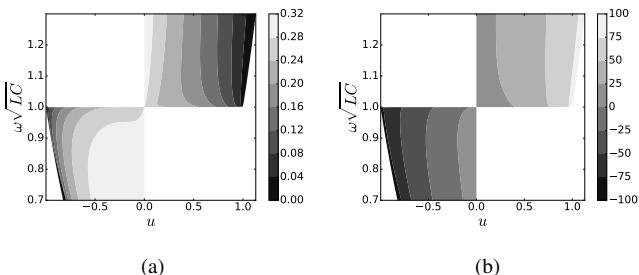


Fig. 4: Analytical solution of the rectifier rearranged in terms of parameter  $u$ . (a)  $I_o/I_s$  (b)  $\underline{Z}_{rect}$

Since Fig. 4 plots are roughly independent of  $\omega\sqrt{LC}$ , they can be approximated into two-dimensional curves in Fig. 5. To make the analysis result easily incorporated into the design

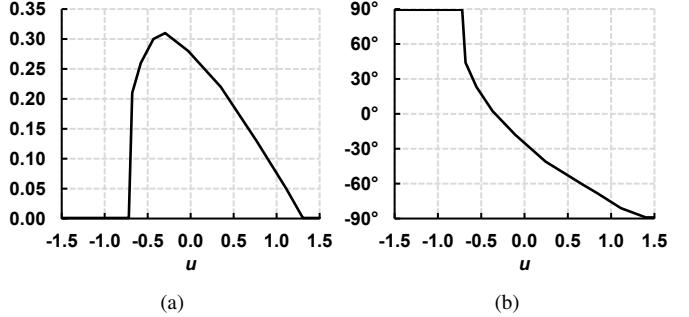


Fig. 5: Dimension-compressed solutions for the class-DE rectifier current gain and input impedance phase. (a)  $I_o/I_s$  (b)  $\underline{Z}_{rect}$

procedure, the current gain ( $I_o/I_s$ ) is re-expressed in terms of the input impedance magnitude  $|Z_{rect}|$ , by noting that  $|Z_{rect}| \approx \frac{V_o}{2I_s}$  as discussed in Subsection II-A:

$$\frac{I_o}{I_s} = \frac{2I_o}{V_o} \cdot \frac{V_o}{2I_s} \approx \frac{2I_o}{V_o} |Z_{rect}|. \quad (4)$$

Using the values found in Fig. 4 the normalized input resistance  $R_{rect,n}$  and the normalized input reactance  $X_{rect,n}$  are calculated as:

$$R_{rect,n} = \frac{2I_o}{V_o} |Z_{rect}| \cos \underline{Z}_{rect} \quad (5)$$

$$X_{rect,n} = \frac{2I_o}{V_o} |Z_{rect}| \sin \underline{Z}_{rect}. \quad (6)$$

Plotting (5) and (6) gives the design curves in Fig. 6. The

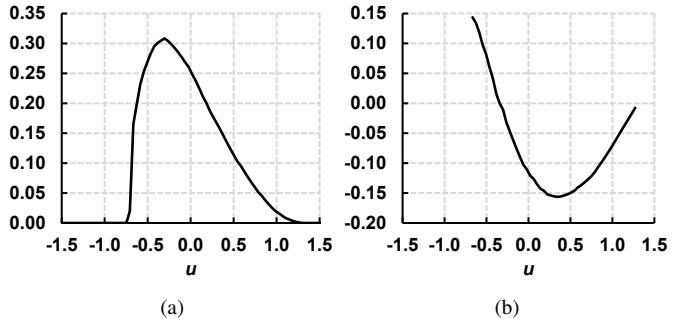


Fig. 6: Design curves for the class-DE rectifier normalized input resistance  $R_{rect,n}$  and reactance  $X_{rect,n}$  plotted versus  $u$ . Note that  $R_{rect,n}$ ,  $X_{rect,n}$  and  $u$  have no unit. (a)  $R_{rect,n}$  (b)  $X_{rect,n}$

curves are experimentally shown to be valid over a wide range of class-DE rectifier designs. They provide a convenient way of determining circuit parameters during the rectifier design process.

### C. Nonlinear resonant capacitance

The curves in Fig. 6 are valid even when the resonant capacitor is nonlinear. The model's validity with nonlinear capacitance is important because significant portion, if not all, of the resonant capacitor may consist of highly nonlinear semiconductor junction capacitance. To make the model useful for nonlinear capacitance, the effective capacitance  $C_{eff}|_{V_o}$  is

introduced.  $C_{eff}|_{V_o}$  is defined as the total amount of charge circulating in the  $LC$  resonant tank divided by the voltage swing  $V_o$ , or simply put, the average of the  $C$  vs.  $V$  curve in the range of 0 to  $V_o$ . In the class-DE rectifier depicted in Fig. 1a,  $C_{eff}|_{V_o}$  is calculated by the following equation:

$$C_{eff}|_{V_o} = C_{extra} + \frac{2 \int_0^{V_o} C_j(v) dv}{V_o} \quad (7)$$

where  $C_{extra}$  is parallel-connected linear capacitance and  $C_j(v)$  is the diode junction capacitance at reverse voltage of  $v$  across the diode.  $C_{eff}|_{V_o}$  is used in place of  $C$  to obtain  $u$  when curves in Fig. 5 are used to design a rectifier with nonlinear capacitance. Simulations confirm that using (7) in place of linear capacitance maintains the validity of design curves in Fig. 6 over a wide range of capacitance grading coefficients [28] from 0 (perfectly linear) to 0.9 (very abruptly decreasing).

#### D. Rectifier Equivalent Circuit

The rectifier in Fig. 1b can be simplified to the equivalent circuit of Fig. 7. Once  $u$  is obtained from given specifications,

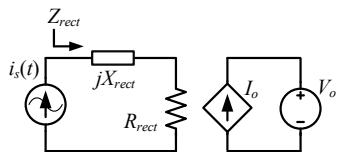


Fig. 7: Simplified circuit model of the class-DE resonant rectifier.

the corresponding  $R_{rect,n}$  and  $X_{rect,n}$  are found in Fig. 5a.  $R_{rect}$  and  $X_{rect}$  are then calculated by the following equations:

$$R_{rect} = \frac{V_o}{2I_o} R_{rect,n} \quad (8)$$

$$X_{rect} = \frac{V_o}{2I_o} X_{rect,n} \quad (9)$$

as discussed in Subsection II-B.

$X_{rect}$  and  $R_{rect}$  may be tailored depending on the design goal. To maximize the overall efficiency,  $R_{rect}$  should be made as large as possible to minimize the influence of the driver's output resistance. If the design goal is to achieve maximum power transfer,  $R_{rect}$  should be made equal to the driver's output resistance. In either case, it is desirable to make the input impedance purely resistive by adding an impedance  $-jX_{rect}$  in series to cancel out  $jX_{rect}$ .

### III. EXPERIMENTAL VERIFICATION OF DESIGN CURVES

We perform experiments to verify design curves in Fig. 5. Rectifiers are operated in a burst mode with the duty ratio lower than 10% and the burst period of one million switching cycles throughout the whole experiments. By this way, the circuit operates for less than one tenth of the time on average and thereby avoid any significant heating that might change the inductor and diode characteristics measured at the room temperature. We monitored the circuit by using a thermal camera to make sure the temperature is kept below 30 °C,

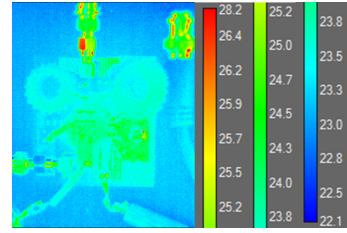


Fig. 8: Thermal image of the class-DE rectifier operating at 27.12 MHz switching frequency, 500 V output voltage and 100 mA output current. Burst duty ratio is 0.005, which is 5000 switching cycles out of the burst period of one million switching cycles. Red hot spots scattered around the image are infrared light reflected by metallic surfaces and are irrelevant to the circuit temperature.

which is 7 °C above the room temperature). Fig. 8 shows one of the thermal images we captured during the experiment.

Table II summarizes physical properties of inductors and capacitors used in all the experiments. We implement inductors by winding a AWG 18 copper wire around a toroidal phenolic core of which the resulting Q falls in the range of 100-130. This value is high enough given that the design method retained its effectiveness when Q was as low as 70 in simulation.

By the inherent characteristic of a class-DE topology, voltage stress across the switch is the same as the dc output voltage. Current stress is not discussed because the maximum current through the switch depends heavily on the linearity of the resonant capacitance. This dependency on nonlinearity makes it very difficult to derive an analytical model for the current stress. Not only the derivation, but the measurement of the current stress is also difficult due to the high sensitivity to the added inductance by a current probe in multi-MHz power converters. Nonetheless, we expect the current stress should be obtainable through simulation with a reasonable accuracy given that voltage waveforms in the experiment are in good agreement with those in our simulation as shown in Fig. 15b and Fig. 18b.

Fig. 9a shows the entire experimental setup in which an RF power amplifier is used to drive the rectifier. Fig. 9b shows the configuration of the input voltage and current probe in detail. We used Pearson 6027 Current Monitor for current measurement.

Fig. 10 shows experimental verifications of proposed design curves denoted by solid lines. Three rectifiers are designed with different resonant inductance, diodes, output voltages and switching frequencies as specified in Table III. Data points are marked on the plots to represent the measured operating state of the rectifiers. The data distribution shows good correlation with the proposed design curves, proving the validity of the presented model.

### IV. RECTIFIER DESIGN EXAMPLES

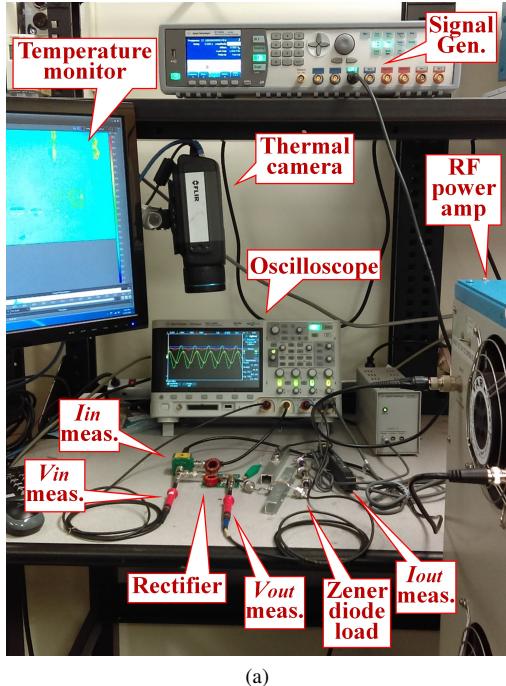
#### A. 350 V 27 MHz Current-Driven Rectifier

The design methodology described above is best illustrated by the following example. Consider designing a class-DE resonant rectifier of Fig. 1a driven by a sinusoidal current source. We want the circuit to meet the following specifications:

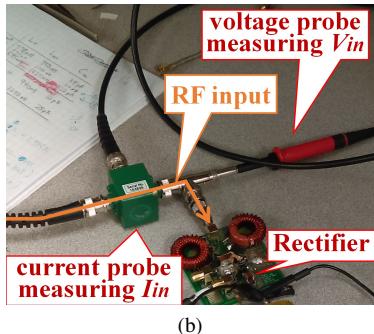
- output voltage  $V_o = 350$  V,

TABLE II: Implementation details of inductors and capacitors used in Section III. Refer to Fig. 1 and Fig. 16 for variable names.

	$L_m, L$	$C_b, C_o$	$C_{extra}$
<b>Dimension</b> (W×L×H [mm <sup>3</sup> ])	T94-0: 27 × 27 × 11 T80-0: 24 × 24 × 9 (core and wire)	10 × 6 × 6 (4 units stacked)	3 × 3 × 2
<b>Weight</b> [g]	4.9-9.2	1.4 (4 units stacked)	< 0.1
<b>Implementation</b>	18 AWG copper wire wound on Micrometals T94-0 or T80-0 toroidal phenolic core	CDE Mica capacitor, 1 kV rated	ATC 800B series NPO ceramic capacitors, 500 V rated



(a)



(b)

Fig. 9: The experimental setup. (a) Entire experimental setup for the rectifier test. Series-connected Zener diodes are being used in place of the load resistor  $R_L$  in this picture. (b) Configuration of the input voltage probe, input current probe and the RF input from the power amplifier. The flow of the input power is marked with an orange arrow.

- switching frequency  $f = 27$  MHz,
- parallel-connected linear capacitance  $C_{extra} = 107$  pF;
- use two C3D04060E SiC diodes [32] for  $D_1$  and  $D_2$ , with the measured  $C$  vs.  $V$  curve in Fig. 11a;
- the load resistance  $R_L$  at the output is 5 kΩ or larger;

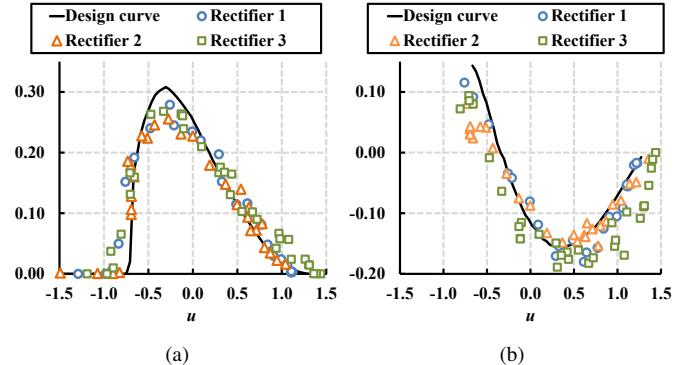


Fig. 10: Experimental verification of proposed universal design curves using three different rectifier designs specified in Table III. Proposed model curves are denoted by black solid lines and experimental data are marked as colored markers. (a)  $R_{rect,n}$  vs.  $u$  (b)  $X_{rect,n}$  vs.  $u$

TABLE III: Rectifier designs for universal design curve verifications in Fig. 10.

Rectifier No.	$D_1, D_2$ Part Number	$C_{extra}$ [pF]	$L$ [nH]	$V_o$ [V]	$f$ [MHz]
1	STPSC406B	107	400	200	16.5-28.8
2	C3D04060E	107	200	350	17.8-33.0
3	IDD03SG60C	107	600	500	17.0-22.0

- the input voltage is in phase with the input current at the switching frequency  $f$ .

We first design the rectifier to meet the full-load condition ( $R_L = 5$  kΩ) in continuous operation. Once the rectifier is designed, the on-off control scheme [29]–[31] (also known as “bang-bang control” or “burst-mode control”) is used to drive the load of 5 kΩ or larger while maintaining the output voltage at 350 V. The on-off control scheme is particularly useful in multi-MHz converters because the fast rise time of the circuit output provides a high control bandwidth [31].

### 1) First Design

$X_{rect}$  should be zero in order to achieve a resistive input impedance. Zero  $X_{rect}$  means  $u = -0.3$  according to Fig. 6b, thus  $R_{rect,n} = 0.3$  according to Fig. 6a.  $R_{rect}$  of the simplified circuit model in Fig. 7 is then calculated as  $\frac{350}{2 \cdot 0.070} = 750$  Ω. Assuming the input power is almost the same as the output power  $P_o = 350$  V · 70 mA = 24.5 W, the necessary input current to drive the rectifier is obtained as  $I_{s,rms} = \sqrt{24.5 \text{ W}/750 \Omega} = 181 \text{ mA}_{rms}$

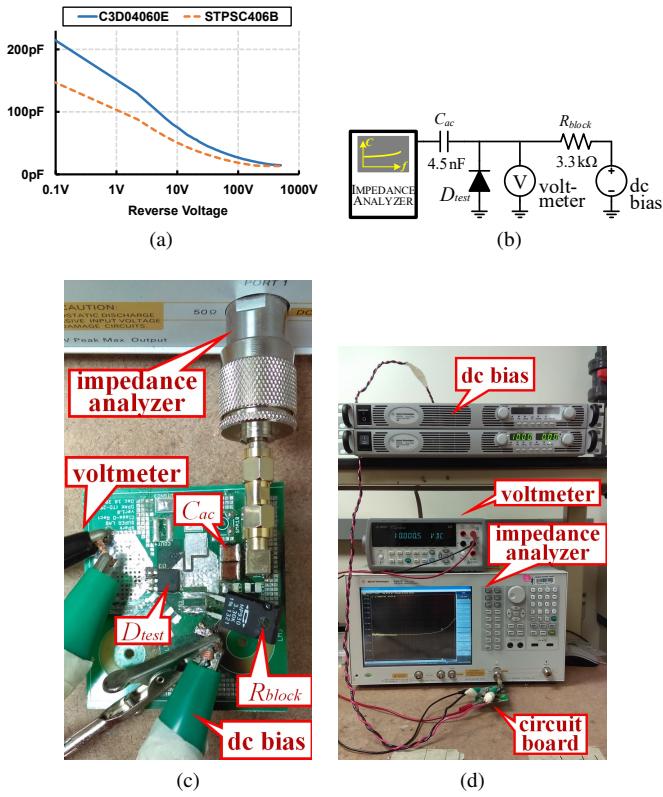


Fig. 11: Measurement of small-signal diode junction capacitances at various reverse voltage levels. (a) Measured  $C - V$  plot for  $C3D04060E$  [32] (blue solid line) and  $STPSC406B$  [33] (orange dotted line) SiC diodes. (b) Schematic of the test board. (c) Test board connected to the impedance analyzer for diode capacitance measurement. (d)  $C - V$  curve measurement setup.

The resonant capacitance is the sum of  $C_{extra}$  and two diodes' junction capacitances  $C_{j1}(v)$  and  $C_{j2}(v)$ , which are highly nonlinear. To calculate  $C_{eff}|_{V_o}$ , we integrate  $C_j(v)$  of  $C3D04060E$  [32] from zero to  $V_o = 350$  V, multiply it by two (since  $C_{j1}(v)$  and  $C_{j2}(v)$  are identical), divide it by  $V_o$  and add  $C_{extra}$  to get  $C_{eff}|_{350\text{ V}} = 166\text{ pF}$ . Combining the obtained  $C_{eff}$  and the definition of  $u$ ,  $L$  that makes  $u = -0.3$  is found to be  $207\text{nH}$ .

Since the dc-blocking capacitor  $C_b$  and the output filter capacitor  $C_o$  should exhibit negligible impedance compared to  $C_{eff}$ , we choose  $C_b = C_o = 50 \cdot C_{eff} \approx 8\text{ nF}$ . Table IV shows component values of the designed circuit.

## 2) Convergence Analysis

The next step of the design process is to check the existence of an undesired operating point. If such a point exists, the rectifier driven by a sinusoidal current source might settle into a steady-state operation of undesired  $V_o$  and  $I_o$  at startup. In order to address this issue, a convergence analysis is carried out by comparing the current consumed by the load with that supplied by the rectifier at multiple output voltages between zero and the target output voltage  $V_o$ . The convergence analysis is a direct logical consequence of the validity of design curves in Fig. 6. Therefore, the analysis described in this subsection is applicable not only to the diode used in this design but to virtually all types of linear and nonlinear

semiconductor junction capacitances.

In order to see if the designed circuit has any operating point other than the intended one, graphical analysis is carried out by drawing  $I_o$  vs.  $V_o$  line and comparing it with the load line for  $R_L = 5\text{ k}\Omega$ . Fig. 12 shows the load line (black dotted line), and the rectifier  $I_o$  vs.  $V_o$  curve (orange solid line). To draw this curve,  $C_{eff}|_{V_o}$  is evaluated for multiple values of  $V_o$  from 0 V to 500 V. This array of  $C_{eff}|_{V_o}$  is entered into

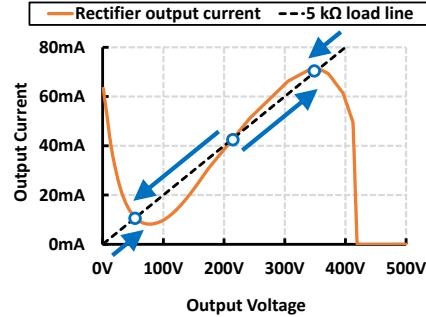


Fig. 12: Output current supplied by the 27 MHz rectifier (orange solid line) and the current drawn by the  $5\text{ k}\Omega$  resistive load (black dotted line). Three intersections of two curves are marked by blue dots, from left to right: the undesired convergence point, divergence point, and the desired convergence point. Blue arrows indicate the direction to which the operating point moves.

the definition of  $u$  to produce the array of  $u_{(V_o)}$ , which in turn is used in conjunction with Fig. 5a to find  $I_o$ . The plot reveals one divergence point at  $(V_o, I_o) = (216\text{ V}, 43\text{ mA})$ , and two convergence points at  $(54\text{ V}, 11\text{ mA}), (350\text{ V}, 70\text{ mA})$ . When the output voltage is between  $54\text{ V}$  and  $216\text{ V}$ , the rectifier  $I_o$  vs.  $V_o$  curve is drawn below the load line, meaning the rectifier cannot supply a larger current than that consumed by the load resistor, thus cannot push  $V_o$  all the way up to the target output voltage  $350\text{ V}$ . This phenomenon occurs because the nonlinear capacitor severely detunes the circuit while the output voltage transitions between  $54\text{ V}$  and  $216\text{ V}$ . Not only the circuit might settle into the undesired convergence point during the start-up, but also it becomes difficult to use the on-off control scheme since the output voltage might never recover once it falls into the aforementioned voltage range.

## 3) Redesign

To remove the unwanted convergence point we need to change at least one of the design specifications. Possible remedies include increasing  $I_o$ , using diodes whose junction capacitance decreases more gradually with voltage or decreasing  $f$ . Here we choose to increase  $I_o$  from  $70\text{ mA}$  to  $200\text{ mA}$  and redesign the rectifier so that the circuit has enough output current headroom for the on-off control. By following the procedure described above,  $L$  changes to  $202\text{ nH}$ , the full load  $R_L$  to  $1.75\text{ k}\Omega$ , and  $I_s$  to  $516\text{ mA}_{rms}$ . The corresponding analysis plot is shown in Fig. 13 by the blue dotted line. The convergence point exists only at  $(V_o, I_o) = (350\text{ V}, 200\text{ mA})$  when the load is  $1.75\text{ k}\Omega$ , which means that we can always make the circuit converge at the desired operating point by using the on-off control strategy when  $R_L$  is  $1.75\text{ k}\Omega$  or higher.

TABLE IV: The list of component values for the current-driven rectifier of Fig. 1a designed in Subsection IV-A1.

$V_o$ [V]	$I_o$ [mA]	$f$ [MHz]	$D_1, D_2$	$C_{extra}$ [pF]	$R_L$ [kΩ]	$C_o, C_b$ [nF]	$L$ [nH]	$I_s$ [mA <sub>rms</sub> ]
350	70	27	C3D04060E	107	5	8	207	181

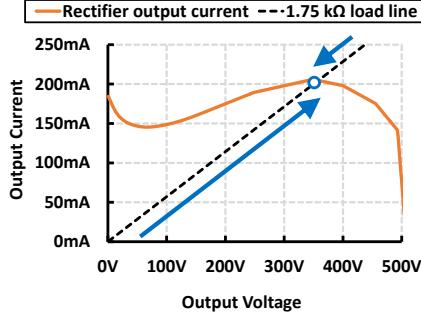


Fig. 13: Output current supplied by the 27 MHz rectifier (orange solid line) redesigned in Subsection IV-A3, and the current drawn by the new 1.75 kΩ resistive load (black dotted line). The single intersection of two curves, marked by the blue dot, indicates the rectifier always converges to the desired convergence point.

TABLE V: Comparison of the rectifier model in Section IV-A and the actual circuit in Fig. 14.

	$I_s$ at $f$ [mA <sub>rms</sub> ]	$\angle Z_{rect}$ at $f$ [degree]	$V_o$ [V]	$I_o$ [mA]
Model	516	0°	350	200
Experiment	600	1.6°	350	203

#### 4) Experiment

The 70 W 27 MHz 350 V rectifier designed in Subsection IV-A3 is implemented and shown in Fig. 14. On the left of Fig. 14 is a 0.4 pF capacitive voltage divider to measure the input voltage. Connecting the voltage probe directly without the capacitive divider adds more than 7 pF capacitance to the input node and would noticeably disrupt the circuit behavior [24].

Fig. 15 shows waveforms of the input current, input voltage and the comparison with the simulation. The rectifier represents a resistive input impedance of  $251 \Omega$ , which can be adjusted by adding an impedance matching network at the input. The efficiency of the rectifier is 80%. Most of the power loss is due to the large circulating current in the  $LC$  tank, which can be reduced by choosing a smaller  $C_{extra}$  value at the beginning of the design procedure.

#### B. 500 V 25 W 25 MHz Voltage-Driven Rectifier

Here we design a class-DE resonant rectifier of Fig. 16 driven by a sinusoidal voltage source. The series inductance  $L_m$  at the input provides a necessary reactance to achieve resistive input impedance. We want the design that meets the following specifications:

- output voltage  $V_o = 500$  V,
- output current  $I_o = 50$  mA at the full-load condition,
- switching frequency  $f = 25$  MHz,
- parallel-connected linear capacitance  $C_{extra} = 101$  pF;

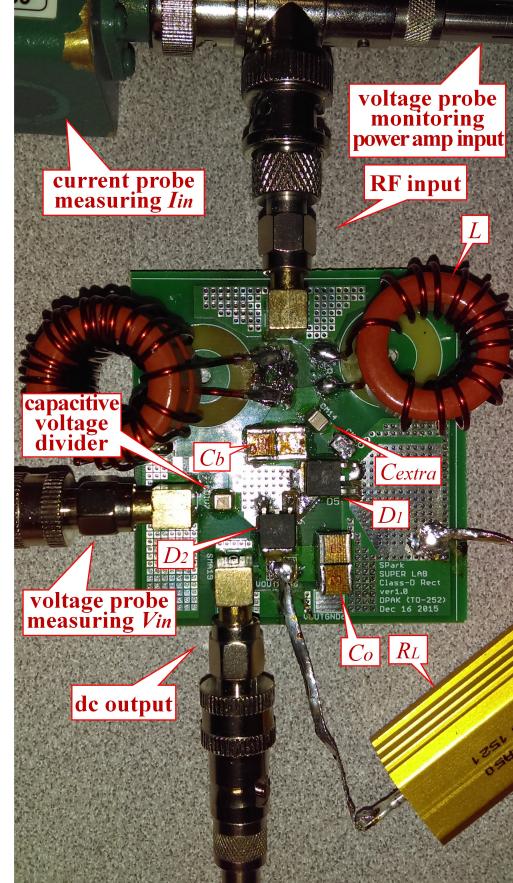


Fig. 14: Implementation of the 70 W 27 MHz 350 V current-driven rectifier designed in Subsection IV-A3. The experimental setup is identical to that in Fig. 9a and Fig. 9b except that the input voltage in this circuit is the voltage across  $D_1$ , which is denoted by  $v_{in}(t)$  in Fig. 1b. The inductor without labeling in the top left is to adjust the input impedance so that the rectifier can be driven by the preceding power amplifier.

- use two STPSC406B SiC diodes [33] for  $D_1$  and  $D_2$ , with the measured C-V curve in Fig. 11a,
- the rectifier input impedance  $Z_{rect} = 50/0^\circ \Omega$  at the switching frequency  $f$ .

Similar to Subsection IV-A, we first design the circuit for the full load and then use the on-off control strategy to regulate the output voltage at 500 V when the circuit is not under the full-load condition.

#### 1) Design

The normalized input resistance of the circuit is  $R_{rect,n} = (2 \cdot 100 \text{ mA}/500 \text{ V})50 \Omega = 0.02$ . Fig. 6a shows  $u$  parameter for  $R_{rect,n} = 0.02$  is either  $-0.71$  or  $1.08$ . We choose to select  $1.08$  since we have a series inductance at the input of the circuit ( $u = -0.71$  will require a series capacitance at the input). Fig. 6a shows that  $X_{rect,n}$  at  $u = 0.54$  is  $0.105$ , which

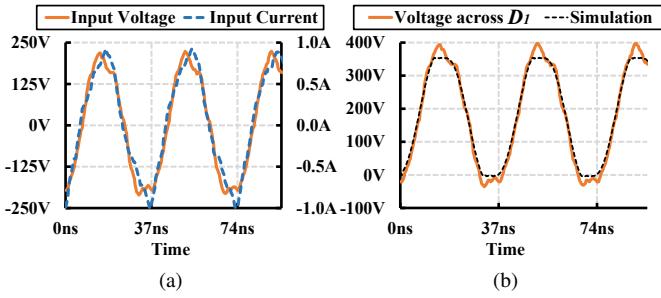


Fig. 15: Experimental voltage and current waveforms of the 27 MHz 350 V current-driven rectifier in a steady state. (a) Input current (blue dotted line) and input voltage (orange solid line) waveforms are in phase as we intended. (b) Experimental and simulation comparison of the voltage across  $D_1$ , which is equal to the input voltage shifted up by half the output voltage. We confirmed that soft switching is occurring in the simulation. Good match of increasing and decreasing sections between two waveforms indicates that soft switching is achieved in the experiment as well. Some discrepancies at the top and bottom are due to the deviation of the input current from an ideal sine wave.

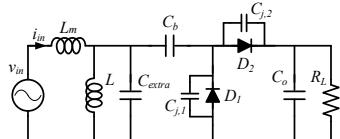


Fig. 16: Class-DE voltage-driven rectifier.

leads to  $X_{rect}$  of  $-262 \Omega$ .  $L_m$  to cancel out  $X_{rect} = -262 \Omega$  at  $f = 25 \text{ MHz}$  is  $262 \Omega / (2\pi(25 \text{ MHz})) = 1668 \text{ nH}$ .

The effective resonant capacitance  $C_{eff}$  is, following the same steps as in Subsection IV-A1, found to be 136 pF.  $L$  is then obtained by combining the definition of  $u$  in Subsection II-B with the approximation in Subsection II-A

$$u \approx (\omega\sqrt{LC} - 1) \frac{2|Z_{rect}|}{\sqrt{L/C}} \quad (10)$$

$$|Z_{rect}| = \sqrt{R_{rect}^2 + X_{rect}^2} \quad (11)$$

$$L = \frac{C}{\omega C - \frac{u}{2\sqrt{R_{rect}^2 + X_{rect}^2}}} = 363 \text{ nH.} \quad (12)$$

Assuming most of the input power appears at the output, the necessary input voltage  $V_s$  to drive the circuit is  $\sqrt{V_o \cdot I_o \cdot 50 \Omega} = 35.4 \text{ V}_{rms}$ . The dc blocking capacitor  $C_b$  and the output filter capacitor  $C_o$  are set to 8 nF for the same reason as in Subsection IV-A1. Table VI summarizes component values of the designed circuit.

## 2) Experiment

The 25 W 25 MHz 500 V rectifier designed in Sub-section IV-B1 is built as shown in Fig. 17. As shown in Fig. 18a, the input voltage and current waveforms are in-phase with phase difference of only  $0.06^\circ$ . Those two waveforms represent a resistive input impedance of  $70.6 \Omega$ , which is somewhat larger than the intended value  $50 \Omega$ . The designer can reduce the input impedance by repeating the design steps in Subsection IV-B with the target input impedance lower than

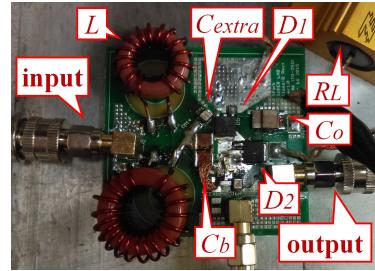


Fig. 17: Implementation of the 25 MHz 500 V 50 mA voltage-driven rectifier designed in Subsection IV-B. The experimental setup is identical to that in Fig. 9a and Fig. 9b.

50  $\Omega$ . This will yield a smaller resonant inductance, larger resonant capacitance, or both. The efficiency of the rectifier is 82%, which can be improved by choosing a smaller  $C_{extra}$  value at the design stage and thus reducing the circulating current in the  $LC$  tank.

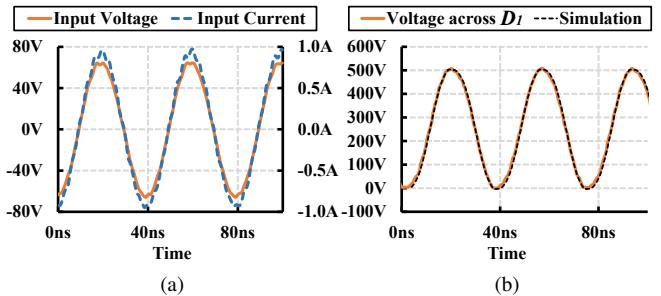


Fig. 18: (a) Experimental input current (blue dotted line) and voltage (orange solid line) of the 25 MHz rectifier in a steady state. The input impedance is  $70.6/\underline{0^\circ}$   $\Omega$ , somewhat larger than the intended  $50/\underline{0^\circ}$   $\Omega$ . (b) Comparison of the voltage across  $D_1$  in the experiment and simulation. Similar to Fig. 15b, a good match between two waveforms indicates that soft switching is indeed occurring in the experiment.

## *C. 2 kV 300 W 27.12 MHz Voltage-Driven Four-Stage Rectifier*

We design a four-stage class-DE rectifier driven by a sinusoidal voltage source [10]. The schematic is shown in Fig. 19. This structure allows us to remove the output filter capacitor  $C_{0(n)}$  because the series connection of  $C_{B,t(n)}$  and  $C_{B,b(n)}$  in any n-th stage provide a low-impedance ac path for the output voltage ripple. The specifications to be met are as follows:

- output voltage  $V_o = 2$  kV,
  - output current  $I_o = 150$  mA at the full-load condition,
  - switching frequency  $f = 27.12$  MHz,
  - use *STPSC406B* SiC diodes [33] for  $D_{(b,t)(n)}$  ( $n = 1$  to 4), with the measured  $C-V$  curve in Fig. 11a;
  - the rectifier input impedance  $Z_{rect} = 50/\underline{0^\circ}$   $\Omega$  at the switching frequency  $f$ .

### *1) Design*

The circuit structure in Fig. 19 is equivalent to four voltage-driven class-DE rectifiers of Fig. 16 connected in parallel. We first design a single rectifier with 500 V output voltage,

TABLE VI: The list of component values for the voltage-driven rectifier of Fig. 16 designed in Subsection IV-B.

$V_o$ [V]	$I_o$ [mA]	$f$ [MHz]	$D_1, D_2$ Part Number	$C_{extra}$ [pF]	$R_L$ [kΩ]	$C_o, C_b$ [nF]	$L$ [nH]	$V_s$ [V <sub>rms</sub> ]
500	50	25	STPSC406B	101	10	8	363	35.4

TABLE VII: Comparison of the rectifier model in Subsection IV-B and the actual circuit in Fig. 17.

	$V_s$ at $f$ [V <sub>rms</sub> ]	$Z_{rect}$ at $f$ [degree]	$V_o$ [V]	$I_o$ [mA]
Model	35.4	50/0°	500	50
Experiment	46.2	70.6/0.06°	500	50

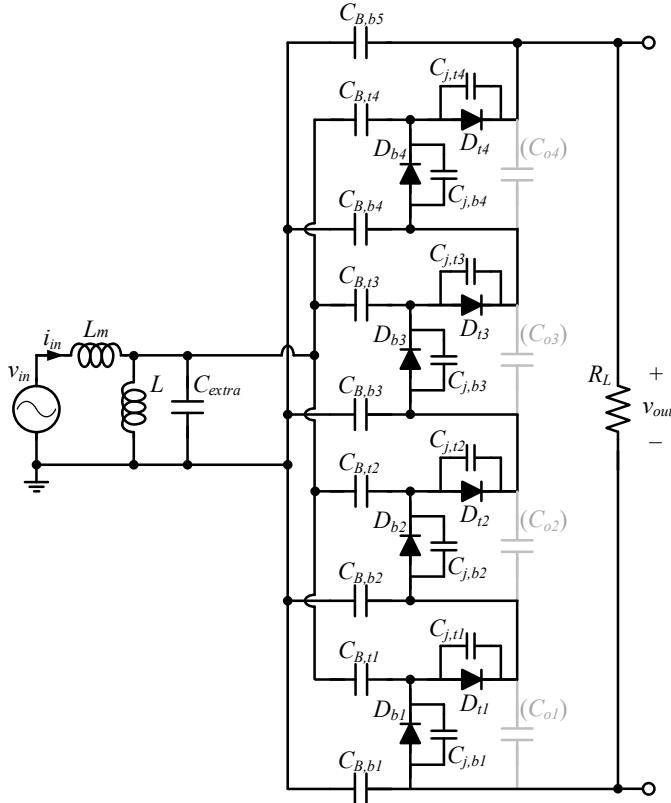


Fig. 19: Four-stage voltage-driven class-DE rectifier. This structure can be seen as four class-DE rectifiers connected in parallel. In this structure, capacitor  $C_{B,b(n)}$  and  $C_{B,b(n+1)}$  in any  $n$ -th stage provide a low-impedance ac path for the output voltage, allowing us to remove the output capacitor  $C_{o(n)}$  that is shown in a gray color.

150 mA output current, 200 Ω input impedance, and  $C_{extra}$  equal to a quarter of the shunt capacitance that the 4-stage rectifier will have. Once the design is finished,  $L_m$ ,  $L$  are divided by 4 and  $C_{extra}$  is multiplied by 4 to make a virtual parallel connection. The manufactured circuit board is found to have a 7 pF parasitic shunt capacitor. Deciding not to add any discrete shunt capacitor, we assume  $C_{extra} = (7 \text{ pF})/4 = 1.75 \text{ pF}$  for a single-stage rectifier. Following the steps outlined in Subsection IV-B1, we find  $u = 0.4755$ ,  $L = 1183 \text{ nH}$ ,  $L_m = 1483 \text{ nH}$ , and the input voltage  $V_{in} = 122 \text{ V}_{rms}$ . Connecting four units in parallel, we obtain  $L = (1183 \text{ nH})/4 = 296 \text{ nH}$ ,  $L_m = (1483 \text{ nH})/4 = 371 \text{ nH}$ , and  $C_{extra} = 4 \cdot (1.75 \text{ pF}) = 7 \text{ pF}$ . Different from

Subsection IV-A and IV-B, we choose dc blocking capacitors  $C_{B,(b,t)(n)}$  to be 820 pF. This choice of the value, which is only about five times the effective diode junction capacitor  $C_{j,b(n)} + C_{j,t(n)}$ , is to achieve a fast rise time during the rectifier start-up at the cost of less accuracy of the prescribed circuit model and a possible necessity to iterate the design steps.

## 2) Experiment

Fig. 20 shows the implemented circuit and the experimental setup. Symbols for diodes and capacitors in Fig. 20a and 20b are in reference to the schematic in Fig. 19. The bottom part of Fig. 20b is an on-off control signal generation circuit. Its schematic is shown in Fig. 20c. The resistive voltage divider scales down the output voltage by 1:400, converting 2 kV nominal output down to 5 V. It is fed to the comparator with 5% hysteresis, which in turn drives a digital isolator that generates the on-off control signal. This control signal can be connected to the gate drive and the inverter (not implemented in this paper) to complete the output voltage regulation feedback.

Fig. 21 depicts voltage and current waveforms of the input and the output. As shown in Fig. 21a, the input impedance is resistive and close to 50 Ω as intended in the design. Fig. 21b is the start-up transient of the output voltage when the rectifier is connected with a full load (a 13.33 kΩ resistor). The circuit turns on at 10 μs. The 0-90% rise time is 15 μs, fast enough to be used in the aforementioned applications [13], [14]. Fig. 21b is the  $RC$  decay waveform of the output voltage when the rectifier turns off. The rectifier input power is measured to be 319 W, the output power 301 W, and the efficiency 94.4%.

Fig. 21d shows the rectifier output voltage and the resulting on-off control signal generated by the control signal circuit in Fig. 20c. We implement the control signal circuit to prove the feasibility of the on-off control scheme in the high frequency high voltage range. In a configuration where a gate drive and an inverter is added in a feedback arrangement, the on-off signal would let the system know whether to turn on or off to maintain the desired output level. In this test, the upper and lower thresholds are set to 1.4 kV and 1.3 kV, respectively, and the rectifier is loaded with a 43.3 kΩ resistor. 9.3 μs after the output voltage exceeds 1.4 kV, the on-off signal turns on to notify the system that the operation should stop. Likewise, the on-off signal turns off in 9.3 μs when the output voltage decreases below 1.3 kV. In this rectifier, the focus was to achieve a fast start-up rise time and this design intention minimized the output filter capacitor and increased the expected voltage ripple in a feedback configuration. Should the designer decide to achieve a more accurate voltage regulation, she can add an output filter capacitor, narrow the hysteresis width or even redesign the rectifier with a smaller output current to slow the output voltage transition.

Fig. 22 shows a thermal performance of the 4-stage rectifier

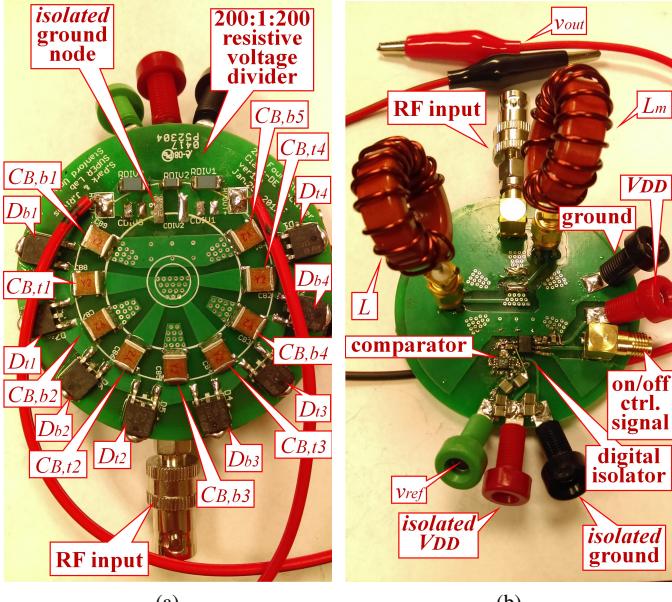


Fig. 20: (a) Front side of the 4-stage rectifier in reference to Fig. 19. (b) Back side of the 4-stage rectifier. The bottom part is for an on-off control signal generation. Its schematic is shown in Fig. 20c. (c) On-off control signal generation circuit. (d) Experimental setup for the 4-stage rectifier.

in which diodes and inductors significantly heats up during a continuous operation. We operated the rectifier for 180 s in a full-load condition (2 kV and 300 W by a 13.3 k $\Omega$  resistive load). The circuit board is 1.6 mm FR4 with 1 oz. copper with no heat sink attached. Fig. 22a captures the thermal images of the rectifier during the 180 s run. Fig. 22b indicates the temperature of the hottest spot of  $L_m$ ,  $L$  and the group of diodes. Those images and plots suggest that most of the rectifier power loss is from lossy diodes at a high voltage high frequency condition [24] and inductor losses captured in those thermal images.

## V. CONCLUSION

This paper presented a design methodology for a class-DE resonant rectifier with an impedance-matching shunt inductance and nonlinear capacitance. We first derived a curve-based design method by defining a new variable  $u$  and using it to compress two-dimensional solution spaces into a pair of one-dimensional curves. We then proposed a way to incorporate nonlinear capacitance into the design process by defining an effective capacitance  $C_{eff}$ . This method is especially useful in high frequency circuits where necessary capacitance values

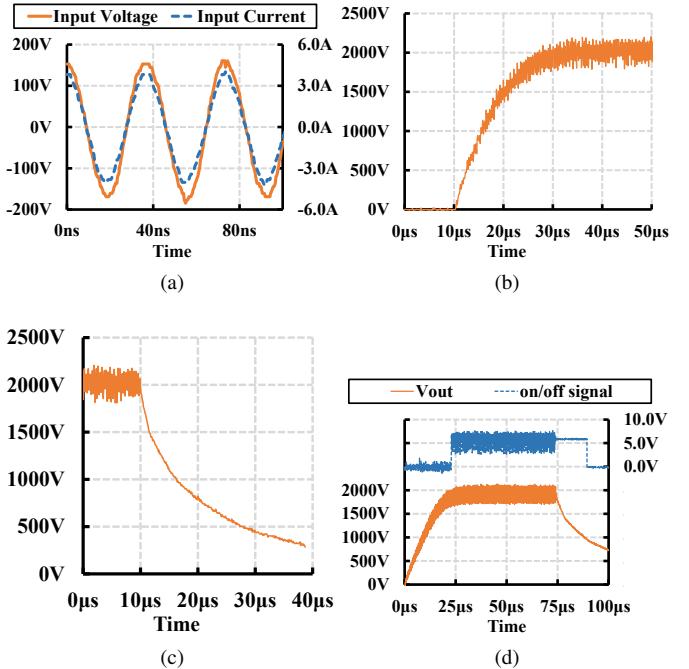


Fig. 21: (a) Input current (blue dotted line) and voltage (orange solid line) of the 4-stage rectifier in a steady state. The input impedance is  $42.7/-0.57^\circ \Omega$ . (b) The output voltage  $v_{out}$  during start-up. The rectifier turns on at  $10 \mu s$ .  $0\text{-}90\%$  rise time is  $15 \mu s$ . The peak-to-peak ripple voltage in a steady state is 411 V, equivalent to 20% of the 2 kV output voltage. (c) The rectifier turns off at  $10 \mu s$  and the  $RC$  time constant is measured to be  $10 \mu s$ . (d) Rectifier output voltage (orange solid line) and the resulting control signal (blue dotted line) from the on-off signal generation circuit in Fig. 20c, when the upper and lower threshold of the hysteresis is set to be 1.4 kV and 1.3 kV, respectively.

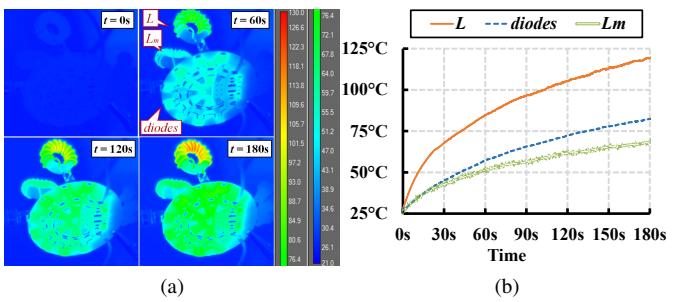


Fig. 22: (a) Thermal images of the rectifier during a 180 s continuous run in a full-load condition (2 kV 300 W). (b) The temperature of the hottest spot of  $L_m$  (green compound line),  $L$  (orange solid line) and the group of diodes (blue dotted line) during the continuous operation.

become comparable to semiconductor junction capacitances. This method also provides accurate designs for circuits with a shunt inductance for low-to-high impedance matching. We not only verified design curves experimentally, but we also successfully demonstrated the effectiveness of proposed design steps by building and testing current- and voltage-driven rectifiers. Model prediction and experimental data matches well in terms of the input impedance, output current and

voltage waveform across the diode.

## APPENDIX

### DERIVATIONS OF THE ANALYTICAL SOLUTION FOR CURRENT GAIN $I_o/I_s$ AND THE INPUT IMPEDANCE PHASE $\angle Z_{rect}$ OF THE RECTIFIER

We use rectifier equivalent circuits and waveforms in Fig. 2 to conduct the analysis. The time origin  $t = 0$  is set when the current through  $D_1$  reaches zero, turning  $D_1$  OFF while  $v_L(0) = -V_o/2$  as shown in Fig. 2a. The input current is defined as

$$i_s(t) = I_s \sin(\omega t - \Phi) \quad (13)$$

where  $\Phi$  represents the phase offset with respect to the time origin.

The operation state at  $t = 0+$  is shown in Fig. 2b where both  $D_1$  and  $D_2$  are OFF and the rectifier is equivalent to an LC tank driven by a current source. The circuit remains in this state until  $v_L(t)$  reaches  $V_o/2$  and turns ON  $D_2$  at  $t = t_1$ . Solving the linear LC resonant tank driven by the sinusoidal current source  $i_s$ , we get the inductor voltage  $v_L(t)$  and current  $i_L(t)$  as follows:

$$\begin{aligned} v_L(t) &= A_o \sin\left(\frac{t}{\sqrt{LC}} + \phi\right) \\ &+ \left(\frac{\omega I_s L}{1 - LC\omega^2}\right) \cos(\omega t - \Phi) \text{ for } 0 \leq t \leq t_1 \end{aligned} \quad (14)$$

$$\begin{aligned} i_L(t) &= -A_o \sqrt{\frac{C}{L}} \cos\left(\frac{t}{\sqrt{LC}} + \phi\right) \\ &+ \left(\frac{I_s}{1 - LC\omega^2}\right) \sin(\omega t - \Phi) \text{ for } 0 \leq t \leq t_1 \end{aligned} \quad (15)$$

where  $\phi$  is the phase offset of the general solution to the differential equation that describes the LC tank.

Our choice of time origin requires  $v_L(0) = -V_o/2$  and that  $D_1$  turns OFF at  $t = 0$ . This means the diode current  $i_{D_1}(t)$  is zero at  $t = 0$ . We therefore get the following two conditions:

$$v_L(0) = A_o \sin \phi + \left(\frac{\omega I_s L}{1 - LC\omega^2}\right) \cos \Phi = -\frac{V_o}{2} \quad (16)$$

$$\begin{aligned} i_{D_1}(0) &= i_s(t) - i_L(t) = 0 \\ &= -A_o \sqrt{\frac{C}{L}} \cos \phi - \left(\frac{I_s}{1 - LC\omega^2}\right) \sin \Phi + I_s \sin \Phi. \end{aligned} \quad (17)$$

Since we define  $t_1$  as the time when  $v_L(t) = V_o/2$  and  $D_2$  turns ON, we get another condition from (14) as follows:

$$\begin{aligned} v_L(t_1) &= \frac{V_o}{2} = A_o \sin\left(\frac{t_1}{\sqrt{LC}} + \phi\right) \\ &+ \left(\frac{\omega I_s L}{1 - LC\omega^2}\right) \cos(\omega t_1 - \Phi). \end{aligned} \quad (18)$$

This new mode of operation applies constant voltage  $V_o/2$  to the inductor  $L$ , resulting a linearly decreasing inductor current

$$i_L(t) = i_L(t_1) + \frac{V_o}{2L}(t - t_1) \text{ for } t_1 \leq t \leq \frac{\pi}{\omega}. \quad (19)$$

The symmetric circuit structure and the periodic steady-state assumption require the current through  $D_2$  be zero after half a cycle, when  $t = \pi/\omega$ . Therefore referring to Fig. 2cb and using (19) we get the fourth condition

$$\begin{aligned} i_{D_2}\left(\frac{\pi}{\omega}\right) &= i_s\left(\frac{\pi}{\omega}\right) - i_L\left(\frac{\pi}{\omega}\right) = 0 \\ &= I_s \sin(\pi - \Phi) - i_L(t_1) - \frac{V_o}{2L}\left(\frac{\pi}{\omega} - t_1\right) \end{aligned} \quad (20)$$

where  $i_L(t_1)$  is given by (15) as

$$\begin{aligned} i_L(t_1) &= -A_o \sqrt{\frac{C}{L}} \cos\left(\frac{t_1}{\sqrt{LC}} + \phi\right) + \\ &\left(\frac{I_s}{1 - LC\omega^2}\right) \sin(\omega t_1 - \Phi). \end{aligned} \quad (21)$$

Following parameters are introduced to simplify (16), (17), (18) and (20):

- $\omega_n := \omega \sqrt{LC}$
- $I_{s,n} := \frac{I_s \sqrt{L/C}}{V_o}$
- $\theta := \omega t_1$
- $A_1 := \frac{A_o}{V_o} \cos \phi$
- $A_2 := \frac{A_o}{V_o} \sin \phi$
- $B_1 := I_{s,n} \cos \Phi$
- $B_2 := I_{s,n} \sin \Phi$

These normalized parameters simplifies (16), (17), (18) and (20) into

$$A_2 + \left(\frac{\omega_n}{1 - \omega_n^2}\right) B_1 = -\frac{1}{2} \quad (22)$$

$$A_1 = -\left(\frac{\omega_n^2}{1 - \omega_n^2}\right) B_2 \quad (23)$$

$$\begin{aligned} \frac{1}{2} &= A_1 \sin\left(\frac{\theta}{\omega_n}\right) + A_2 \cos\left(\frac{\theta}{\omega_n}\right) \\ &+ \left(\frac{\omega_n}{1 - \omega_n^2}\right) B_1 \cos \theta + \left(\frac{\omega_n}{1 - \omega_n^2}\right) B_2 \sin \theta \end{aligned} \quad (24)$$

$$\begin{aligned} B_2 + \frac{1}{2} \left(\frac{\theta - \pi}{\omega_n}\right) &= \\ &- A_1 \cos\left(\frac{\theta}{\omega_n}\right) + A_2 \sin\left(\frac{\theta}{\omega_n}\right) + \\ &\left(\frac{1}{1 - \omega_n^2}\right) B_1 \sin \theta - \left(\frac{1}{1 - \omega_n^2}\right) B_2 \cos \theta. \end{aligned} \quad (25)$$

Equations (22) through (25) form a set of linear equations to which the solution  $A_1$ ,  $A_2$ ,  $B_1$  and  $B_2$  are easily found once  $\omega_n$  and  $\theta$  are given.

### A. Rectifier Input-to-Output Current Gain Plot

Once  $B_1$  and  $B_2$  are determined by (22) through (25) the normalized input current magnitude  $I_{s,n}$  is found from the definition of  $B_1$  and  $B_2$  as

$$I_{s,n} = \sqrt{B_1^2 + B_2^2}. \quad (26)$$

As shown in Fig. 2a,  $I_o$  is the time average of  $i_{D_2}(t)$ , the current through  $D_2$ .  $i_{D_2}(t)$  is nonzero only when  $t_1 \leq t \leq \pi/\omega$ . Therefore,  $I_o$  is determined as

$$I_o = \langle i_{D_2}(t) \rangle_T = \frac{2\pi}{\omega} \int_{t_1}^{\frac{\pi}{\omega}} (i_s(t) - i_L(t)) dt. \quad (27)$$

Similar to  $I_{s,n}$ , a normalized output current is defined as

$$I_{o,n} := \frac{I_o \sqrt{L/C}}{V_o}. \quad (28)$$

Combining (13), (19), (27) and (28), we obtain the expression for  $I_{o,n}$  as a function of  $\theta$  and  $\omega_n$  with four unknowns  $A_1$ ,  $A_2$ ,  $B_1$  and  $B_2$ .

$$\begin{aligned} I_{o,n} = & \frac{1}{2\pi} \left( B_1 \cos \theta + B_2 \sin \theta + B_1 \right) - \left( \frac{\pi^2 - \theta^2}{8\omega_n \pi} \right) \\ & - \left( -A_1 \cos \left( \frac{\theta}{\omega_n} \right) + A_2 \sin \left( \frac{\theta}{\omega_n} \right) \right. \\ & \left. + \left( \frac{1}{1 - \omega_n^2} \right) (B_1 \sin \theta - B_2 \cos \theta) - \frac{\theta}{2\omega_n} \right) \\ & \cdot \left( \frac{\pi - \theta}{2\pi} \right). \end{aligned} \quad (29)$$

Equation (29) in conjunction with (22) through (25) allows us to obtain  $I_{o,n}$  for a given  $\omega_n$  and  $\theta$  pair. Calculating  $I_{o,n}/I_{s,n}$  from (29) and (26) and plotting the result yields Fig. 3a.

### B. Input Impedance Phase Plot

As discussed in Subsection II-A,  $\angle Z_{rect}$  can be approximated as  $\frac{1}{2}\theta - \Phi$ . The input current phase offset  $\Phi$  equals to  $\arctan(B_2/B_1)$  by the definition of  $B_1$  and  $B_2$ . Since  $B_1$  and  $B_2$  can be found for a given  $\omega_n$  and  $\theta$  pair, we can obtain the solution of  $\angle Z_{rect}$  as in Fig. 3b.

## REFERENCES

- [1] S. Park and J. Rivas-Davila, "A design methodology for class-d resonant rectifier with parallel lc tank," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–6.
- [2] D. C. Hamill, "Half bridge class de rectifier," *Electronics Letters*, vol. 31, no. 22, pp. 1885–1886, Oct 1995.
- [3] ———, "Class de inverters and rectifiers for dc-dc conversion," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, vol. 1, Jun 1996, pp. 854–860 vol.1.
- [4] K. N. Bateson, "Class de dc-dc converters," in *Computers in Power Electronics, 1998. 6th Workshop on*, 1998, pp. 119–125.
- [5] C. Ekkaravarodom, A. Nathakaranakule, and I. Boonyaroonate, "Single-stage electronic ballast using class-de low- d v /dt current-source-driven rectifier for power-factor correction," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 10, pp. 3405–3414, Oct 2010.
- [6] C. Ekkaravarodom, K. Jirasereamornkul, and M. K. Kazimierczuk, "Implementation of a dc-side class-de low- dv/dt rectifier as a pfc for electronic ballast application," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5486–5497, Oct 2014.
- [7] K. Fukui and H. Koizumi, "Analysis of half-wave class de low dv/dt rectifier at any duty ratio," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 234–245, Jan 2014.
- [8] M. K. Kazimierczuk and W. Szaraniec, "Class d-e resonant dc/dc converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 29, no. 3, pp. 963–976, Jul 1993.
- [9] L. Raymond, W. Liang, J. Choi, and J. Rivas, "27.12 MHz large voltage gain resonant converter with low voltage stress," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 1814–1821.
- [10] L. Raymond, W. Liang, L. Gu, and J. R. Davila, "13.56 mhz high voltage multi-level resonant dc-dc converter," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–8.
- [11] L. Raymond, W. Liang, K. Surakitbovorn, and J. R. Davila, "27.12 mhz isolated high voltage gain multi-level resonant dc-dc converter," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 5074–5080.
- [12] W. Liang, L. Raymond, M. Praglin, D. Biggs, F. Righetti, M. Cappelli, B. Holman, and J. R. Davila, "Low mass rf power inverter for cubesat plasma thruster using 3d printed inductors," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–7.
- [13] S. H. Jayaram, "Sterilization of liquid foods by pulsed electric fields," *IEEE Electrical Insulation Magazine*, vol. 16, no. 6, pp. 17–25, 2000.
- [14] L. Raymond, W. Liang, K. Surakitbovorn, and J. R. Davila, "Resonant bi-polar dc pulse power supply for electroporation applications," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–5.
- [15] T. Mimura, "High voltage waveform tail steep cutting unit for x-ray intervention radiology," *Orig. Tech. J.*, vol. 64, pp. 19–26, 2001.
- [16] H. Koizumi, T. Suetsugu, M. Fujii, K. Shinoda, S. Mori, and K. Ikeda, "Class de high-efficiency tuned power amplifier," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no. 1, pp. 51–60, Jan 1996.
- [17] S. A. El-Hamamsy, "Design of high-efficiency rf class-d power amplifier," *IEEE Transactions on Power Electronics*, vol. 9, no. 3, pp. 297–308, May 1994.
- [18] L. R. Neron, "Design of a 2.5-mhz, soft-switching, class-d converter for electrodeless lighting," *IEEE Transactions on Power Electronics*, vol. 12, no. 3, pp. 507–516, May 1997.
- [19] M. Albulet, "An exact analysis of class-de amplifier at any output q," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 10, pp. 1228–1239, Oct 1999.
- [20] H. Sekiya, H. Koizumi, S. Mori, I. Sasase, J. Lu, and T. Yahagi, "Fm/pwm control scheme in class de inverter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 7, pp. 1250–1260, July 2004.
- [21] T. Ezawa, H. Sekiya, and T. Yahagi, "Design of class de amplifier with nonlinear shunt capacitances for any output q," in *2008 IEEE International Symposium on Circuits and Systems*, May 2008, pp. 2190–2193.
- [22] H. Koizumi and K. Kurokawa, "Analysis of the class de inverter with thinned-out driving patterns," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 1150–1160, April 2007.
- [23] H. Sekiya, N. Sagawa, and M. K. Kazimierczuk, "Analysis of class de amplifier with nonlinear shunt capacitances at any grading coefficient for high q and 25% duty ratio," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 924–932, April 2010.
- [24] L. C. Raymond, W. Liang, and J. M. Rivas, "Performance evaluation of diodes in 27.12 mhz class-d resonant rectifiers under high voltage and high slew rate conditions," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2014, pp. 1–9.
- [25] H. Sekiya, T. Watanabe, T. Suetsugu, and M. K. Kazimierczuk, "Analysis and design of class de amplifier with nonlinear shunt capacitance," in *2007 7th International Conference on Power Electronics and Drive Systems*, Nov 2007, pp. 937–942.
- [26] ———, "Analysis and design of class de amplifier with nonlinear shunt capacitances," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 10, pp. 2362–2371, Oct 2009.
- [27] M. Acar, A. J. Annema, and B. Nauta, "Analytical design equations for class-e power amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 12, pp. 2706–2717, Dec 2007.
- [28] P. Alinikula, K. Choi, and S. I. Long, "Design of class e power amplifier with nonlinear parasitic output capacitance," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 2, pp. 114–119, Feb 1999.

- [29] Y. S. Lee and Y. C. Cheng, "A 580 khz switching regulator using on-off control," *Electronic and Radio Engineers, Journal of the Institution of*, vol. 57, no. 5, pp. 221–226, September 1987.
- [30] J. M. Rivas, R. S. Wahby, J. S. Shafran, and D. J. Perreault, "New architectures for radio-frequency dc/dc power conversion," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 5, June 2004, pp. 4074–4084 Vol.5.
- [31] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very-high-frequency resonant boost converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1654–1665, June 2009.
- [32] Cree, "Silicon carbide schottky diode," *C3D04060E datasheet*, Aug 2013.
- [33] STMicroelectronics, "600v power schottky silicon carbide diode," *STPSC406 datasheet*, Aug 2015.