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This paper has been accepted for publication by

**IEEE Transactions on Power Electronics.**

**DOI**

10.1109/TPEL.2018.2874420

**Citation**

G. Zulauf, Z. Tong, J. Plummer, and J. Rivas, "Active Power Device Selection in HF and VHF Power Converters," *IEEE Trans. Power Electronics*, pp. 6818-6833, Jul. 2019.

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# Active Power Device Selection in High- and Very-High-Frequency Power Converters

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**Abstract**—This paper aims to provide a road map for selecting power devices in soft-switched, MHz-frequency power converters. Minimizing  $C_{OSS}$  losses, which occur when charging and discharging the parasitic output capacitor of power semiconductors, is critical to efficient operation. These losses are excluded from manufacturer-provided information and measurements are either sparse or not reported at all in existing literature.

We report the first high-frequency  $C_{OSS}$  loss data from Silicon Carbide (SiC) power MOSFETs, with a range of devices tested from 1-35 MHz and up to 800 V. In contrast to GaN HEMTs,  $C_{OSS}$  losses in SiC MOSFETs do not increase with  $dV/dt$  at these frequencies. 3-10% of the stored energy is dissipated in the measured SiC MOSFETs.

We report new  $C_{OSS}$  loss measurements for vertical silicon MOSFETs and expand on existing measurements for superjunctions, finding high variance in  $C_{OSS}$  losses between devices for both constructions. High  $C_{OSS}$  losses preclude the tested silicon MOSFETs from efficient operation at MHz frequencies.

Lastly, we compare devices in soft-switched applications using a loss calculation that includes these  $C_{OSS}$  losses, and demonstrate a 100 W, 17 MHz DC-RF inverter using a custom-packaged SiC MOSFET.

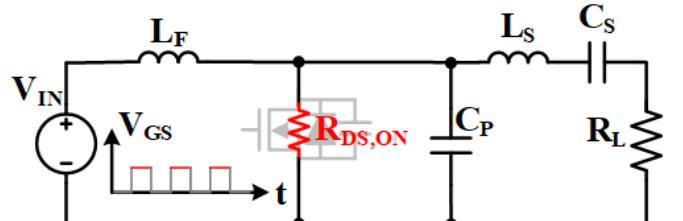
## I. INTRODUCTION

In soft-switched power converters, where power semiconductors are switched on and/or off at zero-voltage and/or zero-current, switching losses are reduced or eliminated, permitting an increase in switching frequency. This increase results in miniaturized, faster power converters [1], and has been pursued as new materials (e.g. Silicon Carbide, or SiC, and Gallium Nitride, or GaN) and constructions (e.g. the superjunction structure) for power devices have enabled higher frequency operation. Soft-switched techniques are critical in power factor correction circuits and converters for television and computer supplies, with switching frequencies up to a few MHz, and a broad range of current academic work is exploring applications in the high-frequency (HF, 3-30 MHz) and very-high-frequency (VHF, 30-300 MHz) switching frequency range, including wireless power transfer (e.g. [2]–[4]), aerospace propulsion [5], [6], and high-ratio DC-DC conversion [7]–[9], among others.

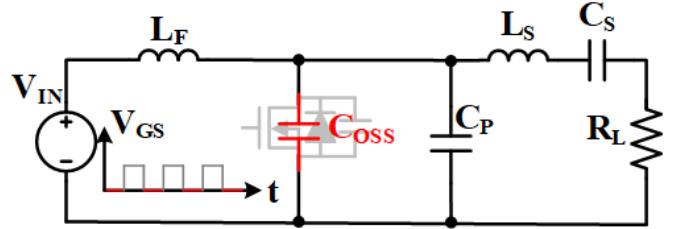
The selection of power devices for these HF/VHF converters is critical to achieving efficient and power-dense circuit operation in this emerging frequency regime. Minimizing the power dissipation in the switching device itself is extremely

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The work was supported by Airbus, Cadence Design Systems, the National Science Foundation, the Stanford Graduate Fellowship program, Stanford's SystemX Alliance, and the TomKat Center for Sustainable Energy.



(a) On-time device model, with a value of  $R_{DS,ON}$  that determines conduction losses.



(b) Off-state device model, with a voltage-dependent value of  $C_{OSS}$  in parallel with  $C_P$ .

**Fig. 1:** Switch modeling in, for example, a Class-E converter [10]. Device connections are shown backgrounded, with the device model overlaid. During the on-time of the device, conduction losses occur based on current and  $R_{DS,ON}$ . In this work, we show that, for nearly all power devices, the off-state losses of the device cannot be ignored for HF/VHF converters.

important, as these losses typically drive the most stringent thermal considerations of the power converter. In general, the components that contribute to power device losses are *a)* conduction during the device on-time (Fig. 1a), *b)* gating losses, *c)* switching losses due to I-V overlap (including reverse recovery), and *d)* switching losses from dissipating the energy stored ( $E_{OSS}$ ) in the device output capacitor ( $C_{OSS}$ ). In hard-switched converters, all of the energy stored in  $C_{OSS}$  is dissipated at device turn-on, while zero-voltage-switched converters are designed to resonantly circulate  $E_{OSS}$  (Fig. 1b) during the off-time of the device. The process of charging and discharging  $C_{OSS}$  has typically been assumed to be lossless, but recent work has shown that losses from this process are non-negligible in a range of soft-switched converters and device types [1], [8], [11]–[15].

In this paper, we focus on incorporating this non-ideality into the selection of the power semiconductor in high-power, HF/VHF converters. This loss mechanism is interchangeably referred to as  $C_{OSS}$  loss (the choice here and in [11]–[14]), intrinsic energy ( $E_i$ ) [15], zero-voltage-switching (ZVS) energy loss [8], or displacement loss [1]. These losses are a measure of the power dissipated when any capacitor is

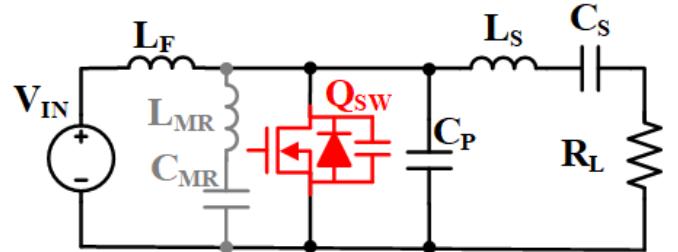
charged and discharged, analogous to the quality factor of a linear capacitor. In power devices, however, these losses cannot be modeled by a series resistor or quality factor, and previous publications have shown significant variation with frequency in GaN high-electron-mobility-transistors (HEMTs) [13], [14], [16], [17] and voltage in Si superjunction (SJ) devices [11], [12] that cannot be summarized simply by a frequency- or  $C_{OSS}$ -dependency [1] or dissipation factor [18]. The selection of this focus is further driven home by *a*) the unavailability of these parameters in manufacturer-provided datasheets or simulation models and the inability to predict these losses *a priori*, *b*) the importance of these losses at MHz operating frequencies, where these  $C_{OSS}$  losses swamp conduction losses in many applications [14], *c*) the lack of literature documenting these losses in SiC and Si MOSFETs, and *d*) even forward-looking device surveys (e.g. [19] for GaN and [20] for Si SJs) completely ignoring  $C_{OSS}$  losses.

We aim to provide a framework for designers to select the best application-specific active power device for a soft-switched converter in the MHz regime across materials, device constructions, and device sizing. Necessarily, we first must document previously-unreported measurements on  $C_{OSS}$  losses in SiC MOSFETs, Si superjunction MOSFETs, and traditional Si MOSFETs before comparing materials and devices. In Section II, we limit the devices considered to medium-voltage, unipolar, gated devices to focus the design space. In Section III, we reintroduce the  $C_{OSS}$  loss measurement procedure and review the basic operating characteristics of the Sawyer-Tower circuit to better understand potential error terms. In Section IV, we report the first  $C_{OSS}$  loss measurements on SiC MOSFETs, and in Section V, we expand on the limited measurements in [11], [12], [15], [21], [22] for silicon devices. Section VI introduces a fitting for the GaN data from [14] for a standardized waveform so that we may compare across device families. Section VII introduces a loss calculation for these devices that includes  $C_{OSS}$  losses and summarize the dependencies for each material and device construction, and we verify this loss calculation in a 17 MHz, 100 W SiC-based inverter in Section VIII. Section IX provides recommendations both for device manufacturers and designers.

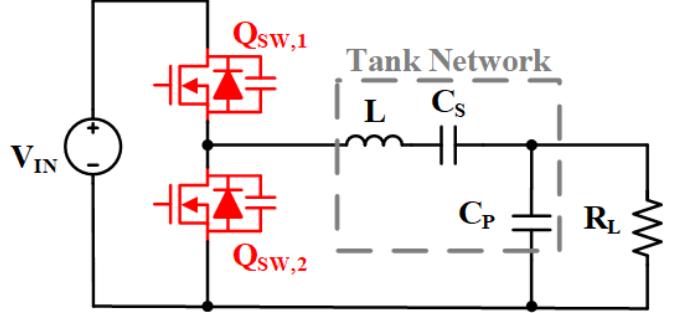
## II. APPLICATION FOCUS

We consider resonant inverter topologies where the active device is zero-voltage-switched at MHz frequencies. In these resonant topologies, the energy stored ( $E_{OSS}$ ) in the device output capacitance ( $C_{OSS}$ ) is resonantly cycled through the circuit with timing such that, at device turn-on, there is zero  $V_{DS}$ , zero  $E_{OSS}$ , and therefore zero energy dissipated when the device is turned on. Two common classes of resonant power amplifiers where these considerations are important are shown in Figure 2. Relative to the half-bridge resonant topologies (Fig. 2b), the ground-referenced single-switch topologies (Fig. 2a) have simpler gate drives but higher device voltage stresses.

At the switching frequencies considered in this paper, the switching device must be majority carrier, eliminating



(a) Ground-referenced single-switch example topologies, the Class-E [10] or Class- $\Phi_2$  [23] (added components shown in grey).



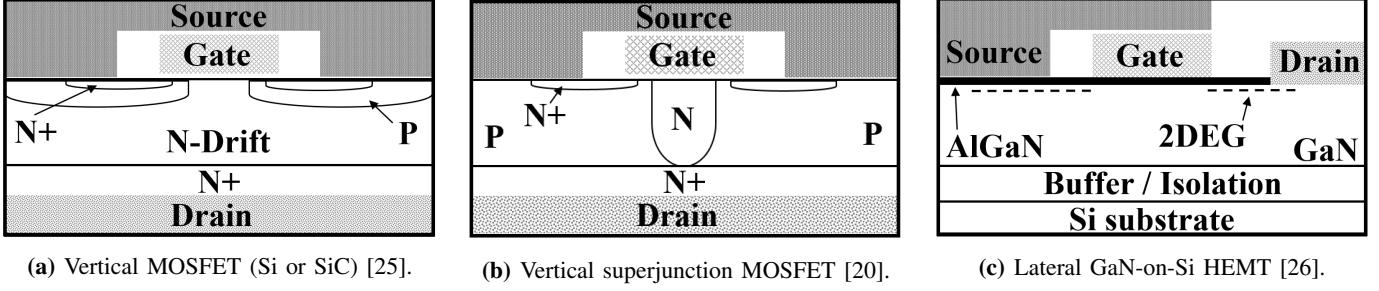
(b) Half-bridge resonant example topology, with a variety of networks capable of replacing the LCC shown above [24].

**Fig. 2:** Two sample classes of topologies where soft-switching can be achieved through resonant waveshaping. The energy stored in the device output capacitor is typically assumed to be resonantly (losslessly) recycled in both circuit topologies.

insulated gate bipolar transistors (IGBTs) from consideration. Within majority carrier constructions, we focus on gated devices, removing Schottky diodes from this work, although the material conclusions presented here are generally transferable to Schottky diodes from the same material.

We constrain our focus to devices capable of operating in resonant inverters with output powers of hundreds to thousands of watts. In the ground-referenced single-switch topologies (e.g. Fig. 2a), which dominate at  $f_{SW} \gtrsim 10$  MHz due to gate drive requirements, the output power scales as  $P_{OUT} \propto k \cdot V_{IN}^2 / R_L$ , with  $k$  less than 1 ( $8/\pi^2$  in the Class- $\Phi_2$ , 0.576 in the Class-E). For converters matched to RF (typically  $50\ \Omega$  or  $75\ \Omega$ ) loads, then, input voltages in the hundreds of volts are required to achieve kW s of output power, requiring switches with  $V_{DS}$  ratings of over 500 V. Similarly, the active devices in the half-bridge topology families (e.g. Fig. 2b) must be rated to at least  $V_{IN}$ , and similar arguments with respect to output power as a function of  $V_{IN}$  apply. This work, then, focuses on medium-voltage (500 V<sub>DS</sub> to 1700 V<sub>DS</sub>), majority carrier, gated devices for kW-power, MHz-frequency operation, with a preference for normally-off devices. Commercially available device candidates are GaN high-electron-mobility-transistors (HEMTs), Si superjunction MOSFETs, standard Si MOSFETs, and SiC MOSFETs. Evaluated device cross-sections are shown in Fig. 3.

Although the unipolar material limits vary by orders-of-magnitude between these materials, realized devices are much closer in specific on-resistance ( $sR_{DS,ON}$ ) at a given breakdown voltage [27], especially between GaN, SiC, and SJ devices. Available Si MOSFETs typically have about an order-



**Fig. 3:** Cross-sections (not to scale) of the considered device constructions. VDMOS structure shown for vertical MOSFETs.

of-magnitude higher  $R_{DS,ON}$  than comparable devices from the three other families, but, if they do not exhibit significant  $C_{OSS}$  losses, might be preferred in some low current, high-frequency applications, and are therefore worth evaluating.

### III. $C_{OSS}$ LOSS MEASUREMENT PROCEDURE

To evaluate  $C_{OSS}$  losses in power devices, we use the Sawyer-Tower circuit, which is shown in Fig. 4. This circuit was originally introduced to measure characteristics of ferroelectric capacitor material candidates [28], and was repurposed in [11] to measure losses in Si SJ devices and modified for our prior work [13], [14] to measure losses in 650 V GaN HEMTs at MHz frequencies.

#### A. General Operating Principle

Because the device capacitance is non-linear, the charge on  $C_{OSS}$  cannot be measured directly through the drain-source voltage. The Sawyer-Tower circuit uses a linear capacitor in series with the non-linear  $C_{OSS}$  to deduce  $Q_{OSS}$  based on the principle that the charge on series capacitors must be equal, or:

$$Q_{OSS} = V_X C_{REF}. \quad (1)$$

Figure 5 shows a simulation of the general circuit operation with a GaN HEMT. A bipolar sine wave is driven at  $V_Y$  by the power amplifier, attempting to apply a bipolar voltage across the device. Because all of the tested devices have some reverse conduction characteristic (a body diode or the body diode-like reverse characteristics of the GaN HEMTs [26]), the negative-going voltage is clamped, and, in these first few cycles, a negative DC bias develops across  $C_{REF}$ . With this negative offset, the steady-state operation is a simple capacitor divider between  $C_{OSS}$  and  $C_{REF}$ .  $C_{DIV}$  is added to reduce the magnitude of  $V_Y$  (through a capacitive divider with the probe capacitance) into the voltage specifications of commercially-available probes at MHz frequencies.

$C_{OSS}$  losses are reported as the energy dissipated during a single charge-discharge cycle ( $E_{DISS}$ ).  $E_{DISS}$  is distinct from the widely-reported  $E_{OSS}$  term in datasheets;  $E_{OSS}$  is the energy stored in  $C_{OSS}$  at a given drain-source voltage, while  $E_{DISS}$  is the energy dissipated in  $C_{OSS}$  during a charge-discharge cycle. The ratio of  $E_{DISS}$  to  $E_{OSS}$  is analogous to the dissipation factor of a linear capacitor (and must be less than one).  $E_{OSS}$  for a charge or discharge cycle can be calculated as:

$$E_{OSS} = \int_{Q_1}^{Q_2} V_{DS}(Q) dQ, \quad (2)$$

and the sum of this integral for the charge and discharge cycles gives the energy dissipated in a cycle,  $E_{DISS}$ :

$$E_{DISS} = E_{OSS,CHARGE} - E_{OSS,DISCHARGE}. \quad (3)$$

#### B. Body Diode Conduction

Some reviews of  $C_{OSS}$  loss measurements have implied or stated that these losses are due to conduction through the body diode (e.g. [29]). The body diode only conducts during the first few cycles when the power amplifier attempts to apply a bipolar voltage on the device, after which no current flows through the body diode. Assuming  $C_{REF}$  is much larger than the large-signal capacitance of  $C_{OSS}$ , the device remains forward-biased due to the  $V_{PP}/2$  DC voltage on  $C_{REF}$ , and the voltage across the DUT's  $C_{OSS}$  swings between 0  $V_{DS}$  and  $V_{PP}$ . This simulated operation (in simulation, the diode current can be separated from the capacitor current, which is not possible in practice) is shown for the PGA26E19BA GaN HEMT in Fig. 5 (1 MHz,  $V_{PP} = 440$  V,  $C_{REF} = 100$  pF). As expected, no current flows through the body diode during steady-state, and the “settling time” is a single cycle (settling time is up to tens of cycles for the Si devices tested here, which have finite reverse recovery charge). With soak times in the minutes, these transient body diode conduction times should not affect  $C_{OSS}$  loss power dissipation.

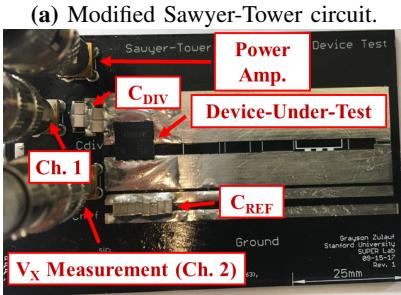
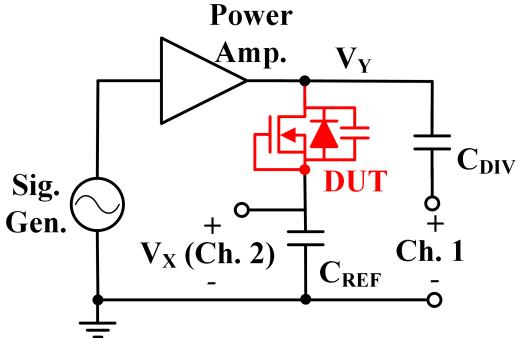
#### C. $C_{REF}$ Selection

Losses in the reference capacitor,  $C_{REF}$ , are inextricably combined with the losses in the device-under-test (DUT). The peak AC energy stored during a cycle in the reference capacitor is the same as the energy in the device, or:

$$E_{C,REF} = \frac{1}{2} C_{REF} V_X^2, \quad (4)$$

where we only consider the AC component of  $V_X$  (changes in the DC bias point occur only during the startup transient, as discussed above). And, beginning with the simple understanding that:

$$Q = \frac{\text{Peak Energy Stored}}{\text{Energy Dissipated Per Cycle}}, \quad (5)$$



(b) Test board.

**Fig. 4:** Modified Sawyer-Tower test circuit, used for GaN HEMTs in [14] and applied to SiC and Si devices in this work (TK20V60W5 shown as DUT).

which we can rearrange to find the energy dissipated per cycle in  $C_{REF}$ :

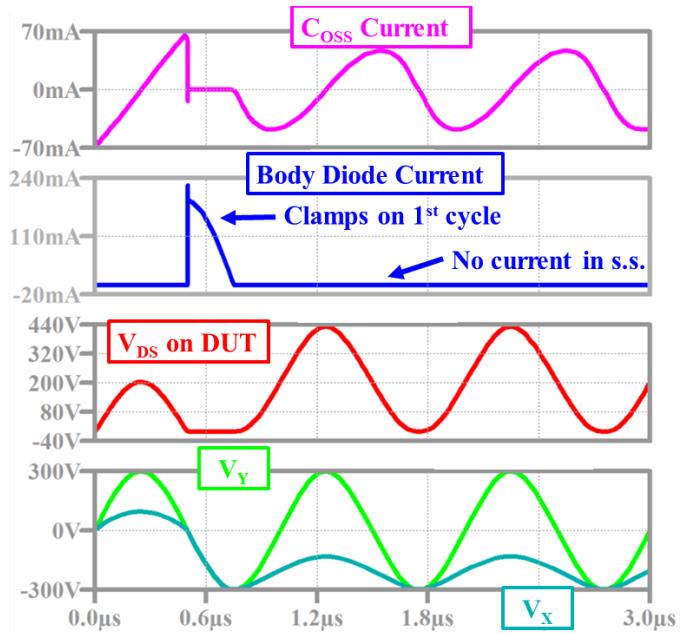
$$E_{DISS,CREF} = \frac{\text{Peak Energy Stored}}{Q} = \frac{C_{REF} \cdot V_X^2}{2 \cdot Q_{C,REF}}. \quad (6)$$

Based on this equation, we see that the percent energy dissipation that we can measure is limited directly by the dissipation factor ( $DF = \frac{1}{Q}$ ) of the selected reference capacitor. Fortunately, the dissipation factor in a Type 1 ceramic capacitor (C0G) is typically only affected by frequency, not operating voltage, so it can be calibrated out of the DUT loss measurements directly. Further, increasing the value of  $C_{REF}$  will decrease the magnitude of the energy dissipated in  $C_{REF}$  (by decreasing  $V_X$ ), although this benefit comes at the cost of reducing the magnitude of the  $V_X$  measurement.

Practically, the capacitance of  $C_{REF}$  should be stable across applied voltage and frequency, and we use C0G or U2J dielectric materials. The voltage rating must be greater than the peak voltage applied at  $V_Y$ . Experimentally, we also find that the self-resonant frequency (SRF) of  $C_{REF}$  should be at least 10× greater than the maximum measurement frequency, adding a practical limit to the capacitance of  $C_{REF}$ .

#### D. Alternative $C_{OSS}$ Loss Test Methods

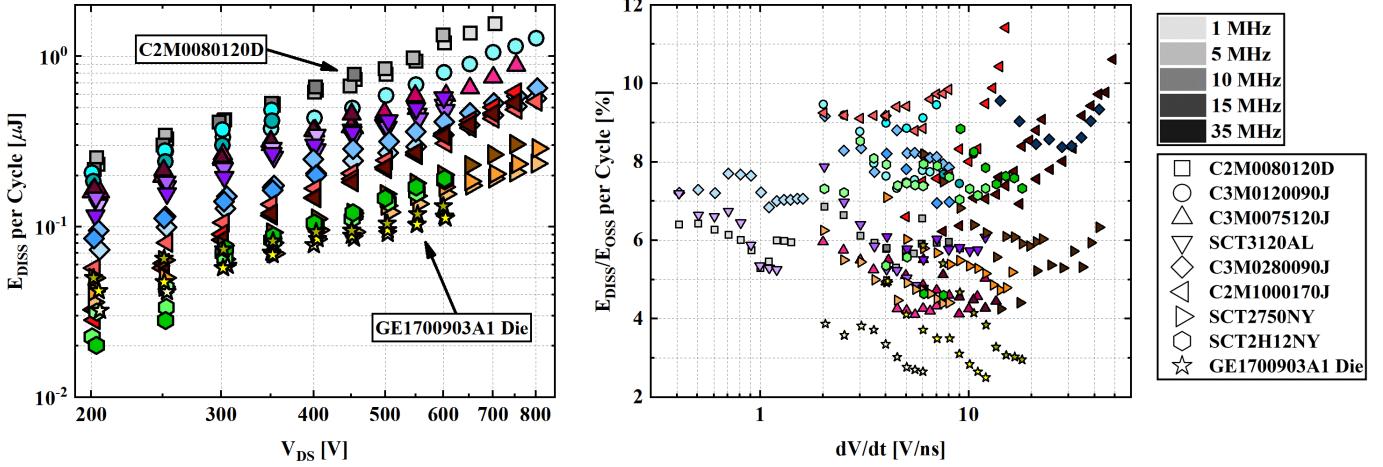
We prefer the Sawyer-Tower circuit for its simplicity and extensibility to high-frequencies and high-voltages; the voltage, frequency, and accuracy limitations are only limited by  $C_{REF}$ , the power amplifier bandwidth, the accuracy of the probes measuring  $V_X$  and  $V_Y$  and the ability to deskew the probes. Nonetheless, because the fundamental measurement is the large-signal characteristics of a non-linear capacitor, a variety of alternative measurement techniques exist.



**Fig. 5:** LTSpice simulation of the Sawyer-Tower test circuit shown in Fig. 4. The DUT is Panasonic GaN HEMT PGA26E19BA, 1 MHz operating frequency,  $V_{PP} = 440$  V, and  $C_{REF}$  of 100 pF. It is apparent that the body diode, for a device with zero  $Q_{RR}$ , only conducts for a single cycle.

Ideally, we would be able to infer  $C_{OSS}$  losses from manufacturer-provided datasheets and/or simulation models, and this class of measurements would not be necessary. Unfortunately, the small-signal  $C_{OSS}$  characteristics provided in the datasheet and used in the simulation models do not provide a known, extensible way of determining large-signal characteristics of the output capacitor. In particular,  $C_O$  magnitude and shape and total energy storage ( $E_O$ ) may all differ quite significantly between large-signal and small-signal measurements. Dissipation factor cannot be estimated in any known way from small-signal measurements. Unfortunately, in hard- or soft-switched power converters,  $C_O$  operates under large-signal conditions, and these measurements are necessary to understand the precise operation and losses of  $C_{OSS}$ .

Techniques for measuring the large-signal characteristics of capacitors are briefly reviewed here. In-situ methods, where the capacitor-under-test is used in an RCD snubber [30] or as an output capacitor [31], [32], combine power dissipation from reverse conduction of the body diode and the desired capacitor losses. These losses cannot be disentangled easily, and these techniques are better for standalone capacitors without an intrinsic body diode. The quasi-DC technique [33] is not usable at frequencies above tens of Hz. Pure thermal or calorimetric measurements [34], [35] are difficult to implement at MHz frequencies, as high thermal isolation and low parasitic inductance are difficult to achieve simultaneously, and are not accurate at low power dissipation magnitudes. The soft-switched double-pulse technique [18] precisely measures energy storage,  $E_{OSS}$ , at high-frequencies and high-voltages, but again combines conduction losses and  $C_{OSS}$  losses, which are difficult to extricate. Finally, the combination of a soft-switched half-bridge and Sawyer-Tower configuration [22] has the advantage of an in-situ-like test waveform but is a) limited in achievable frequency to a few MHz by the half-bridge and



**Fig. 6:**  $C_{OSS}$  losses for SiC devices from 200 to 800 V  $V_{DS}$  from 1-35 MHz. Shape corresponds to device and tint corresponds to test frequency. Legend position corresponds to vertical position in left figure.  $E_{DISS}$  per cycle is shown at left, and  $E_{DISS}$  as a percent of stored energy is shown at right.

b) requires retuning of the resonant inductor for new voltage, frequency, and device test setups.

The Sawyer-Tower circuit, uniquely, provides high-accuracy, high-voltage, and high-frequency measurements of  $C_{OSS}$  losses, the focus of this paper. The technique has three primary shortcomings. Firstly, as described above, the voltage swing across  $C_{OSS}$  starts very near 0 V<sub>DS</sub>, and a DC bias cannot be easily applied. In operating power converters, the large-signal voltage swing across  $C_{OSS}$  always starts after conduction, when the voltage across the device is very near 0 V, and so this lack of flexibility actually approximates the in-situ behavior of  $C_{OSS}$ .

The second weakness is that, because the device-under-test never conducts in steady-state, the Sawyer-Tower circuit will not be able to capture any second-order effects on  $C_{OSS}$  from the conduction period. While trapping may be important in GaN-on-Si HEMTs, we anticipate these effects are negligible in the other device technologies considered here. Lastly, the Sawyer-Tower circuit applies a waveform that is limited by the bandwidth of the power supply, resulting in near-sinusoidal waveforms at high-frequencies. While these waveforms are applicable to some soft-switched converters, greater flexibility in waveform shape would be preferred to better approximate a wider range of in-situ operating conditions.

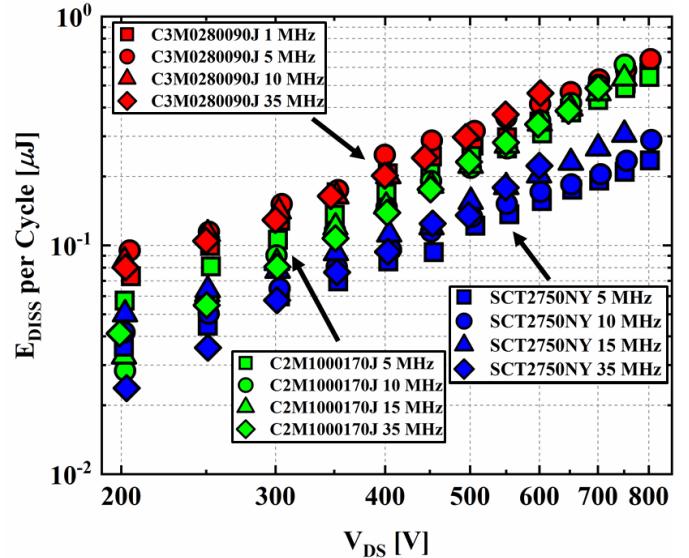
Even in GaN HEMTs, the  $C_{OSS}$  losses characterized using the Sawyer-Tower circuit appear to well-approximate losses in certain resonant converters [14], and any effects from the conduction period appear to be small. We therefore proceed with the Sawyer-Tower circuit to measure  $C_{OSS}$  losses in WBG and Si power devices at frequencies up to 35 MHz and voltages up to 800 V, the limitations of our power amplifier.

#### IV. SILICON CARBIDE (SiC) MOSFETs

##### A. Prior Art

Commercial SiC MOSFETs are focused on high-voltage applications, where channel resistance does not have a major effect on overall device performance [27]. For the voltage range considered here, SiC MOSFETs have similar  $R_{DS,ON}$  values to 650 V GaN HEMTs, but without information on

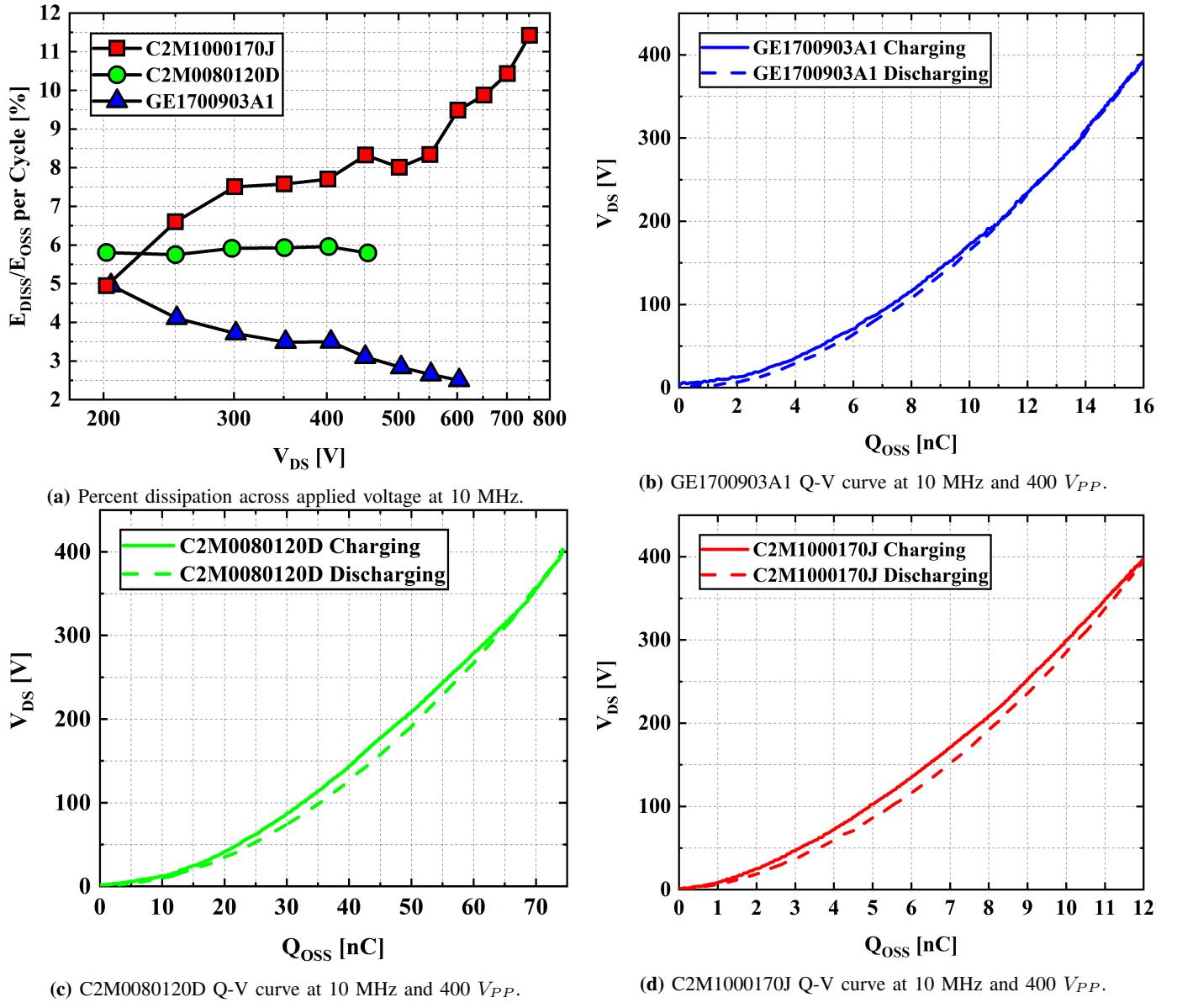
$C_{OSS}$  losses – of which we are aware of none in the literature, apart from a prediction of a 10% dissipation factor in [18] – we cannot compare device performance in HF/VHF soft-switched circuits. To fill this literature gap, we report  $C_{OSS}$  loss data for a broad range of SiC MOSFETs (see Table I) with applied sine waves from 200 to 800 V<sub>PP</sub> and frequencies from 1-15 MHz. All of the tested devices are commercially available except for GE1700903A1 (detailed in [36]), which was provided as a bare die and wire bonded to the test board of Fig. 4b.



**Fig. 7:**  $C_{OSS}$  losses for three devices from 1-35 MHz.

##### B. $C_{OSS}$ Loss Data

Figure 6 summarizes the  $C_{OSS}$  loss data for the tested devices. There are three key takeaways from this data. Firstly, in contrast to GaN HEMTs [14], the tested SiC MOSFETs do not exhibit increasing losses with frequency. In Fig. 6a, this phenomenon manifests with constant dissipated energy ( $E_{DISS}$ ) per cycle across the frequency range. To verify this conclusion, we increase the frequency to 35 MHz for the devices with both  $C_{OSS}$  values and packaging that will support



**Fig. 8:** Percent energy dissipated and Q-V curves for three selected devices at 10 MHz.

this higher frequency testing; Fig. 7 shows the result for the three devices tested at 35 MHz, with, again, no variation in  $E_{DISS}$  from 1 to 35 MHz. This indicates that the loss mechanism must be distinct from GaN-on-Si HEMTs, which have a clear increase of  $E_{DISS}$  with increasing  $dV/dt$ .

Secondly, we find that the prediction in [18] is a good, conservative estimate of energy dissipation for a wide range of operating frequencies – nearly all of the tested devices dissipate under 10% of the energy stored in  $C_{OSS}$ , as shown in Fig. 6b. Fittings for the  $C_{OSS}$  loss per cycle as a function of applied drain-source voltage (again, we find no frequency dependence of loss per cycle) are given in Table V.

Lastly, while the GaN HEMTs exhibited clearly increasing percent dissipation with increasing  $dV/dt$  [14], an inspection of Fig. 6b reveals three distinct characteristics among the SiC MOSFETs, and these are highlighted in Figure 8. Fig. 8a shows the  $E_{DISS}/E_{OSS}$  for three selected devices at 10 MHz: some devices (C2M1000170J) have increasing

percent dissipation with increasing voltage, some devices – analogous to the quality factor of a linear capacitor – dissipate a constant percentage of stored energy (C2M0080120D), and others (GE1700903A1) dissipate a decreasing percentage of stored energy as the voltage is increased. Q-V curves ( $E_{DISS}$  is the area between the charging and discharge curves) are plotted for 400 V and 10 MHz in Fig. 8b-d to illuminate these three characteristics. For the devices with decreasing percent dissipation (Fig. 8b), the majority of the losses are at low voltage (below  $\approx 200$  V for this device), so energy stored increases faster with voltage than energy dissipated. For those losses analogous to quality factor (Fig. 8c), energy dissipation is concentrated at the center of the charge-discharge curves, and, for the devices where  $E_{DISS}/E_{OSS}$  increases with voltage (Fig. 8d), significant energy dissipation occurs throughout the charge-discharge cycle. We suspect the curve shapes reflect trapping mechanisms that have distinct voltage characteristics between the tested devices.

**TABLE I:** SiC MOSFETs tested in this study.  $R_{DS,ON}$  and  $E_{OSS}$  values are obtained from the respective datasheets, except for  $E_{OSS}$  for the GE1700903A1 device, which is measured.

Manufacturer	Part Number	Voltage	Current	$R_{DS,ON}$	$E_{OSS}$ at $V_R$
Wolfspeed/Cree	C3M0280090J	900 V	11 A	280 mΩ	4.5 μJ at 600 V
Wolfspeed/Cree	C3M0120090J	900 V	22 A	120 mΩ	9 μJ at 600 V
Wolfspeed/Cree	C3M0075120J	1200 V	30 A	75 mΩ	33 μJ at 1000 V
Wolfspeed/Cree	C2M0080120D	1200 V	36 A	80 mΩ	45 μJ at 1000 V
Wolfspeed/Cree	C2M1000170J	1700 V	5.3 A	1000 mΩ	7 μJ at 1000 V
Rohm Semiconductor	SCT3120AL	650 V	21 A	120 mΩ	5 μJ at 400 V
Rohm Semiconductor	SCT2H12NY	1700 V	4 A	1150 mΩ	5.4 μJ at 800 V
Rohm Semiconductor	SCT2750NY	1700 V	6 A	750 mΩ	4 μJ at 600 V
General Electric	GE1700903A1	1700 V	8 A	360 mΩ	4.5 μJ at 600 V

## V. SILICON MOSFETS

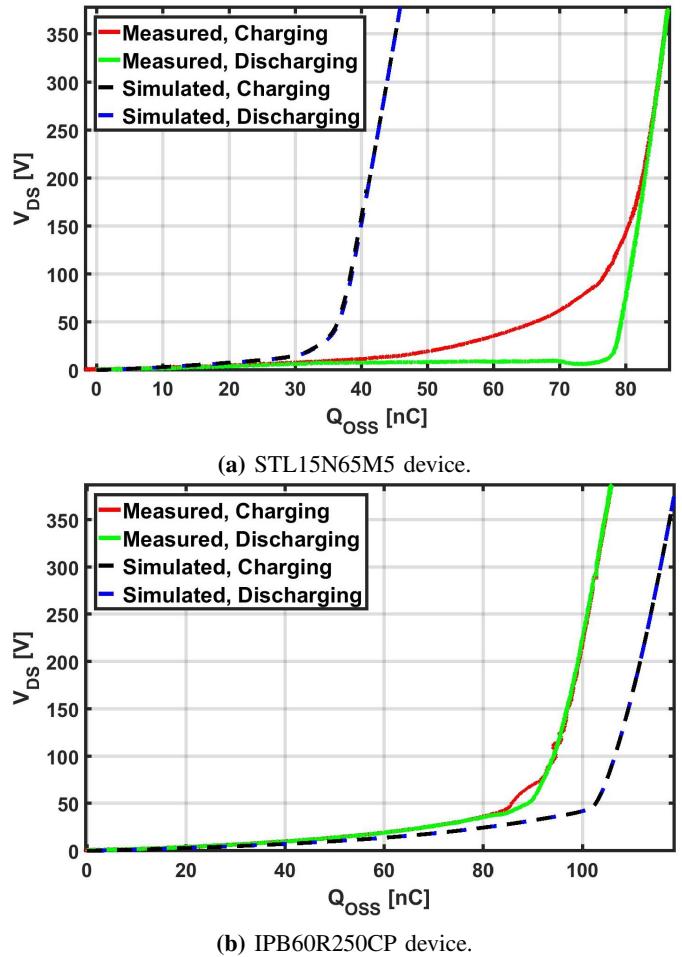
The Silicon (Si) MOSFETs considered here are segmented into two categories – planar Si MOSFETs, which have much higher  $sR_{DS,ON}$  than comparable WBG devices [27], [37], and superjunction (SJ) MOSFETs, where  $sR_{DS,ON}$  is significantly reduced [20], [38] but prior art has uncovered significant  $C_{OSS}$  losses [11], [12], [15], [21], [39]. We endeavor to answer two critical questions for using Si MOSFETs in soft-switched converters at HF and VHF — which, if any, SJ devices do not exhibit high  $C_{OSS}$  losses, and therefore can be used at these frequencies and voltage swings, and will planar Si devices with very low  $C_{OSS}$  losses outperform WBG or SJ devices in certain HF/VHF applications despite much higher  $sR_{DS,ON}$ ?

### A. Superjunction MOSFETs

1) *Prior Art:* Despite commercial use in soft-switched circuits, there is little literature on  $C_{OSS}$  losses in SJs. Since [11] was published in 2014, to our knowledge the only literature is work by the same authors [12], a recent seminar [22], our recent work [39], and mixed-mode simulations to a) attribute the losses to charge stranding [21] and b) attempt to capture transient operation due to hysteresis [15]. Since SJs are used widely in soft-switched converters, we assume that the knowledge of which devices are “lossy” is contained within companies and research laboratories that use SJs.

For example, Fig. 9 compares Sawyer-Tower test results (at 300 kHz) between two devices – one showing extreme  $C_{OSS}$  losses and one without significant losses in charging and discharging the output capacitor. Differentiation between the devices is not apparent from manufacturer-provided simulation models (as shown by the dotted lines in Fig. 9) or datasheets, and can only be identified through testing. Because these losses cannot be predicted, we test a large number of SJ devices across manufacturers, voltage ratings, and current ratings (see Table II) to “search” for the least lossy device. We report a subset of the low-frequency results as a starting point for future designers, while full results for every device are excluded for brevity.

2) *Low-Frequency  $C_{OSS}$  Losses:* For a first evaluation, the SJ devices do not need to be tested in the HF/VHF range in which we intend to use them, as the  $C_{OSS}$  losses are readily apparent at hundreds of kHz [11], [12], [39] and we assume losses will not decrease with frequency. We can first preclude



**Fig. 9:** Comparison in  $C_{OSS}$  losses for a charge and discharge cycle at 300 kHz and 380 V<sub>DS</sub>, with test results and manufacturer-provided simulation results shown on each graph. Note that both simulations predict zero losses for a charge-discharge cycle of  $C_{OSS}$ .

devices with large  $C_{OSS}$  losses at low frequencies, and we characterize the devices in Table II at 200 kHz, 300 kHz, and 500 kHz.

Fig. 10a shows  $C_{OSS}$  losses for three devices from three different manufacturers with similar nominal  $R_{DS,ON}$  (around 340 mΩ). Even with similar on-resistances, the variation in  $C_{OSS}$  losses is over an order of magnitude between manufacturers. In a 500 kHz soft-switched converter with a 400 V voltage swing, the STL15N65M5 device would

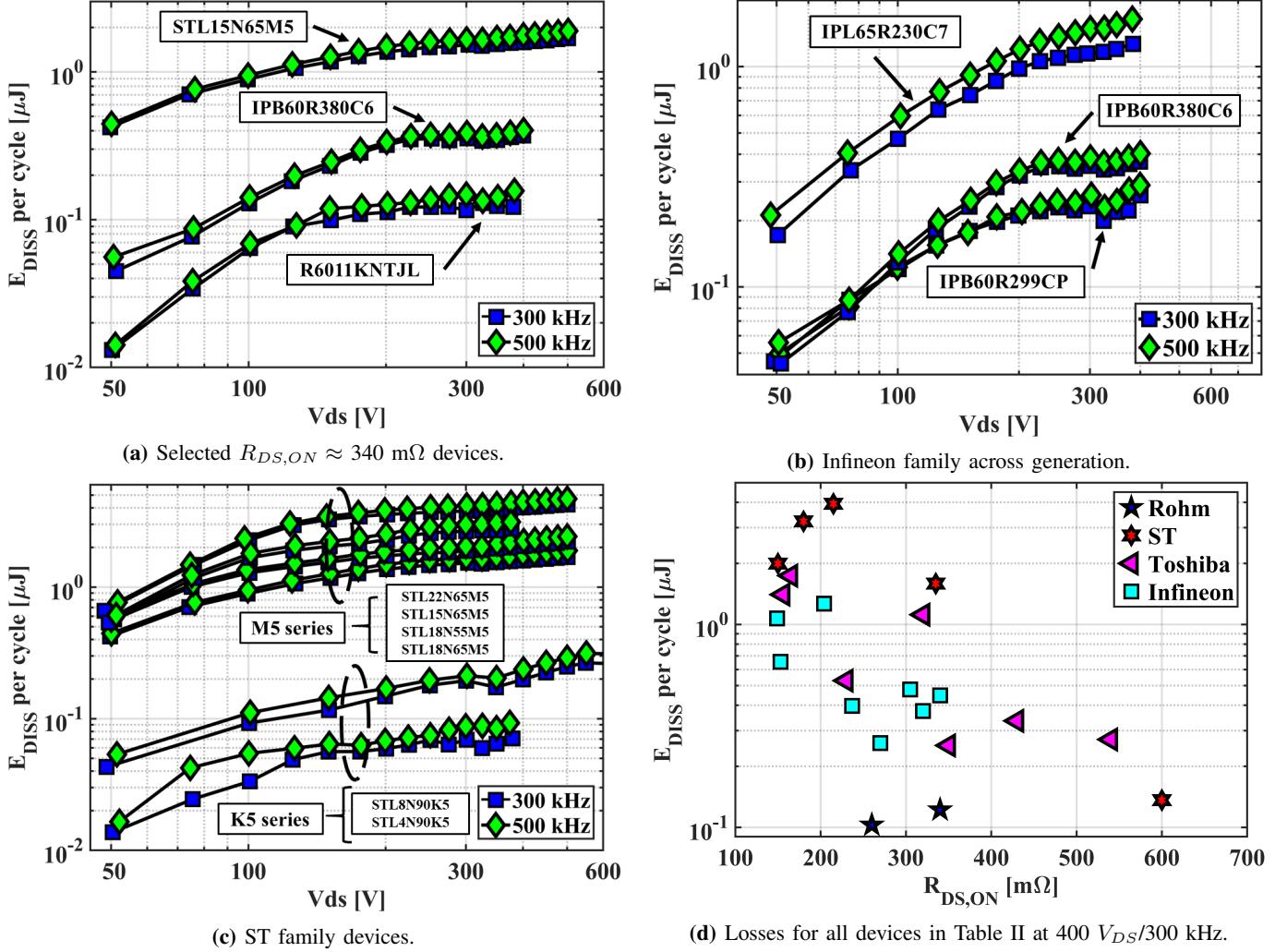


Fig. 10: Silicon superjunction  $C_{OSS}$  loss data.

dissipate 0.5 W more than the R6011KNTJL due to these  $C_{OSS}$  losses. Fig. 10b compares losses as the Infineon families proceed in generation, from CP (2005 release) to C6 (2006) to C7 (2013). The progression in generation corresponds to decreasing cell pitch [40], and we see a significant increase in  $C_{OSS}$  losses in the newer devices, as predicted by [21]. Fig. 10c demonstrates that, even within a single manufacturer, losses vary quite significantly between families. While Ref. [22] reported higher losses in higher voltage devices, the M5 family (550 V – 650 V) has much higher losses than the K5 family (800 V – 900 V). Finally, Fig. 10d summarizes the  $C_{OSS}$  loss data at 400 V and 300 kHz for the complete list of devices in Table II.

There are a few key takeaways from Figure 10. Firstly, we note an order-of-magnitude variation in  $C_{OSS}$  losses among SJ devices with similar  $R_{DS,ON}$ . There is a similar variation even within devices from a single manufacturer. There is a general trend of increasing  $C_{OSS}$  losses with decreasing  $R_{DS,ON}$  and therefore likely with decreasing cell pitch (as described, for example, in [40]), matching the simulated results in [21]. Most importantly for this work, the tested SJs are not viable

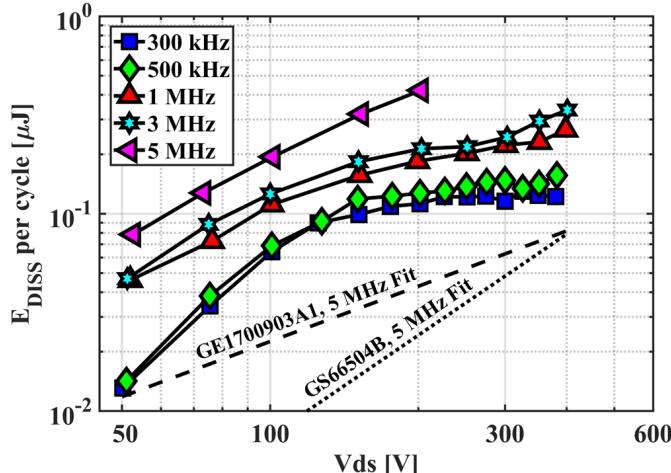
candidates for HF/VHF applications due to high  $C_{OSS}$  losses, which we assume will not decrease with frequency.

3) *High-Frequency  $C_{OSS}$  Losses:* Of the tested devices, the Rohm KNJTL series parts have the smallest  $C_{OSS}$  losses at low frequency, and we characterize this series at higher frequencies to directly compare SJ devices to the WBG devices characterized previously. Fig. 11 compares the  $C_{OSS}$  losses in the R6011KNJTL device ( $R_{DS,ON}$ : 340 mΩ) at frequencies up to 5 MHz with tested GaN (GS66504B,  $R_{DS,ON}$ : 100 mΩ) and SiC (GE1700903A1,  $R_{DS,ON}$ : 340 mΩ) devices.

As the frequency is increased into the HF regime, the losses in the SJ device increase with frequency, and the R6011KNJTL device dissipates over 2 W from  $C_{OSS}$  losses alone at 5 MHz and 200  $V_{PP}$ . This loss dependence on frequency only appears at MHz frequencies, and was not apparent in [11] or during our testing at hundreds of kHz. The comparison in Fig. 11 shows that even the best silicon SJ device in our study is not competitive with the tested WBG devices at HF/VHF, and we rule out the tested SJ devices from further consideration for HF/VHF designs.

**TABLE II:** Silicon superjunction MOSFETs tested in this study.  $R_{DS,ON}$  values are nominal datasheet values at 25 °C and current values are maximum datasheet values at 25 °C.

Manufacturer	Part Number	Max. V <sub>DS</sub>	Current	$R_{DS,ON}$
ROHM	R6011KNJTL	600 V	11 A	340 mΩ
ROHM	R6015KNJTL	600 V	15 A	260 mΩ
ST	STL15N65M5	650 V	10 A	335 mΩ
ST	STL18N65M5	650 V	18 A	215 mΩ
ST	STL18N55M5	550 V	16 A	150 mΩ
ST	STL22N65M5	650 V	15 A	180 mΩ
ST	STL8N90K5	900 V	8 A	600 mΩ
ST	STD4N90K5	900 V	3 A	1900 mΩ
Toshiba	TK13A65U	650 V	13 A	320 mΩ
Toshiba	TK20J60U	600 V	20 A	165 mΩ
Toshiba	TK7P60W5	600 V	7 A	540 mΩ
Toshiba	TK11P65W5	650 V	11 A	350 mΩ
Toshiba	TK20V60W5	600 V	20 A	156 mΩ
Toshiba	TK290P65Y	650 V	12 A	230 mΩ
Toshiba	TK560P60Y	600 V	7 A	430 mΩ
Infineon	IPD60R360P7	600 V	9 A	305 mΩ
Infineon	IPL60R185P7	600 V	19 A	149 mΩ
Infineon	IPL60R360P6S	600 V	11 A	320 mΩ
Infineon	IPL65R230C7	650 V	11 A	204 mΩ
Infineon	IPL60R185CFD7	600 V	14 A	153 mΩ
Infineon	IPD60R280CFD7	600 V	9 A	237 mΩ
Infineon	IPB60R520CP	600 V	6.8 A	470 mΩ
Infineon	IPB60R299CP	600 V	11 A	270 mΩ
Infineon	IPB60R250CP	600 V	12 A	220 mΩ
Infineon	IPB60R380C6	600 V	11 A	340 mΩ



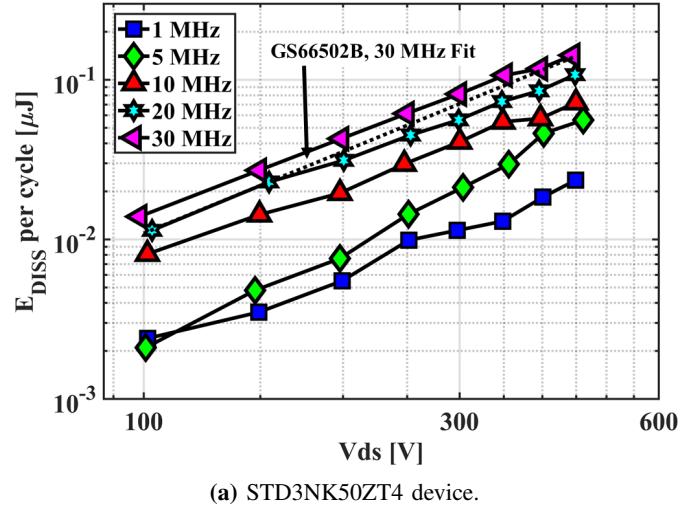
**Fig. 11:**  $C_{OSS}$  losses for the R6011KNJTL device, tested using the Sawyer-Tower circuit. Parasitic package inductance (and the associated distortion in the applied waveform) prevented increasing the applied voltage beyond 200 V at 5 MHz.

### B. Vertical Silicon MOSFETs

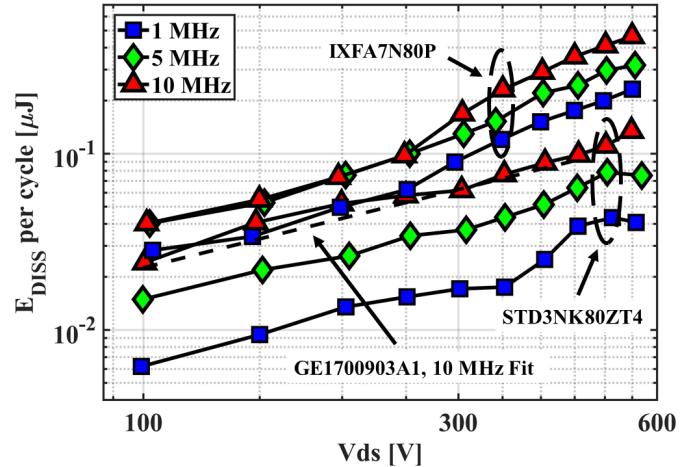
There are many vertical silicon power MOSFET device types and manufacturers, and we cannot begin to test a pluralty or even a representative sample of the devices. Although commercial WBG devices have not yet approached their respective materials limits [27], silicon MOSFETs still have significantly higher  $R_{DS,ON}$  than comparable WBG devices. Silicon MOSFETs, therefore, will only outperform WBG and SJ devices in the applications considered here if their  $C_{OSS}$  losses are nearly negligible. We measure  $C_{OSS}$  losses in a

**TABLE III:** Vertical silicon power MOSFETs tested in this study.  $R_{DS,ON}$  values are nominal datasheet values at 25 °C and current values are maximum continuous datasheet values at 25 °C.

Manufacturer	Part Number	Max. V <sub>DS</sub>	Current	$R_{DS,ON}$
ST	STD3NK50ZT4	500 V	2.3 A	2.80 Ω
Fairchild/ON	FDD7N60NZ	600 V	5.5 A	1.05 Ω
IXYS	IXFA7N80P	800 V	7.0 A	1.44 Ω
ST	STD3NK80ZT4	800 V	2.5 A	3.80 Ω



(a) STD3NK50ZT4 device.



(b) STD3NK80ZT4 and IXFA7N80P devices.

**Fig. 12:**  $C_{OSS}$  losses for the vertical silicon MOSFETs tested in this study, measured with the Sawyer-Tower circuit.

selection of Si MOSFETs (listed in Table III) previously used in high-frequency converters by the authors.

Fig. 12 summarizes the  $C_{OSS}$  losses in the tested vertical Si MOSFETs. STD3NK50ZT4 has the lowest measured  $C_{OSS}$  losses of the tested devices, but still exhibits a significant frequency dependence (Fig. 12a). FDD7N60NZ (which is not shown in Fig. 12 for clarity) has a similar frequency dependence, with approximately three times larger  $C_{OSS}$  losses across the voltage and frequency sweep. Fig. 12a includes a comparison to the best performing GaN device, GS66502B (200 mΩ  $R_{DS,ON}$ ). Because the  $C_{OSS}$  loss frequency dependence and magnitude between the devices is similar, the GS66502B device will be preferred at HF/VHF over the tested

500/600 V Si MOSFETs because of its much lower  $R_{DS,ON}$ .

Similarly, the two tested 800 V Si MOSFETs are compared with the lowest loss SiC device in Fig. 12b. We measure increasing  $C_{OSS}$  losses with frequency, and a large difference in losses between the two devices. The comparable WBG device again outperforms the Si MOSFETs, with similar  $C_{OSS}$  losses and much lower  $R_{DS,ON}$ .

Without knowing the underlying device constructions, which are proprietary, we are hamstrung in determining the root cause, and here we can only report the losses as a comparison with WBG and SJ devices. Further, identifying promising devices is difficult and time-consuming with the exclusion of  $C_{OSS}$  losses from datasheets. Based on these measurements – by no means an exhaustive survey of available Si MOSFETs – WBG devices will be preferred over both traditional and superjunction silicon MOSFETs in HF/VHF, soft-switched applications.

## VI. GAN HEMT FREQUENCY FITTING

To compare the  $C_{OSS}$  losses in the GaN HEMTs characterized in [14] to the  $C_{OSS}$  losses in the devices measured here, we propose a fitting with respect to frequency. In [14], we showed that  $C_{OSS}$  losses vary across a) device manufacturer, b) applied maximum voltage, and c)  $dV/dt$ . The losses also appear to scale linearly with  $C_{O,ER}$  within a particular family and manufacturer, and may vary with device temperature. These loss dependencies complicate a simple comparison in soft-switched converters and we make a few assumptions to perform a comparison.

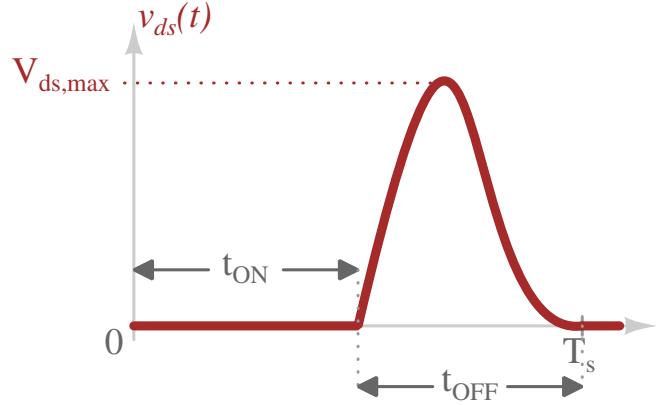
We assume that the applied drain-source voltage in our hypothetical converter is that shown in Fig. 13a, which is similar to the Class E inverter waveform [10] (topology shown in Fig. 1). Further, we assume the duty cycle is 50% and that the  $dV/dt$  is symmetric during the off-time of the device. We fit using the least lossy device (GS66504B) tested in [14] as (see Fig. 13b):

$$E_{DISS} = 2.25 \times 10^{-5} \cdot \left( \frac{V_{DS,MAX}}{650 \text{ V}} \right)^{1.6} \cdot f_{SW}^{0.6}, \quad (7)$$

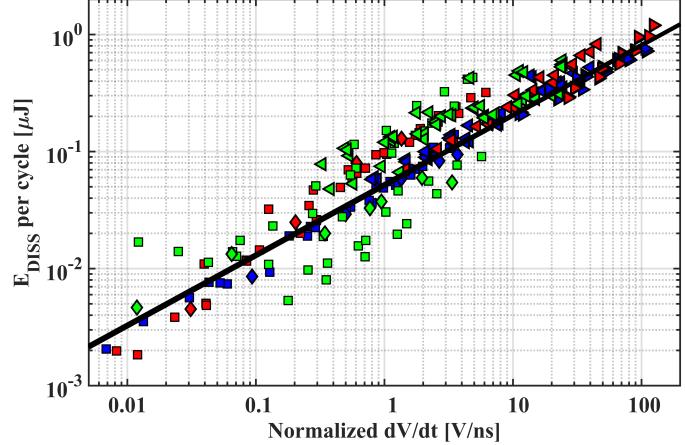
with  $E_{DISS}$  in  $\mu\text{J}$  and  $f_{SW}$  in Hz. This fitting can be scaled by the  $C_{O,ER}$  ratio to include other GaN devices in the same family. With this sample waveform and fitting, we now compare the GaN-on-Si HEMTs to the families of power devices tested here.

## VII. COMPARISON: DEVICES FOR SOFT-SWITCHED CONVERTERS

While to this point, we have focused on  $C_{OSS}$  losses, there are a number of other considerations that may dictate device selection in HF/VHF, soft-switched converters. We discuss gating considerations and then combine the gating,  $C_{OSS}$  los, and conduction loss terms to show how, for each device family, total semiconductor losses scale with frequency, voltage, and  $dV/dt$ . Practical challenges that affect device selection in commercial applications, such as packaging, heat extraction, and gate driver design, are generally application-specific and are excluded here. Table IV summarizes the discussion on gating and the combined power dissipation terms.



(a) Assumed drain-source waveform for fitting, with  $D = 0.5$  and symmetric rise and fall times.



(b) Measured GaN HEMT  $C_{OSS}$  losses from [14], with fitting overlaid to show frequency dependence. Green: TPH3202LS, Red: PGA26E19BA, Blue: GS66504B.

Fig. 13: Assumed waveform (a), similar to a Class E [10], for fitting, with the fitting line overlaid on the data from [14] (b).

### A. Gating

Gate characteristics can limit high-frequency operation in two primary ways, ignoring inductance – the time constant of the gate resistance ( $R_G$ ) and input capacitance ( $C_{ISS}$ ) may approach the device on-time, resulting in distorted gate waveforms and under-driven devices, or the power dissipated may result in efficiency degradation and/or overheating of the gate driver circuit or power device.

The gate input can be modeled as a series resistor  $R_G$  and a capacitance  $C_{ISS}$  (ignoring the variation of  $C_{ISS}$  with drain-source voltage) with time constant  $\tau_G = R_G \cdot C_{ISS}$ . This circuit low-passes the assumed square drive signal, resulting in a gate voltage with finite rise and fall times proportional to  $\tau_G$ . If the rise and fall times are significant, the device will not be fully enhanced for a large portion of the on-time, and the effective  $R_{DS,ON}$  will be much higher than the nominal value. For the exercise of comparing devices, we set an upper bound on the switching frequency as  $\tau_G$  less than 50% of the device on-time, or  $f_{SW,MAX} = \frac{1}{4 \cdot R_G \cdot C_{ISS}}$  for the 50% duty cycle from Fig. 13a. While the actual maximum switching frequency is dependent on the exact device characteristics and

**TABLE IV:** Summary of considerations for device selection at MHz frequencies for 500 V<sub>DS</sub> or greater devices. sR<sub>DS,ON</sub> values for MOSFETs are the unipolar material limits for vertical devices considering only drift region resistance, assuming constant mobility and optimal doping and ignoring edge effects. For SJ, d is column width in cm. SiC MOSFETs are assumed 4H-polytype. GaN HEMT sR<sub>DS,ON</sub> assumes a lateral device and uniform electric field, and only considers the 2DEG resistance with a sheet carrier density of 10<sup>13</sup> cm<sup>2</sup> and an electron mobility of 2000 V · cm<sup>2</sup>/s.

Device Type	sR <sub>DS,ON</sub> [Ω·cm <sup>2</sup> ]	C <sub>OSS</sub> Losses	Gating
<b>Vertical Si MOSFET</b>	Highest $> 5.93 \times 10^{-9} \cdot V_{BV}^{2.5}$ [25]	Highly variable Not preferred at HF/VHF	Low R <sub>G</sub> , High C <sub>ISS</sub> High sR <sub>DS,ON</sub> = large die
<b>SJ Si MOSFET</b>	Moderate $> 0.198 \cdot d^{\frac{5}{4}} \cdot V_{BV}$ [38]	Highly variable Not preferred at HF/VHF	Low R <sub>G</sub> , Moderate C <sub>ISS</sub>
<b>SiC MOSFET</b>	Low $> 1.19 \times 10^{-11} \cdot V_{BV}^{2.5}$ [41]	E <sub>DISS</sub> ≈ 3 – 10% of E <sub>OSS</sub> P <sub>COSS</sub> ∝ f <sub>SW</sub>	High R <sub>G</sub> and C <sub>ISS</sub> Non-self-aligned gates
<b>GaN-on-Si HEMT</b>	Lowest $> 3.577 \times 10^{-12} \cdot V_{BV}^{\frac{7}{3}}$ [42]	E <sub>DISS</sub> ≈ k · f <sub>SW</sub> <sup>0.6</sup> · V <sub>DS</sub> <sup>1.6</sup> P <sub>COSS</sub> ∝ f <sub>SW</sub> <sup>1.6</sup>	Low R <sub>G</sub> and C <sub>ISS</sub> Small die areas, metal gates

application,  $\tau_G = 0.5 \cdot D_{ON}$  results in a triangular gate signal, a generous upper bound on maximum operating frequency. With hard gating, the gate drive power dissipation is  $P_{GATE} = f_{SW} \cdot C_{ISS} \cdot V_G^2$ . Although a portion of this power may be dissipated external to the power device, we include this in total device losses as  $P_{GATE}$  is a consequence of a given device selection. For this exercise, we do not set an upper limit on the power that can be dissipated from the gate drive chip, as high-speed drivers are available in a variety of packages.

For the comparisons below, then, we only limit frequency based on the gate time constant. Gate inductance and package inductance are ignored as frequency limitations. Gating power is not considered as a frequency limitation, but is included in the total power dissipation of Eqn. 8 and assumed to be entirely dissipated in the switching device.

### B. Total Power Dissipation

1) *Proposed Loss Calculation:* We propose the following formula to calculate power dissipation in the active device of a soft-switched converter, which includes C<sub>OSS</sub> losses:

$$P_{DISS,DEVICE} = \frac{1}{N} I_{RMS}^2 R_{DS,ON} + \quad (8)$$

$$f_{SW} E_{DISS} N + f_{SW} C_{ISS} V_G^2 N, \quad (9)$$

where f<sub>SW</sub> is the switching frequency, E<sub>DISS</sub> is the energy dissipated per charge-discharge cycle of the device output capacitor, and N is the number of paralleled devices in operation. This formula makes device selection for a given soft-switched converter in application simple — if each of the parameters is known. E<sub>DISS</sub> cannot be determined from the datasheet, but is reported for a number of devices in this paper. The value for R<sub>DS,ON</sub> should be the effective on-resistance during the on-time of the device, which can be approximated from the datasheet but may need to be altered to include finite gating times and dynamic effects.

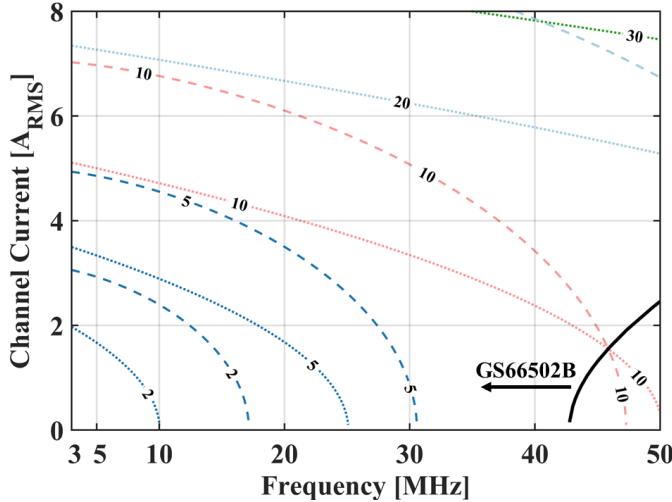
2) *Assumptions:* In these comparisons, we exclude the variation in circulating currents that may accompany changing devices (because of different C<sub>OSS</sub> magnitudes), assuming fixed RMS current through the channel when comparing devices. The exact change in circulating currents is highly circuit-dependent and only significant if C<sub>OSS</sub> is the dominant shunt capacitance.

Dynamic R<sub>DS,ON</sub> is ignored in the calculations for GaN HEMTs, as measurements on recent GaN HEMTs show increases of 10-20% over static R<sub>DS,ON</sub> with lower contributions in soft-switched circuits [43], [44]. While including these effects in power dissipation comparisons would improve accuracy, the combination of device-to-device variation [45] and significant disagreement between reported measurements (e.g. 8% [44] versus 400% [46] increase over static R<sub>DS,ON</sub> for similar conditions) lead us to exclude it from the calculations. Dynamic effects are also ignored in the SiC MOSFET calculations, although low transconductance and high gate resistance may add losses during turn-on/-off and require a gate drive capable of sourcing and sinking large currents. Lastly, the effect of junction temperature on R<sub>DS,ON</sub> and C<sub>OSS</sub> losses is excluded to reduce the design space and simplify the comparison.

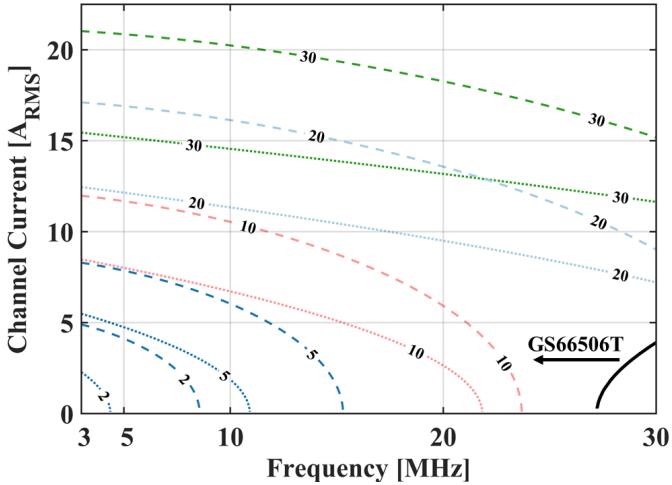
Broadly, including temperature or dynamic effects only requires an update of the R<sub>DS,ON</sub> term in Eqn. 8 to reflect the anticipated effective on-resistance temperature in application. These assumptions to ignore dynamic R<sub>DS,ON</sub> and temperature effects, in both cases, will improve the predicted performance of GaN HEMTs relative to SiC MOSFETs. Precise characterization of dynamic R<sub>DS,ON</sub> at nanosecond on-times lies outside the scope of this work but is imperative to more precisely estimating conduction losses. Even with the exclusion of these effects, we find that C<sub>OSS</sub> losses alone indicate potential for SiC MOSFETs in HF/VHF applications, as discussed below.

3) *Selected Device Comparisons:* To illustrate the utility of this loss equation and the measurements reported here, we compare devices across frequencies and device currents in Fig. 14. Table V shows the compared WBG devices (the tested Si MOSFETs were not competitive with the tested GaN and SiC devices) and the parameters used to calculate dissipated power in each device.

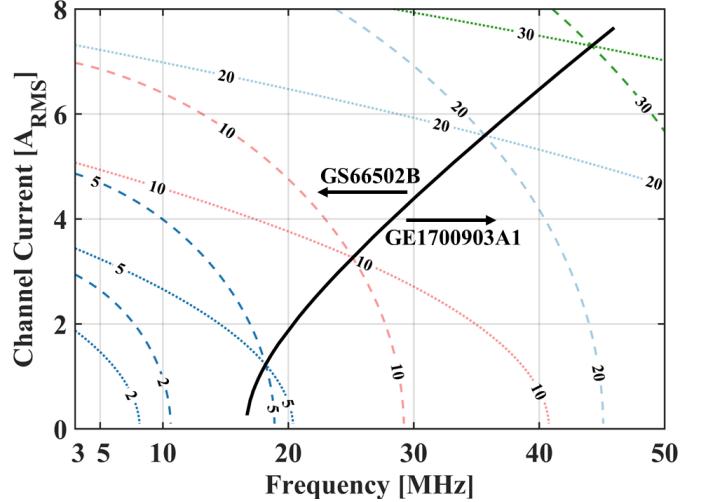
Fig. 14 directly compares the power dissipated in two selected devices, with the assumed waveform of Fig. 13a and the stated maximum voltage. The contour lines show constant device power dissipation in each device and the solid black lines indicate the line of equal power dissipation in the two compared devices. At a given line of constant power, the line that is higher or more to the left is the preferred device, and this preferred device for each part of the graph is indicated by



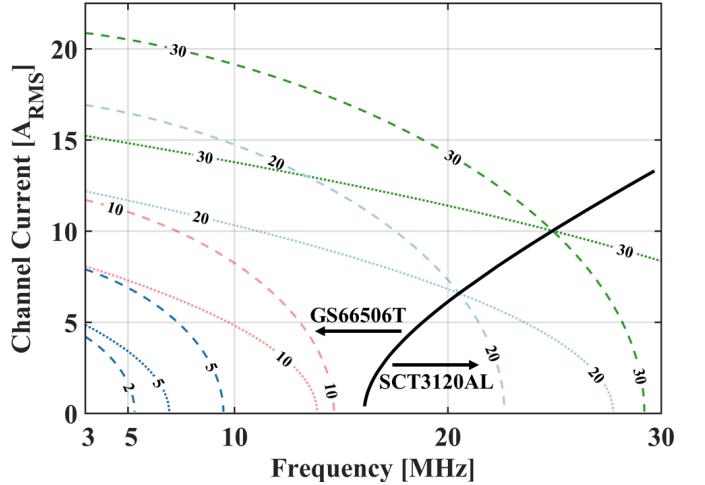
(a)  $400 \text{ V}_{DS}$ , GS66502B (dashed) and GE1700903A1 (dotted).



(c)  $400 \text{ V}_{DS}$ , GS66506T (dashed) and SCT3120AL (dotted).



(b)  $650 \text{ V}_{DS}$ , GS66502B (dashed) and GE1700903A1 (dotted).



(d)  $650 \text{ V}_{DS}$ , GS66506T (dashed) and SCT3120AL (dotted).

**Fig. 14:** Power dissipation of selected devices across frequency and current. Contour lines are constant power dissipation, with the labels showing  $P_{DISS}$ , calculated by (8), in watts. Solid line tracks equal  $P_{DISS}$ , with arrows showing the preferred device on each side. Assumed waveform is shown in Fig. 13a.

the arrows adjacent to the black line.

Subfigures a and b compare the  $\approx 8 \text{ A}$  GaN and SiC devices and subfigures c and d compare the  $\approx 22 \text{ A}$  GaN and SiC devices, with drain-source voltages of  $400 \text{ V}$  and  $650 \text{ V}$  respectively. For both comparisons, we find that GaN outperforms SiC at lower frequencies, higher currents, and lower operating voltages, while SiC devices are less lossy than GaN at higher voltages and as the frequency is increased towards the VHF regime. In particular, SCT3120AL and GS66506T have similar voltage and current ratings, and we see that the SiC device is preferred at higher frequencies – at least until the large gate time constant prevents higher frequency operation (SCT3120AL cannot operate above  $30 \text{ MHz}$  under the gating assumptions outlined above).

Subsequently, we extend the comparison from two devices to all of the devices tested (or with extrapolated  $C_{OSS}$  losses) in this study. In Fig. 15, we sweep device current from 1 to  $25 \text{ A}$  and operating frequency from 3 to  $50 \text{ MHz}$  (with the assumed waveform of Fig. 13a at  $600 \text{ V}$ ), and plot the tested device with the lowest power dissipation at each

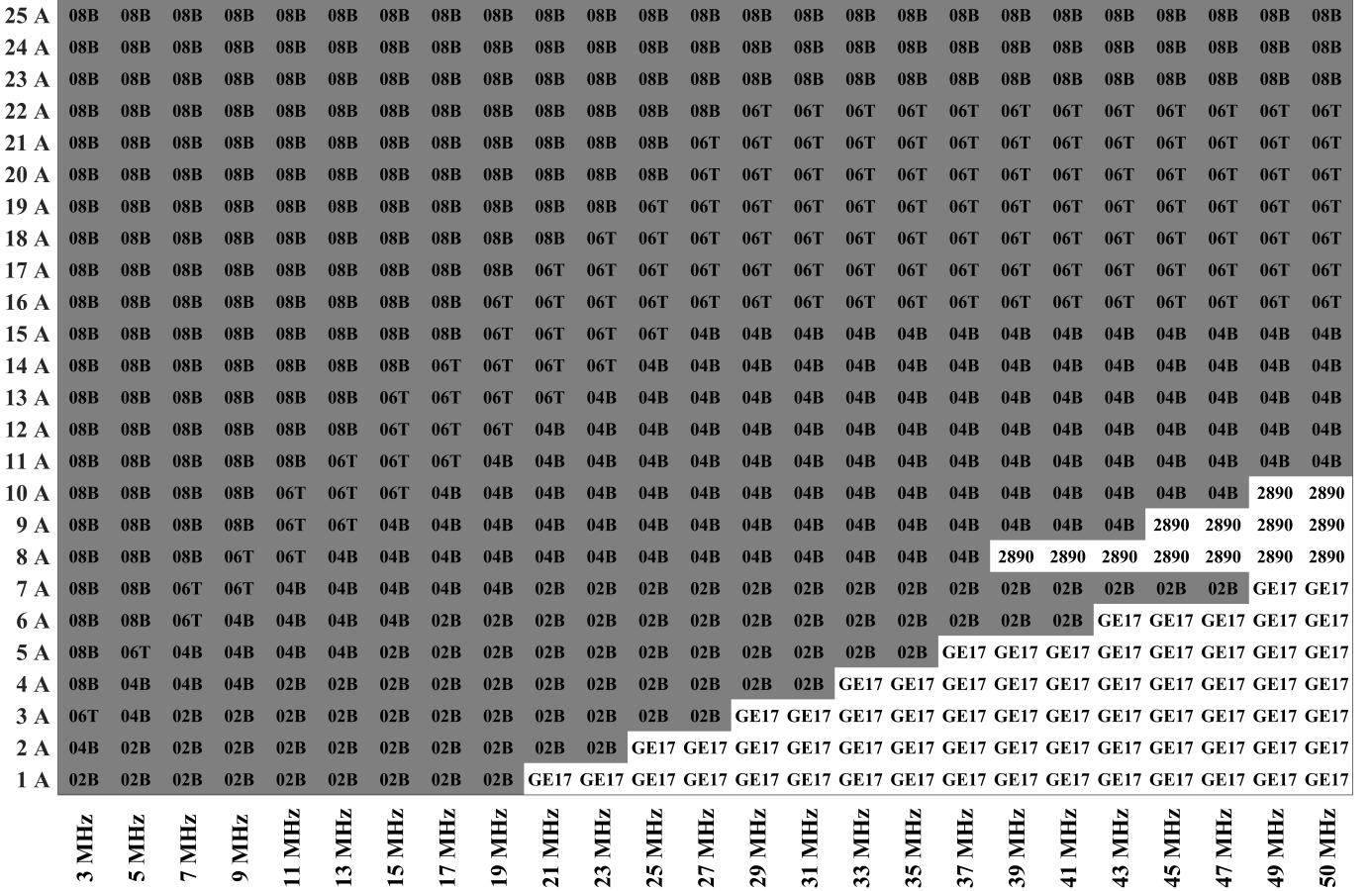
intersection. Table V shows the parameters used for each calculation, and maximum frequency is again only limited by  $f_{SW,MAX} = \frac{1}{4 \cdot R_G \cdot C_{ISS}}$ . Maximum current is limited to the maximum continuous current value at  $25^\circ \text{C}$  given in the datasheet. Package inductances and differences in heat extraction between devices are not considered.

In the HF regime ( $3\text{-}30 \text{ MHz}$ ), the tested GaN devices are preferred, although at some low currents towards the upper end of this range,  $C_{OSS}$  losses dominate and tested SiC devices outperform the tested GaN HEMTs despite higher  $R_{DS,ON}$ . In the VHF frequencies considered here, the smallest tested SiC MOSFETs are preferred at low currents, while at currents above  $\approx 10 \text{ A}$ , the smallest tested GaN devices are the best candidates of the considered devices.

While, as expected, GaN HEMTs broadly dominate the HF/VHF regimes, this comparison reveals some opportunities for small SiC devices at high frequencies and low currents due to the measured frequency-independence of their  $C_{OSS}$  losses. To reach this operating regime, SiC MOSFET manufacturers should package dies with these higher frequency considera-

**TABLE V:** Parameters used for calculations in contour plots (Fig. 14) and comparisons (Fig. 15). Parameters are nominal values from the datasheet, and drain current is at 25 °C. Gate drive voltage is the drive voltage used for nominal  $R_{DS,ON}$  in datasheet. Fitting values for  $E_{DISS}$  are from the data presented in previous sections. Code is the abbreviation shown in Fig. 15.

Device, Code	$V_{DS,MAX}$ (V)	$I_{D,CONT}$ (A)	$R_{DS,ON}$ (mΩ)	$R_G$ (Ω)	$C_{ISS}$ (pF)	$V_{GATE}$ (V)	$E_{DISS}$ (μJ)
GS66502B (GaN), “02B”	650	7.5	200	2.3	65	6	Eqn. 7, 50% $C_{O,ER}$ scale
GS66504B (GaN), “04B”	650	15	100	1.36	130	6	Eqn. 7
GS66506T (GaN), “06T”	650	22.5	67	1.1	195	6	Eqn. 7, 150% $C_{O,ER}$ scale
GS66508B (GaN), “08B”	650	30	50	1.1	260	6	Eqn. 7, 200% $C_{O,ER}$ scale
SCT3120AL (SiC), “3120”	650	21	120	18	460	18	$1.56 \times 10^{-4} \cdot V^{1.27}$
C3M0280090J (SiC), “2890”	900	11	280	26	150	15	$2.63 \times 10^{-5} \cdot V^{1.5}$
C3M0120090J (SiC), “1290”	900	22	120	16	350	15	$1.59 \times 10^{-4} \cdot V^{1.34}$
C3M0075120J (SiC), “7512”	1200	30	75	10.5	1350	15	$1.33 \times 10^{-4} \cdot V^{1.32}$
GE1700903A1 Die (SiC), “GE17”	1700	8	360	3.65	296	20	$3.11 \times 10^{-4} \cdot V^{0.93}$



**Fig. 15:** Device (among those in Table V) with the least power dissipation based on Eqn. 8, with waveform shown in Fig. 13a at 600  $V_{DS}$ . X-axis is operating frequency, and y-axis is RMS current through the channel of the device. Color coding shows the device material (white: SiC, gray: GaN). Package inductance limitations on frequency are not included – operating frequency for a given device is only limited by the gate time constant. Current is limited to the maximum continuous current at 25 °C given in the datasheet.

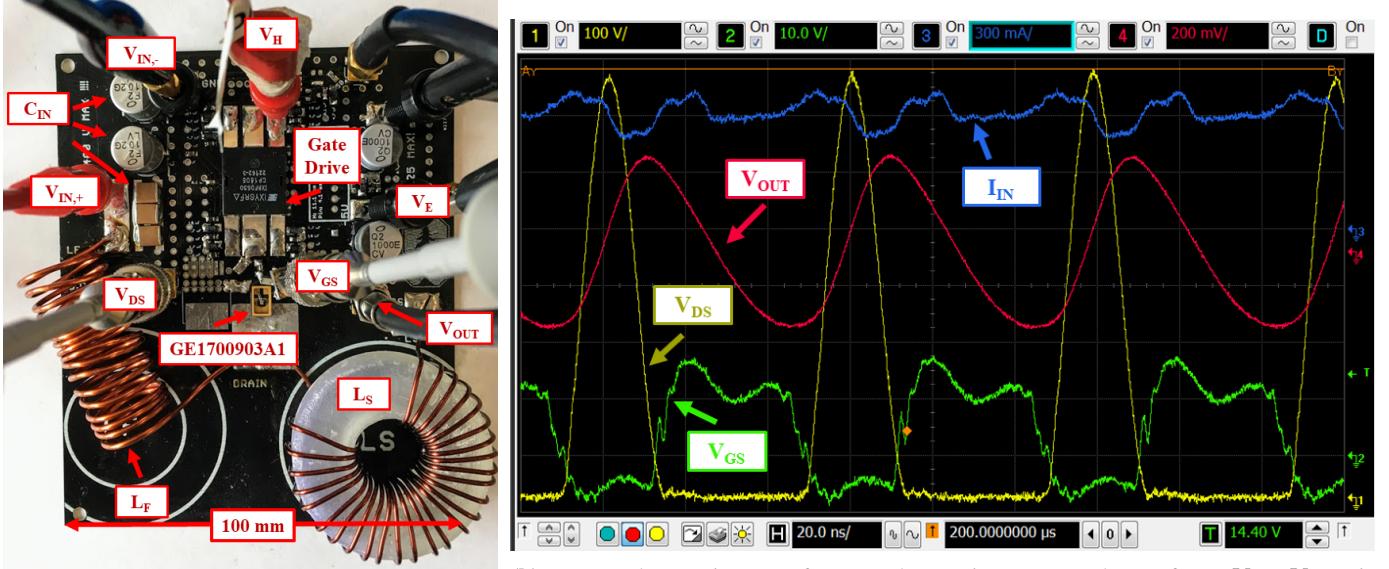
tions in mind for at least a subset of their commercial devices, aiming to lower gate resistances and decrease parasitic package inductances. Further, GaN devices with smaller die areas than are currently available would be preferred in the VHF range, as the lower  $C_{OSS}$  losses would compensate for the necessarily higher conduction losses.

### VIII. HIGH-FREQUENCY SiC INVERTER DEMONSTRATION

In [14], we showed that the inclusion of  $C_{OSS}$  losses in high-frequency converters with GaN-on-Si HEMTs were crucial to predicting converter efficiency and power device

losses. Here, we build a high-frequency inverter with a SiC MOSFET to validate that  $C_{OSS}$  losses are also fundamental to predicting operation of SiC-based converters, and to demonstrate the potential for SiC devices at high-frequencies – if manufacturers improve packaging and reduce  $R_G$ .

To demonstrate the importance of including these losses, and the validity of the fittings in Table V, we build a Class E inverter (see Fig. 1a) utilizing the smallest SiC MOSFET in our study, GE1700903A1, with a 50% duty cycle and a peak drain-source voltage of 650  $V_{DS}$  to replicate the assumed waveform in Fig. 13a. The design is matched to an RF load



(a) Constructed 17 MHz, 100 W Class E converter, with custom-packaged SiC MOSFET.

**Fig. 16:** Constructed Class E inverter (a) and measured waveforms (b). SiC MOSFET GE1700903A1 is custom-packaged in a low-inductance package and operated at a switching frequency of 17 MHz.

of  $50 \Omega$ , and with an energy-related output capacitance of  $\approx 33 \text{ pF}$  from 0 to  $650 \text{ V}_{DS}$ , the maximum frequency for zero-voltage, zero- $dV/dt$  Class E operation is 17.7 MHz [47]. We select an operating frequency near this maximum of 17 MHz.

To operate at this frequency, the SiC MOSFET package must not add significant inductance, and we use the open-tool SMD 0.2 package from Kyocera (with wire bonds to the gate and source). Figure 16a shows the constructed converter and Table VI details each component. The SiC MOSFET is driven using the IXYS IXRFD630 gate driver, although a custom gate driver that could drive stably at higher gate voltages at high-frequency would improve overall converter efficiency.

The inverter is operated in burst mode (20% duty cycle at 100 Hz burst frequency) from  $110 \text{ V}_{IN}$  to  $165 \text{ V}_{IN}$ , with 102 W pulsed input power at  $165 \text{ V}_{IN}$ . Figure 16b shows the measured waveform at this maximum tested power, with ZVS and zero- $dV/dt$  operation achieved. Although the measured waveforms match simulation nearly identically (Figure 17), the measured efficiency is significantly lower than that predicted by simulation (Figure 18). When we include the measured  $C_{OSS}$  losses, calculated as (from Table V)  $P_{COSS} = f_{SW} \times 3.11 \times 10^{-4} \times V_{DS,MAX}^{0.93}$ , an additional 1.6 W (at  $110 \text{ V}_{IN}$ ,  $471 \text{ V}_{DS,MAX}$ ) to 2.5 W (at  $165 \text{ V}_{IN}$ ,  $761 \text{ V}_{DS,MAX}$ ) are added to the simulated losses, and the measured efficiency much more closely matches the expected efficiency.

This demonstration – while not optimized for efficiency – shows that SiC MOSFETs are capable of efficient, predictable operation at switching frequencies in the tens of MHz if *a*) packaged in low-inductance packaging and *b*) the device has reasonable  $R_G$  and  $C_{ISS}$  values. Although gate drives for SiC MOSFETs will generally be larger footprint and more complex than a similar circuit for GaN HEMTs, the additional gate drive complexity may be worth the frequency-independent  $C_{OSS}$  losses in some high-frequency applications.

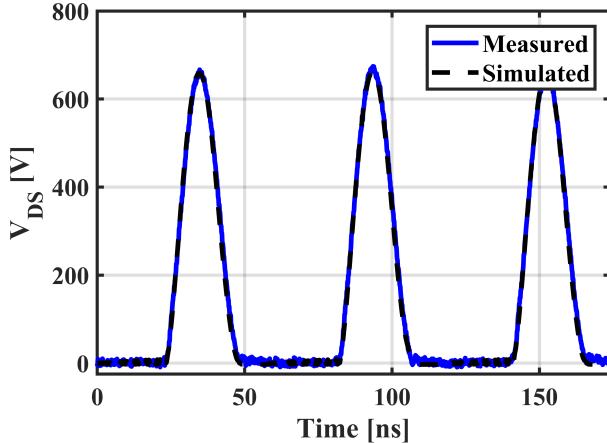
**TABLE VI:** Circuit components for the Class E inverter (see Fig. 1a and Fig. 16a).

Component	Design Value	Implementation
$C_{IN}$	$16.6 \mu\text{F}$	$2 \times 10 \mu\text{F}$ Nichicon ULV2G100MNL1GS + $3 \times 2.2 \mu\text{F}$ TDK C5750X6S2W225K250KA
$L_F$	$2 \mu\text{H}$	Solenoid Air-Core, $Q = 125$ at 17 MHz
$L_S$	$3.1 \mu\text{H}$	Toroidal Air-Core, $Q = 150$ at 17 MHz
$C_S$	$49 \text{ pF}$	$4 \times 12 \text{ pF}$ Murata GRM42A5C3F120JW01L
$C_P$	$C_{OSS}$ only	N/A
$R_{LOAD}$	$50 \Omega$	Pasternack PE7411-50 + Oscilloscope $50 \Omega$ input
Gate Driver	N/A	IXYS IXRFD630 +12 V/-5 V, $R_G = 3.3 \Omega$

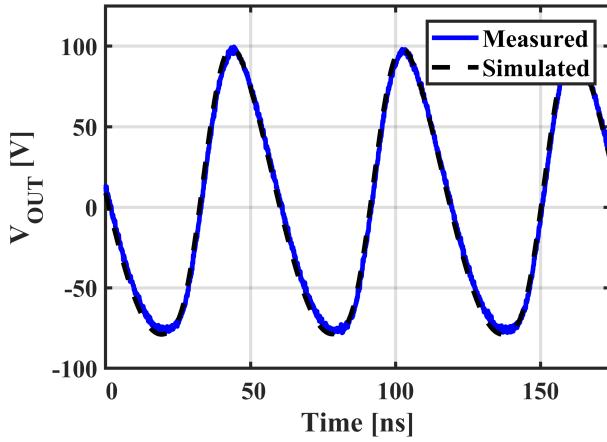
## IX. CONCLUSION

Building on prior work on GaN HEMTs, which demonstrated the importance of  $C_{OSS}$  losses in MHz-frequency, soft-switched power converters, we report  $C_{OSS}$  losses in SiC MOSFETs, Si superjunctions, and Si vertical MOSFETs at high- and very-high-frequencies. These findings have implications for market segmentation for manufacturers, with the caveat that they are only valid for current devices; future progress, especially on mitigating  $C_{OSS}$  losses and defining ns-scale dynamic  $R_{DS,ON}$  in GaN HEMTs, will require a re-assessment of the optimal device at each power and switching frequency operating point.

Generally, the device community has predicted that GaN will dominate the high-frequency (100 kHz to 100 MHz) market with applications including photovoltaic inverters, computer power supplies, and data center servers, while SiC will win the high-power market segment that is currently dominated by IGBTs (for railways, wind turbines, and elec-



(a) Drain-source voltage,  $V_{DS}$ . Zero-voltage-switching is apparent in measured and simulated waveforms.



(b) Output voltage,  $V_{OUT}$ . Measurement is made through a 50 dB attenuator matched to  $50 \Omega$ .

Fig. 17: Comparison of simulated and measured waveforms at  $150 V_{IN}$  for the constructed Class E inverter.

tric vehicles). Current devices reflect this anticipation – SiC MOSFETs are generally high-current dies in large packages with excellent heat extraction (for high power) and high package inductance (for low frequency), while GaN HEMT packaging is very low inductance for the target high-frequency applications.

Our findings indicate that there may be an opportunity for both segments to explore new markets. For SiC, where  $C_{OSS}$  losses are  $dV/dt$ -independent at the frequencies considered here, high-frequency markets (with smaller dies in low inductance packages, such as the demonstrated SiC MOSFET in a 17 MHz inverter) could be attractive if gate resistances can be lowered. For GaN, where commercial devices already have exceptionally low  $sR_{DS,ON}$ , much smaller devices, with moderate  $R_{DS,ON}$  but smaller  $C_{OSS}$  losses, would be attractive for expanding the target market. More importantly, GaN-on-Si manufacturers must diagnose and remedy the root cause of these  $C_{OSS}$  losses to make MHz-frequency operation attractive for a wide variety of applications. Overall, wide-bandgap devices are preferred at high- and very-high-frequencies, and

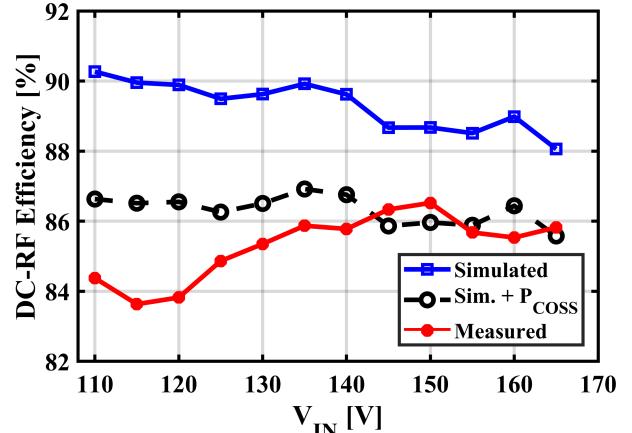


Fig. 18: Measured, predicted, and simulated DC-RF efficiency for the Class E inverter. Max. measured input power is 102 W at  $165 V_{IN}$  (shown in Fig. 16b). Efficiency does not include power supplied for gate drive circuitry.

continued improvements in these new semiconductors are critical to achieving efficient power conversion in this frequency regime.

#### ACKNOWLEDGMENT

The authors would like to thank General Electric for supplying bare dies for testing.

G. Zulauf would like to thank L. Raymond and K. Surakitbovorn for their insights.

Z. Tong would like to thank the Stanford Nano Shared Facilities (SNSF) and Clifford F. Knollenberg.

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