



## Stanford University Power Electronics Research Laboratory (SUPER Lab)

### Selecting the Right Power Semiconductors for Multi-MHz Power Converters

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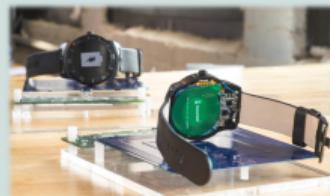
September 1, 2020

# Introduction

# Multi-MHz Power Converters: Market and Applications

## Wireless Power

- ▶ 6.78 MHz, 13.56 MHz DC-DC systems
- ▶ At higher frequency, coils are smaller and cheaper, safety and regulation are improved [Airfuel].



[Source: Nucurrent]

## Plasma Generation

- ▶ 13.56 MHz, 40.68 MHz DC-RF Inverters.
- ▶ High Power and Efficient: (100's of W to 10's of kW).
- ▶ Semiconductor etchers, spacecraft propulsion.



[Source: Liang et al., JESTPE 2017]

## Magnetic Resonance Imaging

- ▶ RF generators for high-frequency magnetic fields.



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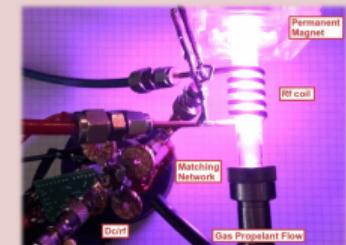
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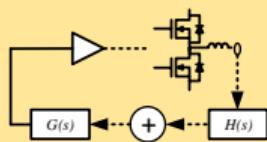
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## *Control*



Periods become shorter and delays in feedback become more challenging.

## *EMI*



Higher frequency current creates noise that propagates farther.

## *Magnetics*



Core loss and winding loss increase with frequency.

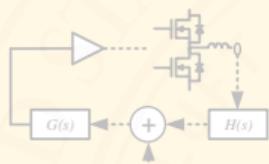
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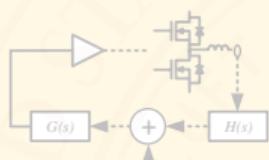
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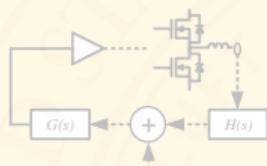
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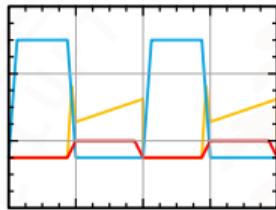
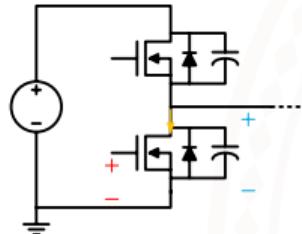
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# Soft-switching Enables High-Frequency Power Electronics

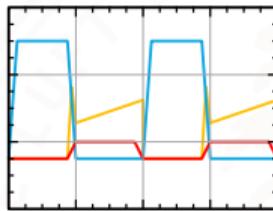
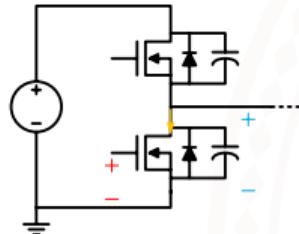
## Hard-Switching



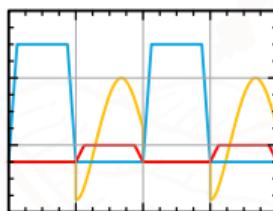
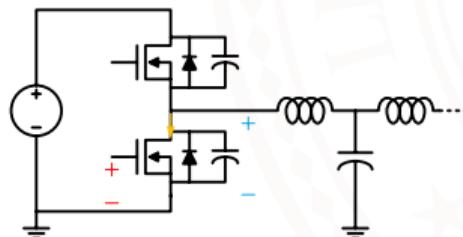
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## Hard-Switching



## Soft-Switching



- ▶ Switching loss  $\propto f_{sw}$ .
- ▶ Efficiency  $\downarrow$  as  $f_{sw} \uparrow$ .
- ▶ Adding additional resonant elements enables soft-switching.

# Frequency vs. Conduction Loss Tradeoff

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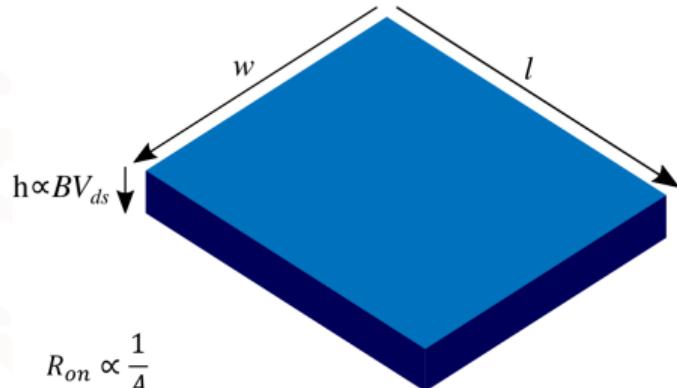
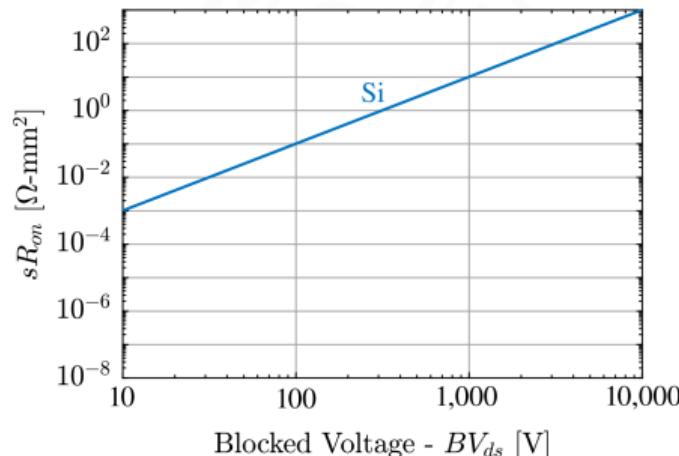
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- ▶ conduction losses  $\uparrow$ , and efficiency  $\downarrow$ .

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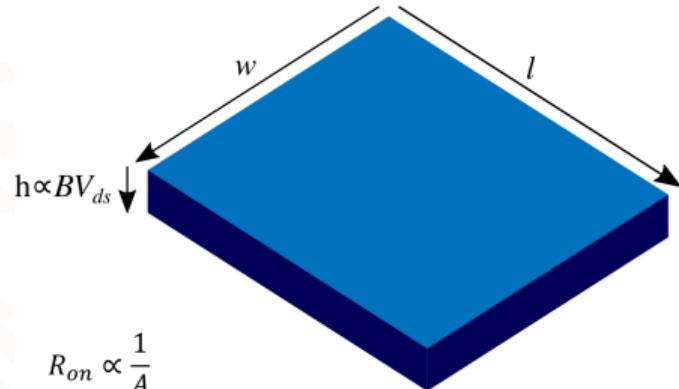
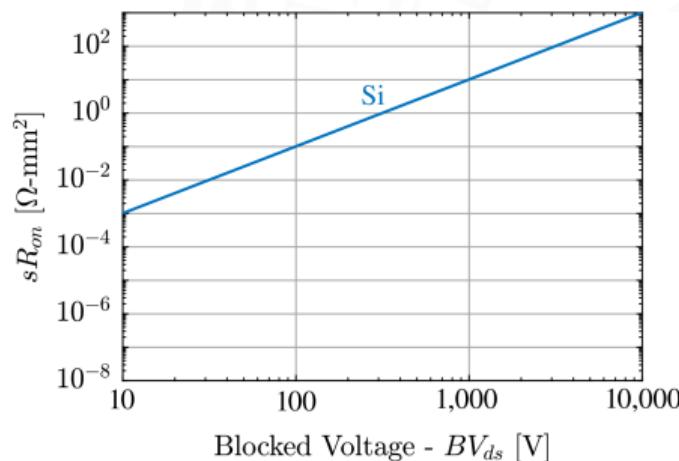


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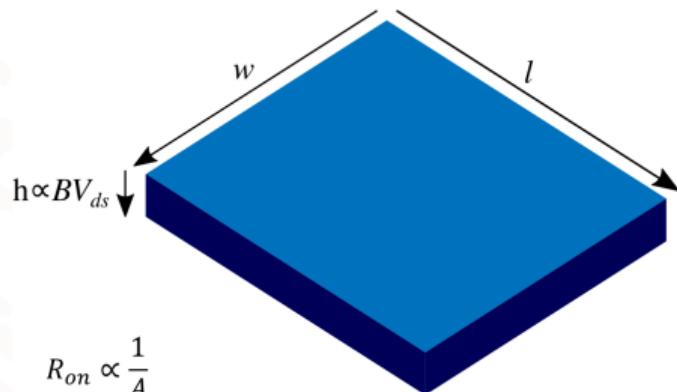
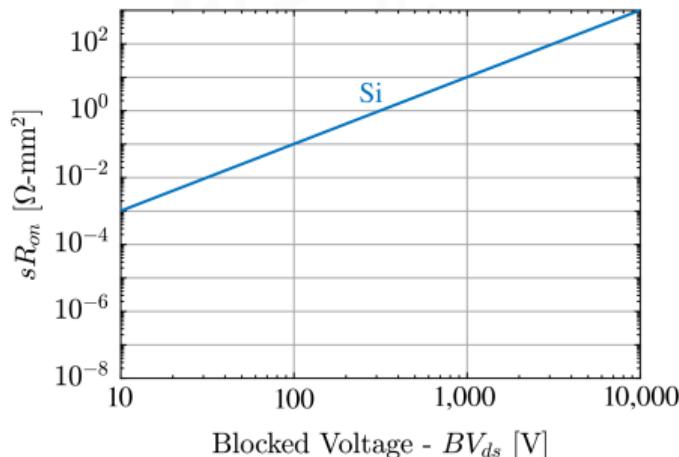


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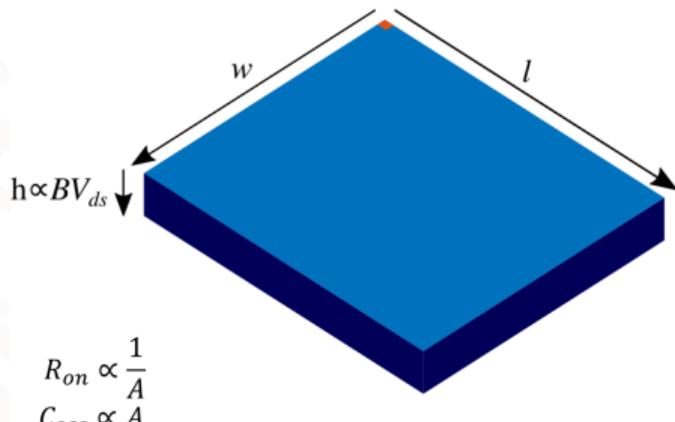
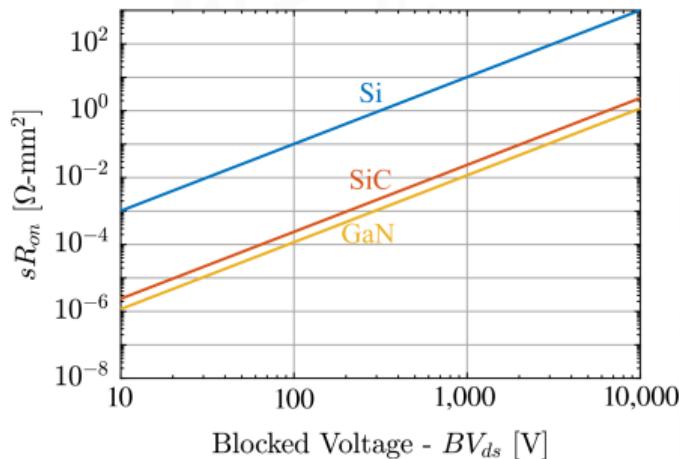


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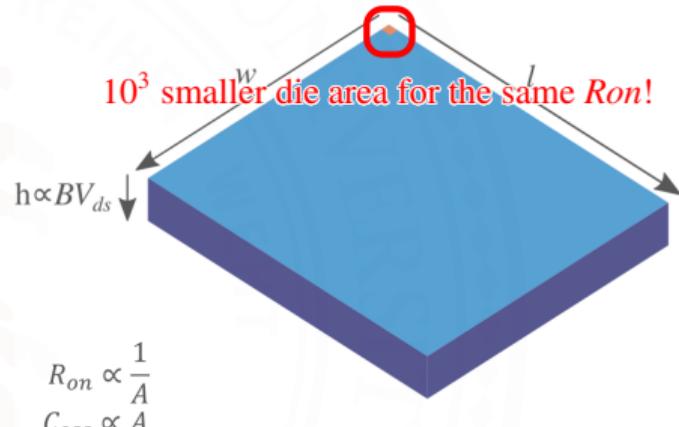
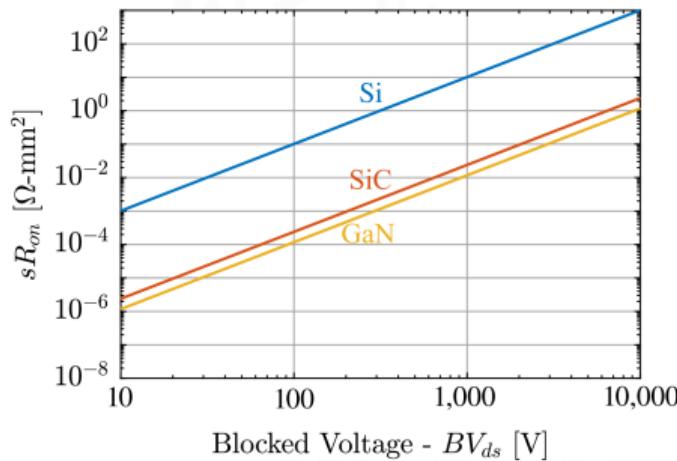


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**The Takeaway:** WBG devices allow  $\downarrow C_{oss}$  for the same  $R_{on}$  and  $V_{BV}$  which  $\uparrow$  efficiencies at higher switching frequencies compared to Si.

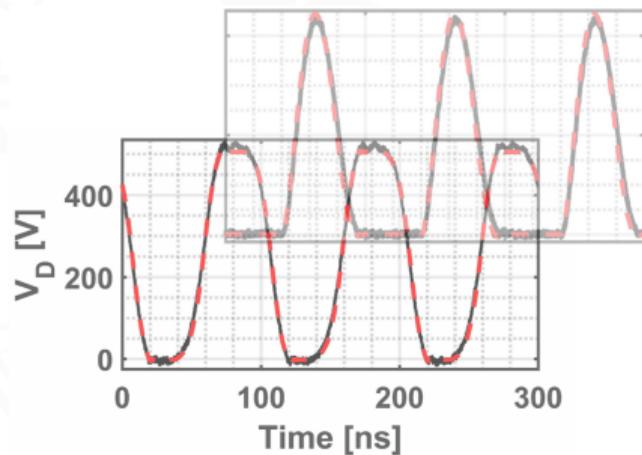
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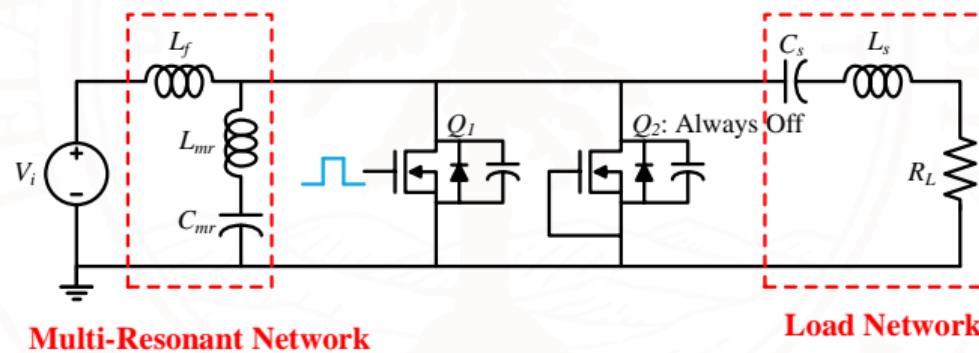
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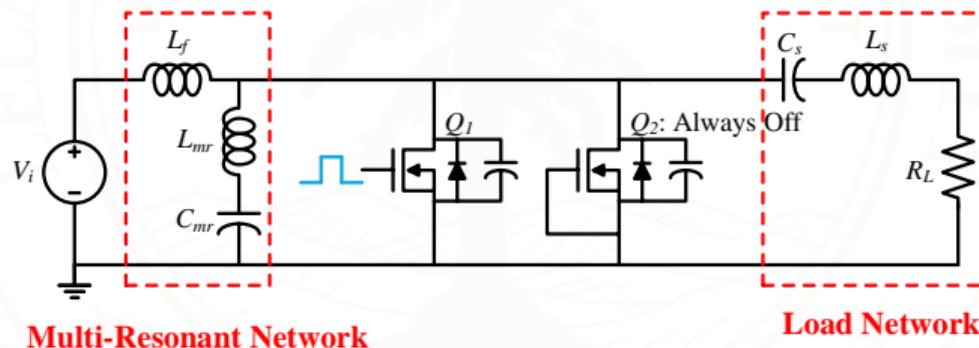
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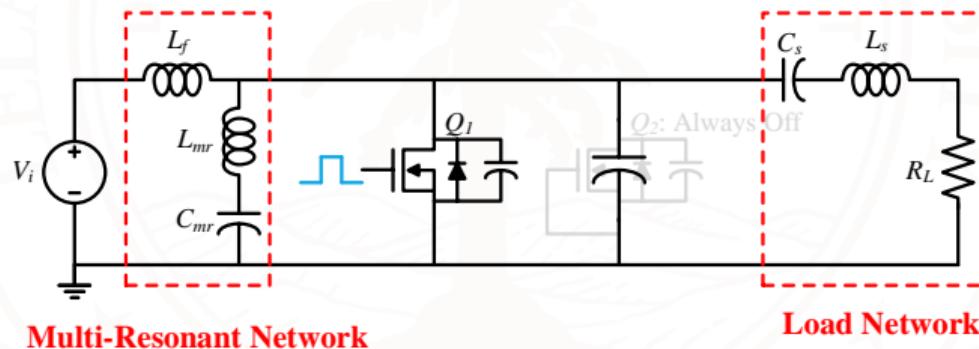
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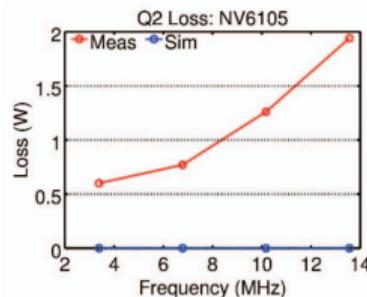
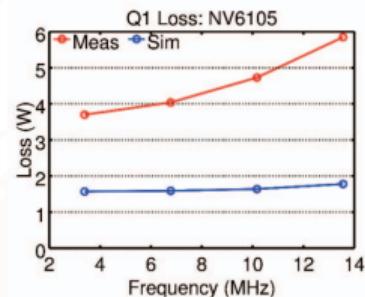
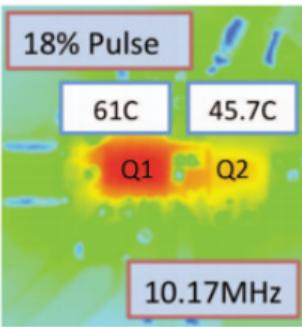
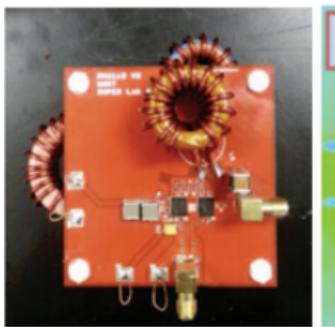
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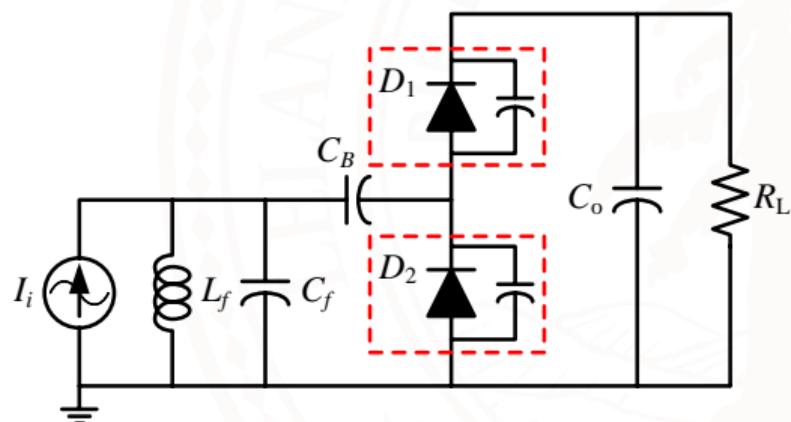
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  - ▶ The second switch serves as a parallel capacitor.
  - ▶ Expect 94% efficiency in simulation, but only get 89%.
  - ▶ And both FETs exhibit losses!



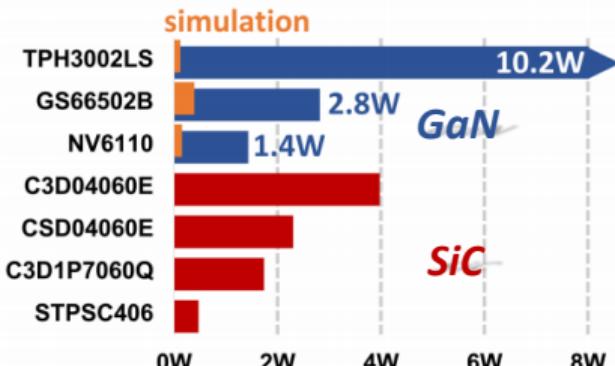
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- ▶ Same performance is observed in GaN and SiC Schottky diodes.
- ▶ Suspected the extra losses are from charging/discharging of the  $C_{oss}$  during off-state.



27.12 MHz, 25 W Rectifier



Park and Rivas-Davila, "Power loss of GaN transistor reverse diodes in a high frequency high voltage resonant rectifier," APEC 2017.

# $C_{oss}$ Loss Characterization: Sawyer-Tower Circuit

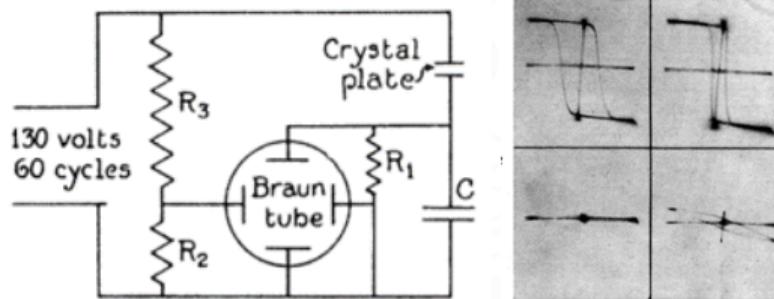
# Measuring Capacitor Losses: History

- ▶ In 1929: Sawyer and Tower developed a method to characterize dielectric hysteresis in Rochelle Salt.

## ROCHELLE SALT AS A DIELECTRIC

BY C. B. SAWYER AND C. H. TOWER  
THE BRUSH LABORATORIES, CLEVELAND

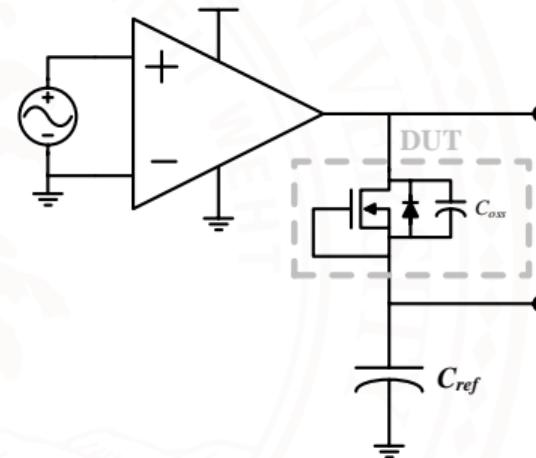
(Received November 6, 1929)



Sawyer and Tower, "Rochelle Salt as a Dielectric", Phys. Rev. 35, 1929

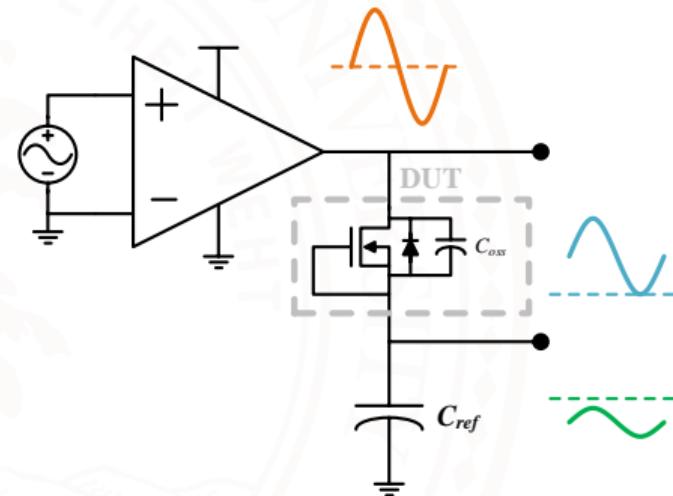
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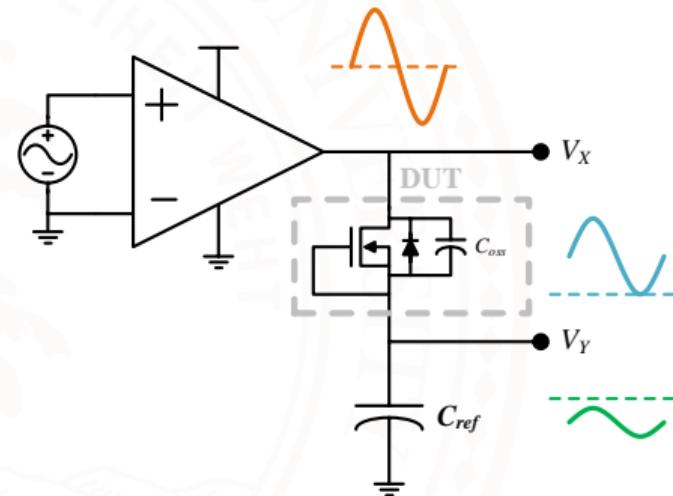
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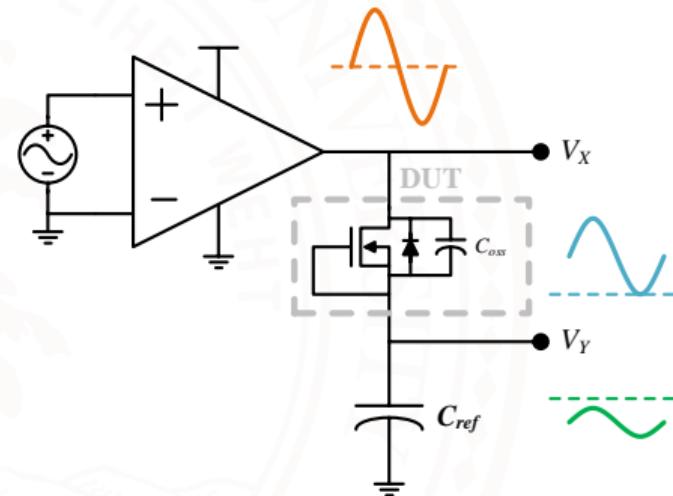
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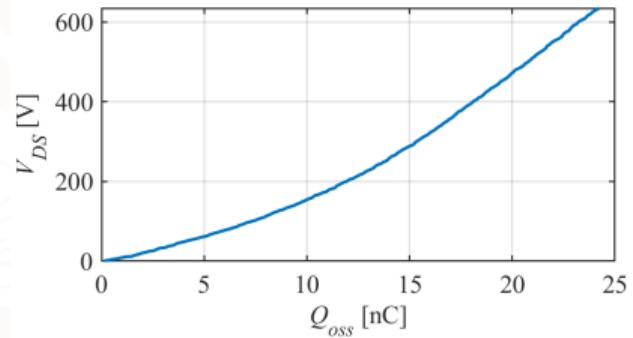
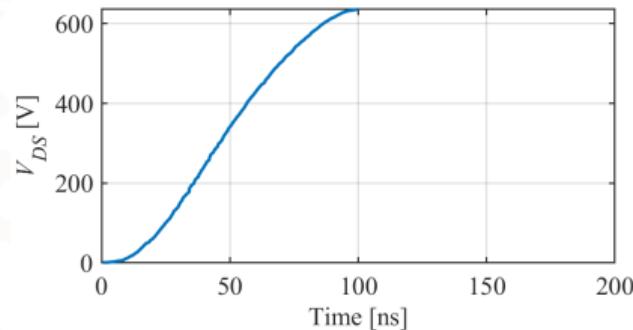
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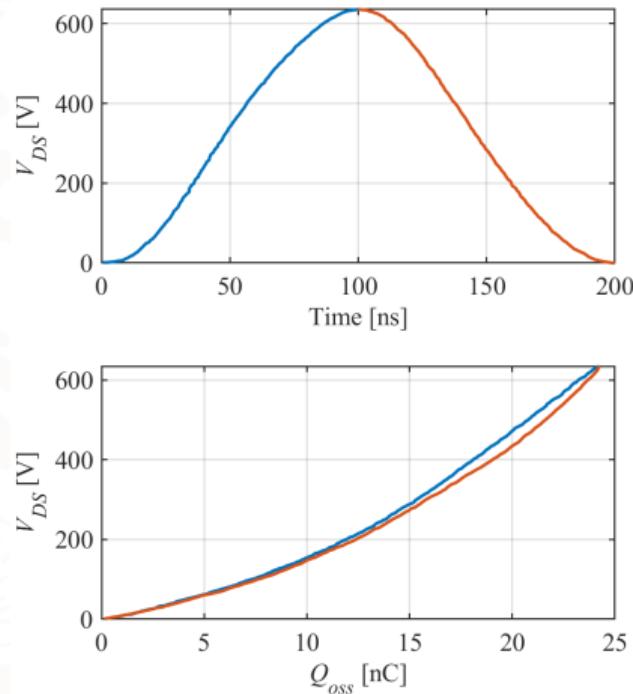
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- ▶ Obtain a  $Q$ - $V$  curve for charging...



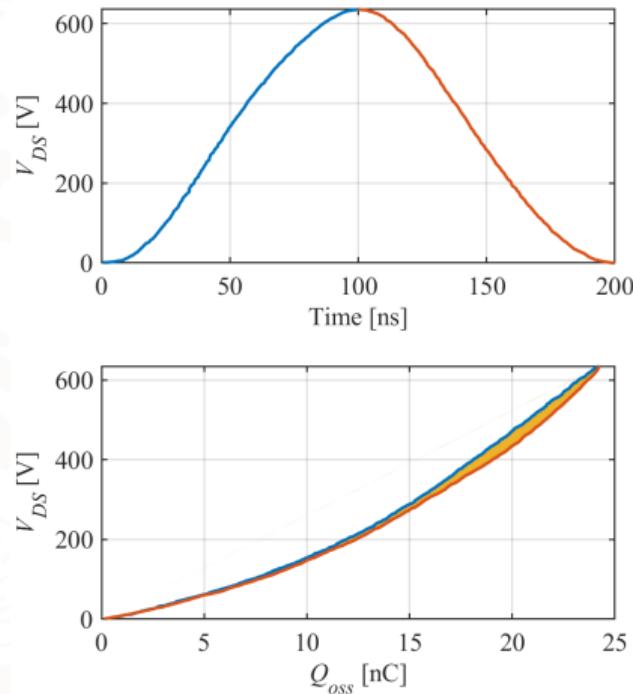
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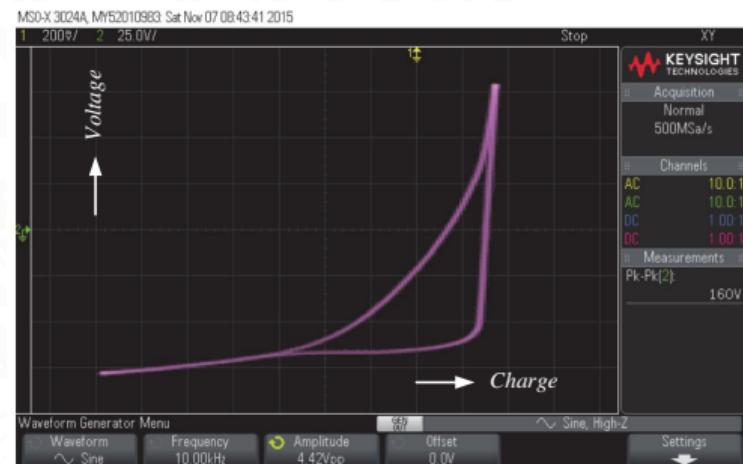
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- ▶ Obtain a  $Q$ - $V$  curve for charging and discharging. Hysteresis equates to **Losses ( $E_{diss}$ ) per Cycle**.



# Early Measurements on Power Devices: Si Superjunction MOSFETs

- ▶ In 2014/16: Fedison used the Sawyer-Tower circuit to characterize Si SJ MOSFETs at 200 kHz.
- ▶ Results indicate certain devices have significant hysteresis.

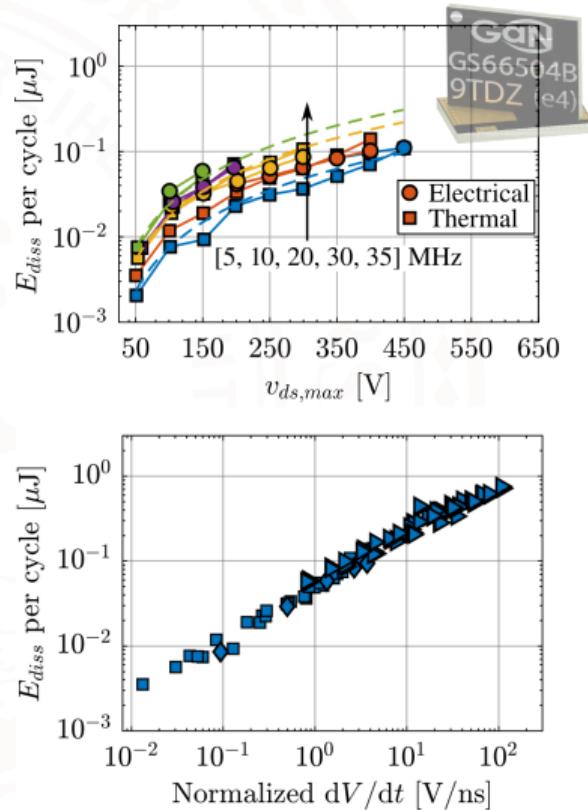


Fedison and Harrison, "C<sub>oss</sub> Hysteresis in Advanced Superjunction MOSFETs", APEC 2016.

Fedison et al., "C<sub>oss</sub> related energy loss in power MOSFETs used in zero-voltage-switched applications", APEC 2014.

# Our Findings on GaN

- ▶ **Recently:** We measured commercial GaN-on-Si HEMTs.
- ▶ Results can be modeled using Steinmetz fitting similar to magnetic core losses.
  - ▶ Increases with  $V_{DS}$  and  $f_{sw}$
  - ▶  $P_{diss} = kf^{1.6}V^\beta$
- ▶ Losses increase with  $dV/dt$ , indicating devices perform worse at faster frequencies.

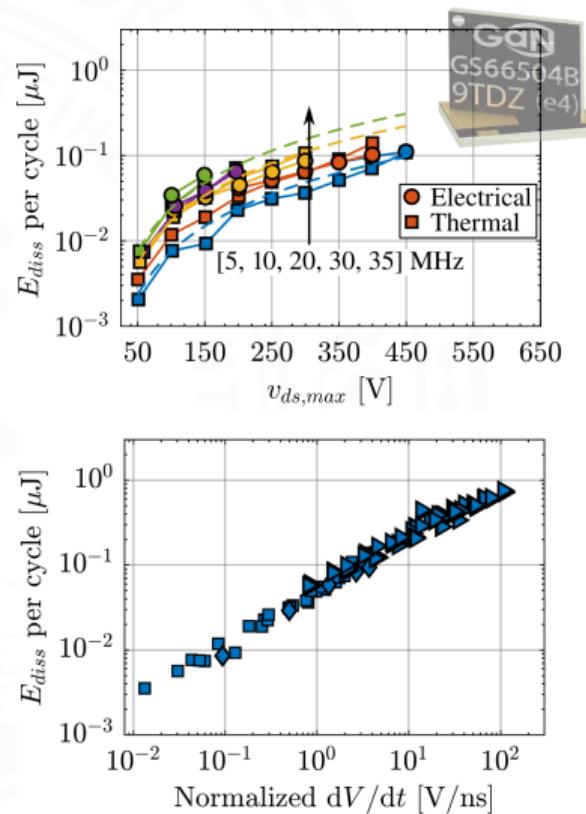


Zulauf et al., "Coss Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters", TPEL 2018.

# Our Findings on GaN

- ▶ **Recently:** We measured commercial GaN-on-Si HEMTs.
- ▶ Results can be modeled using Steinmetz fitting similar to magnetic core losses.
  - ▶ Increases with  $V_{DS}$  and  $f_{sw}$
  - ▶  $P_{diss} = kf^{1.6}V^\beta$
- ▶ Losses increase with  $dV/dt$ , indicating devices perform worse at faster frequencies.

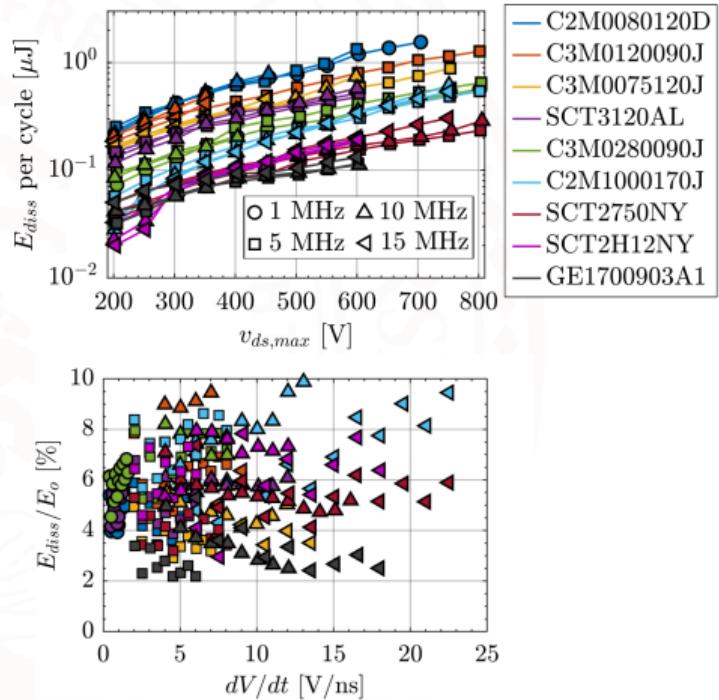
$f_{sw}$	$dV/dt$	$E_{diss}$	$P_{diss}$
10 MHz	70 V/ns	0.7 $\mu$ J	7 W
30 MHz	150 V/ns	0.9 $\mu$ J	27 W
54 MHz	250 V/ns	1.5 $\mu$ J	81 W



Zulauf et al., "Coss Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters", TPEL 2018.

# Our Findings on SiC

- ▶ Same study done on SiC MOSFETs and diodes.
- ▶ Results indicate  $E_{diss}$  is independent of frequency and  $dV/dt$ , so  $P_{diss} \propto f_{sw}$ .
- ▶ Losses can scale with  $f_{sw}$  slower than GaN!



Zulauf et al., "Active Power Device Selection in High- and Very-High-Frequency Power Converters," TPEL 2018.

# Device Selection Road Map

# Charting the Soft-switching Losses

- Total semiconductor losses in soft-switching conditions can be categorized as:

$$P_{dev} = \frac{P_{cond}}{\text{"ON"-State Losses}} + \frac{P_{C_{oss}}}{\text{"OFF"-State Losses}} + \frac{P_{gate}}{\text{Gating Losses}}$$



$$P_{dev} = R_{on} I_{rms}^2 + k f_{sw}^{\alpha} V^{\beta} + f_{sw} C_{iss} V_{gate}^2$$

# Comparing Si, SiC, and GaN Devices

## Vertical Si MOSFET



- ▶ **High  $sR_{on}$** ,  $5.93 \times 10^{-9} V_{BV}^{2.5} [\Omega\text{cm}^2]$

## Si Superjunction MOSFET



- ▶ **Moderate  $sR_{on}$** ,  $0.2d^{\frac{5}{4}} V_{BV} [\Omega\text{cm}^2]$

## Vertical SiC MOSFET



- ▶ **Low  $sR_{on}$** ,  $1.2 \times 10^{-11} V_{BV}^{2.5} [\Omega\text{cm}^2]$

## GaN-on-Si HEMTs



- ▶ **Lowest  $sR_{on}$** ,  $3.6 \times 10^{-12} V_{BV}^{\frac{7}{3}} [\Omega\text{cm}^2]$

Zulauf et al., "Active Power Device Selection in High- and Very-High-Frequency Power Converters," TPEL 2018.

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- ▶  $P_{C_{oss}} \propto f_{sw}^{1.6}$ .

Zulauf et al., "Active Power Device Selection in High- and Very-High-Frequency Power Converters," TPEL 2018.

# Comparing Si, SiC, and GaN Devices

## Vertical Si MOSFET



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- ▶  $P_{C_{oss}} \propto f_{sw}^2$ , but can be very low for LV devices.
- ▶ **Moderate  $P_{gate}$** : Large  $C_{iss}$  and  $V_{gate} \approx 10$  V.

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- ▶  $P_{C_{oss}} \propto f_{sw}$ .
- ▶ **High  $P_{gate}$** : Large  $C_{iss}$  and  $V_{gate} \approx 20$  V.

## GaN-on-Si HEMTs



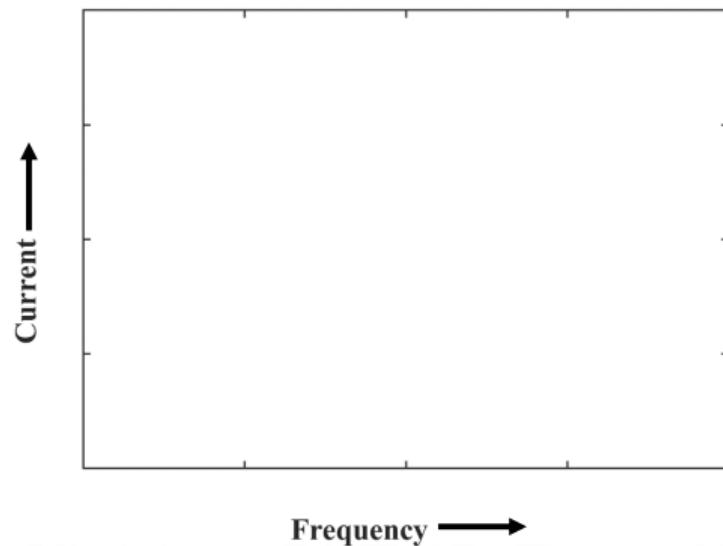
- ▶ **Lowest  $sR_{on}$** ,  $3.6 \times 10^{-12} V_{BV}^{\frac{7}{3}} [\Omega\text{cm}^2]$
- ▶  $P_{C_{oss}} \propto f_{sw}^{1.6}$ .
- ▶ **Low  $P_{gate}$** : small  $C_{iss}$  and  $V_{gate} \approx 5$  V.

Zulauf et al., "Active Power Device Selection in High- and Very-High-Frequency Power Converters," TPEL 2018.

# Comparing Si, SiC, and GaN Devices

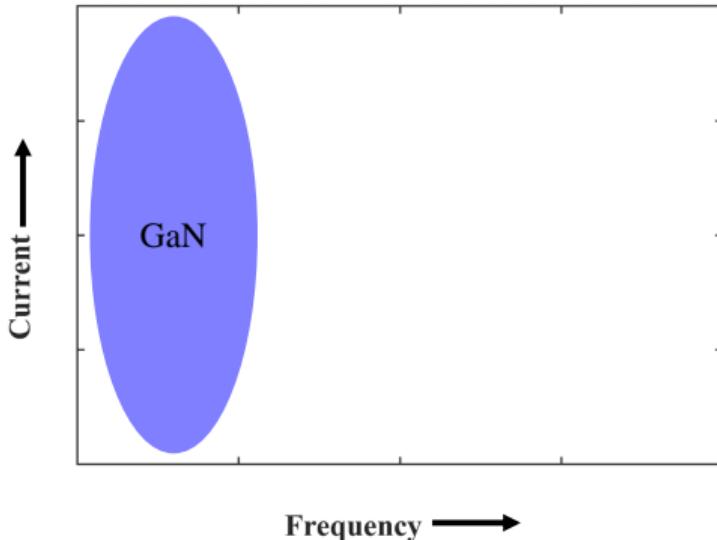
- ▶ **Verdict:** GaN and SiC typically preferable over Si for maximum efficiency.
- ▶ However, Si can still be used for  $\leq 200$  V applications; HV Si devices have much higher  $C_{oss}$  losses and  $R_{on}$ .
- ▶ **Caveats:**
  - ▶ Cost of WBG devices can be much higher.
  - ▶ Thermal dynamics are not considered for simplicity.
  - ▶ GaN HEMTs are not avalanche-rated.

## Case Study: GaN vs. SiC



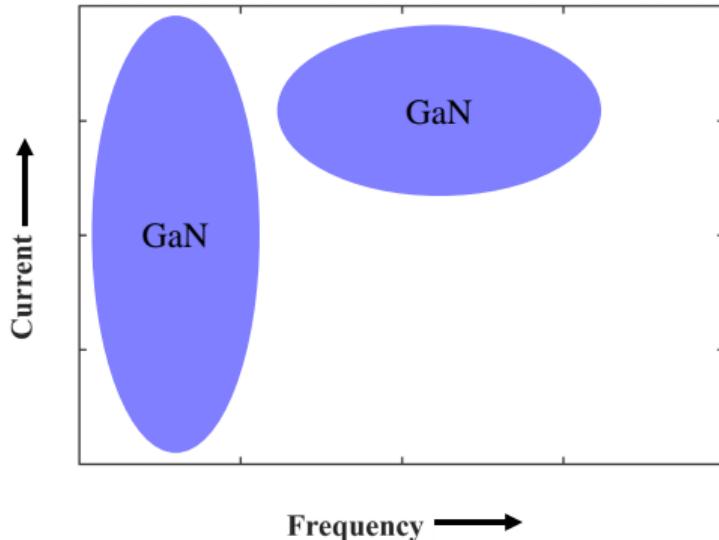
- ▶ For a fixed voltage application, consider  $P_{total} = P_{cond} + P_{C_{oss}}$

# Case Study: GaN vs. SiC



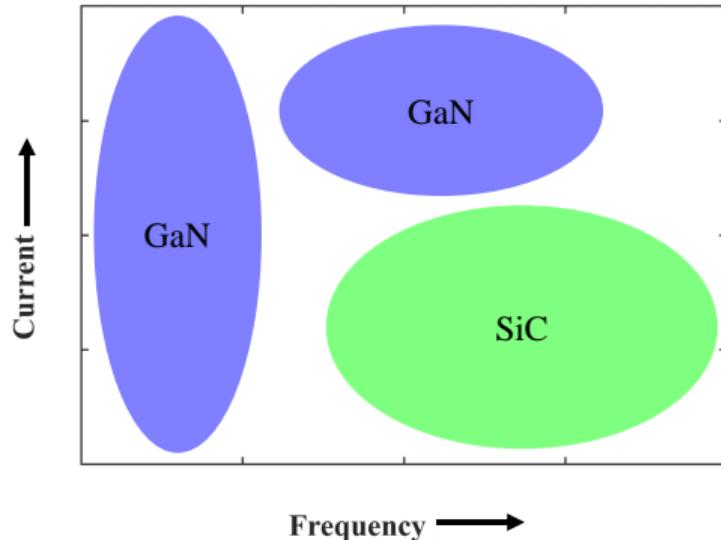
- ▶ For a fixed voltage application, consider  $P_{dev} = P_{cond} + \cancel{P_{C_{oss}}}$
- ▶ At low  $f_{sw}$ ,  $C_{oss}$  losses are negligible, so GaN is favored.

## Case Study: GaN vs. SiC



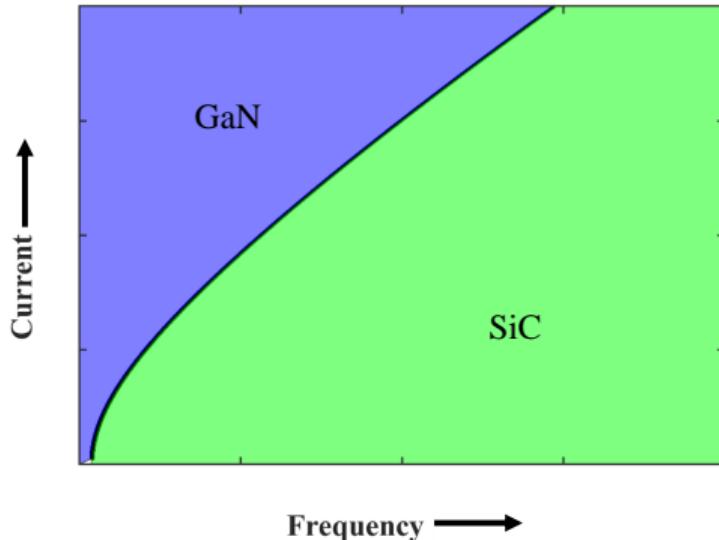
- ▶ For a fixed voltage application, consider  $P_{dev} = P_{cond} + P_{C_{oss}}$
- ▶ At higher current and higher-frequency,  $P_{cond} \gg P_{C_{oss}}$ .

## Case Study: GaN vs. SiC



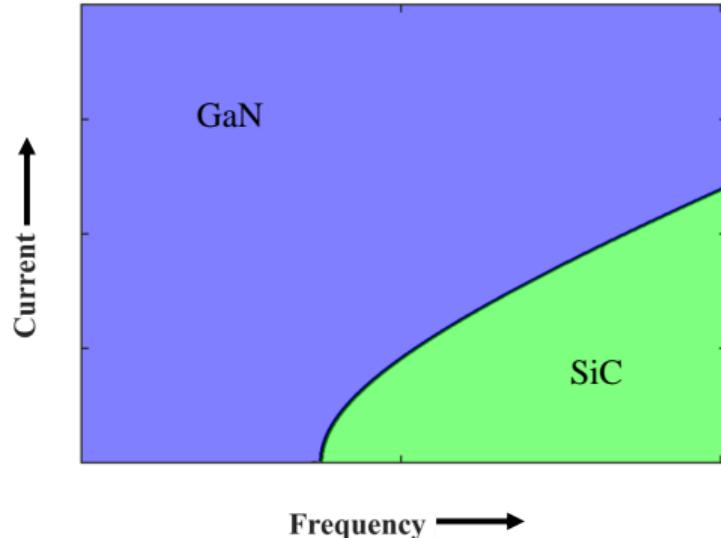
- ▶ For a fixed voltage application, consider  $P_{dev} = P_{cond} + P_{C_{oss}}$
- ▶ At lower current and higher-frequency,  $P_{cond} \ll P_{C_{oss}}$ .

# Case Study: GaN vs. SiC



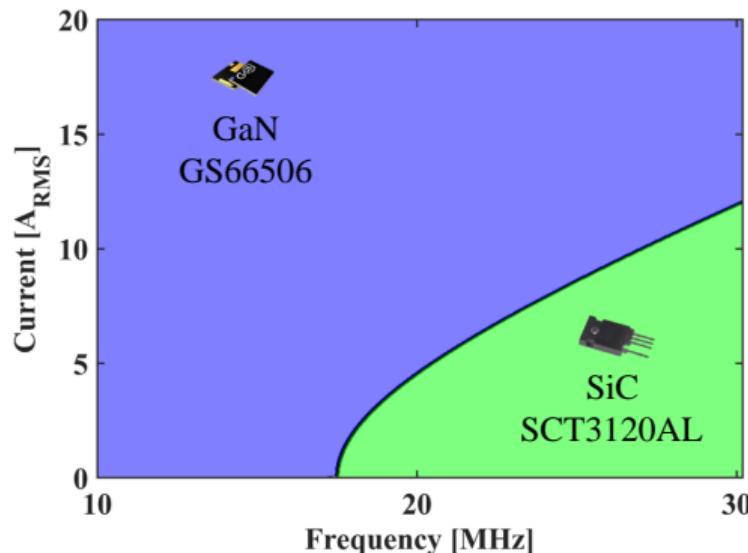
- ▶ For a fixed voltage application, consider  $P_{dev} = P_{cond} + P_{C_{oss}}$
- ▶ Fill in the gaps.

# Case Study: GaN vs. SiC



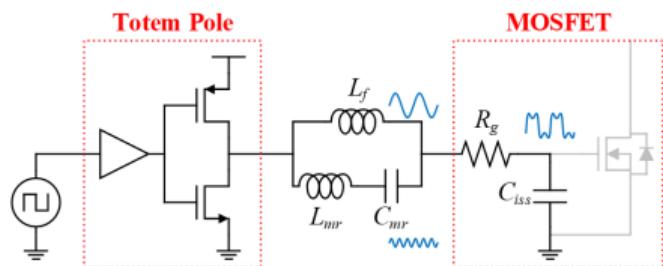
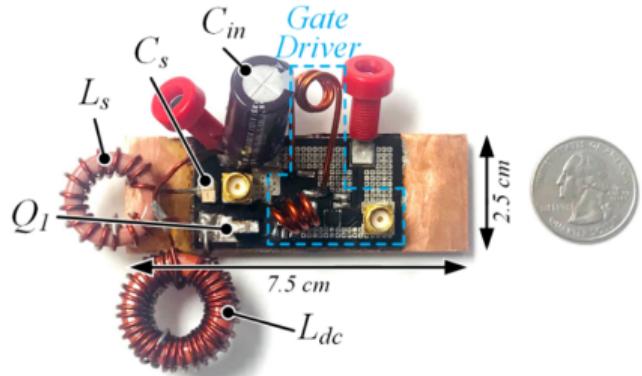
- ▶ For a fixed voltage application, consider  $P_{dev} = P_{cond} + P_{C_{oss}} + P_{gate}$
- ▶  $P_{gate}$  is much higher in SiC than GaN.

# Case Study: GaN vs. SiC

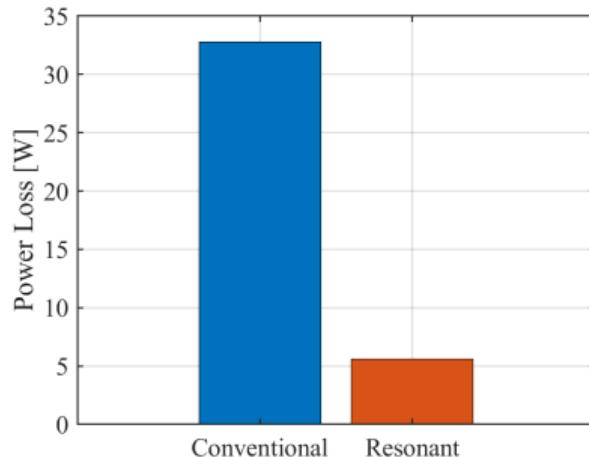


- ▶ For a fixed voltage application, consider  $P_{dev} = P_{cond} + P_{C_{oss}} + P_{gate}$
- ▶ We observe this with real devices ( $\approx 650$  V, 22 A rating).

# SiC Gating Solution: Resonant Gating



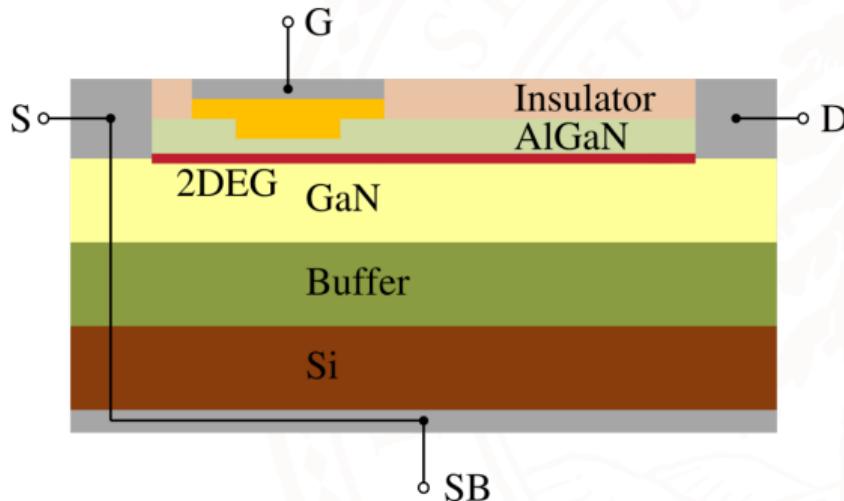
- ▶  $P_{gate} = f_{sw} C_{iss} V_{gate}^2$  can be reduced with resonant gate drives.
- ▶ Demonstrated a 30 MHz resonant gate drive using a SiC device with  $5 \times$  lower gating losses.



Tong et al., "On the Techniques to Utilize SiC Power Devices in High- and Very High-Frequency Power Converters," TPEL 2019.

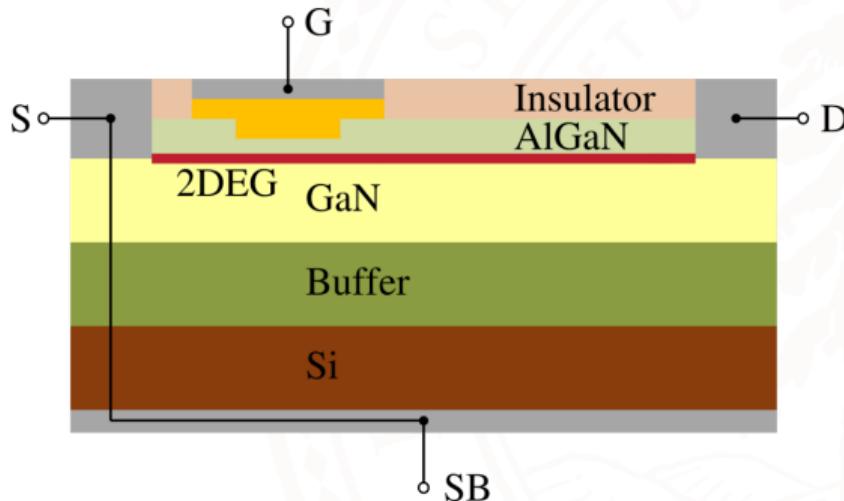
# Origins of $C_{oss}$ Losses: GaN

# GaN D-HEMT Power Devices



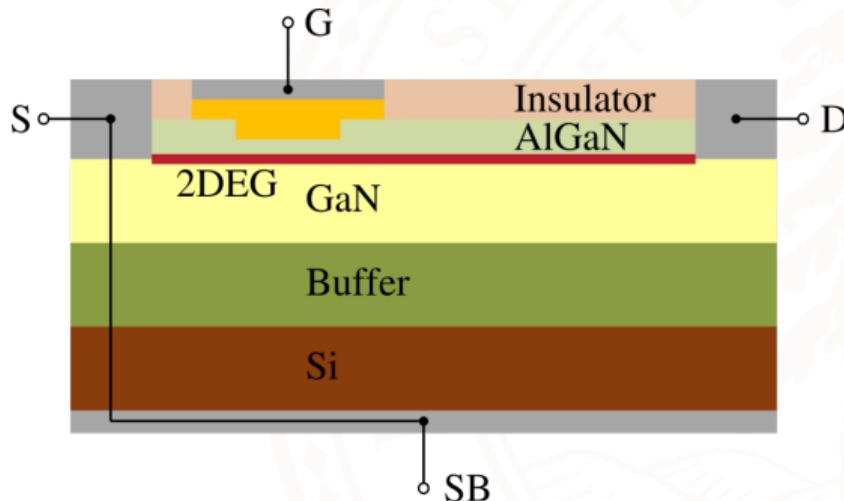
- ▶ GaN is usually grown on Si substrate for power devices.
- ▶ GaN and Si have large thermal and lattice mismatches

# GaN D-HEMT Power Devices



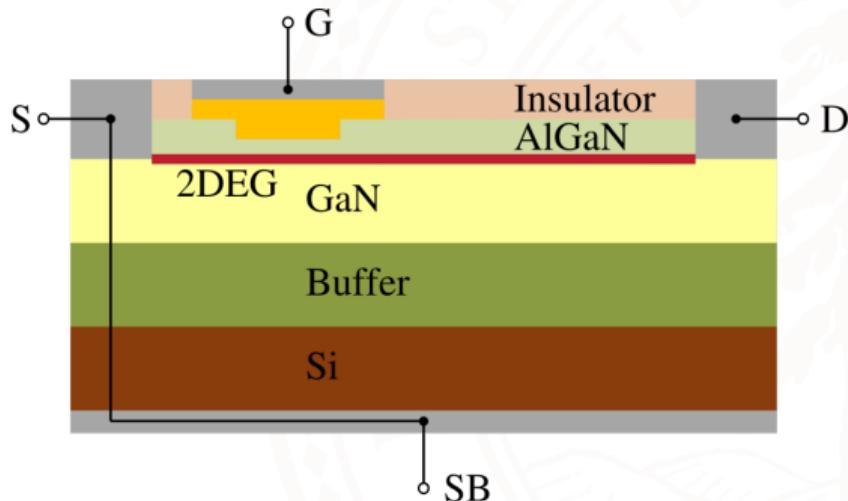
- ▶ GaN is usually grown on Si substrate for power devices.
- ▶ GaN and Si have large thermal and lattice mismatches
- ▶ Buffer layers are designed as an insulator to reduce mismatch and suppress vertical leakage.

# GaN D-HEMT Power Devices



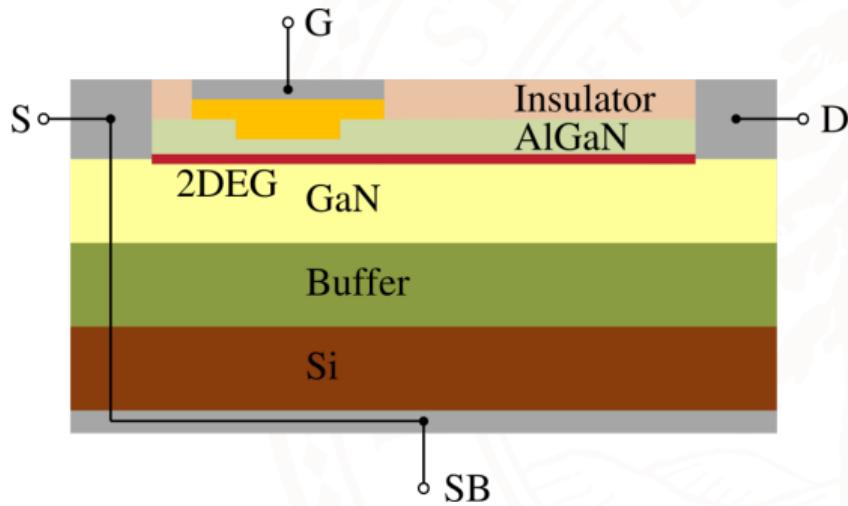
- ▶ **Issue 1:** The substrate is usually lightly Boron-doped, p-type Silicon, which results in high substrate resistance.

# GaN D-HEMT Power Devices



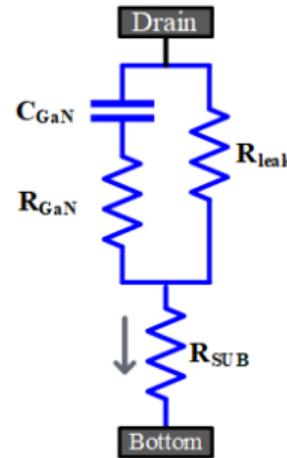
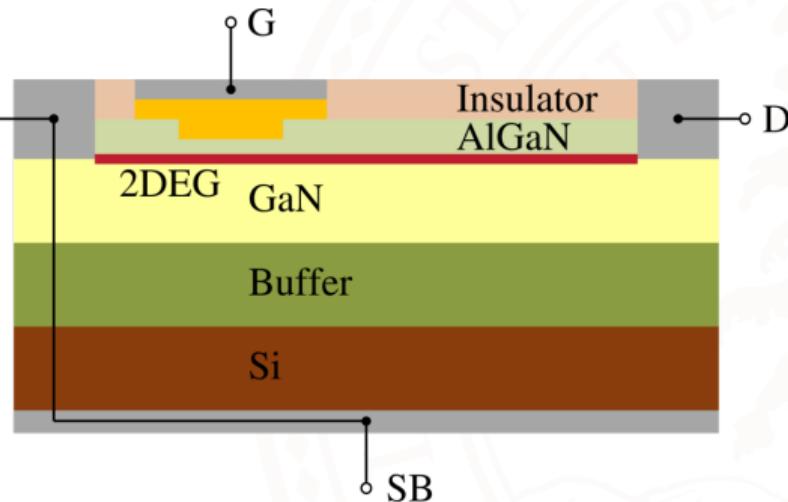
- ▶ **Issue 1:** The substrate is usually lightly Boron-doped, p-type Silicon, which results in high substrate resistance.
- ▶ **Issue 2:** Defects and traps exist in the buffer layers.
- ▶ Trapping dynamics have been one of the most critical issues in GaN HEMTs.
  - ▶  $V_{TH}$  and  $R_{ON}$  shift
  - ▶ Dynamic  $R_{DS,ON}$

# GaN D-HEMT Power Devices



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  - ▶  $V_{TH}$  and  $R_{ON}$  shift
  - ▶ Dynamic  $R_{DS,ON}$
  - ▶  $C_{OSS}$  losses in soft-switching

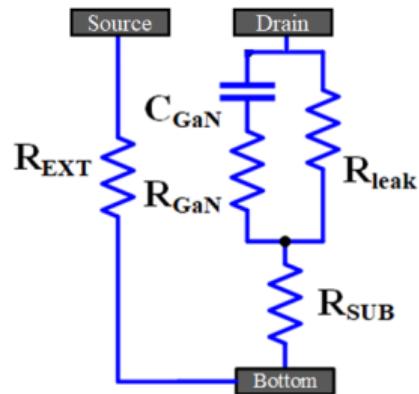
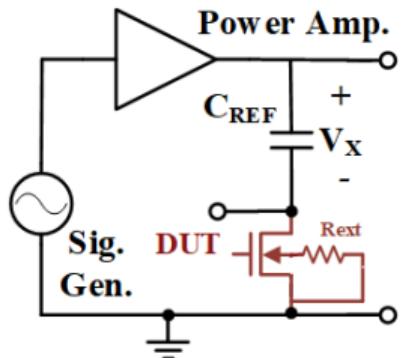
# GaN HEMTs: Separating the $C_{OSS}$ Loss Contributions



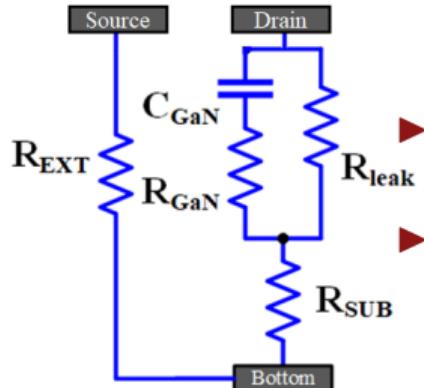
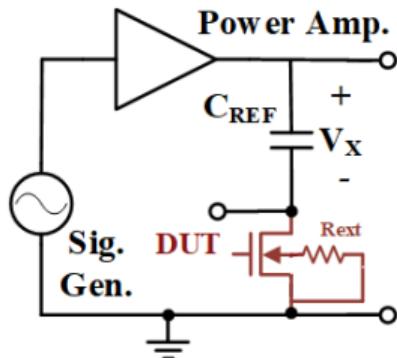
- ▶ To better model the  $C_{OSS}$  losses, the loss contribution from different layers are separated.
  - ▶ resistive loss from lightly doped substrate ( $R_{SUB}$ )
  - ▶ leakage current path from buffer ( $R_{GaN}$ )
  - ▶ trapping related capacitive hysteretic loss from buffer ( $C_{GaN}$ )

Zhuang et al., IEEE COMPEL 2019.

# $C_{oss}$ Loss with External Substrate Resistance

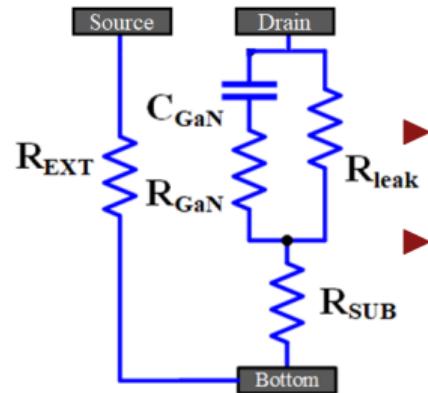
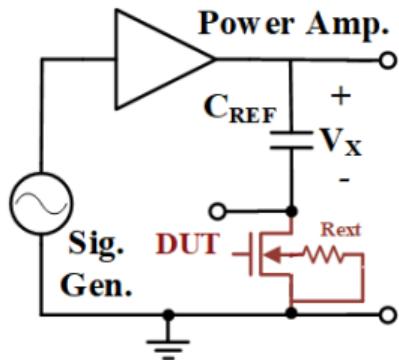


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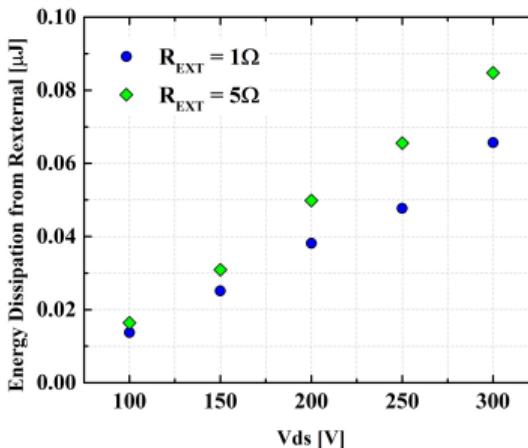
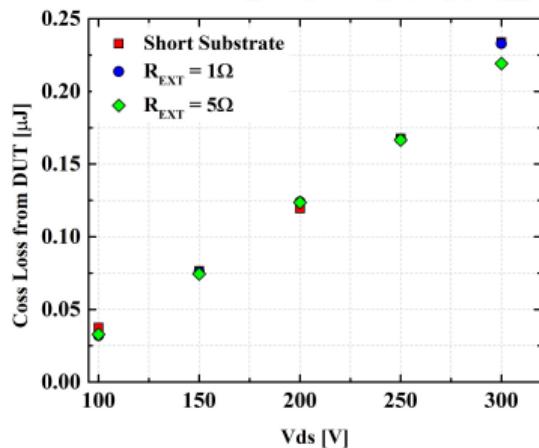


- ▶ The loss measured directly across device does not change much.
- ▶ With higher  $R_{EXT}$  value, the additional loss is higher.

# $C_{oss}$ Loss with External Substrate Resistance

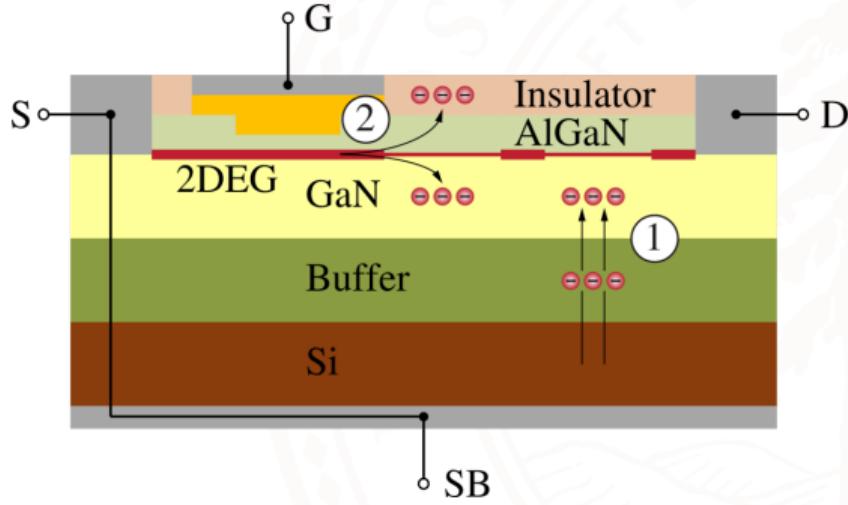


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- With higher  $R_{EXT}$  value, the additional loss is higher.



Zhuang et al., IEEE COMPEL 2019.

# Surface and Buffer Traps



► Two types of traps dominate in GaN HEMTs:

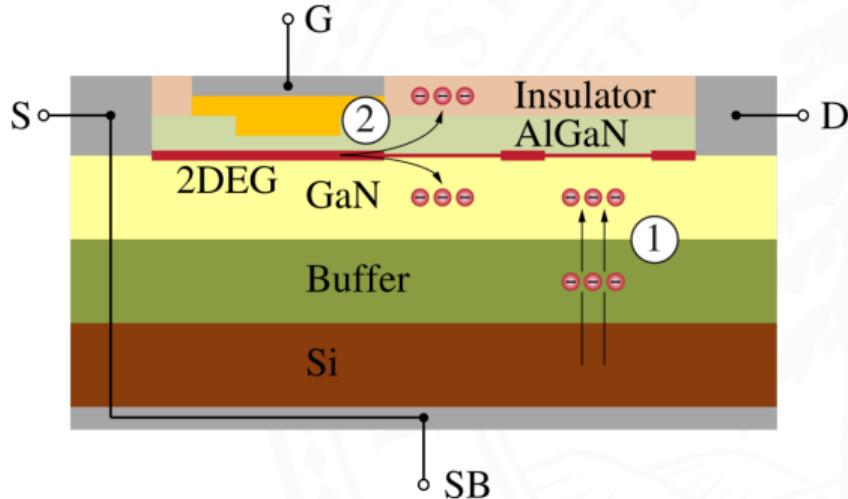
## ① Buffer traps

- originated from carbon doping and fabrication process etc.
- usually deeper traps with high activation energy

## ② Surface traps

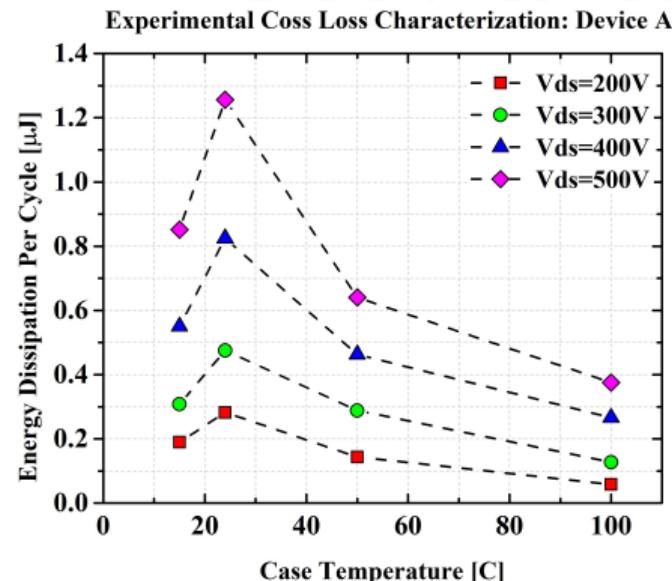
- originated from dielectric material, mask design etc.
- usually shallower traps with low activation energy

# Surface and Buffer Traps



- ▶ To estimate how trapping affects the measured  $C_{OSS}$  loss - temperature is varied in Sawyer-Tower setup.
- ▶ To better capture the trapping dynamics, a Sentaurus TCAD device simulation of the HEMT stack is built and calibrated.

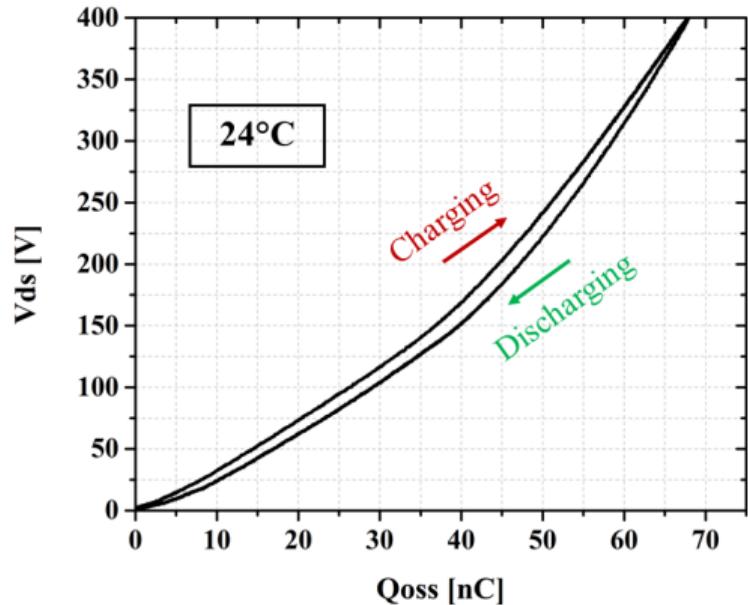
# Temperature-Dependent $C_{OSS}$ Loss - Trap-related loss



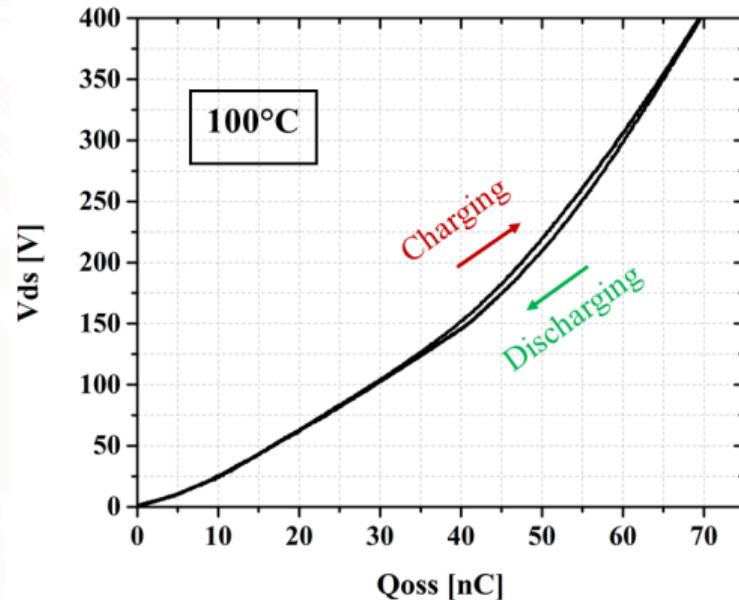
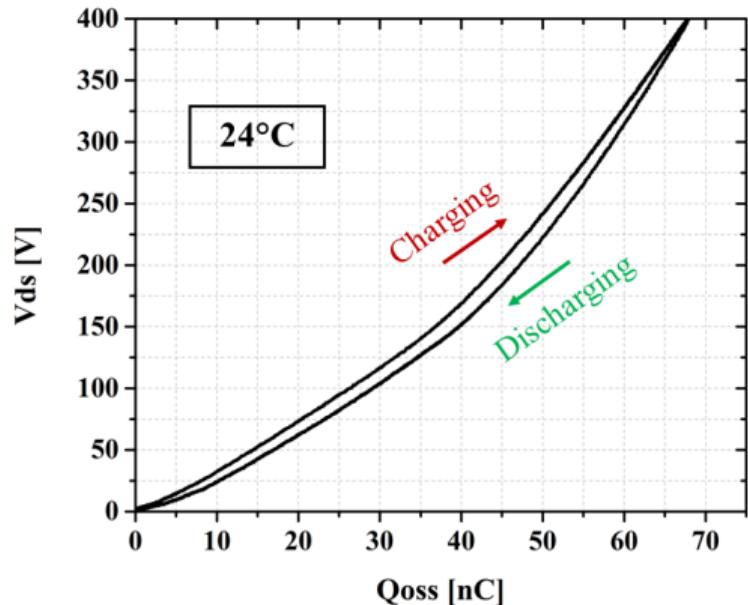
Zhuang et al., IEEE COMPEL 2019.

- ▶ Above 100°C,  $C_{OSS}$  losses are nearly insensitive to temperature.
- ▶ To estimate the contribution of each loss mechanism, we assume that at 100°C trap-related losses are eliminated.

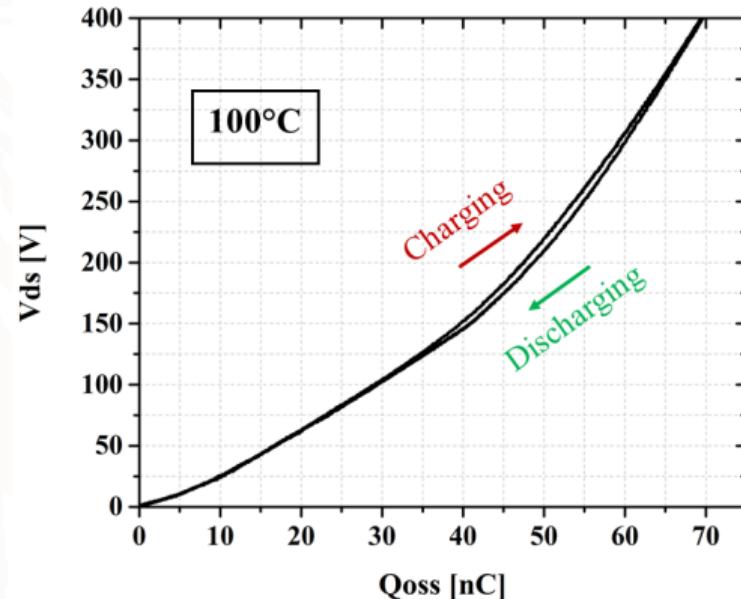
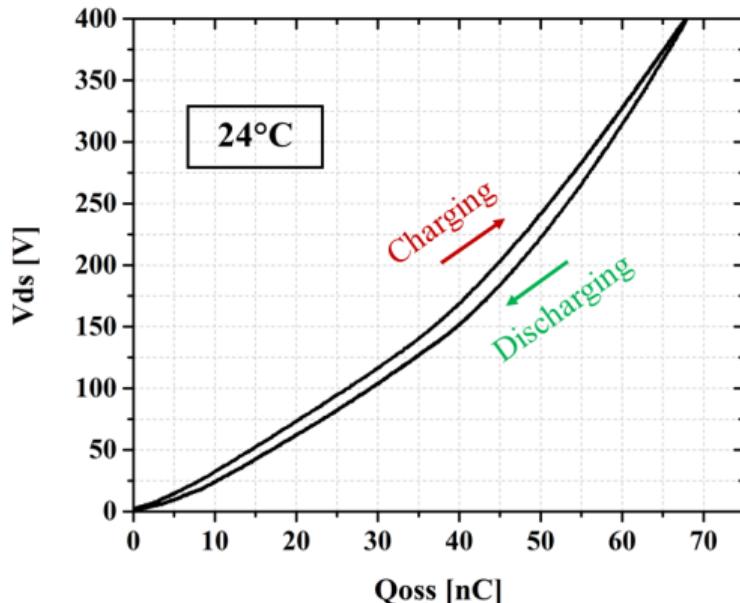
# Temperature-Dependent $C_{oss}$ Loss



# Temperature-Dependent $C_{OSS}$ Loss

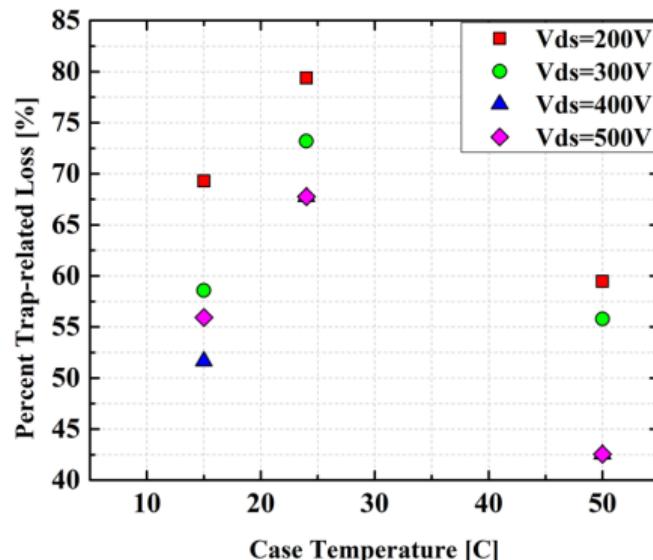


# Temperature-Dependent $C_{OSS}$ Loss



- ▶ Charge stored and discharged in output capacitance at  $V_{DS}=400$  V at 24°C (left) and 100°C (right)
- ▶ The total charge stored is identical (70 nC) but the losses are 3× higher at room temperature.

# Temperature-Dependent $C_{OSS}$ Loss - Trap-related loss

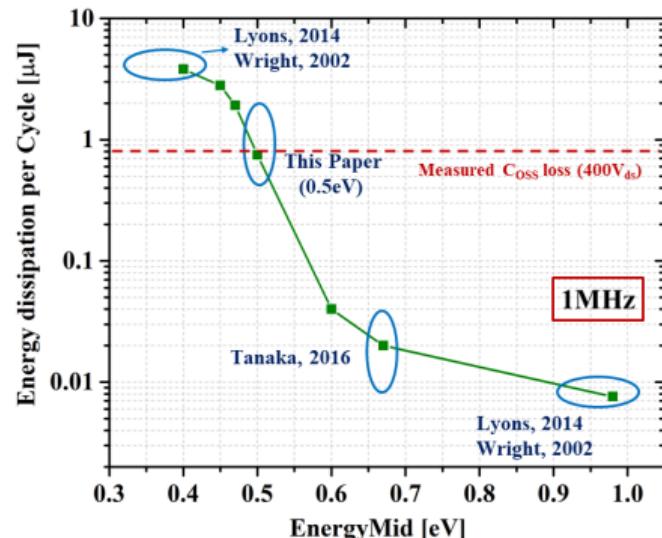


- ▶ At room temperature, the measured trap-related losses are around 68% to 80% of the total  $C_{OSS}$  losses.
- ▶ Guacci, 2018: 70% reduction with buffer redesign

Zhuang et al., IEEE COMPEL 2019.

Guacci et al., IEEE TPEL 2018.

# From TCAD: $C_{OSS}$ Losses vs. Trapping levels



- ▶ A mixed-mode simulation (Sawyer-Tower circuit + HEMT physical stack) is built in Sentaurus TCAD.
- ▶ Traps with a wide range of energy levels are added to the buffer layers, and the simulated  $C_{OSS}$  is plotted.
- ▶ It is observed that the traps that are mainly responsible for  $C_{OSS}$  losses is in the range of 0.5eV from valence band.

Zhuang et al., ECCE 2020.

# GaN Devices: Summary

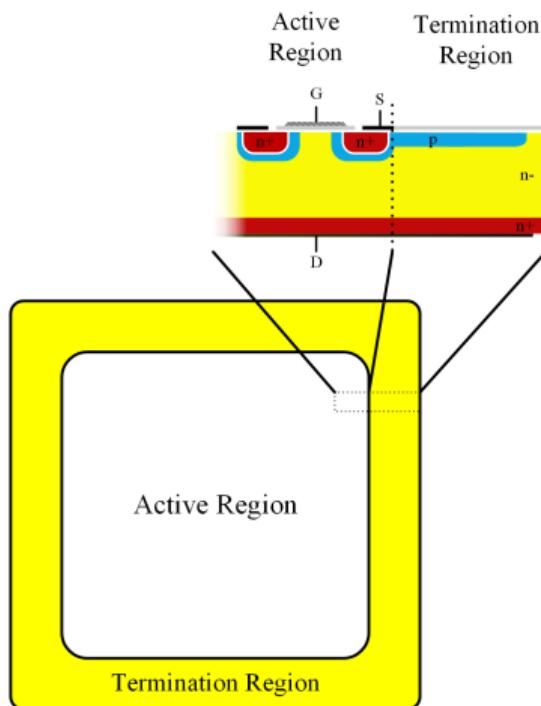
- ▶  $C_{oss}$  losses can be separated into contributions from highly-resistive substrate and trapping related buffer layers.
- ▶ Identifying trap energy levels and origins can provide guidelines on buffer and fabrication optimizations.

# Origins of $C_{oss}$ Losses: SiC

# SiC Device Physics and Structures: Incomplete Ionization

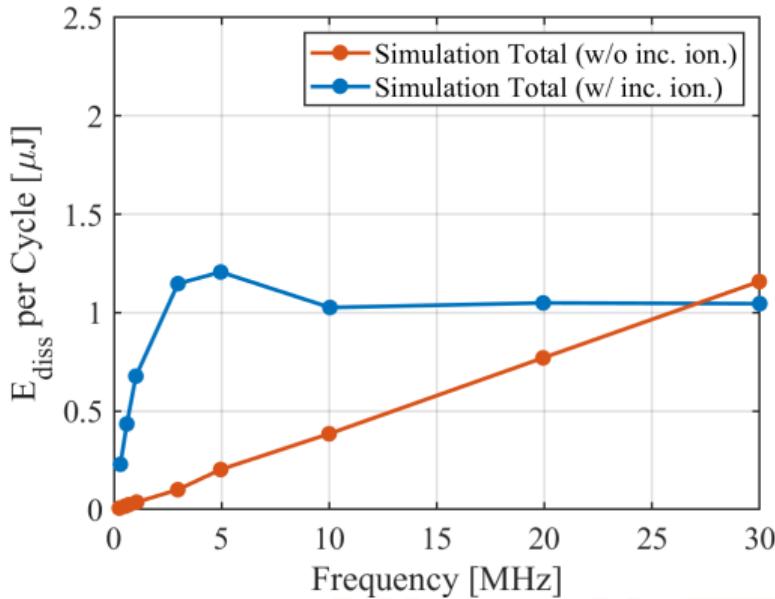
- ▶ **Incomplete Ionization:** In WBG devices, dopants require more energy and time to form  $e^-$  and  $h^+$  from an excitation.
- ▶ Resistance and capacitance of the device structure are dynamic when excited by high-frequency voltage/currents.

# SiC Device Physics and Structures: Termination Region



- ▶ **Termination Region:** In vertical power devices, the edges of the die require support of high electric fields.

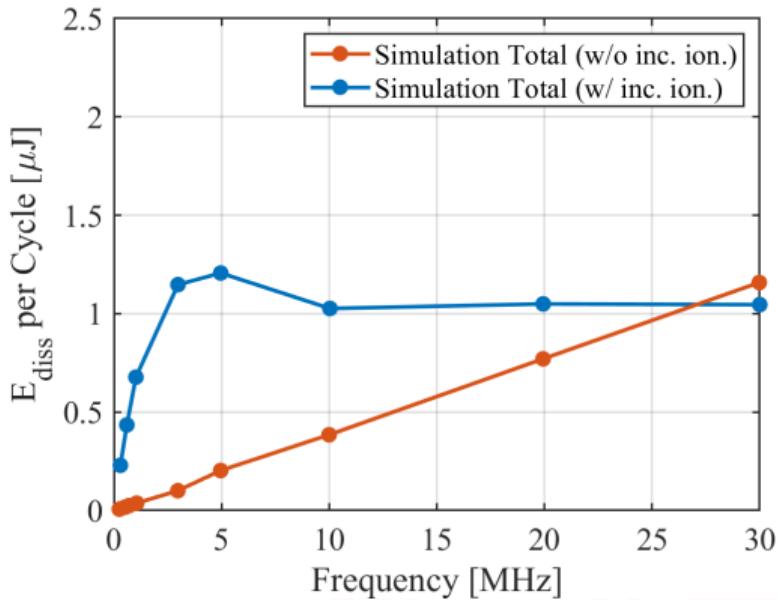
# SiC Devices $C_{oss}$ Losses: The Culprit



- ▶ Through collaboration with ON Semi., we used TCAD to identify the loss origins.
- ▶ Simulated a 1200 V ON Semi SiC Power MOSFET with incomplete ionization physics **activated** and **deactivated**.

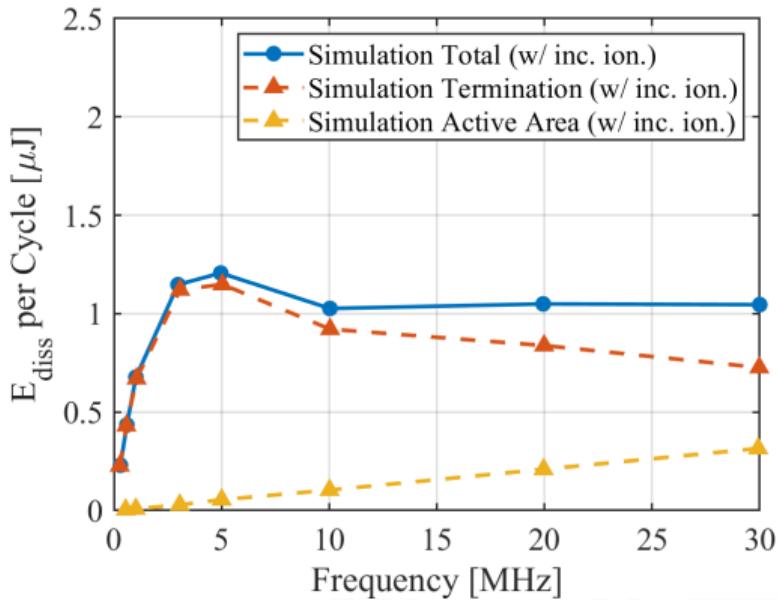
Z. Tong *et al.*, “Origins of Soft-switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications,” in JESTPE, Pre-print.

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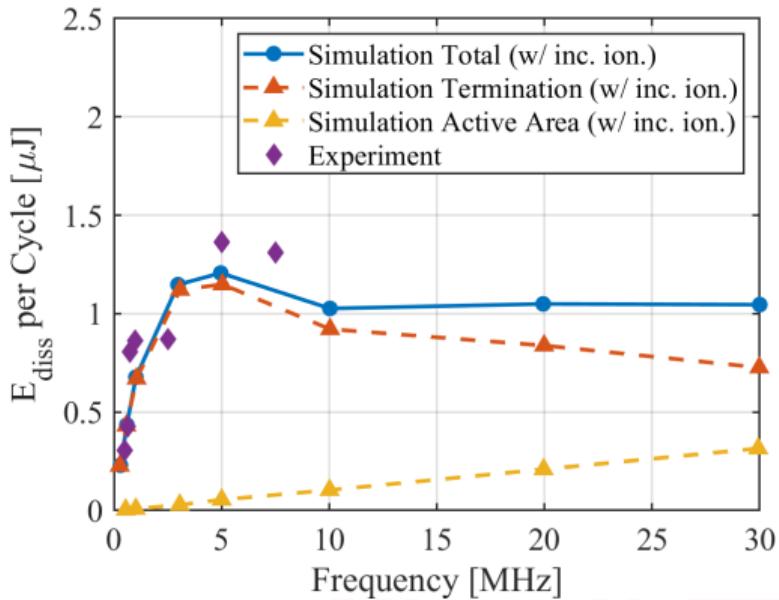
- ▶ **Observation 1:** Incomplete ionization explains  $C_{oss}$  loss behavior.
- ▶ Losses are frequency independent with incomplete ionization.

# SiC Devices $C_{oss}$ Losses: The Culprit



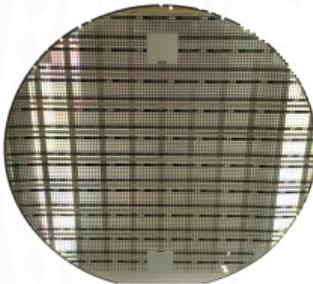
► **Observation 2:** Majority of the  $C_{oss}$  losses occur at the termination.

# SiC Devices $C_{oss}$ Losses: The Culprit



- ▶ **Observation 3:** Trends and values between experiment and simulation match.
- ▶ Indicates proper modeling of the device and physics.

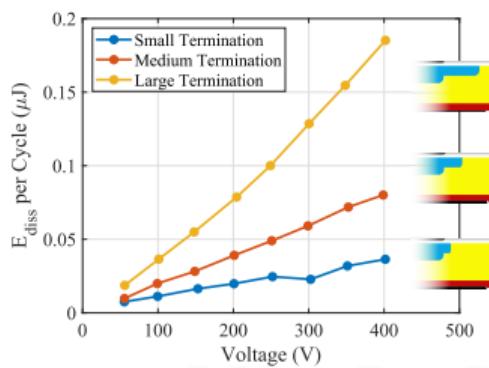
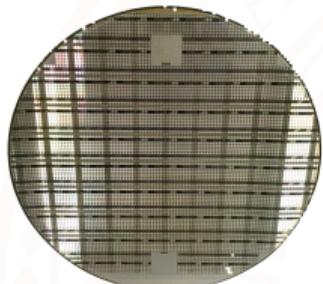
# SiC Devices $C_{oss}$ Losses: The Culprit



- ▶ Tested custom SiC dies from ON Semi. with different termination sizes and patterns.

Z. Tong *et al.*, “Origins of Soft-switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications,” in JESTPE, Pre-print.

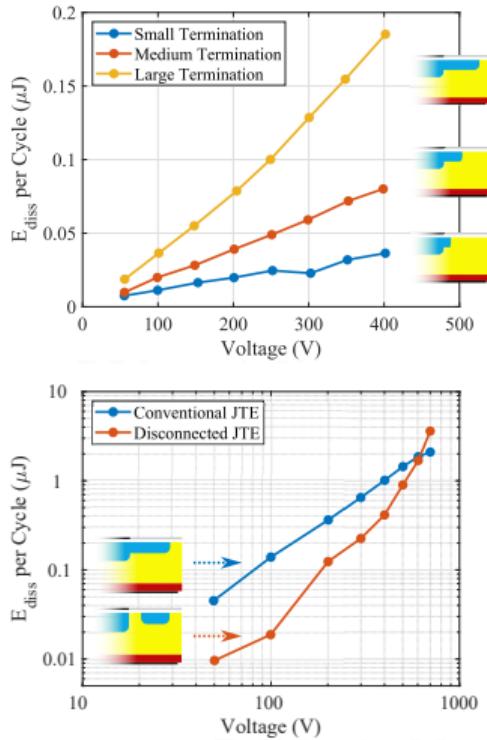
# SiC Devices $C_{oss}$ Losses: The Culprit



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- ▶ **Observation 4:** Different lengths and structures of the termination create different loss trends.
- ▶  $C_{oss}$  losses increase with termination length.

Z. Tong et al., "Origins of Soft-switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications," in JESTPE, Pre-print.

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- ▶ **Observation 4:** Different lengths and structures of the termination create different loss trends.
- ▶  $C_{oss}$  losses increase with termination length.
- ▶ Losses scale differently between guard ring (disconnected JTE) and JTE terminations.
  - ▶ JTE is better for higher voltages.
  - ▶ Guard ring is better for lower voltages.

Z. Tong et al., "Origins of Soft-switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications," in JESTPE, Pre-print.

# SiC Devices: Summary

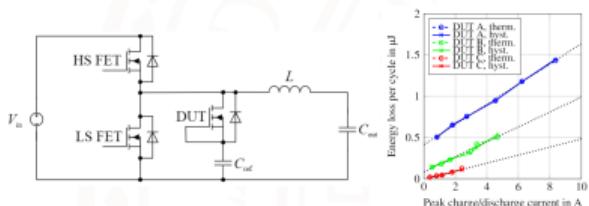
- ▶  $C_{oss}$  losses occur mainly due to resistive charging/discharging path through the termination.
- ▶ Behavior is controlled by incomplete ionization physics.
- ▶ The size and type of termination structure significantly affect losses.
- ▶ Leaves an opportunity for better modeling of SiC devices for HF converters and optimization of termination designs.

# Conclusion

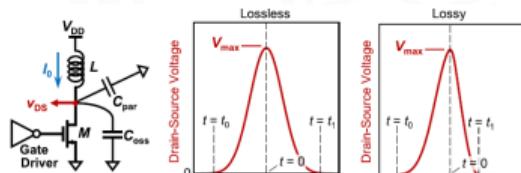
# Other Works

## ► Measurement and Modeling:

- *Bosch*: Developed a  $dV/dt$  (current-controlled) Sawyer-Tower testing method.

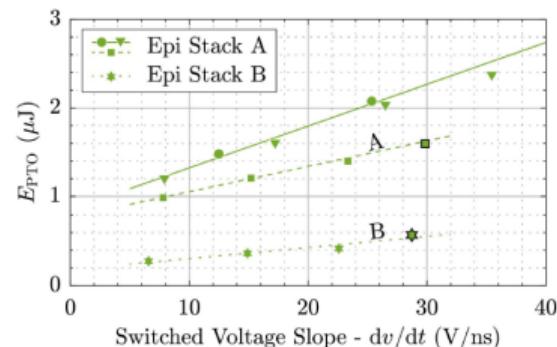


- *EPFL*: Utilized low-cost, nonlinear resonant method to characterize  $C_{oss}$  losses.



## ► Loss Origins/Mitigation:

- *ETH Zurich/Infineon*: Showed that the design of the buffer region influences  $C_{oss}$  losses in GaN devices.



*Bura et al., "Hysteresis Losses in the Output Capacitance of Wide Bandgap and Superjunction Transistors," EPE'18 ECCE Europe 2018.*

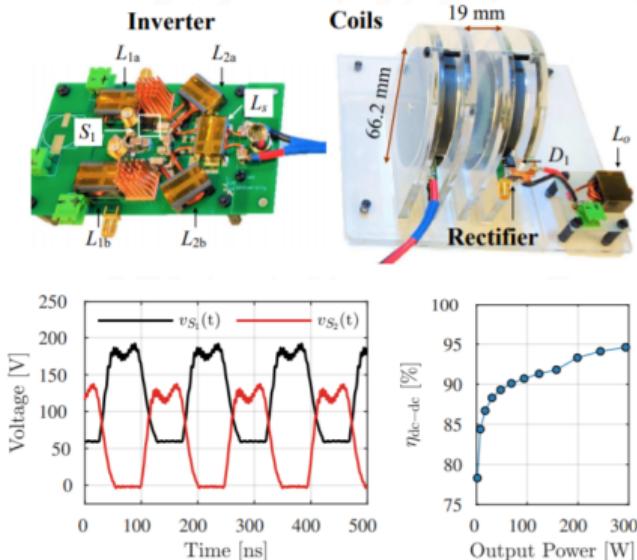
*Nikoo et al., "Measurement of Large-Signal  $C_{OSS}$  and  $C_{OSS}$  Losses of Transistors Based on Nonlinear Resonance," TPEL 2020.*

*Guacci et al., "On the Origin of the  $C_{oss}$ -Losses in Soft-Switching GaN-on-Si Power HEMTs," JESTPE 2019.*

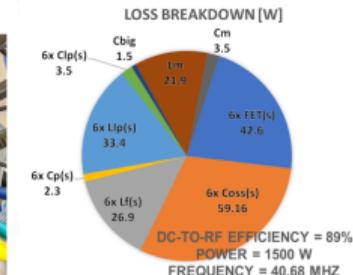
# Current Performance Benchmarks at MHz Frequency

*De-rating devices and understanding the  $C_{oss}$  losses → better performance.*

- **Wireless power transfer - 6.78 MHz, 95% DC-DC efficiency Using 150 V Si**



- **Radio frequency Power Amplifier - 40.68 MHz, 90% efficiency**



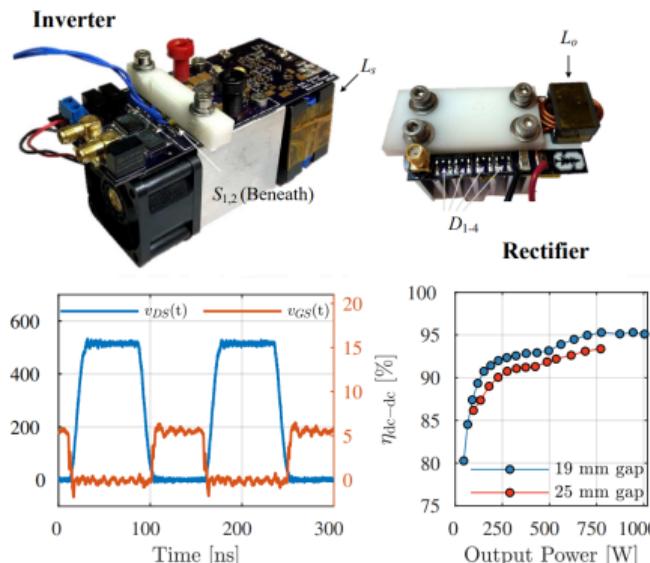
Gu et al., "6.78 MHz Wireless Power Transfer with Self-Resonant Coils at 95% DC-DC Efficiency," TPEL 2020.

Surakitbovorn et al., "A Simple Method to Combine the Output Power from Multiple Class-E Power Amplifiers," JESTPE 2020.

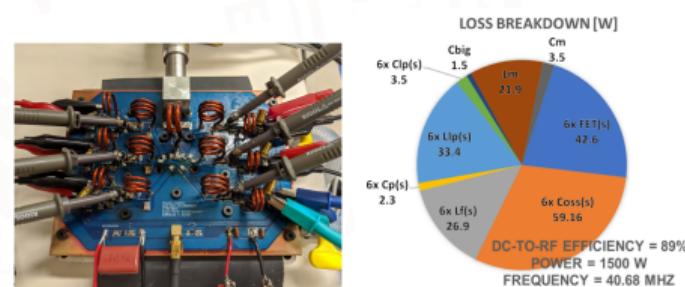
# Current Performance Benchmarks at MHz Frequency

*De-rating devices and understanding the Coss losses → better performance.*

- ▶ **Wireless power transfer - 6.78 MHz, 95% DC-DC efficiency Using GaN & SiC with Lowest  $C_{OSS}$  losses**



- ▶ **Radio frequency Power Amplifier - 40.68 MHz, 90% efficiency**



*Gu et al., "6.78 MHz Wireless Power Transfer with Self-Resonant Coils at 95% DC-DC Efficiency," TPEL 2020.  
Surakitbovorn et al., "A Simple Method to Combine the Output Power from Multiple Class-E Power Amplifiers," JESTPE 2020.*

# Conclusion

## Symptom

- ▶ The  $C_{OSS}$  losses inhibit the performance of soft-switching converters in high-frequency applications.

## Diagnosis

- ▶ Sawyer-Tower circuit is used to characterize  $C_{OSS}$  losses in GaN and SiC devices.
- ▶ GaN and SiC have different trends with voltage and frequency.

## Treatment

- ▶ For GaN: Identifying trap energy levels and optimization on buffer design is critical in reducing  $C_{OSS}$  losses.
- ▶ For SiC: understanding and improving the termination structure is the top priority for better high-frequency performance.

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# Acknowledgments

## Sponsors

- ▶ Stanford SystemX Alliance: ONSemiconductor, Daihen, Texas Instruments, LAM Research
- ▶ The Precourt Institute for Energy & the TomKat Center for Sustainable Energy
- ▶ National Science Foundation

## Students and Collaborators

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  - ▶ Former students: Prof. Jungwon Choi (UMN), Dr. Wei Liang, Dr. Luke Raymond, Dr. Grayson Zulauf.