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This paper has been accepted for publication by

IEEE Transactions on Industrial Electronics.

DOI

10.1109/TIE.2019.2899557

Citation

L. Gu, Z. Tong, W. Liang, and J. Rivas, "A Multi-Resonant Gate Driver for High-Frequency Resonant Converters," *IEEE Trans. Industrial Electronics*, in press.

IEEE Xplore URL

<https://ieeexplore.ieee.org/document/8648471>

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A Multi-Resonant Gate Driver for High-Frequency Resonant Converters

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Abstract—This paper presents the design and implementation of a High-Frequency/Very-High-Frequency (HF/VHF) multi-resonant gate drive circuit. The design procedure outlined here is greatly simplified compared with other VHF self-oscillating multi-resonant gate drivers presented in previous works. The proposed circuit can reduce the long start-up time required in a self-oscillating resonant gate drive circuit and utilize the fast transient capability of VHF converters better. We demonstrate a prototype resonant gate driver, which reduces up to 60% of the gate driving power in a 20 MHz 32 W Class-E power amplifier using a Si MOSFET. The proposed technique could also drive a high-voltage rated SiC MOSFET at 30 MHz with a slew-rate of 2.5 V/ns at the gate, while an integrated hard-switching gate driver only provides a 1.8 V/ns slew-rate and is five times less efficient than the proposed resonant gate driver.

Index Terms—Resonant power conversion, Power amplifiers, Resonant gate driver circuits, SiC MOSFETs

I. INTRODUCTION

A clear way to achieve reduced size and weight, fast transient response, and full integration of state-of-art power converters is to increase switching frequencies. During the past three decades, resonant converters [1]–[5] have been successfully demonstrated with switching frequencies up to 10s of MHz. Applying RF circuit design techniques to dc-dc power conversion has pushed the switching frequency of power converters using discrete components beyond 100 MHz [6], [7]. As switching frequency further increases, the percentage of gate driving losses among the total power loss can become unacceptable in both hard-switching PWM converters and resonant converters.

To first principles, the conventional gate driving loss is equal to $f_s V_g Q_g$ [8], where f_s is the switching frequency, V_g is gate drive supply voltage, Q_g is the total gate charge of the MOSFET. Fig 1 shows a typical MOSFET Q_g vs V_g plot assuming a constant gate charging current. Referring to Fig. 1a, during interval 1 when V_{DS} is constant, the gate current I_G charges C_{GS} and C_{GD} simultaneously. The sum of C_{GS} and C_{GD} when C_{DS} is shorted is also called C_{iss} . After V_{GS}

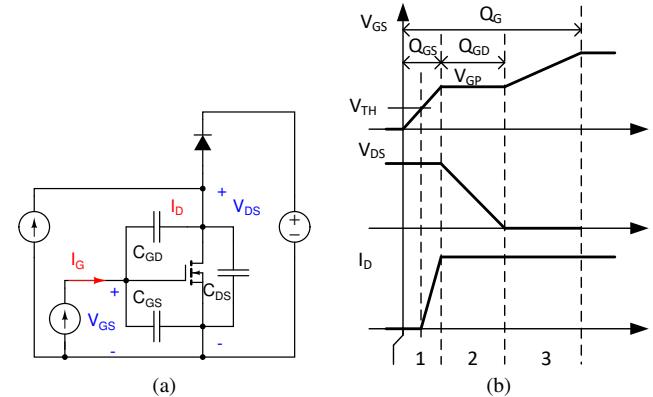


Fig. 1: Gate charge Q_g measuring and characteristics of a MOSFET. (a) Q_g measuring circuit, gate charging/discharging current is constant. V_{DS} is clamped by voltage source, while I_{DS} being clamped by current source. (b) Turn-on intervals of a MOSFET, x -axis is time, with constant charging current, it also represents Q_g .

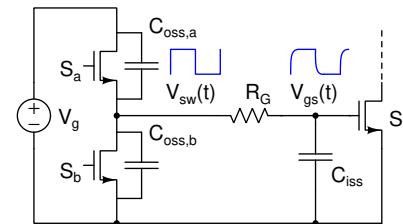


Fig. 2: Conventional gate driver.

passes threshold voltage, it reaches the plateau voltage V_{GP} and remains constant. During interval 2, the gate current I_G only charges C_{GD} , and V_{DS} drops to zero. The charge provided to C_{GD} in this period is Q_{GD} . During the last interval 3, the gate supply provides the rest of the charge to C_{iss} . The MOSFET channel is fully enhanced with a gate voltage of V_g , and the total charge provided equals Q_g . When operating under Zero-Voltage Switching (ZVS) conditions, Q_{GD} is provided by the load current, which reduces the total Q_g delivered by the gate supply and so reduces the driving losses. Fig. 2 shows a conventional gate-driver circuit.

For HF/VHF resonant converters switching at above 10 MHz, the required gating power of an advanced Si MOSFET can be higher than the total conduction loss [7]. To reduce the gate-driving loss, [9]–[11] describe several resonant gate drive techniques for PWM converters. The prevailing idea is using an inductor with an inductance value chosen to behave

Manuscript received August 09, 2018; revised November 06, 2018 and January 16, 2019; accepted January 28, 2019.

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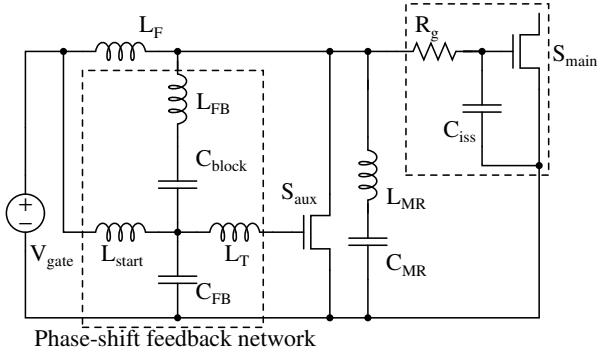


Fig. 3: Self-oscillating multi-resonant gate driver used in [6], [7]. The converter is enabled by applying V_{gate} , and disabled by setting V_{gate} to zero. The start-up time refers to the duration from when the dc voltage V_{gate} is applied to when a stable $V_{gs}(t)$, with the correct frequency and amplitude, is generated across the C_{iss} of the main active device S_{main} .

like a current source to losslessly charge and discharge the gate capacitance. The experimentally reported energy savings for driving the gate using these techniques are typically lower than 50%. [12] and reference within summarize some of the advantages and disadvantages of using resonant gate drive circuits in PWM converters.

In general, SiC MOSFET exhibit a smaller C_{iss} value than their Si counterpart at similar voltage and current rating. Due to the existence of near-interfacial oxide traps, the threshold-voltage V_{th} of SiC MOSFET may vary considerably when operating under different bias voltage, temperature conditions, and age [13]. Therefore, most of the manufacturer recommend driving a SiC MOSFET with a positive V_g of up to 20 V for reliable operation. This makes driving SiC MOSFET efficiently difficult at HF/VHF frequencies (3-300 MHz) [14]. On the other hand, GaN FET requires a much lower Q_g and V_g to operate compared with a Si and SiC MOSFET. Theoretically, GaN device can achieve about an order of magnitude reduction in conduction and switching losses when operating at high frequencies [15]. However, many commercially available GaN FETs come in small packages with little thermal mass, exposing the die to high temperature even when the power dissipation in the device is low. The on-state resistance $R_{DS,ON}$ of these devices can increase by a factor of two or three with higher junction temperature [16], which affects the performance of the converter. Therefore, resonant gate drive may be a viable design choice in HF/VHF converters using wide-bandgap (WBG) power devices [17].

Different from PWM converters, resonant converters are more sensitive to changes in switching frequency but less sensitive to duty cycle variations when operating under ZVS and zero dv/dt conditions. The duty cycle of the gate-driving clock in a series/parallel resonant converter and a class E² dc-dc converter is often close to 50% [1], [3], [18]. Class E amplifiers can also operate at any switch duty cycle other than 50% [19]–[21]. Due to the switching frequency sensitivity and to avoid complexity, several resonant gate driving techniques used in VHF converters are self-oscillating [6], [7], [18], [22]. A passive phase shift network is added between the drain and gate of a transistor to achieve conditions that result in self-sustained oscillation.

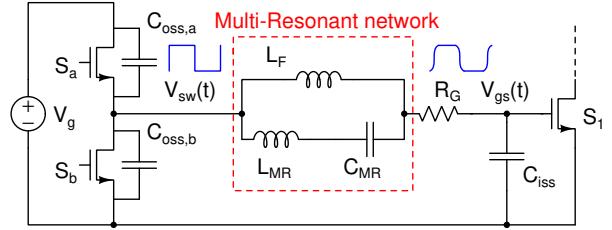


Fig. 4: Proposed multi-resonant gate drive.

Sinusoidal resonant gate drive circuits [7], [22], [23] are simple to design but lead to higher conduction losses in the main switching devices as the slow-rising gate signal may prevent the full enhancement of the MOSFET during significant portion of the switching cycle. [6] demonstrated a 100 MHz self-oscillating multi-resonant gate driver, which drives the main power MOSFET with a quasi-square wave $V_{gs}(t)$. Fig. 3 shows the circuit of this self-oscillating multi-resonant gate driver. The circuit uses a multi-resonant network to synthesize a quasi-square voltage waveform by summing the 1st and 3rd harmonic component with specific ratio. Effectively, this quasi-square wave $V_{gs}(t)$ resembles a trapezoidal shape with a faster rising and falling edge than the sinusoidal case. This self-resonant gate drive in [6] was able to recover 90% of the gate energy. However, a drawback of this gate drive circuit (oscillator) is that the start-up time is long. The long start-up time limits the regulation bandwidth of the converter and leads to overly sized filter capacitors at the input and output. Moreover, the design involves fine tuning of a multi-resonant phase-shift network to achieve a self-sustained oscillation. This repetitive tuning makes such self-oscillating resonant gate drive approach complicated and challenging to implement.

This paper presents the design of a multi-resonant gate driver which drives the main MOSFET with a quasi-square wave but not using self-oscillating typologies presented in [6], [7], [18], [22]. Fig. 4 shows the proposed the circuit. Consequently, the design procedure is greatly simplified and the long start-up time of a self-oscillating gate driver can be reduced. The proposed driver uses an auxiliary half-bridge circuit with a multi-resonant passive network to generate a quasi-square wave to drive the main MOSFET in an HF/VHF converter. This paper expands from our earlier conference publication [24] and presents extended theoretical analysis and experimental results.

The rest of the paper is organized as follows. Section II analyzes the power loss in a quasi-square wave resonant gate-driver circuit. A simple model is proposed to estimate the gate energy saving given the frequency, the gate capacitance, and the internal resistance. Section III discusses the design principles of the proposed circuit. Two Class-E power amplifiers with both conventional gate driver and the proposed resonant driver circuit are built to prove the concept. Section IV presents the simulation and experimental results. The prototype resonant gate driver can drive a Si trench MOSFET with a 20 MHz quasi-square wave $V_{gs}(t)$ and save 60% of the gating power without affecting the Class-E converter's drain efficiency and transient performance.

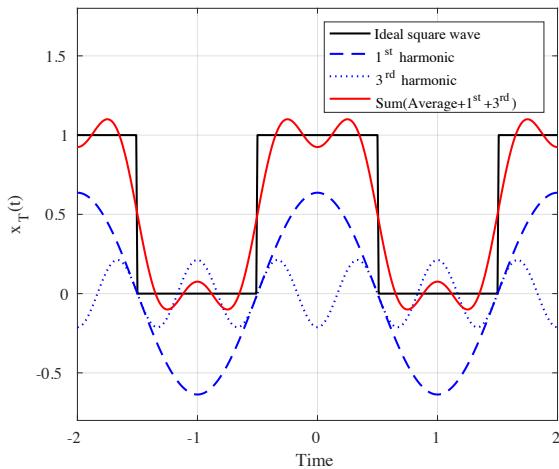


Fig. 5: A ideal 50% square wave and its 1st and 3rd harmonic components, the sum of its average, 1st and 3rd harmonics resembles a quasi-square wave.

The total efficiency including the gating loss increases from 81.5% to 84.5% compared with conventional gate driver. Section V demonstrates the advantages of the proposed gate driving technique over a conventional gate-drive circuit in the application of driving a SiC MOSFET at high frequencies above 10 MHz.

II. QUASI-SQUARE WAVE GATE DRIVING POWER

Fig. 2 shows a conventional gate-driver circuit, while Fig. 4 shows the proposed multi-resonant gate driver. Generally, the output of a conventional gate-driver consists of a half-bridge circuit. During the turn-on period, the gate-drive supply V_g delivers Q_g to the gate capacitance. The total energy provided is $V_g Q_g$, but only half of the energy $\frac{1}{2}V_g Q_g$ is stored in the capacitor [8]. The difference is dissipated on the resistive element R_g . When turning off, the previously stored energy $\frac{1}{2}V_g Q_g$ is also dissipated on R_g . Therefore, the average gate-driving power is

$$P_{\text{hard}} = f_s V_g Q_g. \quad (1)$$

R_g is the total resistance along the charging/discharging path including the resistance of S_a/S_b , internal gate resistance of the MOSFET, and any other parasitic resistance or damping resistance added externally. The actual $V_{gs}(t)$ would have exponential rising/falling edge, whose time constant is approximately $R_g C_{iss}$. Similar to other resonant gate driving techniques in [9]–[12], the proposed resonant gate driver circuit can reduce the gating loss through inductive charging/discharging and recycling part of the energy. The advantage of the proposed gate driver over other techniques is that the proposed circuit does not need extra auxiliary switches and accurate control of these switches other than a totem-pole circuit. The disadvantage is that the proposed circuit only works at a fixed frequency once designed.

Generally, the active devices in a resonant converter only conduct during half of the switching cycle. To synthesize a 50% square wave at certain frequency, we can use its harmonic components. From Fig. 5, we can see that the sum of the

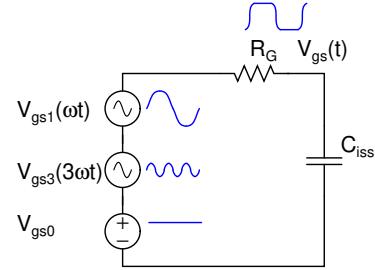


Fig. 6: Simplified circuit model for quasi-square wave gate driver. The gate voltage only consists of DC, 1st, and 3rd harmonic components.

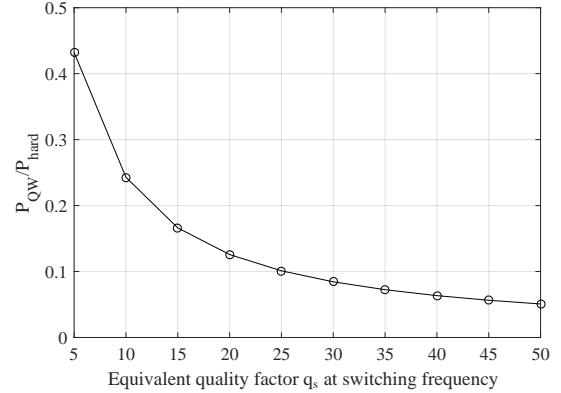


Fig. 7: Ratio of quasi-square gating power and hard gating power versus internal quality factor q_s of gate capacitance.

1st and 3rd harmonic components can resemble closely a 50% quasi-square wave. To calculate the power losses, Fig. 6 shows a simplified circuit model of the proposed resonant gate driver. Here we ignore the switching losses inside the gate-driver circuit, and assume that the internal gate resistance of the MOSFET dominates the total R_g . The gate voltage only consists of DC, 1st and 3rd harmonic components of the switching frequency. The DC component does not incur any losses. The total gate driving loss P_{QW} dissipated on R_g results from the currents at ω_S and $3\omega_S$ and can be calculated with

$$\begin{aligned} P_{\text{QW}} &= \frac{1}{2}R_g \times \left(\frac{V_g^2 A_1^2}{\left(\frac{1}{\omega_s C_{iss}}\right)^2 + R_g^2} + \frac{V_g^2 A_3^2}{\left(\frac{1}{3\omega_s C_{iss}}\right)^2 + R_g^2} \right) \\ &= \frac{V_g^2}{2R_g} \times \left(\frac{A_1^2}{q_s^2 + 1} + \frac{A_3^2}{\frac{1}{9}q_s^2 + 1} \right), \end{aligned} \quad (2)$$

where q_s is the equivalent quality factor of the series branch $R_g - C_{iss}$ at the switching frequency,

$$q_s = \frac{1}{\omega_s C_{iss} R_g}. \quad (3)$$

A_1 is the normalized Fourier series of the fundamental component of a square wave, and A_3 is the Fourier series of the 3rd harmonic component. If the duty cycle is 50%,

$$A_1 = \frac{2}{\pi}, \quad A_3 = \frac{2}{\pi} \times \frac{1}{3}, \quad (4)$$

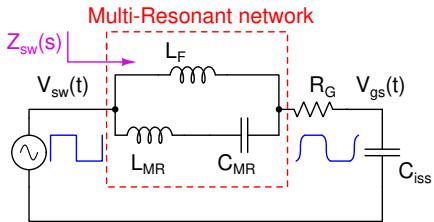
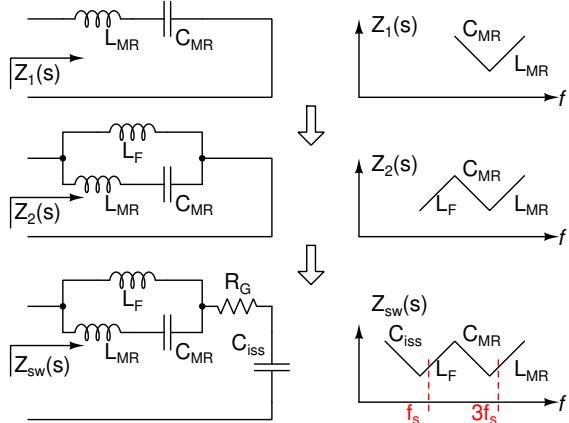


Fig. 8: Simplified circuit model of the proposed gate drive.

Fig. 9: Step-by-step derivation of $Z_{sw}(s)$. The impedance at f_s and $3f_s$ look inductive.

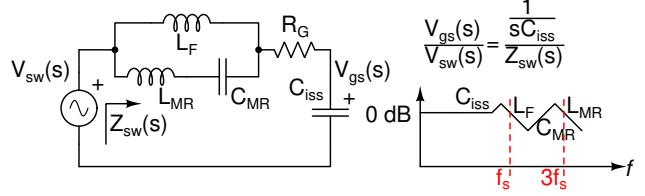
The ratio of quasi-square wave gate driving power P_{QW} over conventional hard-switching gate driving power P_{hard} is

$$\begin{aligned} \frac{P_{QW}}{P_{hard}} &= \frac{1}{2R_gC_{iss}f_s} \left(\frac{A_1^2}{q_s^2 + 1} + \frac{A_3^2}{\frac{1}{9}q_s^2 + 1} \right) \\ &= \pi q_s \left(\frac{A_1^2}{q_s^2 + 1} + \frac{A_3^2}{\frac{1}{9}q_s^2 + 1} \right). \end{aligned} \quad (5)$$

Without considering the switching losses and other energy dissipated to generate the control signal for the gate drive, this calculates the maximum energy that can be recovered by using a quasi-square wave gate driver. Fig. 7 shows this ratio, P_{QW}/P_{hard} , versus the internal quality factor q_s of the gate capacitance with detail numbers. For example, if a MOSFET's C_{iss} is 400 pF, internal $R_g = 1 \Omega$, $V_g = 10$ V, $f_s = 20$ MHz, the quality factor $q_s = 20$, then the gating power using a quasi-square wave driver is 12.5% of the conventional driver case. In other words, 87.5% of the gate driving loss can potentially be saved.

III. DESIGN METHODOLOGY

In the proposed multi-resonant gate drive in Fig. 4, the half bridge consisting of S_a and S_b generates an ideal square $V_{sw}(t)$. The multi-resonant network consisting of L_F , L_{MR} , and C_{MR} only allows the 1st and 3rd harmonic components pass through and reach C_{iss} . With the appropriate ratio of the 1st and 3rd harmonic components, the rising and falling edge of $V_{gs}(t)$ can be adjusted. Thus, the transfer function of $V_{gs}(s)/V_{sw}(s)$ determines the shape of $V_{gs}(t)$. To operate the proposed gate drive circuit efficiently, the design principles of are:

Fig. 10: Frequency response of the multi-resonant gate drive. The gain at f_s and $3f_s$ are the same or similar.

1) The gate drive FETs S_a and S_b should operate with ZVS to minimize the switching losses due to the parasitic capacitance $C_{oss,a}$ and $C_{oss,b}$ in the half-bridge circuit, therefore the input impedance of this multi-resonant network $Z_{sw}(s)$ should be inductive at the switching frequency f_s ;

2) To shape a quasi-square wave $V_{gs}(t)$ across C_{iss} , the amplitudes of 1st and 3rd harmonic components, $v_{gs1}(t)$ and $v_{gs3}(t)$, should have a ratio of 3:1. Also, the phase of $v_{gs1}(t)$ and $v_{gs3}(t)$ should be the same. As $V_{sw}(t)$ is already a 50% square wave, its 1st and 3rd harmonic components satisfy this requirement. When passing $v_{sw1}(t)$ and $v_{sw3}(t)$ to C_{iss} , this multi-resonant filter should maintain the original amplitude ratio and relative phase. Therefore, it should have a gain of the same magnitude at f_s and $3f_s$, which is,

$$\left| \frac{V_{gs}(j\omega_s)}{V_{sw}(j\omega_s)} \right| \simeq \left| \frac{V_{gs}(j3\omega_s)}{V_{sw}(j3\omega_s)} \right|; \quad (6)$$

3) Define ϕ_1 as the phase shift at f_s , and ϕ_3 as the phase shift at $3f_s$,

$$\phi_1 = \angle \frac{V_{gs}(j\omega_s)}{V_{sw}(j\omega_s)}, \quad \phi_3 = \angle \frac{V_{gs}(j3\omega_s)}{V_{sw}(j3\omega_s)}. \quad (7)$$

Both ϕ_1 and ϕ_3 are within $-\pi$ and $+\pi$. To maintain the same relative phase of 1st and 3rd harmonic components after the multi-resonant network, they should satisfy the relationship of

$$\phi_1 = \frac{\phi_3 + 2k\pi}{3}, k = 0, \pm 1. \quad (8)$$

Fig. 8 shows a simplified circuit model to analyze the gain and phase. An ideal square voltage $V_{sw}(t)$ drives a multi-resonant circuit, and the voltage across C_{iss} is $V_{gs}(t)$. The impedance presented at the switch node $Z_{sw}(s)$ should be inductive at f_s and $3f_s$ to ensure ZVS operation of S_a and S_b . Fig. 9 shows a step-by-step derivation of this impedance $Z_{sw}(s)$ presented to the half bridge circuit. Fig. 10 shows a symbolic frequency response of the voltage gain $V_{gs}(s)/V_{sw}(s)$ of the circuit. The ideal square wave $V_{sw}(t)$ has a swing of 0-to- V_g . The gain $V_{gs}(s)/V_{sw}(s)$ at f_s and $3f_s$ can be set as 0 dB if the same 0-to- V_g swing is desired on the $V_{gs}(t)$. It can also be above 0 dB if a negative voltage is preferred to drive the gate. For example, $V_{sw}(t)$ can be 0-to-10 V, while the $V_{gs}(t)$ can be -5-to+15 V. In this case, the gain at f_s and $3f_s$ is 20 V:10 V = 2, which is 6 dB. The average value of $V_{sw}(t)$ and $V_{gs}(t)$ are both 5 V, and this cannot be changed.

From Fig. 9 and 10, we can see that L_F and C_{iss} roughly resonate at f_s , while L_{MR} and C_{MR} resonate close to $3f_s$.

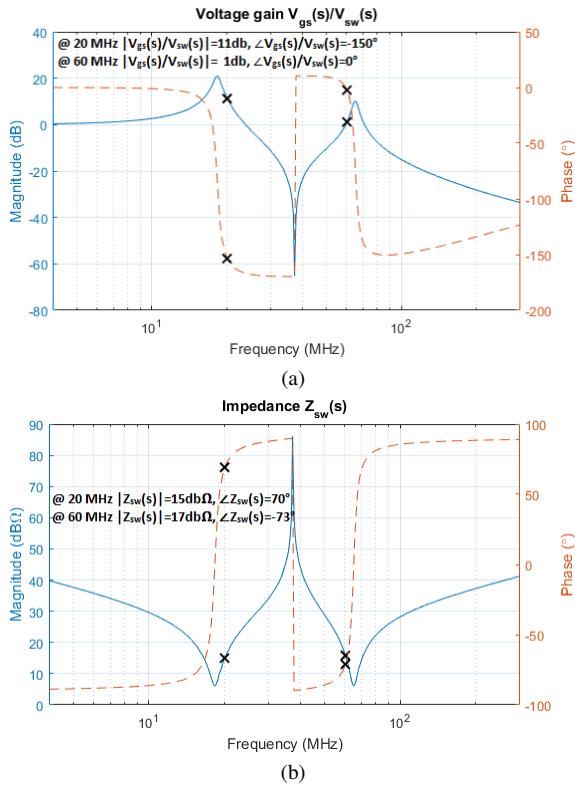


Fig. 11: LTSpice ac simulation, $C_{iss} = 390 \text{ pF}$, $C_{MR} = 68 \text{ pF}$, $L_F = 163 \text{ nH}$, $L_{MR} = 104 \text{ nH}$. (a) the gain of $V_{gs}(s)/V_{sw}(s)$. (b) the impedance of $Z_{sw}(s)$.

Therefore, the initial values of L_F , L_{MR} , and C_{MR} can be calculated by

$$L_F = \frac{1}{(2\pi f_s)^2 C_{iss}}, \quad L_{MR} = \frac{1}{(2\pi \cdot 3f_s)^2 C_{MR}}, \quad (9)$$

where C_{MR} is a design parameter that can be chosen by the reader. Typically, $C_{MR} = \frac{1}{5}C_{iss}$ is a reasonable starting value. Notice that the values obtained using (9) do not meet all the tuning guidelines, and further tuning is required to achieve an ideal quasi-square wave $V_{gs}(t)$ and ZVS operation of S_a and S_b . The specific values depend on the parasitic parameters present in the circuit.

Following the principles above, a prototype multi-resonant gate drive to generate a 0-10 V 20 MHz quasi-square wave is designed and presented below as an example. The Si MOSFET in the primary power circuit is FDMC86248 from ON Semiconductor [25]. The C_{iss} is 390 pF and R_g is 0.8 Ω. C_{MR} can be chosen as 68 pF. Then,

$$L_F = \frac{1}{(2\pi \times 20 \text{ MHz})^2 \times 390 \text{ pF}} = 163 \text{ nH}, \quad (10)$$

$$L_{MR} = \frac{1}{(2\pi \times 3 \times 20 \text{ MHz})^2 \times 68 \text{ pF}} = 104 \text{ nH}.$$

Fig. 11 shows the gain and impedance of the resonant gate drive. It is simulated in LTSpice and using these values calculated above. The input impedance $Z_{sw}(s)$ is inductive at 20 MHz, while capacitive at 60 MHz. After tuning the inductance values, $L_F = 223 \text{ nH}$, $L_{MR} = 150 \text{ nH}$, Fig. 12 shows the updated gain and impedance plot. $Z_{sw}(s)$ is now inductive at both 20 MHz and 60 MHz. The gain $V_{gs}(s)/V_{sw}(s)$ at 20 MHz

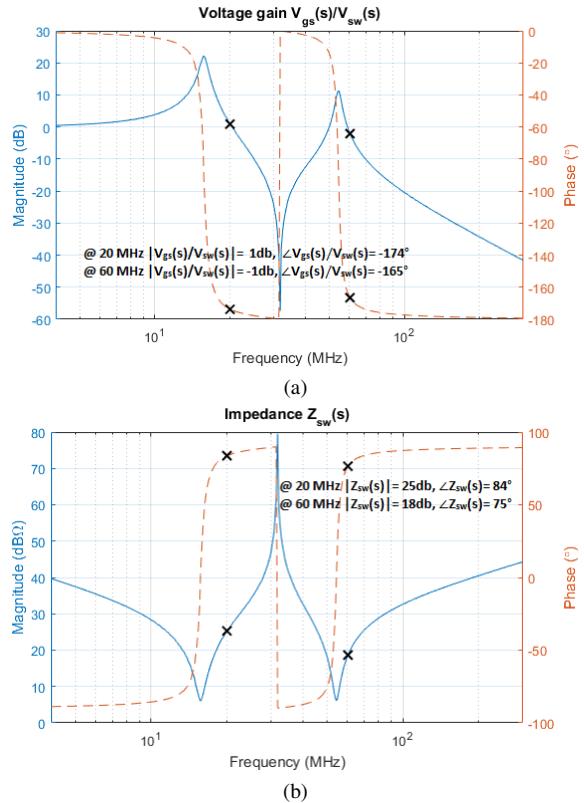


Fig. 12: LTSpice ac simulation, $C_{iss} = 390 \text{ pF}$, $C_{MR} = 68 \text{ pF}$, $L_F = 223 \text{ nH}$, $L_{MR} = 150 \text{ nH}$. (a) the gain of $V_{gs}(s)/V_{sw}(s)$. (b) the impedance of $Z_{sw}(s)$.

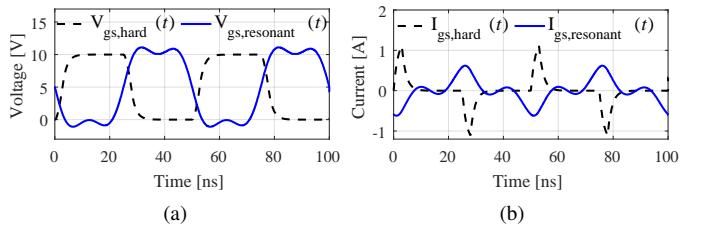


Fig. 13: LTSpice transient simulation waveform. (a) the gate voltage, (b) the current of gate drive supply.

and 60 MHz are both around 0 dB. ϕ_1 is -174° , ϕ_3 is -165° . Refer to the design principle 3, $(-165^\circ - 360^\circ)/3 = -175^\circ$. ϕ_1 is close to this value.

Fig. 13 shows the time-domain waveform in LTSpice simulation for both conventional and proposed resonant gate drive. The charging/discharging current supplied by V_g is smaller in the proposed resonant gate driver compared to hard gating case. R_g is set as 2 Ω, which includes 0.8 Ω internal gate resistance of FDMC86248 and the output resistance from S_a and S_b . It can be seen that the rising/falling time are similar in both cases. The loss in proposed resonant gate driver is 180 mW while in the conventional driver reaches 780 mW.

IV. EXPERIMENTAL RESULTS OF SI MOSFET

To experimentally verify the energy saving of the proposed resonant gate driver in VHF converters, two 20 MHz 32 W

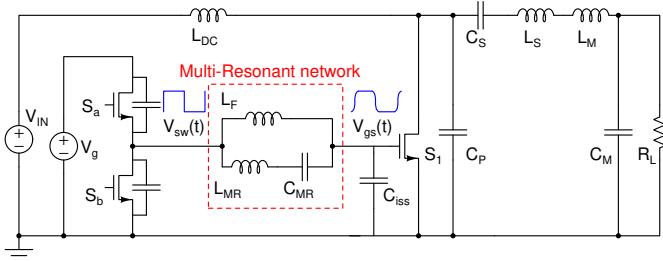


Fig. 14: Class-E RF amplifier with proposed resonant gate drive, L_M and C_M is a low-pass matching network, $R_L = 50 \Omega$.

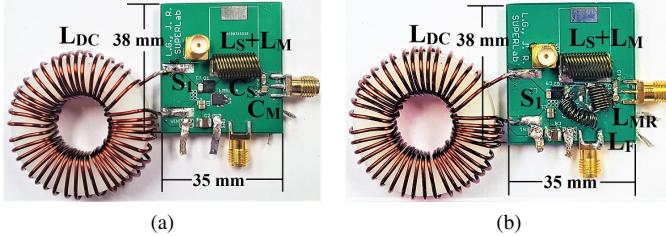


Fig. 15: Photographs of Class-E converters. (a) Hard gating; (b) Resonant gating.

Class-E RF amplifiers with the same components are built. One amplifier is driven by conventional hard-switching gate drive, while the other uses the multi-resonant gate drive designed above. Fig. 14 shows the circuit. Table I lists the key components of the Class-E power amplifier and the resonant gate driver. Due to the non-linearity of the C_{iss} , the values of L_{MR} and L_F are slightly different from the values used in the transient simulation with ideal C_{iss} in Fig. 12. Fig. 15 shows the photographs of the converters.

Fig. 16 shows the measured gate-to-source voltage waveform $V_{gs}(t)$ when the 24 Vdc input is disconnected. The measured $V_{gs}(t)$ in Fig. 16 is trapezoidal and similar to the quasi-square wave in Fig. 5 and Fig. 13.

With the Class-E amplifier operating, Fig. 17 captures the measured drain-to-source voltage $V_{ds}(t)$, gate-to-source voltage $V_{gs}(t)$, and the output voltage $V_{RL}(t)$ across the load. In both hard gating and resonant gating cases, S_1 is operating with ZVS and zero dv/dt condition. The slower falling edge of $V_{gs}(t)$ in the resonant gating shown in Fig. 17b is due to the feedback of the drain voltage through the C_{gd} . Table II summarize the measured efficiency η of the two Class-E amplifiers.

The proposed resonant gate drive can increase the total efficiency from 81.5% to 84.5% and saves the gating power by 60%. Furthermore, when the gate drive IC LM5114 is loaded open circuit, it consumes 850 mW to drive the parasitic capacitance inside the driver IC. That is more than the total resonant gating power with the Class E amplifier operating in the prototype. This proves that the inductive impedance makes S_a and S_b inside the gate drive IC operate with ZVS.

Fig. 18 shows the transient of the prototype converters. As predicted, the proposed resonant gate drive reduces the long start-up time in the self-oscillating resonant gate driver in [6]. The Class-E amplifier with the proposed resonant gate driver

TABLE I: Key components of the Class-E amplifier and resonant gate driver.

Part	Description
R_L	50 Ω RF attenuator
L_{DC}	3.3 uH, Toroid, AWG 18, 41 turns
L_F	181 nH, Coilcraft 132-14SMGL
L_{MR}	160 nH, Coilcraft 2222SQ-161
L_{S+LM}	500 nH, Coilcraft 2929SQ-501
C_{MR}	68 pF, 250 V C0G Ceramic, 251R15S680JV4S
C_P	43 pF, 250 V C0G Ceramic, 251R15S430JV4S
C_S	220 pF, 250 V C0G Ceramic, 251R15S221JV4S
C_M	400 pF, 250 V C0G Ceramic, 180 pF (251R15S181JV4S) and 220 pF (251R15S221JV4S)
S_1	FDMC86248 On Semi., 150 V Si Trench MOSFET
$S_{a,b}$	LM5114, Texas Instruments gate drive IC

TABLE II: Experimental results of prototype amplifiers using Si MOSFETs.

	Hard gating	Resonant gating
V_g	10 V	10 V
V_{in}	24 V	24 V
I_{in}	1.56 A	1.53 A
V_{RL}	40.02 V _{rms}	39.78 V _{rms}
R_L	50 Ω	50 Ω
η w/o gating loss	85.6%	86.1%
Gating loss	1.8 W	720 mW
η with gating loss	81.5%	84.5%

reaches steady state within 12 switching cycles, similar to the hard gating case.

V. MULTI-RESONANT GATE DRIVER OF SiC MOSFET

One of the advantages of WBG devices over Si MOSFETs is the much lower C_{iss} input capacitance required to charge the gate. Table III compares several sample Si, GaN, and SiC devices with similar $R_{DS,ON}$. However, since the gate energy scales with V_g^2 , the much higher enhancement voltages greatly worsens the gating loss for SiC devices. From Table III, we can see that SiC MOSFETs can have higher gating loss than both Si and GaN devices at high frequencies. Another challenge of driving SiC MOSFETs at HF/VHF frequencies is that currently, very few commercial gate drivers can operate with supply voltages above 15 V and output signals that have fast rise and fall time transitions (≤ 4 ns). To resolve these challenges, we can apply the same multi-resonant circuit to drive a SiC MOSFET, in order to partially recycle the energy transmitted from the gate driver to the C_{iss} , as well as to provide a large gate voltage that commercial gate drive ICs cannot provide.

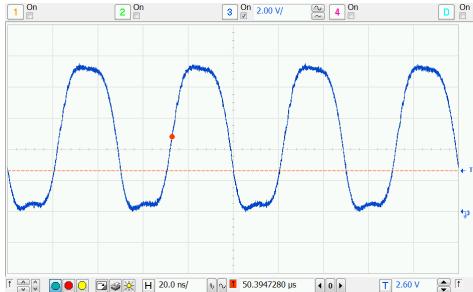
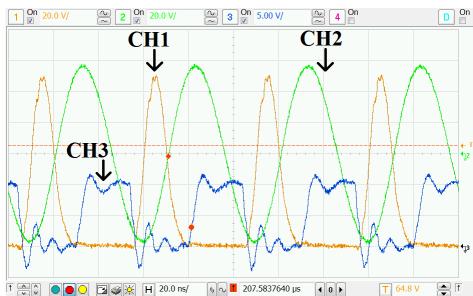
To drive the SiC MOSFET with a large positive voltage and a negative valley voltage, we set the gain at the first and third harmonics of $V_{gs}(s)/V_{sw}(s)$ to be greater than unity, which is different from the Si example in Section III. With certain target of gain, Equations (11) and (12) can approximately calculate the initial values of the resonant components L_F , L_{MR} , and C_{MR} .

$$\left| \frac{V_g(j\omega_s)}{V_{sw}(j\omega_s)} \right| \approx \frac{\omega_0^2}{\sqrt{(\omega_0^2 - \omega_s^2)^2 + (\frac{\omega_s R_g}{L_F})^2}} \quad (11)$$

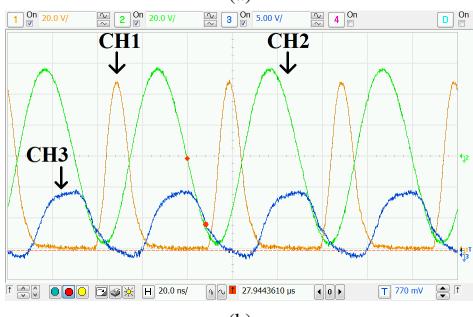
$$\omega_0 = \frac{1}{\sqrt{L_F C_{iss}}}.$$

TABLE III: Comparison of different power devices with similar $R_{DS,ON}$.

Device	Manufacturer	Material	$V_{DS,max}$	$R_{DS,ON}$	$V_{g,max}$	$C_{iss}@1\text{ MHz}$	Calculated Gating Loss		
							13.56 MHz	27.12 MHz	40.68 MHz
R6015KNJTL	Rohm Semiconductor	Si	600 V	290 mΩ	10 V	1050 pF	1.42 W	2.85 W	4.27 W
GE1700903A1	General Electric	SiC	1700 V	360 mΩ	20 V	400 pF	1.63 W	3.25 W	4.88 W
C3M0280090J	Cree/Wolfspeed	SiC	900 V	280 mΩ	15 V	150 pF	0.46 W	0.92 W	1.37 W
GS66502B	GaN Systems	GaN	650 V	220 mΩ	7 V	50 pF	0.033 W	0.066 W	0.1 W

Fig. 16: $V_{gs}(t)$, DC input V_{in} is disconnected.

(a)



(b)

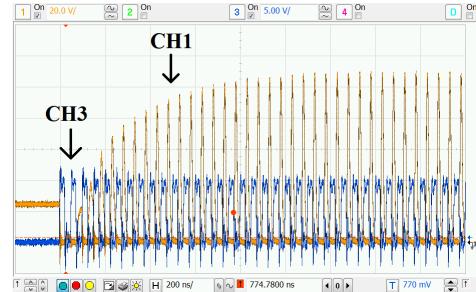
Fig. 17: Experimentally measured waveform. CH1- $V_{ds}(t)$, CH2- $V_{RL}(t)$, CH3- $V_{gs}(t)$. (a) Class-E with hard gating; (b) Class-E with resonant gating.

Generally, Equation (11) gives 2 possible solutions for L_F . We select the larger solution because this allows $Z_{sw}(s)$ to have an inductive impedance at f_s .

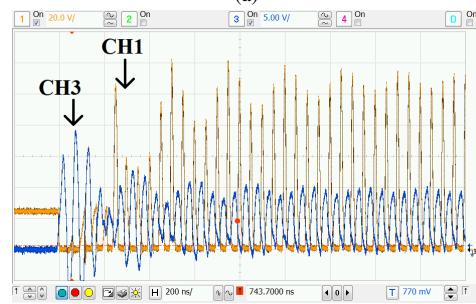
$$\left| \frac{V_g(j3\omega_s)}{V_{sw}(j3\omega_s)} \right| \approx \frac{\omega_1^2}{\sqrt{(\omega_2^2 - (3\omega_s)^2)^2 + (\frac{3\omega_s R_g}{L_{MR}})^2}}, \quad (12)$$

$$\omega_1 = \frac{1}{\sqrt{L_{MR} C_{iss}}}, \quad \omega_2 = \frac{1}{\sqrt{L_{MR} C_{MR}}}.$$

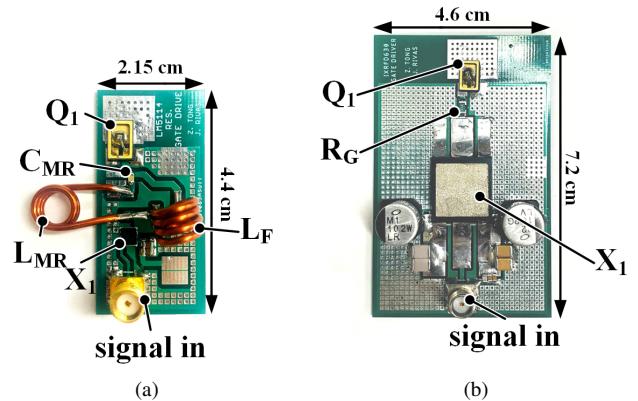
Equation (12), which computes an approximate transfer function at $3f_s$, gives a relationship between C_{MR} and L_{MR} based upon the desired 3rd harmonic gain. Similar to the design procedure in Section III, an initial value of C_{MR} can be $C_{iss}/5$ and L_{MR} can be solved using Equation (12).



(a)



(b)

Fig. 18: Start-up transient, CH1- $V_{ds}(t)$, CH3- $V_{gs}(t)$. The multi-resonant gate drive takes 12 switching cycles to reach steady state, which is similar as the hard gating case. (a) Class-E with hard gating; (b) Class-E with resonant gating.

(a)

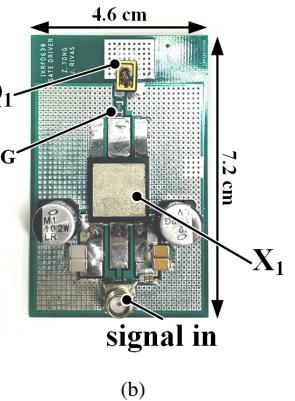
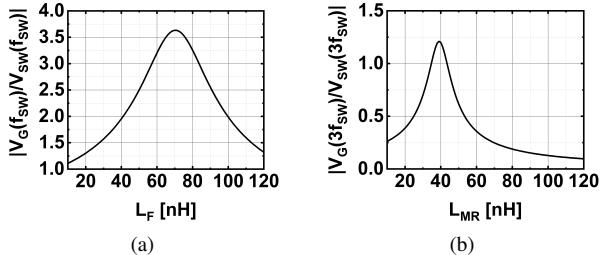


Fig. 19: Photograph of the two prototype gate drivers of a SiC MOSFET. (a) The proposed multi-resonant gate driver, components listed in Table IV. (b) A conventional hard-switching gate driver IXRFD630.

As an example, we demonstrate the multi-resonant gate driver at 30 MHz for a 1700 V rated GE1700903A1 SiC MOSFET from General Electric. We model the gate as a RC tank with $R_g=3.65\Omega$ and $C_{iss}=400\text{ pF}$, which are measured values using Agilent E5061B network analyzer. We also select a LM5114 gate driver IC to serve as the totem pole of the resonant gate driver. We supply the LM5114's V_{DD} with 11 V,

TABLE IV: Key components of the resonant gate driver for SiC MOSFET.

Parameter	Value
f_s	30 MHz
Q_1	GE1700903A1
R_g of Q_1	3.65 Ω at 1 MHz
C_{iss} of Q_1	400 pF, measured at 30 MHz
X_1	LM5114, Texas Instruments gate drive IC
L_F	73 nH
L_{MR}	38 nH
C_{MR}	82 pF

Fig. 20: Multi-resonant network gain $V_{gs}(s)/V_{sw}(s)$ vs different L_F and L_{MR} values. (a) First harmonic gain versus L_F plotted Equation (11), (b) Third harmonic gain versus L_{MR} plotted Equation (12), with $L_F=100$ nH and $C_{MR}=80$ pF.

and aim to achieve a gate voltage with an 18 to 20 V peak in order to fully enhance the SiC FET. Thus, our targeted gain is between 1.6 to 1.7 (4.1 to 4.6 dB). With Equation (11), we plotted the relationship between the first harmonic gain and L_F in Fig. 20a. Therefore, initial value for L_F is selected as 100 nH to get a gain around 2. Initial value for C_{MR} is selected as 80 pF ($C_{iss}/5$). Then using Equation (12), we plot the third harmonic gain versus L_{MR} value in Fig. 20b, and select L_{MR} to be 40 nH to achieve the largest third harmonic gain.

Fig. 21a shows the simulated transient waveform as well as the small-signal input impedance and gain from the initial values of L_{MR} , C_{MR} , and L_F . With the selected initial values, the first harmonic gain and phase are slightly lower than the targeted values. Both issues can be resolved by lowering the value of L_F , leading to a final value of 75 nH. With the adjusted values, Fig. 21b displays the updated simulation waveform and Fig. 21c displays the measured results using the prototype circuit in Fig. 19a. During the prototyping, before testing the transient performance, we recommend to match the small-signal impedance and voltage gain measurements using a network analyzer with simulation results, like we displayed in Fig. 21. Detuning of the resonance point could cause instantaneous over-voltage across the gate-to-source port which may potentially damage the active device.

Additionally, we compare the gating power between the multi-resonant gate drive with a conventional hard-switching gate drive. For the hard-switching gate drive, we select an IXRFD630 gate driver IC from IXYS, capable of operating up to 30 V with 4 ns rise and fall times. Fig. 19b shows the prototype where we supplied 20 V on the gate driver V_{DD} to drive the GE1700903A1. Table V compares the gating losses between the hard-switching driver IXRFD630 and the resonant gate driver.

From Table V, compared to the hard-switching IXYS gate driver, resonant gating experimentally reduces the gate power

TABLE V: Comparison between hard-switched and resonant gate drivers for SiC MOSFET.

Parameter	Hard-Switching	Resonant
Gate supply V_{DD}	20 V	11 V
Gate supply current	1.82 A	0.51 A
P_{gate}	36.3 W	5.6 W
P_{gate} (Equations 1 and 2)	3.6 W	1.9 W

dissipation by five times. For the resonant gate driver, the additional power dissipation is due to the extra resistances of the totem-pole switches not included in the R_g and the extra losses generated by the other digital circuits inside the IC. For the hard-switching gate driver, the losses in the experiment are over 10 times the calculated losses. This is due to the non-idealities in the IXRFD630 gate driver IC. From the manufacturer's datasheet [26], the gate drive IC draws 2.6 A of current at 30 MHz when C_L equals 1 nF and the supply voltage is 15 V. In addition to saving considerable amounts of power, the resonant gate drive provides faster rise and fall transition times as shown in Fig. 22, with a slew rate of 2.5 V/ns while the IXYS gate driver has a slew of 1.8 V/ns.

Lastly, we demonstrate the operation of our gate driver in a Class-E converter switching at 30 MHz. Similar to the Si example, Fig. 14 illustrates the entire schematic. Fig. 23b displays the steady-state V_{ds} , V_{gs} , and V_{out} waveform. The measured V_{ds} waveform match closely with the simulation. Table VI lists the values of the components. With an DC input voltage of 60 V, the inverter delivers 44.2 W output power to a $12.5\ \Omega$ RF load with a drain efficiency of 85.7%.

TABLE VI: Components of the SiC Class-E amplifier and resonant gate driver.

Part	Description
R_L	12.5 Ω RF dummy load
L_{DC}	1.38 uH, Q factor 140, AWG 18, 34 turns
L_S	320 nH, Q factor 138.6, AWG 18, 15 turns
L_F	75 nH, Solenoid
L_{MR}	40 nH, Solenoid
C_P	N/A
C_{in}	100 uF, 200 V Electrolytic
C_S	230 pF, 500 V COG Ceramic
C_{MR}	80 pF, 100 V COG Ceramic
S_1	GE1700903A1, General Electric, 1700 V rated SiC MOSFET
$S_{a,b}$	LM5114, Texas Instruments, gate drive IC
L_M	short
C_M	open

VI. CONCLUSION

This paper presents the design of a simple multi-resonant gate drive for HF/VHF converters. It drives the gate of a MOSFET with a trapezoidal quasi-square wave voltage. The design procedure is greatly simplified compared to some of the self-oscillating multi-resonant gate drivers presented in previous works [6], [7], [18], [22]. We analyze the majority of the conduction loss in this quasi-square wave resonant gate driver and propose a simple model to estimate the energy saving given the internal quality factor of gate capacitance. The proposed circuit can reduce the long start-up time of some self-oscillating gate drivers demonstrated in previous works. Compared with a conventional hard-switching gate driver, a

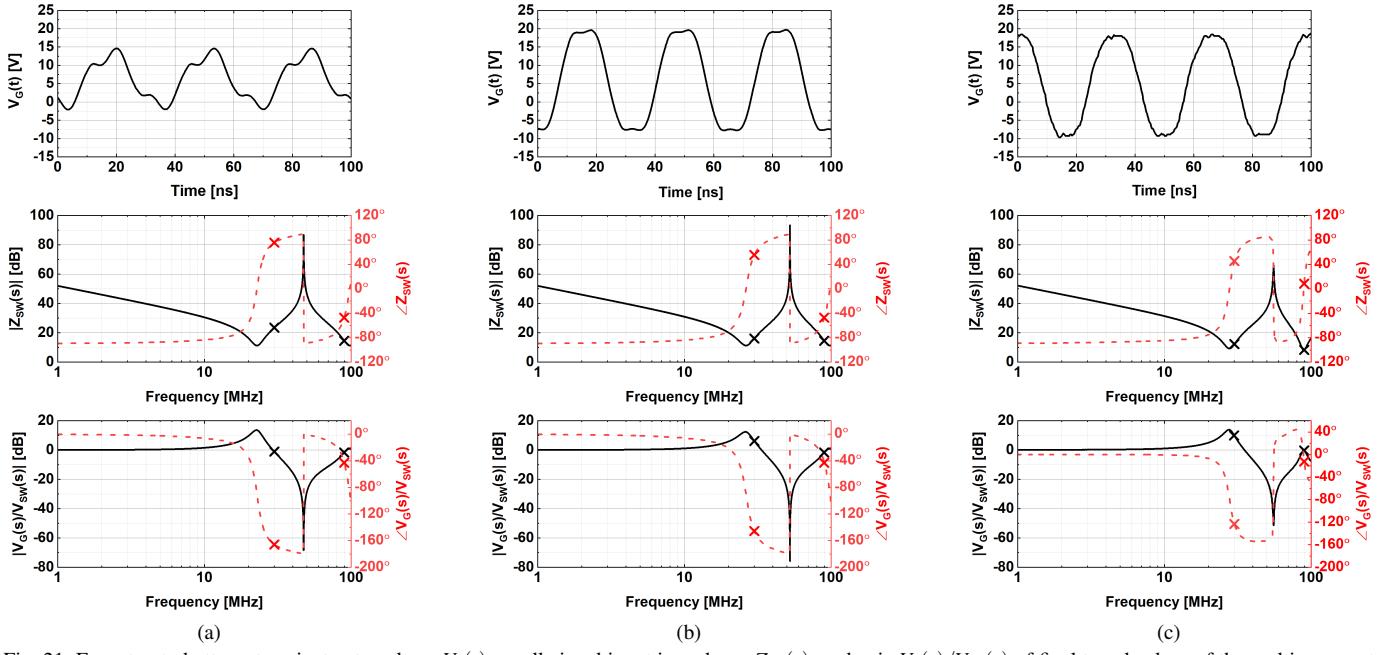


Fig. 21: From top to bottom: transient gate voltage $V_g(t)$, small-signal input impedance $Z_{sw}(s)$, and gain $V_g(s)/V_{sw}(s)$ of final tuned values of the multi-resonant gate driver from (a) initial tuning in simulation, (b) final adjusted tuning in simulation, (c) experimental measurement of the circuit shown in Fig. 19a.

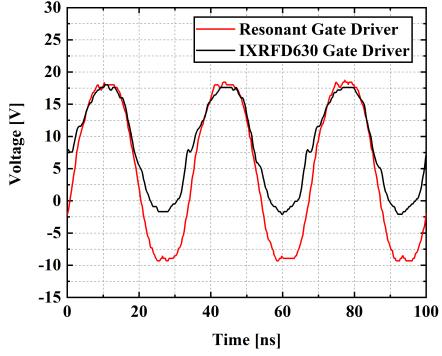


Fig. 22: A comparison of the gate signals provided by the resonant gate driver in red and the hard-switching gate driver in black.

prototype resonant driver saves 60% of the gating power in a 20 MHz Class E amplifier using a Si MOSFET without affecting the transient and drain efficiency. We also demonstrate the effectiveness of this multi-resonant gate driver circuit on a high-voltage SiC MOSFET at a frequency of 30 MHz. With the proposed technique, we were able to drive a high-voltage SiC MOSFET with a slew-rate of 2.5 V/ns at the gate, while an integrated hard-switching gate driver can only generate a 1.8 V/ns slew-rate and is 5 times less efficient than the proposed resonant gate driver. To authors' knowledge, this is the fastest frequency that any high-voltage SiC MOSFET has been operating with. No commercially-available gate drivers are capable of driving SiC MOSFETs efficiently at 30 MHz. The proposed resonant gate driving technique addresses a key challenge of operating a SiC MOSFET efficiently at MHz frequency range.

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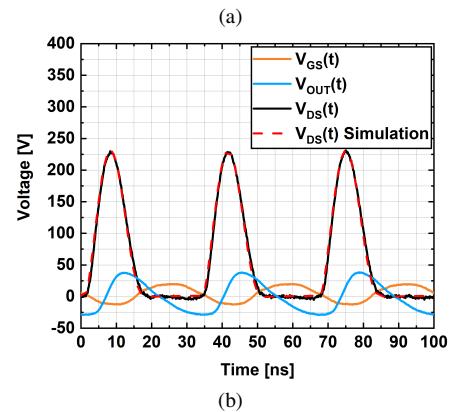
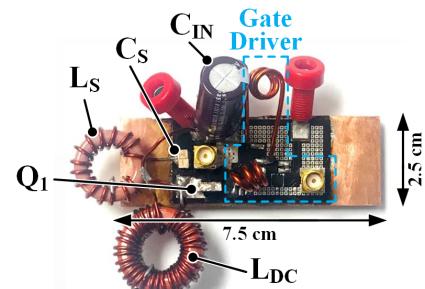
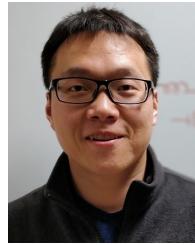


Fig. 23: (a) Photograph of the prototype class-E resonant converter using a flip-IC packaged MOSFET and a copper heat sink. (b) Drain, gate, and output waveforms of the Class-E inverter.

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