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High-Frequency Bidirectional Resonant Converter for High Conversion Ratio and Variable Load Operation

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***Abstract*—Applying RF circuit design techniques to dc-dc resonant converters has enabled switching frequencies well beyond 10 MHz, leading to higher power densities and faster transient response. Synchronous rectification is advantageous for low-voltage high-power applications but is challenging to implement in a high-frequency dc-dc converter. This paper proposes an HF/VHF resonant converter structure in which the rectifier and the inverter switches can be driven with the same gate signal. The presented structure enables efficient bidirectional power delivery in the HF/VHF range for applications that require a large voltage conversion ratio. A 64 MHz, 12 W, 36 V-to-12 V prototype converter verifies the operation of the structure. This paper further explores an interleaved architecture of the same circuit to improve efficiency and transient performance. Lastly, a 13.56 MHz 210 V-to-30 V prototype converter with 90 % peak efficiency at 200 W demonstrates the advantages of the interleaved architecture.**

I. Introduction

A means of improving power density, transient response, and realizing a higher level of integration of state-of-art power converters is to increase the switching frequency [1]. Resonant power converters can reduce switching losses and absorb and utilize some of the component parasitics. Fig. 1 shows a basic structure of a resonant dc-dc converter, which consists of an inverter, a transformation stage, and a rectifier. For a converter operating in the High Frequency (HF) / Very High Frequency (VHF) range (3∼300 MHz), RF power amplifiers, like the Current-Mode Class D, Class E, F, and EF or EF^{-1} [2]–[9], are preferred. These amplifiers (inverters) can operate with zero-voltage switching (ZVS) or zero-current switching (ZCS) and have a single ground-referenced switch that is simple to drive. Previous work has demonstrated successful dc-dc power conversion at switching frequencies greater than 10 MHz, and even beyond 100 MHz [10]–[15]. These works demonstrated the expected benefits of VHF power conversion, such as drastically reduced passive component size, higher power density, increased loop-gain bandwidth, and improved load transient. Ref. [16] summarizes the component stress factors, control/regulation techniques, and gate driver designs for typical VHF power conversion circuits. Detailed design considerations of HF/VHF dc-dc converters are discussed in [17]. Along this same path, efforts to further improve the performance, such as reducing component counts, transformer synthesis, and integrated transistor optimization have been demonstrated in [18]–[21].

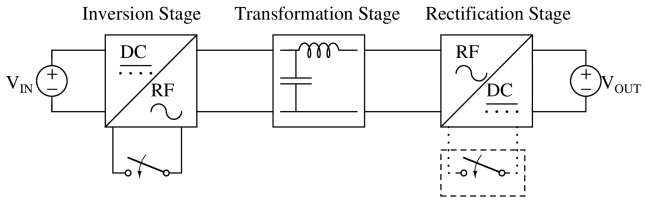

Fig. 1: Structure of a HF/VHF resonant dc−dc converter

In addition to the work mentioned above, synchronous rectification is also a key topic for the design of radio frequency dc-dc power conversion. In these HF/VHF converters, Schottky diodes are typically used in the rectifier stage. Synchronous rectification can reduce the diode conduction loss under large current conditions [22], [23]. Self-gating-based synchronous rectifiers have been demonstrated in low-power and low-voltage HF/VHF dc-dc power converters in [24], [25]. Another method of introducing a fixed time delay for the rectifier gating signal has also been demonstrated in a higher power and higher voltage bidirectional converter [26].

One feature of this type of HF/VHF converter is that the dc-dc gain varies significantly with load [27]. Mainly, this is because the gain of the transformation stage (i.e. a narrow-band matching network) is generally dependent on the load. On the other hand, the design of a conventional Class E or higher order tuned Class E amplifier variations relies on the loading impedance to achieve ZVS [3], [6], [8]. As a result, the ZVS operation cannot be maintained when the load varies more than two times.

In this paper, we focus on the challenge of designing an efficient bidirectional converter operating at 3-300 MHz. We present an HF/VHF resonant topology with synchronous rectification that is capable of maintaining a constant dc-dc gain across a wide load range. The circuit utilizes a symmetric bandpass matching network for voltage conversion, which maintains zero phase shift between the inverter and rectifier. As a result, the rectifier switch can be driven by the same gate signal as the inverter switch across a wide range of operation.

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This greatly reduces the difficulty of accurately adjusting the timing of the gating signal for the synchronous switch under different load conditions at high frequencies. Both the inverter and rectifier are designed to maintain ZVS operation across a wide load range. To allow design flexibility, they do not operate with zero dv/dt turn-on as usually demonstrated in a conventional Class E amplifier design. This paper compiles the methods outlined in earlier conference publications [28]–[30] and presents an extended theoretical analysis that includes experimental results.

The rest of this paper is organized as follows. Section II explains the basic operating principles of the proposed HF/VHF converter architecture with a single-phase circuit example. Section III presents the experimental results of a single-phase, 64 MHz, 36 V-to-12 V prototype designed using the principles above. Improving on these results, Section IV shows that interleaving operation and a series-stacked structure can further reduce the component count and allow the use of low-voltage semiconductor devices. With these techniques, we can further improve the transient response, efficiency, and power density performance of HF/VHF converters. A 13.56 MHz, 200 W, 210 V-to-30 V bidirectional push-pull prototype is built to demonstrate the performance improvements using the interleaving technique, with the experimental results in Section V. Section VI concludes the paper.

II. Converter Operation

As shown in Fig. 1, a resonant DC-DC converter operating at 3-300 MHz generally consists of three parts: an inverter, an impedance transformation stage, and a rectifier. Soft-switching PWM converters using monolithic modules in a normally-Off GaN process can also achieve very efficient power conversion for envelope tracking applications [31]. In Fig. 1, the inverter generates an RF voltage/current signal at a switching frequency f_s, while the resonant rectifier converts the RF energy back to DC. In resonant converters, most of the power is delivered at the fundamental frequency [32] and the harmonic components deliver a negligible amount of energy to the load. The transformation stage sets the gain, matches the impedance to deliver the desired amount of power, and may adjust the phase between the ac voltage and current to achieve ZVS/ZCS [17]. In a converter operating at frequencies below ~1 MHz, a transformer is typically used to provide a large gain [33], [34]. To set the conversion ratio at higher switching frequencies (e.g., above 10 MHz), a narrowband matching network is preferred due to the limited availability of suitable core materials [35], [36].

Fig. 2a shows the structure of the HF/VHF converter family that is the focus of this paper, consisting of a ZVS inverter, a bandpass matching network, and a ZVS rectifier. Fig. 2b shows the example converter schematic. We select a Φ_2 circuit for both the inverter and the rectifier stage because it can generate a high-frequency ac signal with ZVS but has a lower device voltage stress compared to a Class E [7]. The design methodology presented in this paper, however, can be applied

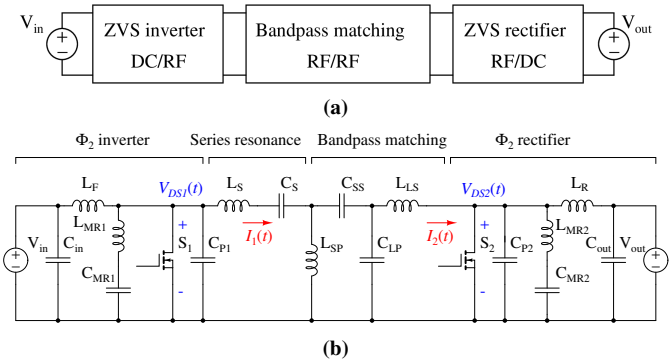


Fig. 2: Proposed converter structure and a single-phase example. (a) HF/VHF resonant converter with bandpass matching network; (b) Single-phase Φ_2^2 converter with bandpass matching network.

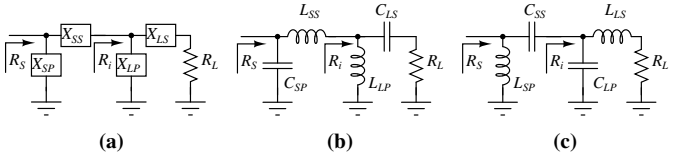


Fig. 3: Dual-stage bandpass matching networks, $R_S > R_L$. (a) X is the imaginary impedance of each component; (b)(c) Electrically equivalent circuit representations.

to a Class E, F, or higher-order tuned amplifier if the inverter and the rectifier topologies are the same. The low-Q series resonance L_S-C_S in Fig. 2b provides DC blocking without significantly affecting the large-signal transient response.

A bandpass matching network consists of two cascaded L matching stages – one high-pass and one low-pass, as shown in Fig. 3. Depending on the order, we can have two circuit representations, but electrically they perform the same function. The parasitic resistances in the inductors and capacitors will contribute to power losses, and should be minimized. Bandpass matching is selected because a dual-stage matching network provides the best efficiency for the ratios of voltage conversion needed here [37], [38]. Although we used the conventional approach to design the multi-stage matching network, Ref. [39], [40] introduce an optimization algorithm for multi-stage matching networks that can achieve better efficiency, and could be expected to improve performance beyond that achieved here. Many high-frequency applications, including wireless charging [41]–[43], could benefit from optimized multi-stage matching networks designs.

A. Synchronous driving of S_1 and S_2

In the converter of Fig. 2b, the bandpass matching network enables S_1 and S_2 to be driven with the same gate signal. Fig. 4 shows a typical drain-to-source voltage $V_{DS}(t)$ waveform in a Φ_2 inverter circuit [7]. When the Φ_2 circuit operates as a

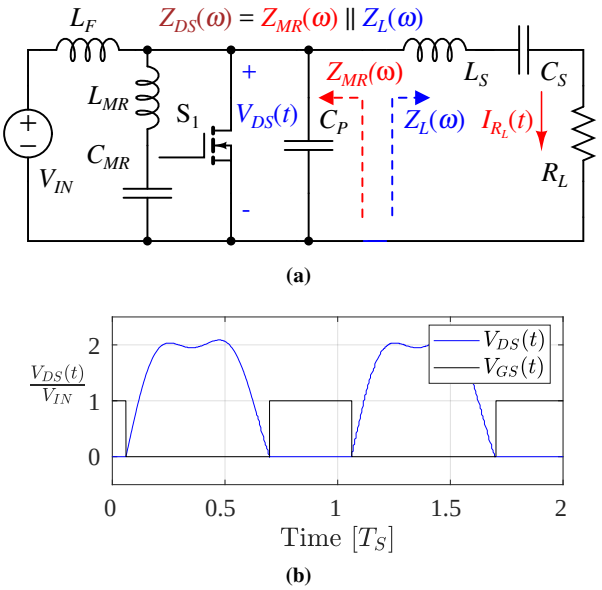


Fig. 4: Φ_2 inverter and typical waveform. (a) Φ_2 inverter circuit; (b) Typical drain-to-source voltage $V_{DS}(t)$ waveform in a Φ_2 inverter circuit, ZVS is achieved and peak voltage is $2V_{IN}$.

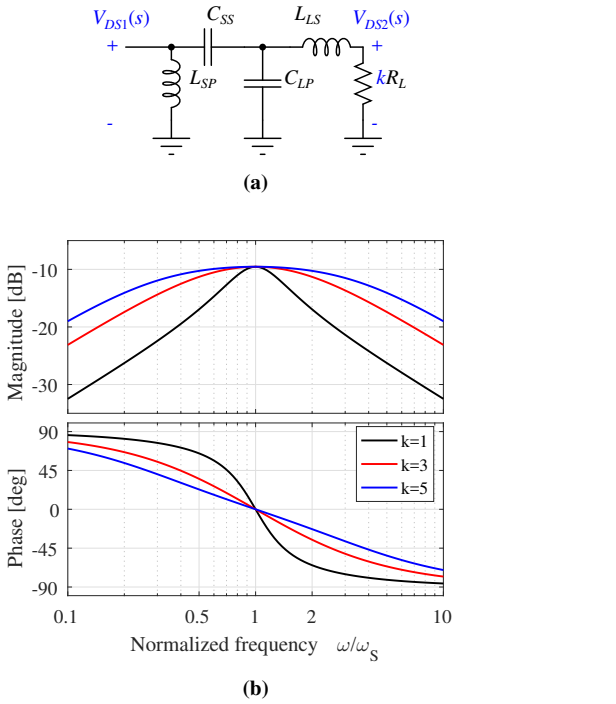


Fig. 5: Bandpass matching network with variable resistance, k represents the load variation. (a) simplified circuit for ac analysis; (b) voltage gain $\frac{V_{DS2}(j\omega)}{V_{DS1}(j\omega)}$ vs frequency ω, at resonant frequency $\frac{V_{DS2}}{V_{DS1}}=\frac{1}{3}$.

rectifier, the voltage across the rectifier switch will also be a quasi-square wave similar to the one in Fig. 4b [26]. Therefore, $V_{DS1}(t)$ and $V_{DS2}(t)$ will exhibit the same quasi-square wave but with different magnitudes.

Fig. 5 shows the bode plot of the frequency response of a bandpass matching network. Notice that the network maintains a zero phase shift between the input and output ac voltages at the resonant frequency. In the Φ_2^2 converter of Fig. 2b, L_S and C_S are resonant at f_s to maintain the phase of $V_{DS1}(t)$ between the inverter and matching network. Therefore, the bandpass matching network makes the inverter voltage $V_{DS1}(t)$ and rectifier voltage $V_{DS2}(t)$ in phase, as illustrated in Fig. 6. This means that we can drive the two switches S_1 and S_2 with the same gate clock signal, as the zero values of the two voltage waveforms occur during the same time. This greatly simplifies the synchronization of the two gate signals in the HF/VHF range.

B. Load independent operation

1) Bandpass matching network: Using a bandpass matching network can bring convenience to the design and achieve the highest efficiency [37]–[39]. Crucially, the synchronization of S_1's and S_2's drain voltages remains under different load conditions, as we show analytically below.

When matching the impedance of two resistive ports ($R_S > R_L$) for maximum bandwidth design, we typically set R_i to the geometric mean of R_S and R_L [44],

$$R_i = \sqrt{R_S \times R_L}. \tag{1}$$

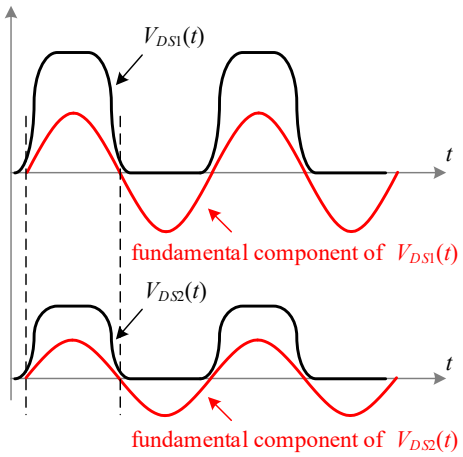


Fig. 6: Bandpass matching maintains zero phase shift between inverter voltage $V_{DS1}(t)$ and rectifier voltage $V_{DS2}(t)$.

R_i is the impedance looking from the mid-point. The quality factor of each L matching stage Q_i is

$$Q_i = \sqrt{\left(\frac{R_S}{R_L}\right)^{\frac{1}{2}} - 1}. \tag{2}$$

The relationship between the resistances is

$$R_S \;=\; (1+Q_i^2)R_i \;=\; (1+Q_i^2)^2 R_L, \tag{3}$$

and the relationship between the reactances is

$$Q_i \;=\; \frac{R_S}{|X_{SP}|} \;=\; \frac{|X_{SS}|}{R_i} \;=\; \frac{R_i}{|X_{LP}|} \;=\; \frac{|X_{LS}|}{R_L}. \tag{4}$$

For Fig. 3, Ls and Cs can be calculated by

$$\begin{aligned} C_{SP} &= \frac{Q_i}{\omega_s(1+Q_i^2)^2 R_L}, \quad L_{SS} = \frac{Q_i(1+Q_i^2)R_L}{\omega_s}, \\ L_{LP} &= \frac{(1+Q_i^2)R_L}{\omega_s Q_i}, \quad C_{LS} = \frac{1}{\omega_s Q_i R_L}, \end{aligned} \tag{5}$$

$$\begin{aligned} L_{SP} &= \frac{(1+Q_i^2)^2 R_L}{\omega_s Q_i}, \quad C_{SS} = \frac{1}{\omega_s Q_i (1+Q_i^2) R_L}, \\ C_{LP} &= \frac{Q_i}{\omega_s(1+Q_i^2)R_L}, \quad L_{LS} = \frac{Q_i R_L}{\omega_s}. \end{aligned} \tag{6}$$

The frequency response of the bandpass matching network in Fig. 5a can be expressed as

$$\frac{V_{DS2}(j\omega)}{V_{DS1}(j\omega)} \;=\; \frac{1}{1+Q_i^2} \cdot \frac{1}{1+j\frac{Q_i}{k}\left(\frac{\omega}{\omega_s} - \frac{\omega_s}{\omega}\right)}. \tag{7}$$

At the resonant frequency $\omega = \omega_s$, the voltage gain is constant

$$\frac{V_{DS2}(j\omega_s)}{V_{DS1}(j\omega_s)} \;=\; \frac{1}{1+Q_i^2}, \tag{8}$$

which is independent of the load variation coefficient k. Therefore, independent of R_L (the rectifier's input impedance), the bandpass matching maintains a constant gain and zero phase shift between the inverter and rectifier voltages. Fig. 5b shows this, with the zero crossing fixed at $\omega = \omega_s$ as the rectifier impedance is varied from 1 to 5 times.

2) Φ_2 inverter/rectifier: Similarly, we select the Φ_2 inverter because it maintains ZVS operation when the loading resistance changes. In a DC/RF power amplifier with a single ground-referenced switching device, the total impedance across the semiconductor determines the time-domain waveform. For example, Fig. 7 shows the general structure of an RF power amplifier using a single MOSFET. As the MOSFET is being switched on and off periodically at f_s, the impedance Z_{DS} across the drain and source at the fundamental frequency and its harmonic components determines the time-domain waveform [6].

Fig. 8 shows an example of a 50 MHz Φ_2 inverter and its ability to main ZVS independent of the output power. The general rules of designing a Φ_2 inverter that operates with ZVS across a wide resistive load range are (modified from the design guidelines outlined in [45], [46]) :

1) The Φ_2 inverter can be conceptually separated into two parts, the multi-resonant network Z_{MR} and the loading network Z_L. The loading network Z_L is designed to be resistive at f_s.

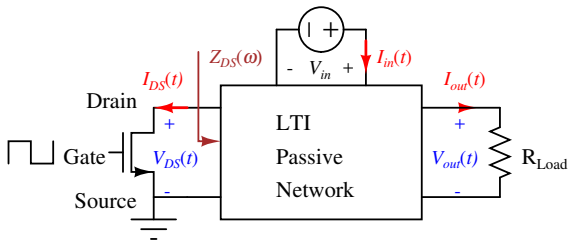


Fig. 7: Power amplifier with single ground-referenced MOSFET.

2) L_S and C_S resonate at f_s. The nominal value of R_L is determined by the maximum output power. The quality factor of this series resonance (Q_s) determines the THD of the output current.
3) The impedance magnitude of Z_L is set to be larger than the multi-resonant ZVS network's impedance Z_{MR} at f_s and its harmonic components under different load conditions.
4) The impedance of Z_{MR} is inductive in phase at the fundamental frequency (f_s) and capacitive at the third harmonic ($3f_s$). L_{MR} and C_{MR} resonate at $2f_s$ to create a short in Z_{MR}.

Fig. 8a shows the transient simulation of the example converter, with ZVS operation maintained across a ten times variation in the output power.

With the considerations listed above, we can design a Φ_2 circuit that can produce a constant ac voltage independent of the amplitude of the load current. The voltage and current are always in phase and ZVS operation can be maintained on the switch. When the Φ_2 circuit is operating as a synchronous rectifier, it can also maintain an ac impedance that is mostly resistive at the input, i.e., the fundamental components of the voltage $V_{DS2}(t)$ and the current $I_2(t)$ are in phase. When the output power changes, the effective input resistance changes inversely in proportion to the rectifier power.

III. Single-Phase 64 MHz Converter

This section shows the experimental results of a 64 MHz 36 V-to-12 V dc-dc prototype converter that corresponds to the circuit in Fig 2b. We first design the inverter and rectifier separately and verify their operation. We then put the inverter and rectifier together on a single PCB with the bandpass matching network. Table I lists the bill-of-materials (BOM) of the prototype converter. Fig. 9 shows the photograph of the prototype.

Fig. 10 shows the simulated drain waveform. We can see that S_1 and S_2 can both maintain ZVS even when the output power changes from 3 W to 15 W. Fig. 11 shows the measured drain waveform. This experimentally verifies that S_1 and S_2 can maintain ZVS and be driven by the same clock across a wide load range. Fig. 12 shows that the 64 MHz prototype converter reaches steady-state in 60 ns. Fig. 13a shows the output voltage versus power. The measured V_{out} varies from

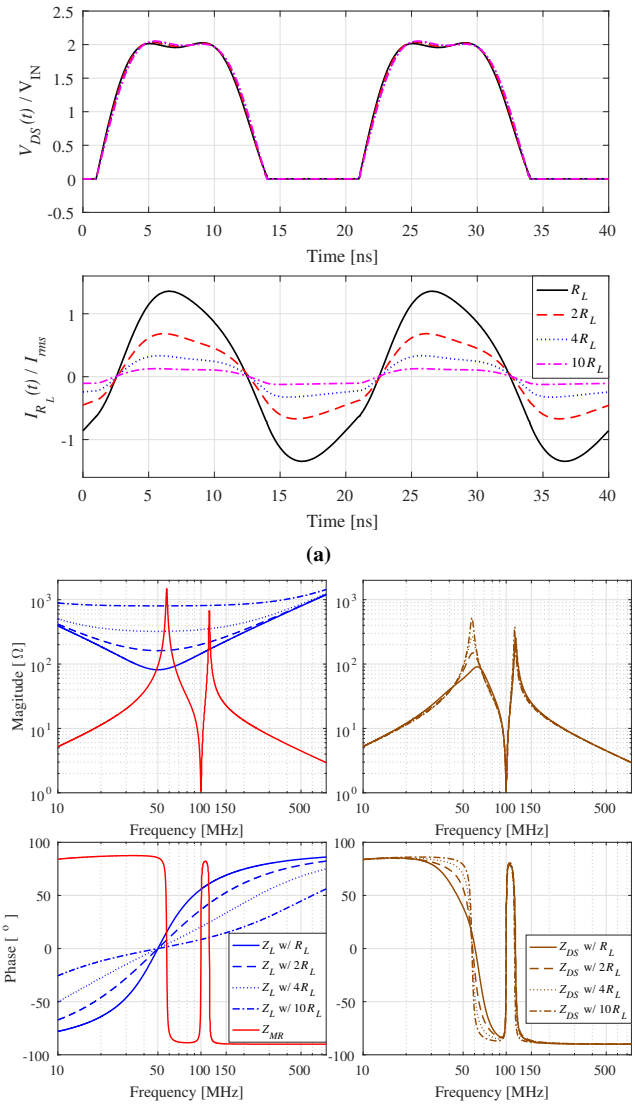


Fig. 8: A 50 MHz Φ_2 inverter designed for variable resistive load. L_F = 80 nH, L_{MR} = 169 nH, C_{MR} = 15 pF, C_P = 73 pF. (a) $V_{DS1}(t)$ waveform, ZVS is achieved when R_L is changed from nominal load to 10 times value; (b) Impedance bode plots Z_{MR} and Z_L (left), Z_{DS} (right).

11.8 V to 10.3 V when P_{out} is changed from 1 W to 11 W. In simulation, V_{out} changes from 12.2 V to 11.8 V as I_{out} varies from 0.1 A to 1.1 A. The effective output resistance of the converter is 0.4 Ω. Fig. 13b shows the measured efficiency of the prototype. The C_{OSS} losses can be one of the reasons that cause the difference between the simulated and measured output resistances, as [47], [48] reported that existing GaN devices could have significant losses in the C_{OSS} under high dV/dt soft-switching conditions. Comparison of the C_{OSS} loss in different types of power devices with similar voltage ratings, including GaN FETs, SiC MOSFETs, Si Trench MOSFET, and

TABLE I: BILL-OF-MATERIALS (BOM) OF THE 64 MHZ PROTOTYPE.

Device	Component Description
Gate driver	SN74LVC2G34, 2-bit non-inverting buffer
S_1	EPC8010, 100 V, 2.7 A GaN FET
S_2	EPC8009, 65 V, 2.7 A GaN FET
L_F	56 nH, Coilcraft 1812SMS-56N
$L_{MR1,2}$	155 nH, Coilcraft 1812SMS-R15
L_S	47 nH, Coilcraft 1812SMS-47N
L_{SP}	114 nH, Coilcraft 1812SMS-R12
L_{LS}	28.6 nH, Coilcraft 1812SMS-27N
L_{F2}	22 nH, Coilcraft 1812SMS-22N
$C_{MR1,2}$	10 pF, 50V C0G 0603
C_{P1}	39 pF, 250V C0G 0603
C_{P2}	150 pF, 100V C0G 0603
C_S	130 pF, 100V C0G 0603
C_{SS}	82 pF, 100V C0G 0603
C_{LP}	159 pF, 100V C0G 0603

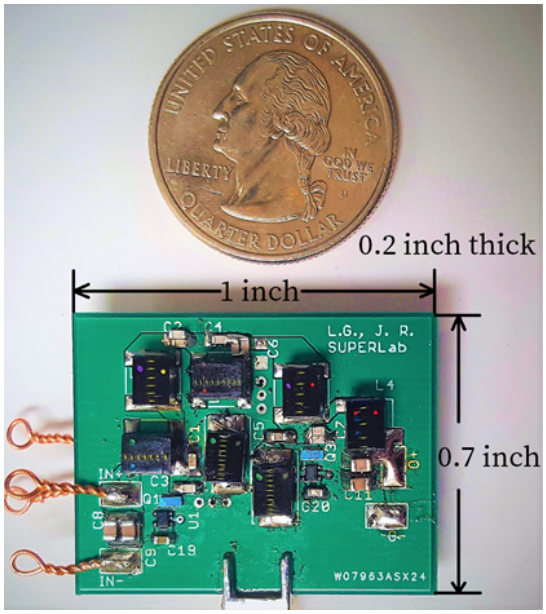


Fig. 9: 64 MHz single-phase Φ_2^2 dc-dc prototype converter

Si Super-junction MOSFETs, is presented in [49].

IV. CONVERTER INTERLEAVING

One disadvantage of the single-phase configuration of Fig. 2b is that the input and output currents can have much larger high-frequency ripples than the average values. As a result, a large filter capacitance is necessary at both ports, which slows down the load transient. A method of overcoming this issue is to use interleaving, where two identical converters are paralleled and operated with a 180° phase shift. Fig. 14b shows a specific example.

The subscript label in each component indicates the corresponding phase. The two switches in the same phase are still driven by the same clock signal, but phase a and b are running with a phase difference of 180°.

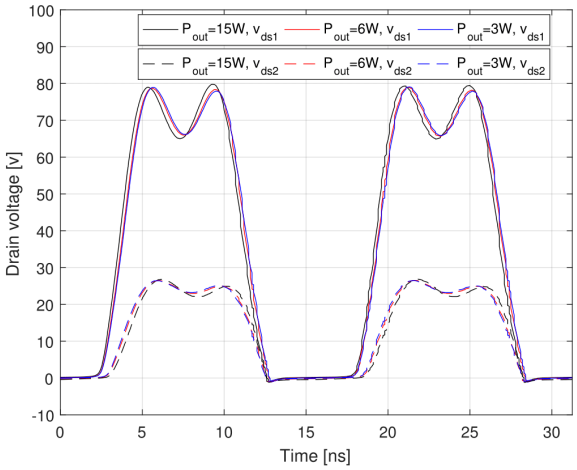
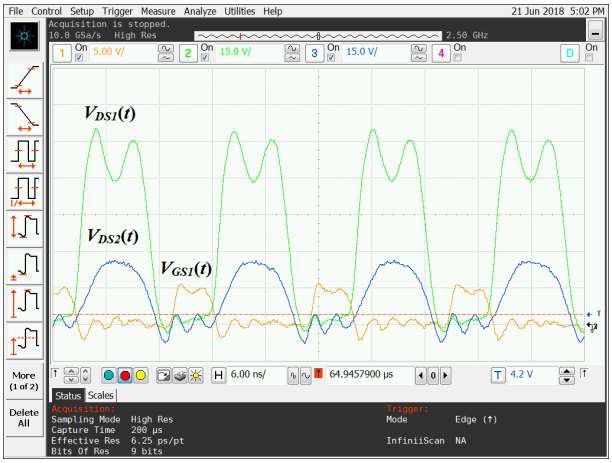


Fig. 10: Simulation drain voltage waveforms, $V_{in} = 36$ V.



(a)

(b)

Fig. 11: Measured drain voltage, V_{in}=36 V, CH1 $V_{GS1}(t)$, CH2 $V_{DS1}(t)$, and CH3 $V_{DS2}(t)$. (a) V_{out}=10.7 V, R_{out}=12.5 Ω, P_{out}=9.2 W; (b) V_{out}=11.7 V, R_{out}=50 Ω, P_{out}=2.8 W.

Interleaving creates a differential ground, which means that some components can be combined [50] to simplify the circuit and improve efficiency. In Fig. 14a, the current of C_{SPa} and C_{SPb} have the same amplitude but opposite phase. This implies that we can combine C_{SPa} and C_{SPb} into a single capacitor C_{SP} that has half of the value, i.e., $C_{SP} = 0.5C_{SPa}$, as shown in Fig. 14b. Similarly, we can use one inductor L_{LP} to replace two separate ones, L_{LPa} and L_{LPb}. The relationship between the inductance is $L_{LP} = 2L_{LPa}$. Moreover, the low-Q series resonant circuit L_S-C_S in Fig. 14a can be eliminated, as it only provided DC-blocking in the single-phase converter and is not necessary in the modified converter of Fig. 14b. In the end, this push-pull configuration can improve the efficiency, transient response, and power density of the single-phase Φ_2^2 converter.

Fig. 15 shows the key simulation waveforms. We can see that the ripple of the input and output currents $i_{in}(t)$ and $i_{out}(t)$ are greatly reduced compared with the ripple in a single-phase converter. This greatly reduces the required filtering capacitance and improves the transient response of the converter.

Notice that the bandpass matching network of the push-pull converter of Fig. 14b is from Fig. 3b, while the single-phase converter of Fig. 2b uses the alternate bandpass matching in Fig. 3c. Electrically, these two circuits have the same functionality. By putting the inductors adjacent in Fig. 14b, we can replace the 3-inductor structure L_{SSa}-L_{LP}-L_{SSb} with a coupled transformer, as shown in Fig. 16. With this, we not only include galvanic isolation but also improve the power density by sharing a magnetic structure [51].

A further improvement uses a series-stacked architecture or multi-level structure, similar to what is widely used in switched-capacitor and hybrid resonant converters to allow the utilization of lower-voltage semiconductor switches [52]–[57]. This can substantially improve the efficiency of these converters based on half-bridge switch pairs. Similarly, we can apply the same structure to our push-pull Φ_2^2 converter in Fig. 14b, and an example of this input series-stacked push-pull Φ_2^2 converter is shown in Fig. 17. C_{CP1} and C_{CP2} are ac coupling capacitors. Their impedance at the switching frequency are negligible compared to other resonant passive components. The dc voltages on the input buffer capacitors C_{in1} and C_{in2} are self-balanced. As long as the values of C_{in1} and C_{in2} are large enough, the dc voltages across C_{in1} and C_{in2} are stable around $0.5V_{in}$. This series-stacked structure enable the use of lower voltage semiconductor switches for S_{1a} and S_{1b}. The built-in step-down function also reduces the conversion stress on the matching network and improves its efficiency [58]. Another practical benefit, if existing GaN FETs are selected, is the soft-switching losses discovered in C_{OSS} are proportional to the dV/dt [48]. Therefore, by reducing the voltage swing on the GaN FET using the series-stacked structure, we can further improve the experimental efficiency.

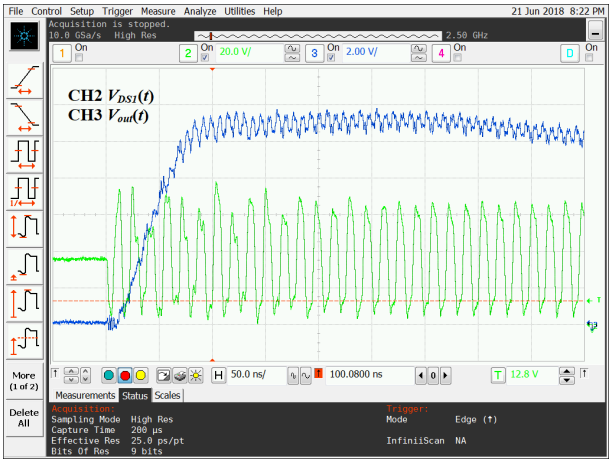


Fig. 12: 64 MHz prototype $V_{out}(t)$ turn-on transient, V_{in}=36 V, V_{out}=10.6 V, R_{out}=12.5 Ω.

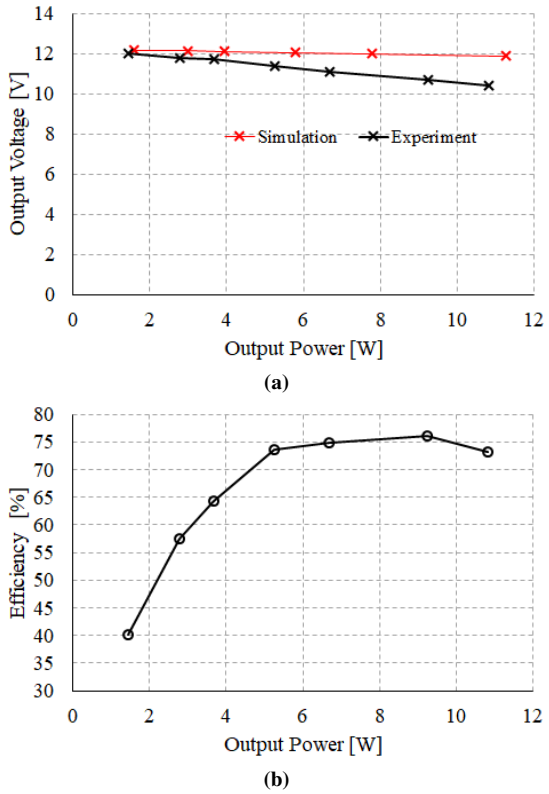


Fig. 13: 64 MHz prototype measured performance vs output power, V_{in} = 36 V. (a) V_{out} vs output power. (b) Efficiency vs output power.

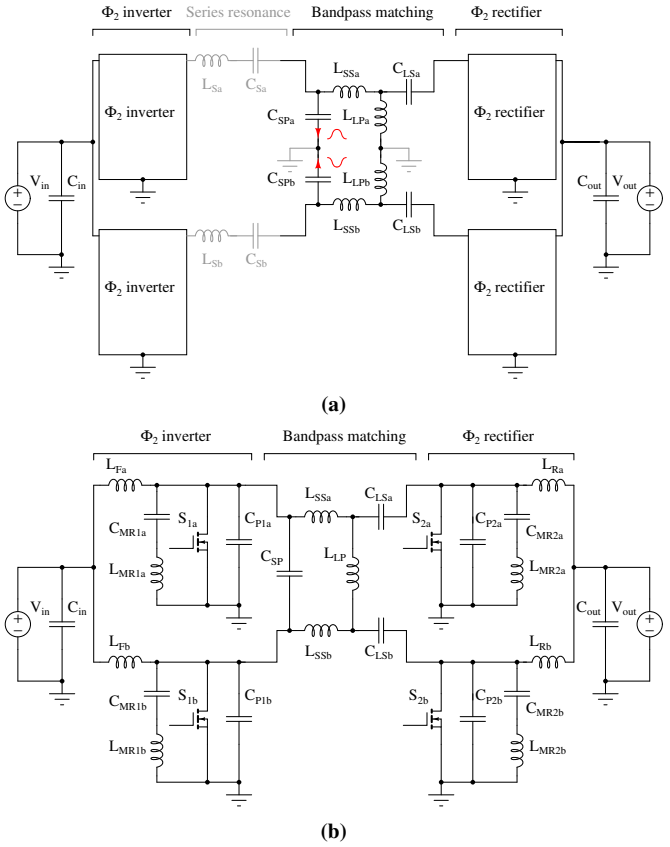


Fig. 14: Converter interleaving. **(a)** Two-phase interleaved Φ_2^2 converters connected in parallel, the components labeled in light color can be eliminated. **(b)** The equivalent circuit with unnecessary components combined and eliminated.

TABLE II: BOM OF THE 13.56 MHZ PUSH-PULL PROTOTYPE.

Device	Component Description
Gate drive	UCC27516
$S_{1a,b}$	GS66502B, 650V
$S_{2a,b}$	GS61004B, 100V
$L_{Fa,b}$	660 nH, Q=260@13.56MHz, 10 turns of AWG16
$L_{MR1a,b}$	500 nH, Q=80@13.56MHz, Coilcraft 2929SQ-501
$C_{MR1a,b}$	69 pF, C0G Ceramic 1.5kV
$C_{P1a,b}$	56 pF, C0G Ceramic 1kV
C_{SP}	78 pF, C0G Ceramic 1kV
$L_{SSa,b}$	1550 nH, Q=220@13.56MHz, 10 turns of AWG16
L_{LP}	476 nH, Q=200@13.56MHz, 12 turns of AWG16
$C_{LSa,b}$	680 pF, C0G Ceramic 100V
$L_{MR2a,b}$	123 nH, Q=100@13.56MHz, Coilcraft 2014VS-111
$C_{MR2a,b}$	280 pF, C0G Ceramic 300V
$C_{P2a,b}$	940 pF, C0G Ceramic 200V
$L_{Ra,b}$	50 nH, Q=110@13.56MHz, Coilcraft 1212VS-42N

V. A 13.56 MHZ PUSH-PULL Φ_2^2 PROTOTYPE

To experimentally demonstrate the operation principles of the push-pull Φ_2^2 converter in Fig. 14b, a 13.56 MHz, 200 W, 200 V-to-30 V prototype is designed and built. Table II lists the key components used in the prototype. Fig. 18 shows the constructed converter. All of the passive components and the gate-drive circuits are placed on one side of the PCB, while the GaN FETs are placed on the other side to improve heat extraction.

When the converter is delivering power from the high-voltage to the low-voltage side, the measured drain-to-source

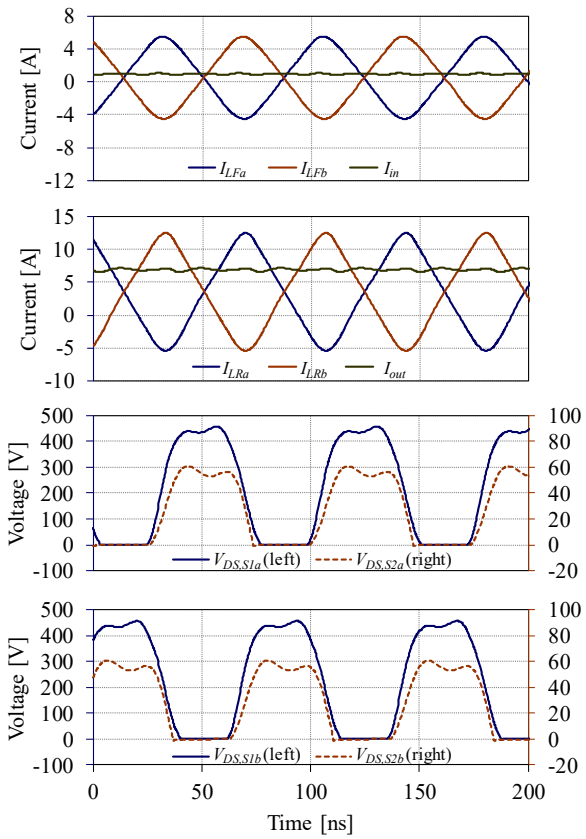


Fig. 15: Key waveform in LTSPICE of a push-pull Φ_2^2 converter, V_{in}=270 V, V_{out}=28 V, P_{out}=200 W, f_s=13.56 MHz.

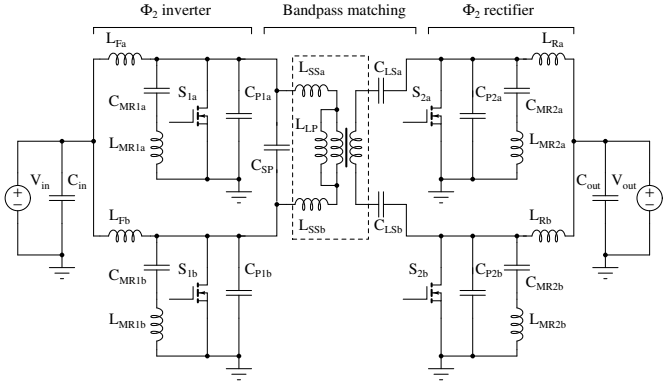


Fig. 16: Two-phase interleaved Φ_2^2 converter with transformer.

voltage waveforms $V_{DS}(t)$ of all the switches are shown in Fig 19. We can see that for the two switches in Phase a, $V_{DS,S1a}(t)$ is in phase with $V_{DS,S2a}(t)$, shown on the top of Fig. 19. The same in-phase property is found in the Phase b $V_{DS}(t)$ waveform, shown on the bottom of Fig. 19. Phase a and b are operating 180° out of phase. This phase relation between the $V_{DS}(t)$ of all the switches holds true under

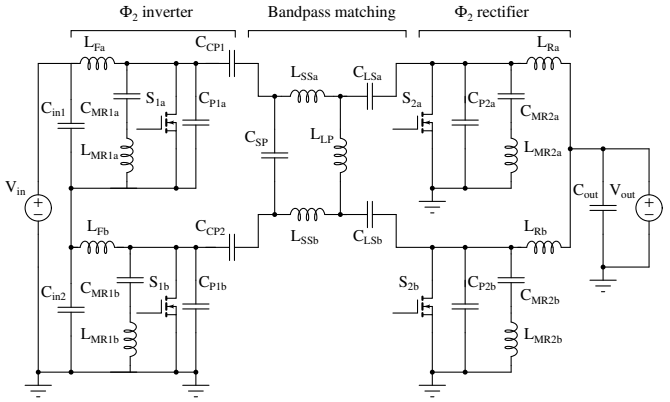


Fig. 17: Series-stacked two-phase interleaved Φ_2^2 converter.

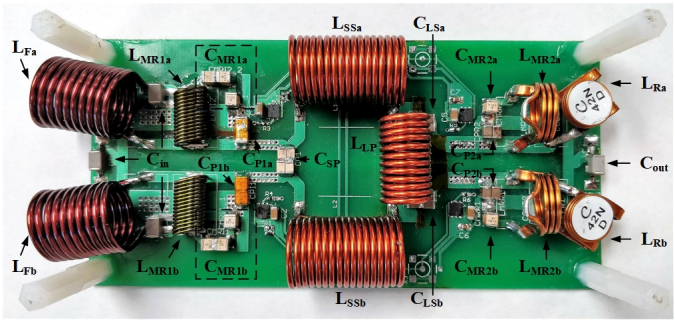
different output power conditions.

Fig. 20 shows the the drain-to-source voltage $V_{DS}(t)$ and gate-to-source voltage $V_{GS}(t)$ of the inverter switches S_{1a} and S_{1b} for forward direction power delivery. We can see that both switches achieve ZVS operations, which is also maintained over a wide load range.

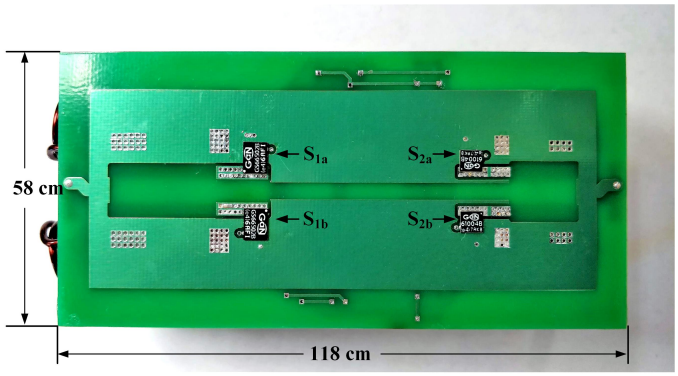
When the converter is delivering power in reverse from the low-voltage to the high-voltage side, the measured waveforms are shown in Fig. 21 and Fig. 22. The same in-phase relation and ZVS operation are demonstrated and hold for different load conditions. Fig. 23 shows the measured efficiency of the push-pull converter prototype, with a maximum of 90% at 200 W.

VI. Conclusion

Synchronous rectification can improve the efficiency but is challenging to implement in a high-frequency dc-dc converter. By selecting a proper matching stage, this paper demonstrates that multiple challenges can be addressed simultaneously. This paper proposes a structure for an HF/VHF resonant converter that uses a bandpass matching network for the ac conversion stage. The bandpass matching network maintains a close-to-zero phase shift between the inverter and rectifier voltage, enabling the synchronous switch to be driven by the same clock signal as the inverter switch. This simplifies the synchronization of multiple gate signals in the HF/VHF range (3-300 MHz). The structure can also maintain a constant dc-dc conversion ratio at different loads. A 64 MHz single-phase prototype converter demonstrates the effectiveness of the presented method for synchronous rectification. This paper further presents interleaved and series-stacked architectures that can improve the transient performance, efficiency, and power density performance relative to a single-phase implementation. A 13.56 MHz 210 V-to-30 V prototype converter with 90 % peak efficiency at 200 W demonstrates the advantages of the interleaved architecture.



(a)



(b)

Fig. 18: Photograph of 13.56 MHz push-pull Φ_2^2 prototype converter. **(a)** Top of the converter, including all the resonant passives and gate-drive circuits. **(b)** Bottom of the converter, 4 GaN FETs.

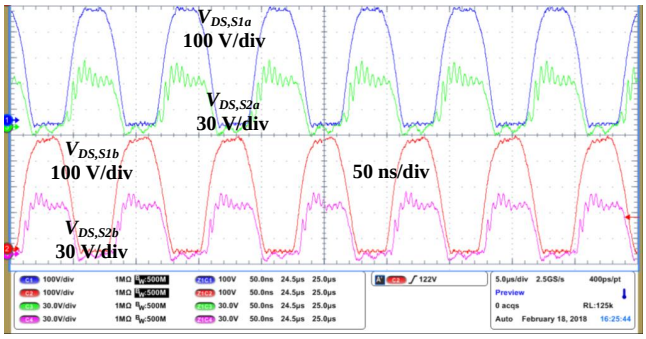


Fig. 19: Forward direction, drain-to-source waveform, V_{in} = 210 V, V_{out} = 30 V, R_{out}=10 Ω, CH1 $V_{DS,S1a}(t)$, CH2 $V_{DS,S1b}(t)$, CH3 $V_{DS,S2a}(t)$, CH4 $V_{DS,S2b}(t)$.

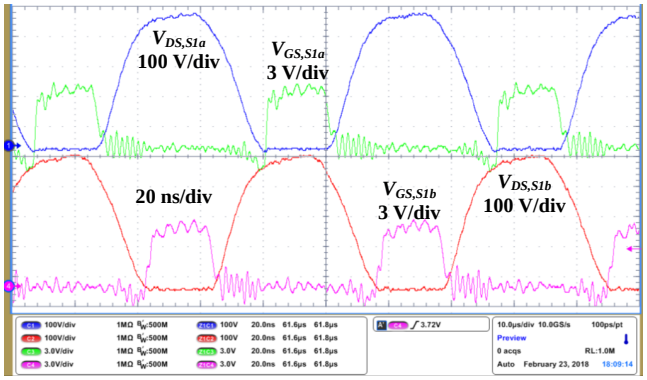


Fig. 20: Forward direction, drain and gate waveform of the high voltage switches, V_{in} = 210 V, V_{out} = 30 V, R_{out} = 10 Ω, CH1 $V_{DS,S1a}(t)$, CH2 $V_{DS,S1b}(t)$, CH3 $V_{GS,S1a}(t)$, CH4 $V_{GS,S1b}(t)$.

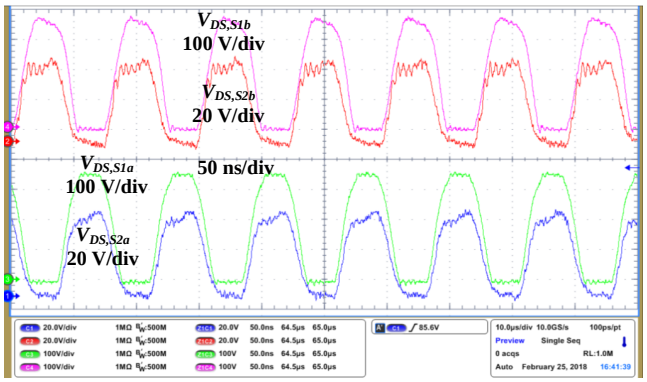


Fig. 21: Reverse direction, drain waveform, V_{in} = 30 V, V_{out} = 193 V, R_{out} = 333 Ω, CH1 $V_{DS,S2a}(t)$, CH2 $V_{DS,S2b}(t)$, CH3 $V_{DS,S1a}(t)$, CH4 $V_{DS,S1b}(t)$.

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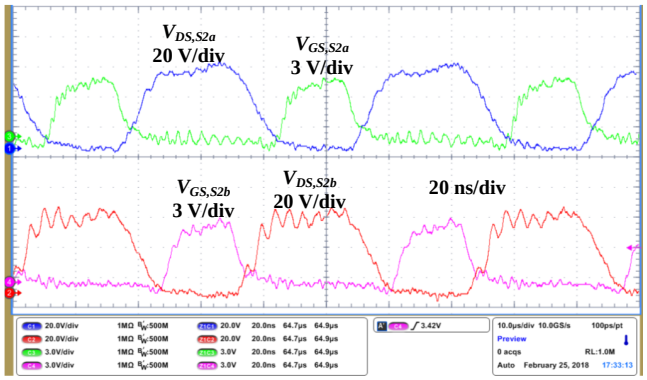

Fig. 22: Reverse direction, drain and gate waveform of low voltage switches, V_{in} = 30 V, V_{out} = 193 V, R_{out}=333 Ω, CH1 $V_{DS,S2a}(t)$, CH2 $V_{DS,S2b}(t)$, CH3 $V_{GS,S2a}(t)$, CH4 $V_{GS,S2b}(t)$.

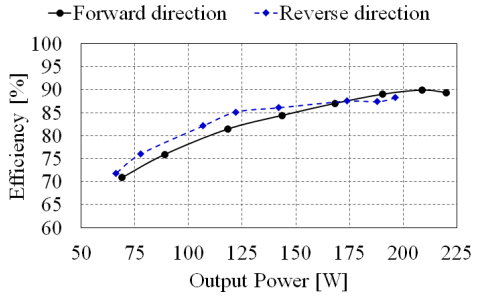

Fig. 23: 13.56 MHz prototype measured efficiency vs output power

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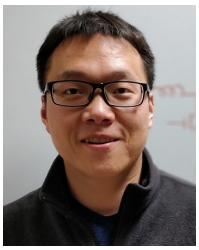

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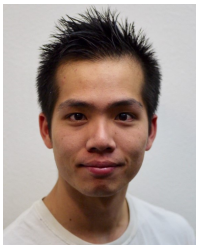

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