CS6135 VLSI Physical Design Automation

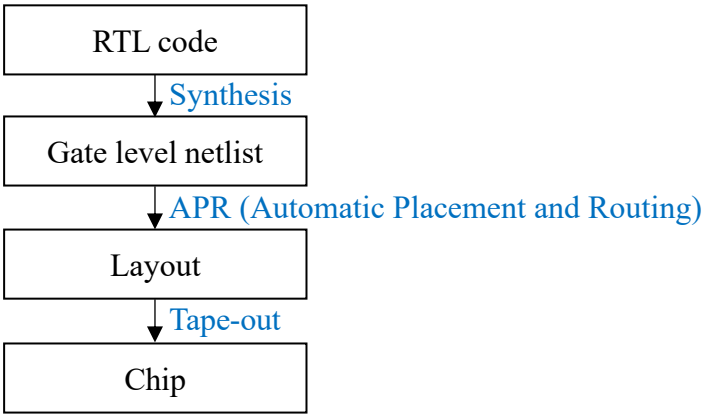
Homework 1: P&R Tool

Due: 23:59, October 12, 2023

1. Goal

In this homework, you are asked to use Cadence Innovus to complete the P&R (Place and Route) flow for a given synthesized standard-cell design. The goal is to acquaint you with Innovus and the P&R flow. Besides, you are encouraged to try to optimize timing, total area of chip, and total wire length without violating any timing or DRC constraints.

In a clear way, we want you to utilize a P&R tool (Cadence Innovus) to do APR to generate a layout.



2. Working Items

- Follow the procedures described in Section 6 step by step to get familiar with Innovus.
- Try your best to use Innovus for optimizing the timing (clock period in the SDC file) and the area (try to adjust the core utilization in Design Planning stage) of the circuit. (Hint: You need to adjust the value of the clock period (2x and x) in the .sdc file to optimize the timing.)
  - `create_clock [get_ports clk] -name CLK -period 2x -waveform {0 x}`
- Try to switch the timing-driven option on and off and change congestion-driven effort setting, respectively, when placing standard cells to see how they affect the result. Please also try to explain the difference(s) between the timing-driven placement and congestion-driven placement in your submitted report.
- Please explain why we need to insert filler cells into the design.

- Show the information of clock period (design.sdc), slack time (timing.rpt), total area of chip (summary.rpt), total wire length (summary.rpt), and DRC (drc.rpt) in the report.
- Make sure that the slack must be non-negative and the number of DRC violations must be zero for your physical implementation.

3. Report

Your report should at least contain the following contents.

(1) Your name and student ID

(2) A comparison table like the following one, and an explanation of the result (The table should be built under a fixed core utilization and clock period and you should specify them in the report.)

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
slack	???	???	???	???	???	???
total wire length	???	???	???	???	???	???

(L, M, and H stand for Low, Medium, and High congestion effort.)

(3) The difference(s) between the congestion-driven placement and timing-driven placement

(4) An explanation of why we insert filler cells

(5) Show your best result (including clock period, total area of chip, total wire length, slack, congestion-driven effort and timing-driven on/off setting, and their snapshots) to maintain a non-negative slack and no DRC violation.

(6) Show the final chip layout of your best result generated by Innovus (use print-screen to save the final layout and paste on the report)

4. The File to be Handed in

Please package all the following items in one file named **CS6135_HW1_{STUDENT_ID}.zip** and submit it to eeclass.

(1) CS6135_HW1_{STUDENT_ID}.tar.gz

- An archive containing your post P&R design

```
$ tar -zcvf CS6135_HW1_{STUDENT_ID}.tar.gz HW1/
```

For example:

```
$ tar -zcvf CS6135_HW1_112062500.tar.gz HW1/
```

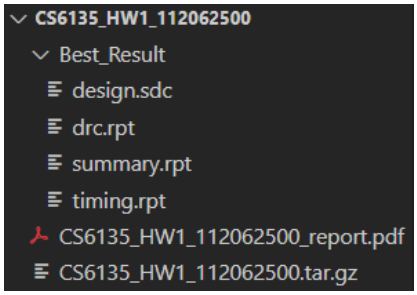
(2) CS6135_HW1_{STUDENT_ID}_report.pdf

- Your report

(3) A folder called “Best_Result”

- Contain design.sdc, drc.rpt, summary.rpt, and timing.rpt

The file structure would be like the following figure:



5. Grading

- ✓ 50%: The completeness of your submitted report
- ✓ 50%: The quality (clock period, total area of chip, and total wire length) of your physical implementation

6. Procedures

Please follow the steps below to complete your physical implementation of the given design. Note that each figure shown below is just an example, so your result may not be the same as it.

To follow the procedures, you'd better have a basic understanding of CLI (command-line interface). If you are not familiar with how to operate shell and vim, please study the "Shell Tutorial.pdf" that has been uploaded to eeclass.

A. Design Preparation

Step 1. Log in to the workstation (using MobaXterm for ease)

Please download "HW1.tar.gz" from eeclass. Then, upload the file to the server nthucad.cs.nthu.edu.tw.

```
$ scp HW1.tar.gz {YOUR_ACCOUNT}@nthucad.cs.nthu.edu.tw:.
```

("$" is a prompt, not a command, so don't type it. "scp" stands for **s**ecure **c**o**p**y.)

Next, login to the server nthucad.cs.nthu.edu.tw (by using the command "ssh" in some sort of command windows such as putty, Cygwin, MobaXterm, terminal.app, etc), and then change your password by entering the command "yppasswd".
("ssh" stands for **s**ecure **sh**ell. "-XY" means to enable X11 forwarding to see GUI.)

```
$ ssh -XY {YOUR_ACCOUNT}@nthucad.cs.nthu.edu.tw
$ yppasswd
```

The server nthucad.cs.nthu.edu.tw is just a proxy server (or a so-called relay server), which is used to connect other servers on a private network. That means it only contains some basic services, so you need to log in to another workstation server with Linux system (ic51) to run Innovus, e.g.,

```
$ ssh -XY ic51
```

Also, you could enter "lab_uptime" to see the loading information of each available server. You could choose the server which has fewer active users to log in.

```
nthucad:~> lab_uptime
Not support gcc-9.3.0 on nthucad
--------users---load average------------------users---load average---
ic21 (l): 2   0.00, 0.05, 0.39    ||    ic22 (l): 6   4.82, 5.30, 5.50
ic51 (l): 5   4.79, 4.78, 4.79    ||    ic53 (l): 4   1.85, 2.36, 2.82
ic55 (l): 1   0.00, 0.01, 0.05    ||    ic56 (l): 0   0.00, 0.01, 0.05
last updated: 公曆 20廿三年 九月 十八日 週一 廿二時十三分一秒
(l) Linux, (s) SunOS, (D) Shutdown
```

Step 2. Invoke Innovus

```
$ tar -zxvf HW1.tar.gz                    # untar the archive
$ cd HW1/
```

Before invoking Innovus with GUI, you might need to set the environment variable "DISPLAY" to your IP address and also make sure that you have already installed X server such as Xming or X-win32 in your computer. (Hint: Use MobaXterm in Windows or XQuartz in OS X at the beginning, and then you won't worry about it.)

```
$ innovus                                 # invoke Innovus
```

(If you didn't set up a X server on your PC and forward X11 to the workstation properly, you will get the following error.)

```
C: unknown locale

Cadence Innovus(TM) Implementation System.
Copyright 2021 Cadence Design Systems, Inc. All rights reserved worldwide.

Version:        v21.13-s100_1, built Fri Mar 4 14:32:31 PST 2022
Options:
Date:           Mon Sep 18 22:17:57 2023
Host:           ic51 (x86_64 w/Linux 3.10.0-1160.25.1.el7.x86_64) (16cores*64cpus*Intel(R) Xeon(R) Gold 6226R CPU @ 2.90GHz 22528KB)
OS:             CentOS Linux release 7.9.2009 (Core)

License:
                [22:17:57.370629] Configured Lic search path (20.02-s004): 5280@nthucad:5280@lstc:26585@lshc::1717@lshc

                invs    Innovus Implementation System   21.1    checkout succeeded
                8 CPU jobs allowed with the current license(s). Use setMultiCpuUsage to set your required CPU count.
**WARN: (IMPSYT-1507):  The display is invalid and will start in no window mode
Create and set the environment variable TMPDIR to /tmp/innovus_temp_95042_ic51_chlu19_T4YVvT.

Change the soft stacksize limit to 0.2%RAM (256 mbytes). Set global soft_stack_size_limit to change the value.

**INFO:  MMMC transition support version v31-84
```

B. Design Setup

First, we need to import the given design and read in all required files. Each time you enter a command, it's very important for you to check whether the error messages show in the console.

Step 1. Set CPU Usage and Process Node

Window > Tools > Set Multiple CPU Usage …

Local Machine

Number of Local CPU(s)	8

Then click **OK**

```
innovus> setDesignMode -process 45
```

Step 2. Import Design

Window > File > Import Design…

Netlist

Verilog	Selected
Files	Camellia.v
Top Cell	Select “Auto Assign”

Technology/Physical Libraries

LEF Files	Selected
LEF Files	NangateOpenCellLibrary.lef

Power

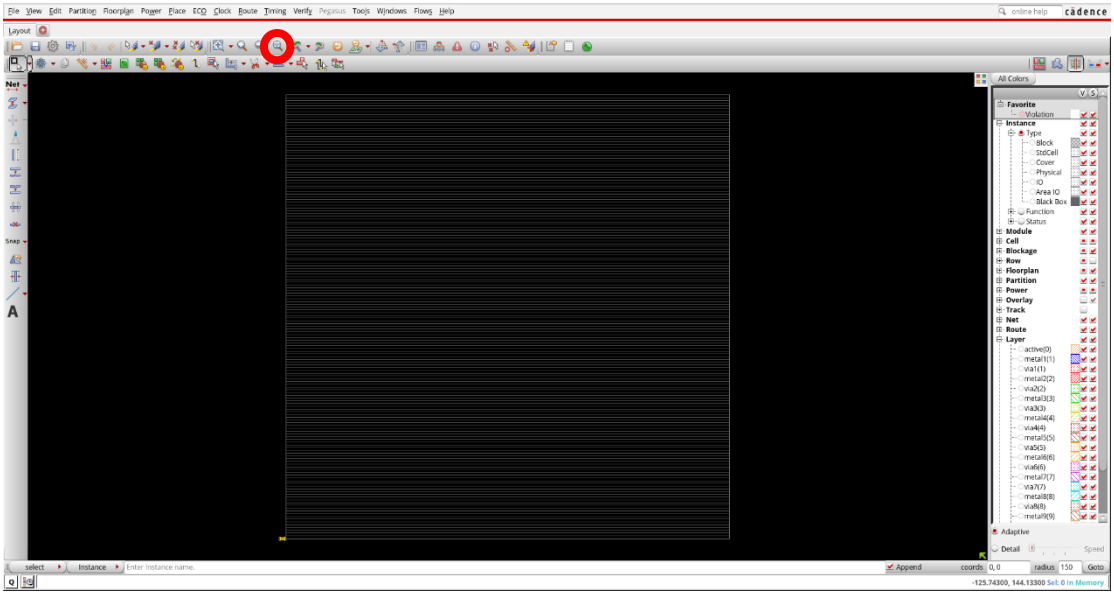
Power Nets	VDD
Ground Nets	VSS

Analysis Configuration

MMMC View Definition File	mmmc.view

Then click **OK**

Then it will open a layout window like the following figure. (You can click on the marked bottom first to fit the design to the window size.)



Step 3. Save design

Window > File > Save Design…

Data Type	Select “Innovus”
File Name	setup

Then click **OK**

P.S. Any time you want to restore a design

Window > File > Restore Design…

Data Type	Select “Innovus”
Restore Design File	setup (Your saved design)

Then click **OK**

After restoring the design, please make sure you are in the "Physical view" rather than the "Floorplan view." You can find the view mode buttons at the upper-right corner.

C. Floorplan and Placement

Next, we specify a region and put our design in it.

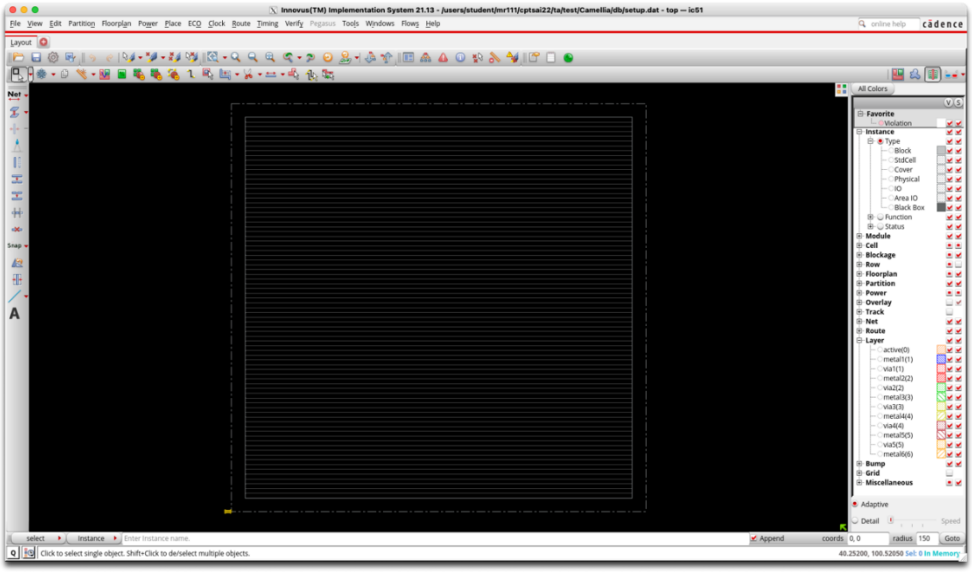
Step 1. Initialize floorplan

Window > Floorplan > Specify Floorplan… > Basic

Specify By	Select “Size”
Core Size by	Select “Aspect Ratio”
Ratio (H/W)	1.0
Core Utilization	0.7 (Depends on you, 0 < utilization < 1)
Core Margins by	Select “Core to Die Boundary”
Core to Die Boundary	Core to Left: 4.0
	Core to Right: 4.0
	Core to Top: 4.0
	Core to Bottom: 4.0

Then click **OK**

The initial floorplan should be like the following figure. The gray solid rectangle is the core area in which you will put all your standard cells.



Step 2. Full Placement

Window > Place > Place Standard Cell…

Run Full Placement	Selected

Window > Place > Place Standard Cell… > Mode…

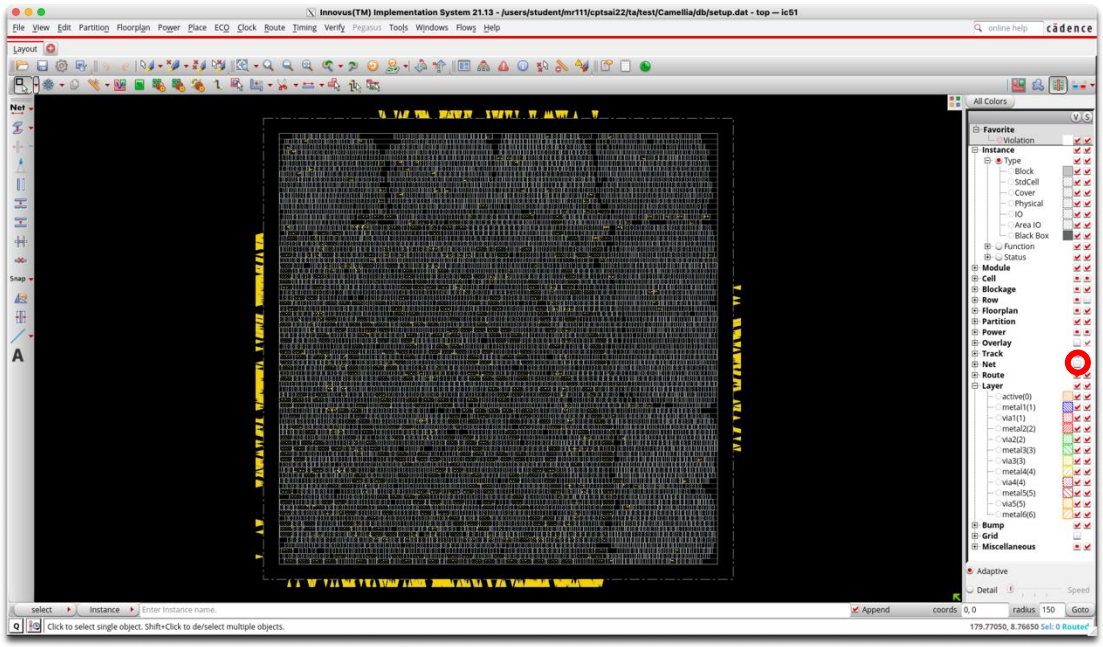
Placement

Congestion Effort	Depends on you
Run Timing Driven Placement	Depends on you
Place IO Pins	Checked

Then click **OK**

And click **OK** again in the previous pop-up window

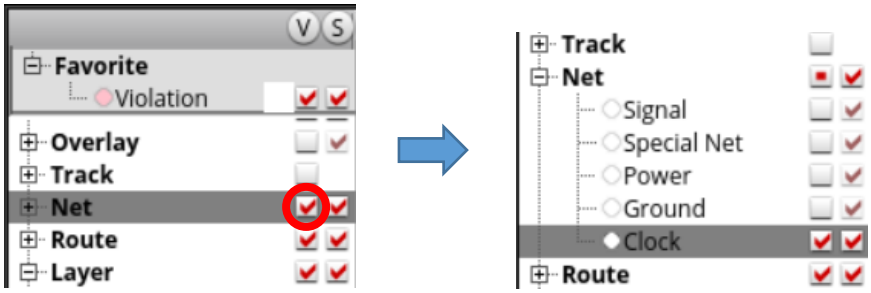
In order to see the placed standard cell, please remember to uncheck the marked checkbox to hide the routing net. You can use the zooming utility to observe the layout.



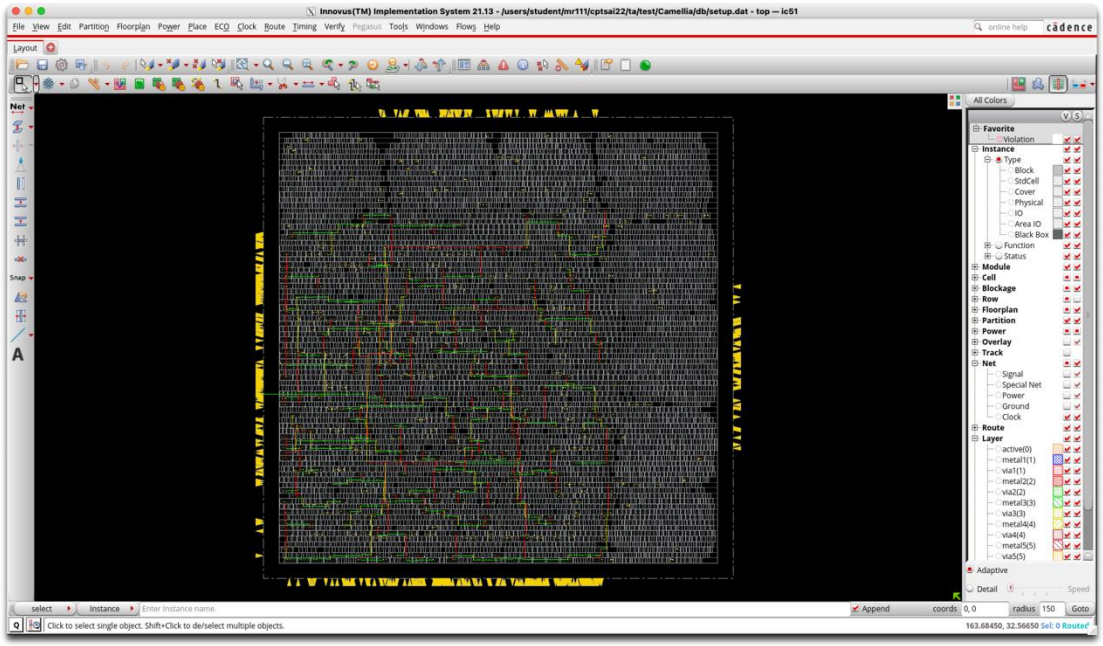
D. Clock Tree Synthesis (CTS)

You can see the clock tree by doing the following instruction:

1. Make sure “Route” checkbox is checked and uncheck the “Net” checkbox.
2. Double click on the “Net” and then check the “Clock” checkbox.



After these steps you can see picture like this (the clock tree is showed):



E. Power Planning

Step 1. Connect Global Net

Window > Power > Connect Global Net…

Power Ground Connection > Connect

Pin	Selected
Pin Name(s)	VDD

Power Ground Connection > Scope

Apply All	Selected

Power Ground Connection

To Global Net	VDD

Then click **Add to List**

Power Ground Connection > Connect

Pin	Selected
Pin Name(s)	VSS

Power Ground Connection > Scope

Apply All	Selected

Power Ground Connection

To Global Net	VSS

Then click **Add to List**

Click **Apply** and **close the pop-up window**

Step 2. Construct Power Network

Window > Power > Power Planning > Add Ring…

Basic

Net(s)	VDD VSS

Ring Configuration

Layer (T/B/L/R)	6/6/5/5
Width (T/B/L/R)	0.6/0.6/0.6/0.6
Spacing (T/B/L/R)	0.5/0.5/0.5/0.5
Offset: Center in channel	Selected

Then click **OK**

Window > Power > Power Planning > Add Stripe…

Basic

Set Configuration

Net(s)	VDD VSS
Layer	metal6(6)
Width	0.4
Spacing	0.5

Set Pattern

Set-to-set distance	5

First/Last Stripe

Relative from core or selected area	Start: 0.5

Then click **Apply**

Set Configuration

Net(s)	VDD VSS
Layer	metal5(5)
Width	0.4
Spacing	0.5

Set Pattern

Set-to-set distance	5

First/Last Stripe

Relative from core or selected area	Start: 0.5

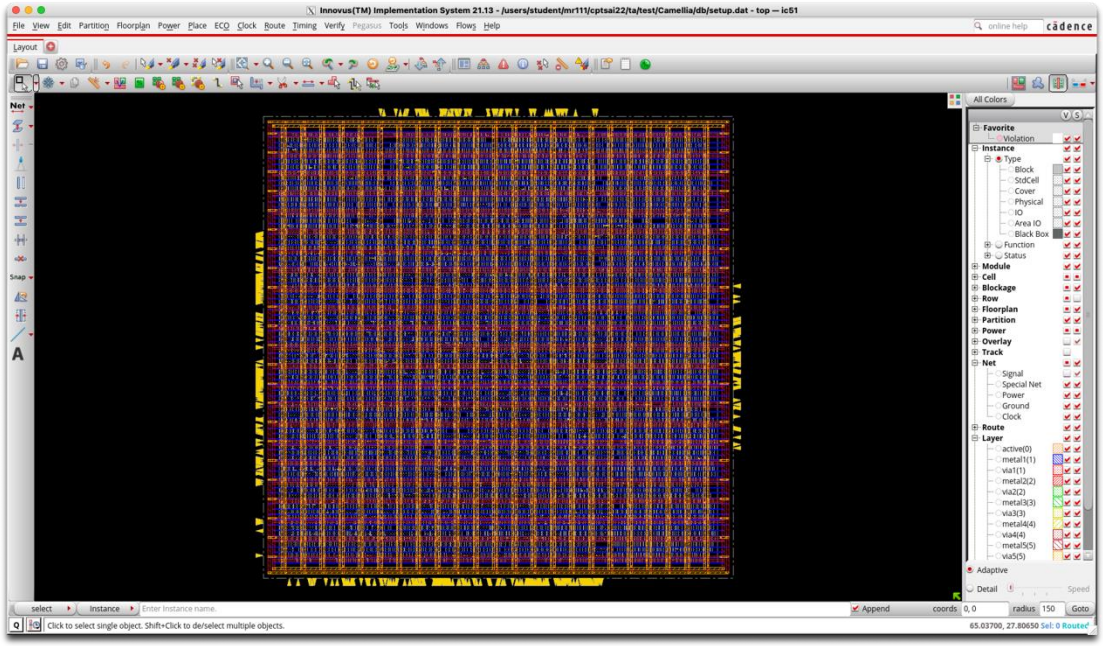
Then click **OK**

Window > Route > Special Route…

Net(s)	VDD VSS

Then click **OK**

After these steps you can see the power planning result like this (remember to check the “Net” checkbox)



Step 3. Save design

Window > File > Save Design…

Data Type	Select “Innovus”
Path Name	placement

Then click **OK**

F. Route (Clock Nets and Signal Nets)

Step 1. Route Design

Window > Route > NanoRoute > Route…

Then click **OK**

Step 2. Analyze timing (setup and hold) and check routability

```
innovus> report_timing
```

Is there any timing violation (slack < 0)?

(slack = required time - arrival time. If slack < 0, it is failed.)

Step 3. Optimize routing results

If there is any timing violation, you can try to fix them by following command:

```
innovus> setAnalysisMode -analysisType onChipVariation
innovus> optDesign -postRoute
```

(Only when there is a problem are the Innovus commands with a gray background required to execute.)

Step 4. Fix DRC violations

Check if there are any DRC violations in the current design by the following command:

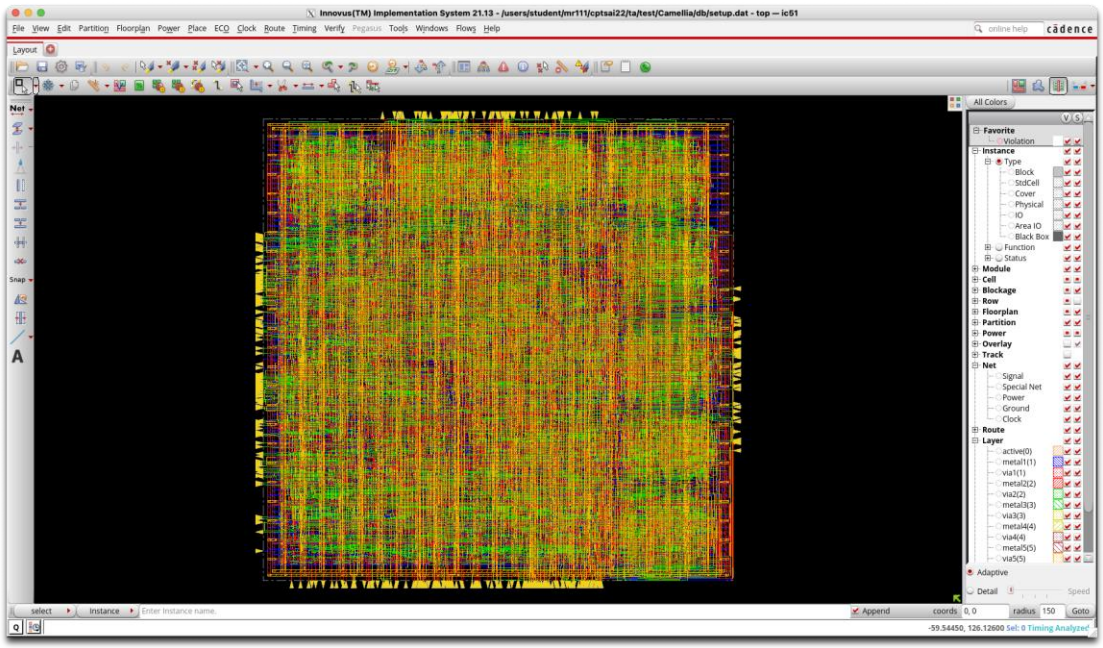
```
innovus> verify_drc
```

If there are any DRC violations, you can try to fix them by the following command:

```
innovus> ecoRoute -fix_drc
```

If there are still any DRC violations, you should attempt to reduce core utilization during the floorplan stage and then redo all the steps mentioned above.

You can see the routing results as follows.



Step 5. Save design

Window > File > Save Design…

Data Type	Select “Innovus”
Path Name	route

Then click **OK**

G. Insert Filler Cells

(Why insert filler cells? Please google it and write down the explanations in your report.)

Step 1. Insert standard cell filler and connect P/G nets of cells

```
innovus> getCTSMode -engine -quiet
innovus> getFillerMode -quiet
innovus> addFiller -cell {FILLCELL_X1 FILLCELL_X2 FILLCELL_X4
FILLCELL_X8 FILLCELL_X16 FILLCELL_X32} -prefix FILL
```

Step 2. Save design

Window > File > Save Design…

Data Type	Select “Innovus”
Path Name	post_route

Then click **OK**

Step 3. Dump report

```
innovus> report_timing > timing.rpt
innovus> summaryReport -noHtml -outfile summary.rpt
```

You can find the total area of chip (`Total area of Chip`) and total wire length (`Total wire length`) in the summary.rpt file.

```
innovus> verify_drc > drc.rpt
```

Step 4. Take a snapshot of your final layout

Paste this layout figure into your report.

Step 5. Exit

```
innovus> exit
```

P.S. Using TCL

When the last time you exit the Innovus, all your GUI operations are translated as commands and are stored in the file “innovus.cmd.” You could copy it into “apr.tcl” and modify it as you wish. Next time you can just enter the following command in Innovus to complete the whole process.

```
innovus> source apr.tcl
```