Org: Interrupts

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Contents

1 Interrupts in 8086/8088

- 256 types
- type × 4 = PA of interrupt vector
- IVT: first 1KB

2 Hardware Interrupts

- maskable interrupt (INTR)
    - IF = 1, enable
    - STI sets IF, CLI clears IF
    - interrupt requests from external I/O
- non-maskable (NMI)
    - RAM parity check error
    - interrupt from co-processor

2.1 Procedure

- CPU responds to INTR
    - check INTR on the last cycle, INTR and IF = 1
    - CPU sends 2 negative pluses on !INTA pin
    - upon receiving second !INTA, I/O device sends interrupt type on data bus
- CPU executes ISR of INT N
    - reads N from data bus
    - push FR in stack
    - clear IF, TF
    - push CS, IP to stack
    - load ISR entrance
    - upon return, pop IP, CS, FR, returns previous program

3 Software Interrupts

- `INT xx`
    - e.g. `INT 21H` DOS service
- exceptions (predefined)
- CPU always responds (ignore IF)

3.1 Difference between INT and CALL

- call far can jump anywhere (within 1MB)
- call is in sequential instructions

- call cannot be masked
- call doesn’t save FR
- RETF / RET

3.2 Predefined conditional interrupts

- 00 divide error
- 01 single step
- 03 breakpoint
- 04 signed number overflow

4 Interrupt Priority

- INT > NMI > INTR

4.1 Priority of INTR

- software polling, sequence of checking
- hardware checking, location in daisy chain
- interrupt controller (8259) programmable

4.2 Interrupt Nesting

- higher priority interrupts lower priority
- STI: controls whether responds to interrupt (IF)
- EOI: service complete (IS in 8259)