Arch: Multi-Cycle Processor

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1 Clocking Methodology

- Cycle Time = CLK-to-Q + Longest Delay Path + Setup + Clock Skew

2 Instruction Critical Path

- instruction and memory access
- ALU and adders
- register file access
- different inst has different critical path, which is a waste
- functional units has to be duplicated

3 Multi-cycle Approach

- balance amount of work in each step
- use every major unit per cycle
- store values
  - IR
  - MDR
  - A and B
  - ALUout
  - program visible state
- therefore
  - multiplexer before functional unit
  - read from register file
  - r/w to register happens at the beginning of clock cycle
  - all stage in parallel
    - one ALU op, one memory access, one register file, one OP

4 Five Stage

- instruction fetch
- instruction decode / register fetch
- ALU (execute)
- memory access
- write back
- refer to RTL in slides
- key idea: control unit is a state machine, which produces signals state by state