Johns Hopkins Engineering

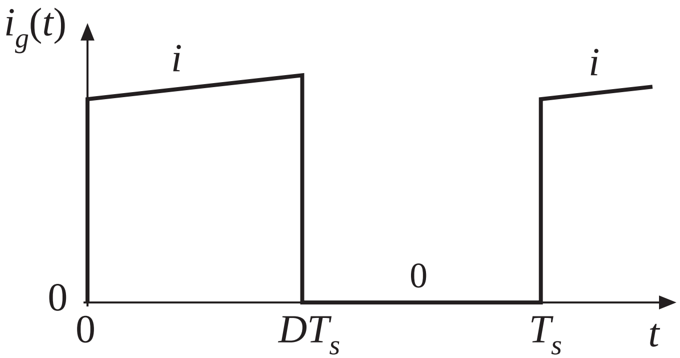
Power Electronics 525.725

Module 10 Lecture 10

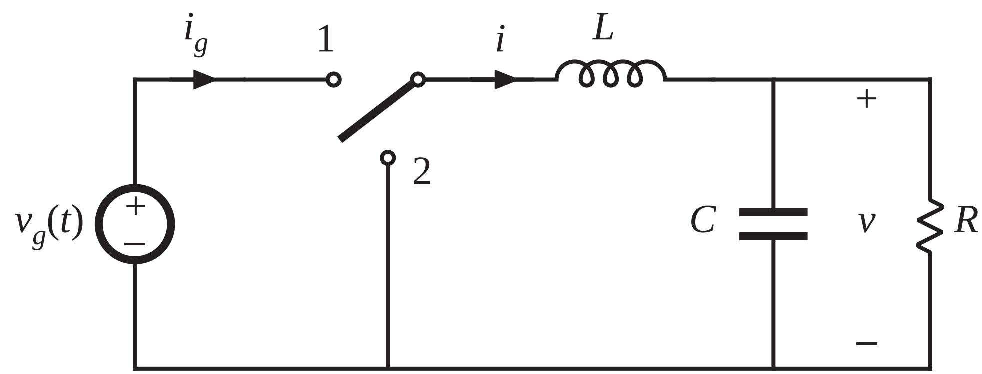
Conducted EMI and Filter Design

10.1.1 Conducted Electromagnetic Interference (EMI)

Input current $i_g(t)$ is *pulsating*:



Buck converter example

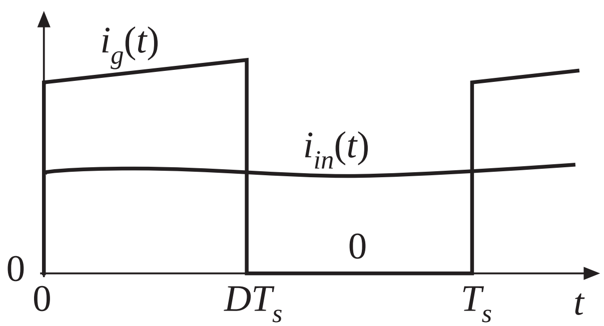


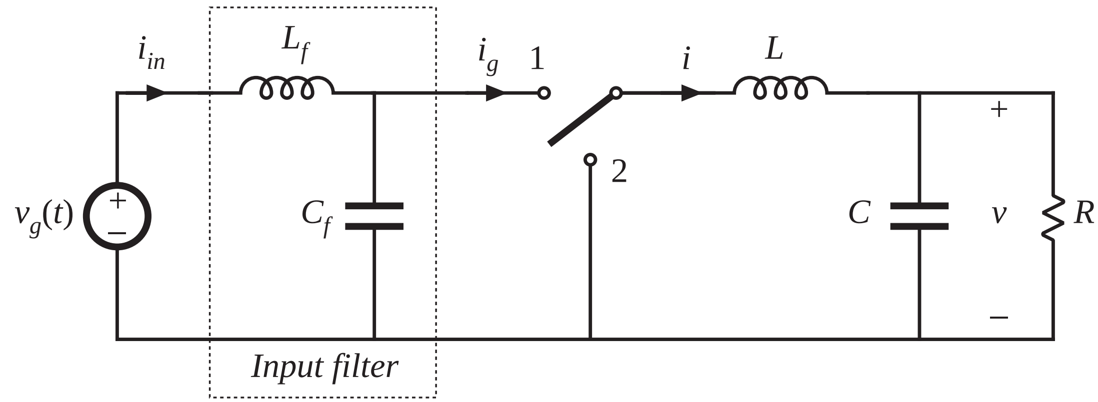
Approximate Fourier series of $i_g(t)$:

$$i_g(t) = DI + \sum_{k=1}^{\infty} \frac{2I}{k\pi} \sin\left(k\pi D\right) \cos\left(k\omega t\right)$$

High frequency current harmonics of substantial amplitude are injected back into $v_g(t)$ source. These harmonics can interfere with operation of nearby equipment. Regulations limit their amplitude, typically to values of 10 µA to 100 µA.

Addition of Low-Pass Filter





Magnitudes and phases of input current harmonics are modified by input filter transfer function $H(s)$:

$$i_{in}(t) = H(0)DI + \sum_{k=1}^{\infty} \left\| H(kj\omega) \right\| \frac{2I}{k\pi} \sin\left(k\pi D\right) \cos\left(k\omega t + \angle H(kj\omega)\right)$$

The input filter may be required to attenuate the current harmonics by factors of 80 dB or more.

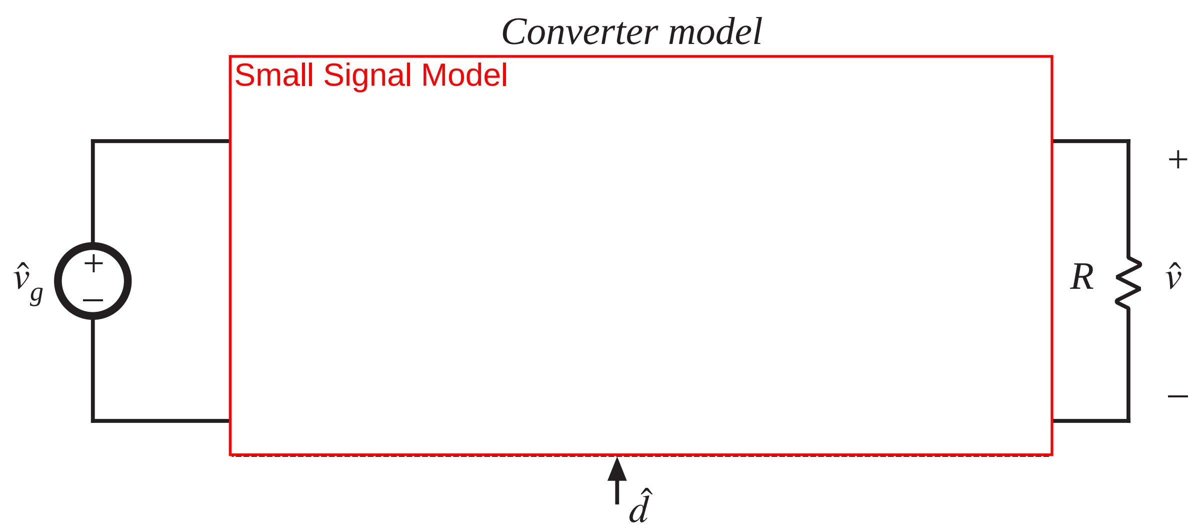
10.1.2 The Input Filter Design Problem

A typical design approach:

1. Engineer designs switching regulator that meets specifications (stability, transient response, output impedance, etc.). In performing this design, a basic converter model is employed, such as the one below:

(no input filter)

(buck converter example)

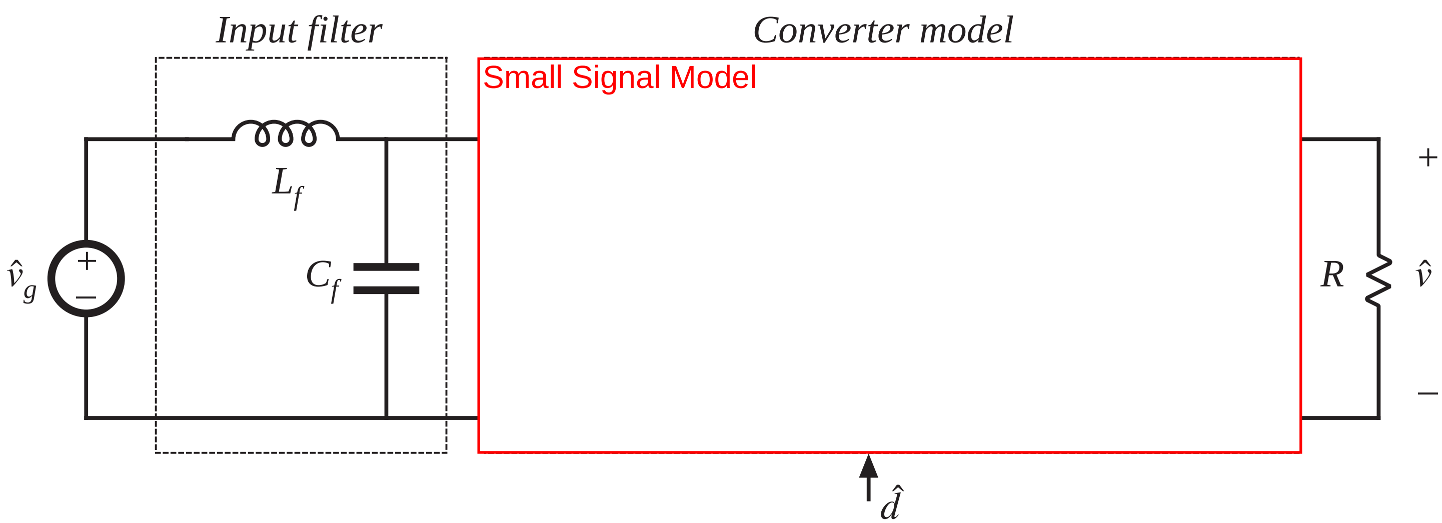


Input Filter Design Problem, p. 2

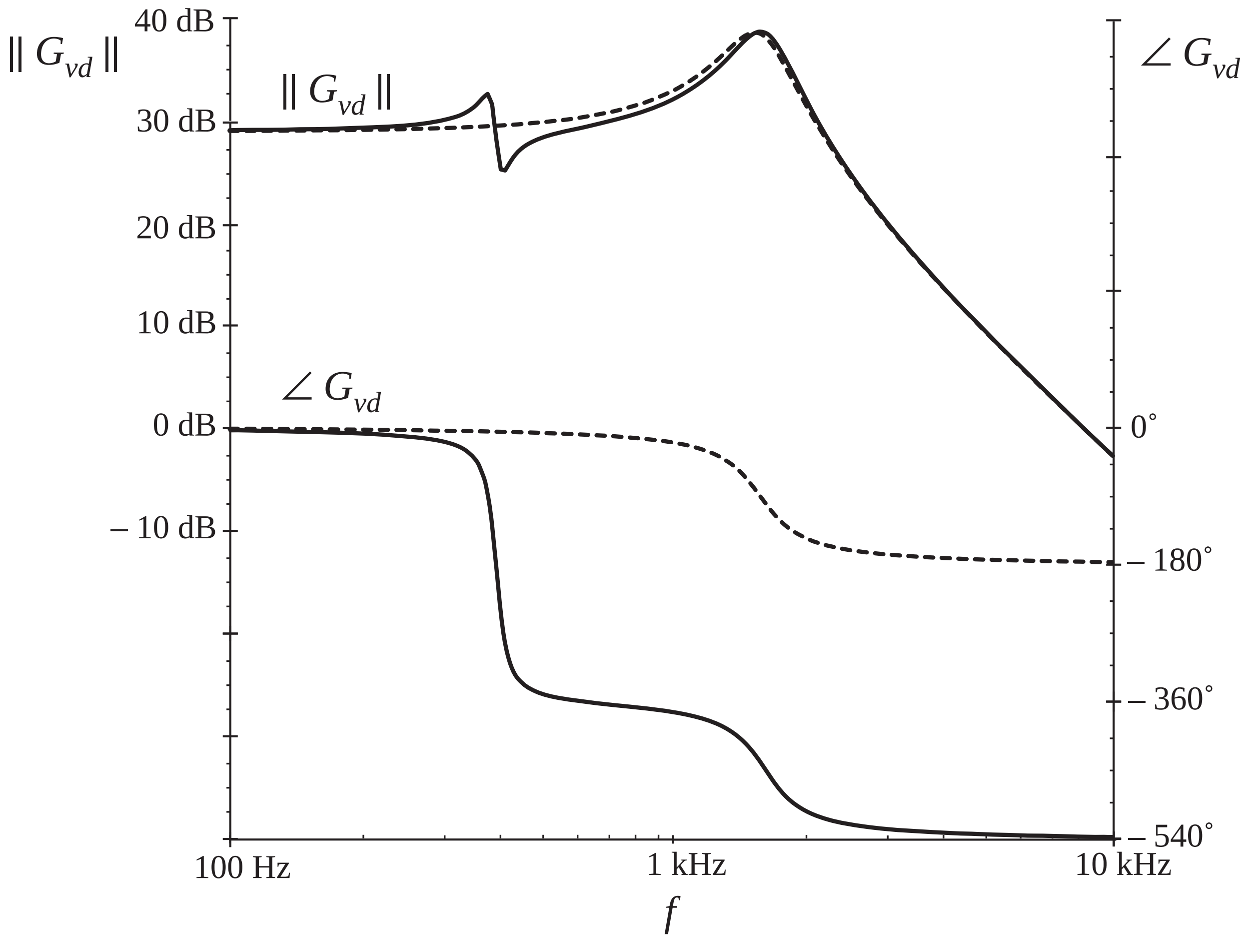
2. Later, the problem of conducted EMI is addressed. An input filter is added, that attenuates harmonics sufficiently to meet regulations.
3. A new problem arises: the controller no longer meets dynamic response specifications. The controller may even become unstable.

Reason: input filter changes converter transfer functions

Converter ac model is modified by input filter



Input Filter Design Problem, p. 3

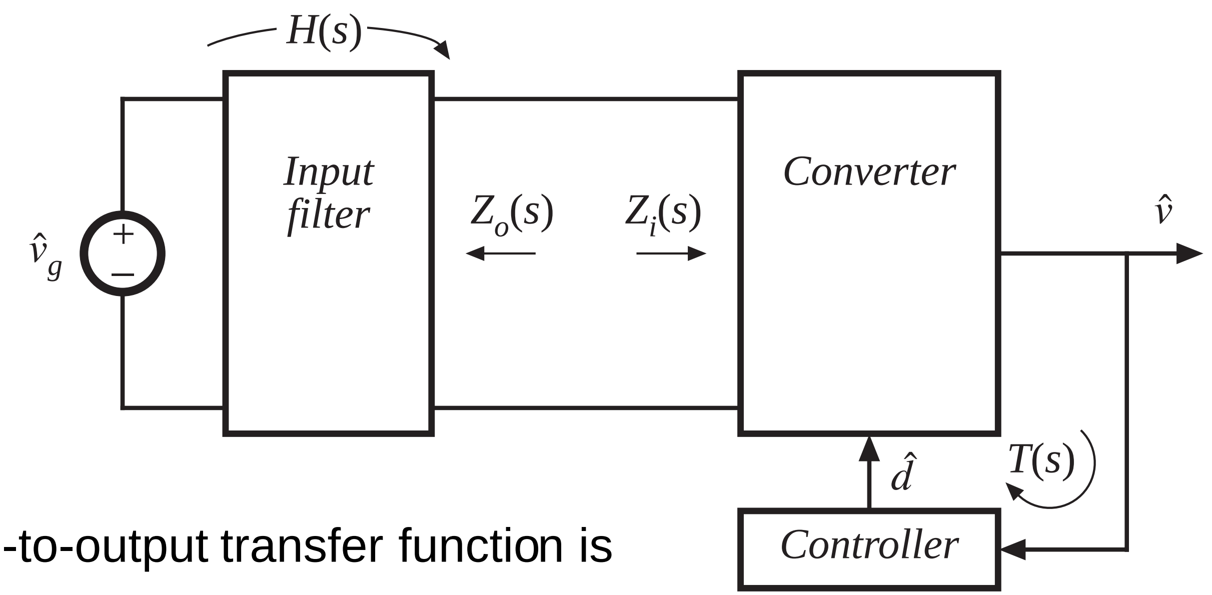


Effect of L-C input filter on control-to-output transfer function $G_{vd}(s)$, buck converter example.

Dashed lines: original magnitude and phase

Solid lines: with addition of input filter

10.2 Effect of an Input Filter on Converter Transfer Functions



Control-to-output transfer function is

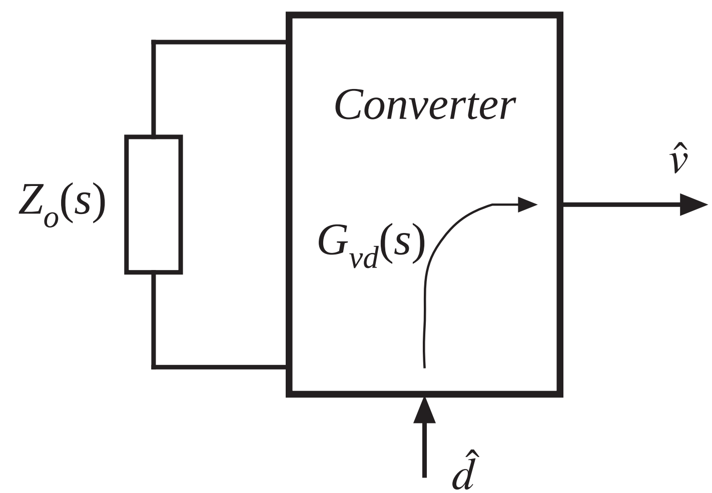
$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s) = 0}$$

Determination of $G_{vd}(s)$

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s) = 0}$$

$\hat{v}_g(s)$ source ➞ short circuit

$Z_o(s)$ = output impedance of input filter



We will use Middlebrook's Extra Element Theorem to show that the input filter modifies $G_{vd}(s)$ as follows:

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s) = 0} \right) \frac{\left(1 + \frac{Z_o(s)}{Z_N(s)}\right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)}\right)}$$

10.2.2 Impedance Inequalities

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s) = 0} \right) \frac{\left(1 + \frac{Z_o(s)}{Z_N(s)} \right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)} \right)}$$

The *correction factor* $\frac{\left(1 + \frac{Z_o(s)}{Z_N(s)} \right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)} \right)}$ shows how the input filter modifies the transfer function $G_{vd}(s)$.

The correction factor has a magnitude of approximately unity provided that the following inequalities are satisfied:

$$\left\| Z_o \right\| \ll \left\| Z_N \right\|, \quad \text{and}$$
$$\left\| Z_o \right\| \ll \left\| Z_D \right\|$$

These provide design criteria, which are relatively easy to apply.

How an input filter changes $G_{vd}(s)$
Summary of result

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s)=0} \right) \frac{\left(1 + \frac{Z_o(s)}{Z_N(s)}\right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)}\right)}$$

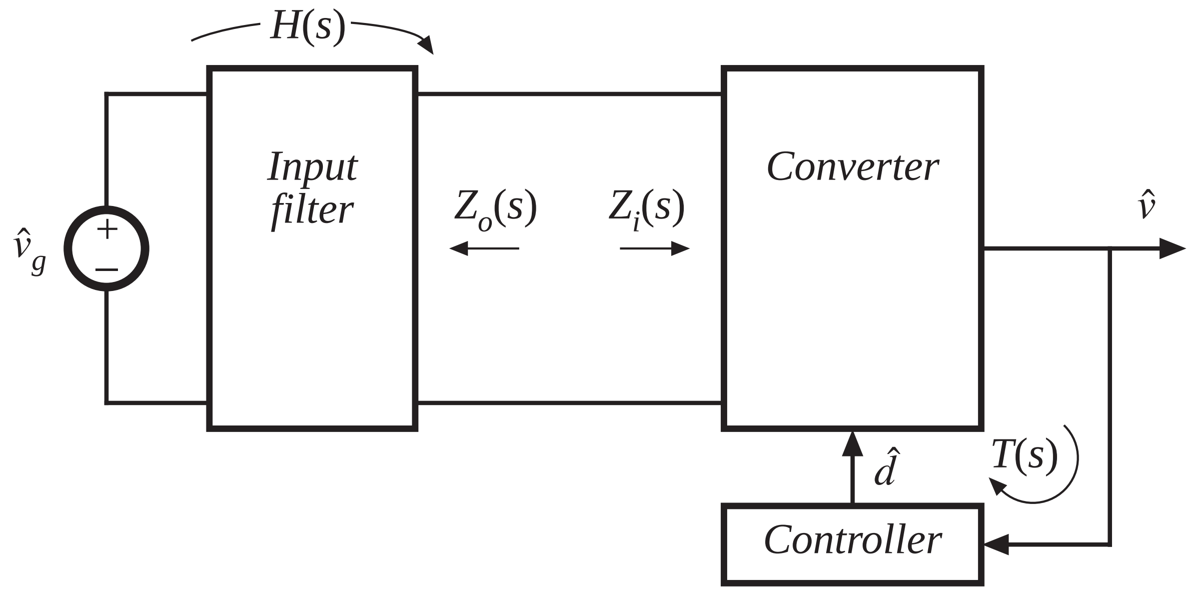
$G_{vd}(s) \Big|_{Z_o(s)=0}$ is the original transfer function, before addition of input filter

$Z_D(s) = Z_i(s) \Big|_{\hat{d}(s)=0}$ is the converter input impedance, with $\hat{d}$ set to zero

$Z_N(s) = Z_i(s) \Big|_{\hat{v}(s) \xrightarrow[\text{null}]{} 0}$ is the converter input impedance, with the output $\hat{v}$ nulled to zero

(see Appendix C for proof using EET)

10.2.1 Discussion



$Z_N(s) = Z_i(s)\Big|_{\hat{v}(s) \xrightarrow[\text{null}]{} 0}$ is the converter input impedance, with the output $\hat{v}$ nulled to zero

Note that this is the same as the function performed by an ideal controller, which varies the duty cycle as necessary to maintain zero error of the output voltage. So Z_N coincides with the input impedance when an ideal feedback loop perfectly regulates the output voltage.

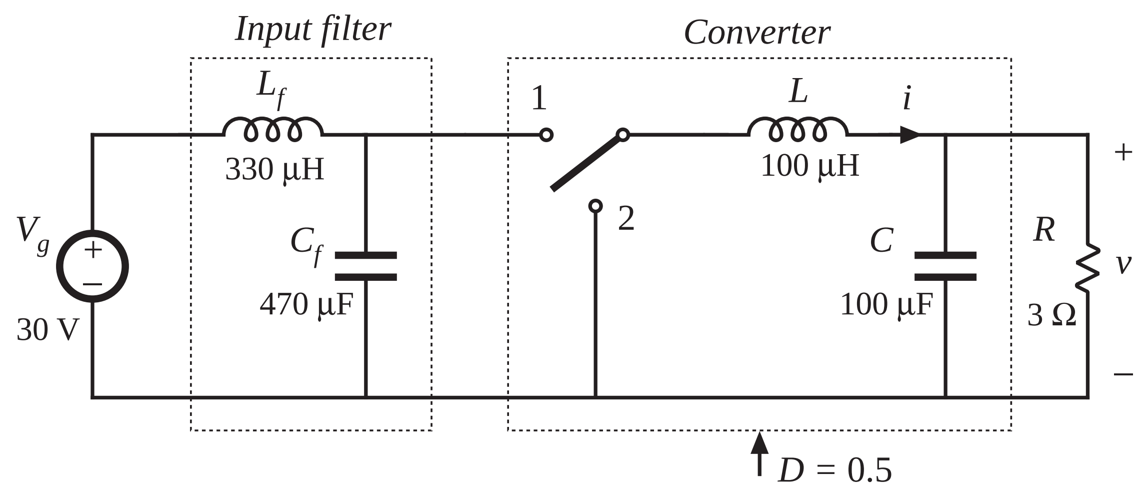
Design criteria for basic converters

Table 10.1 Input filter design criteria for basic converters

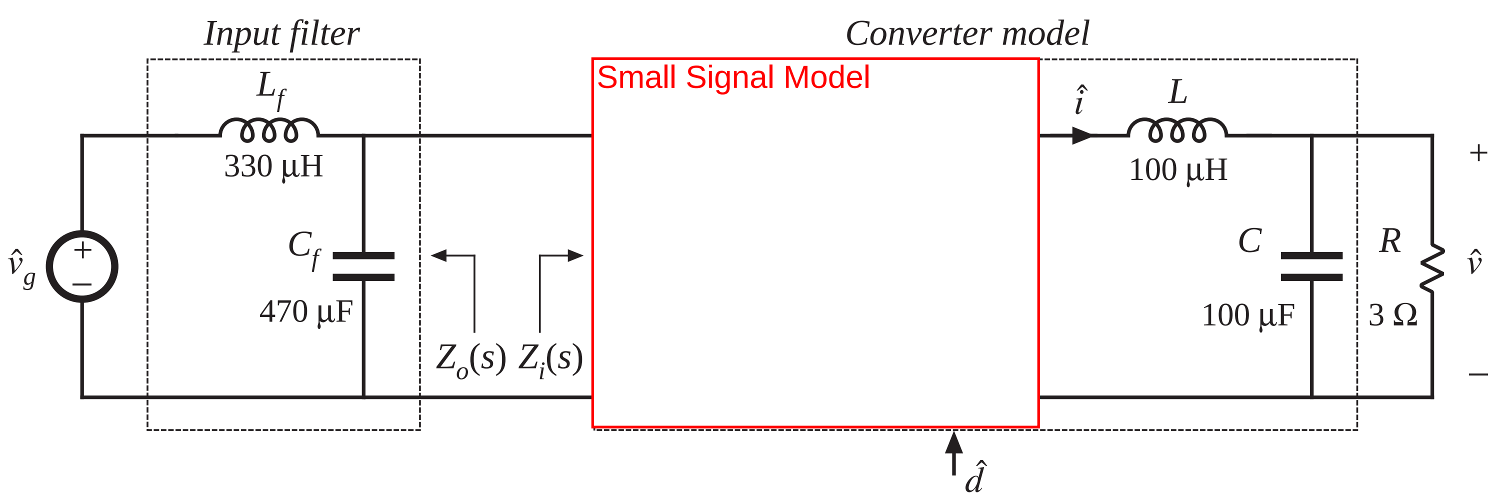
Converter	$Z_N(s)$	$Z_D(s)$	$Z_e(s)$
Buck	$-\frac{R}{D^2}$	$\frac{R}{D^2}\frac{\left(1+s\frac{L}{R}+s^2LC\right)}{\left(1+sRC\right)}$	$\frac{sL}{D^2}$
Boost	$-D'^2R\left(1-\frac{sL}{D'^2R}\right)$	$D'^2R\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{\left(1+sRC\right)}$	sL
Buck–boost	$-\frac{D'^2R}{D^2}\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{D'^2R}{D^2}\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{\left(1+sRC\right)}$	$\frac{sL}{D^2}$

10.3 Buck Converter Example
10.3.1 Effect of undamped input filter

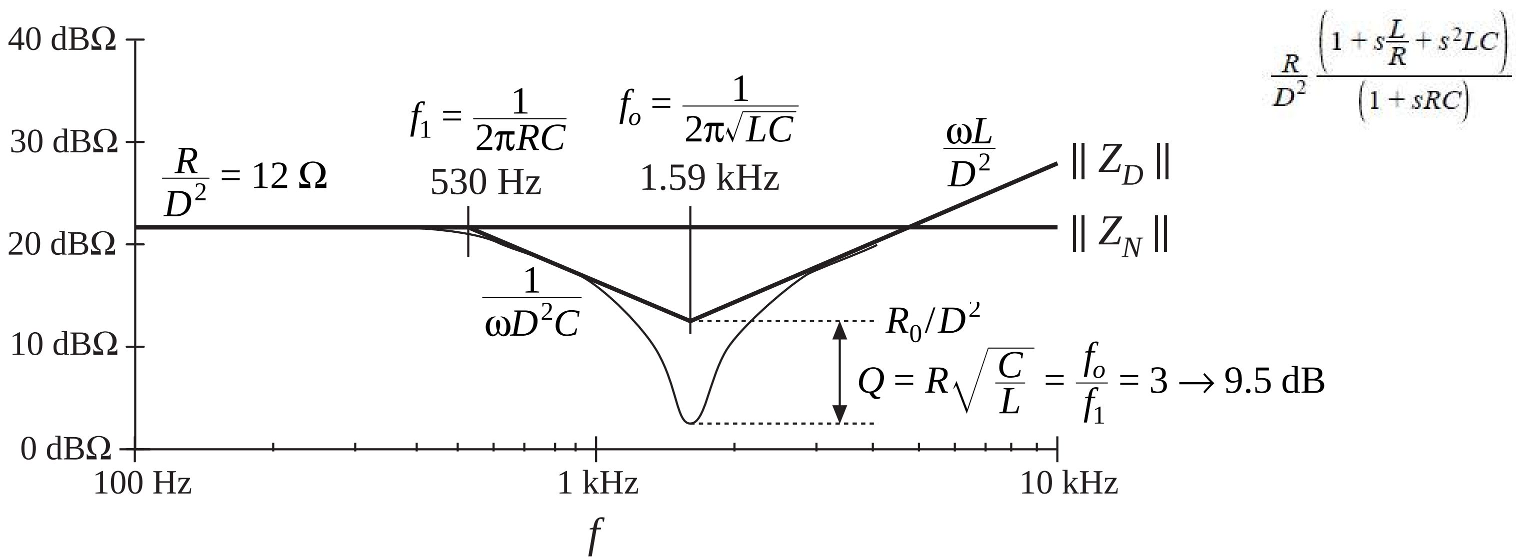
Buck converter with input filter



Small-signal model



Determination of Z_D



Determination of Z_N

Solution:

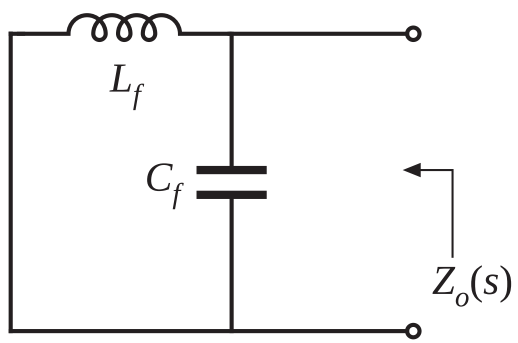
$$\hat{i}_{test}(s) = I\hat{d}(s)$$

$$\hat{v}_{test}(s) = -\frac{V_g \hat{d}(s)}{D}$$

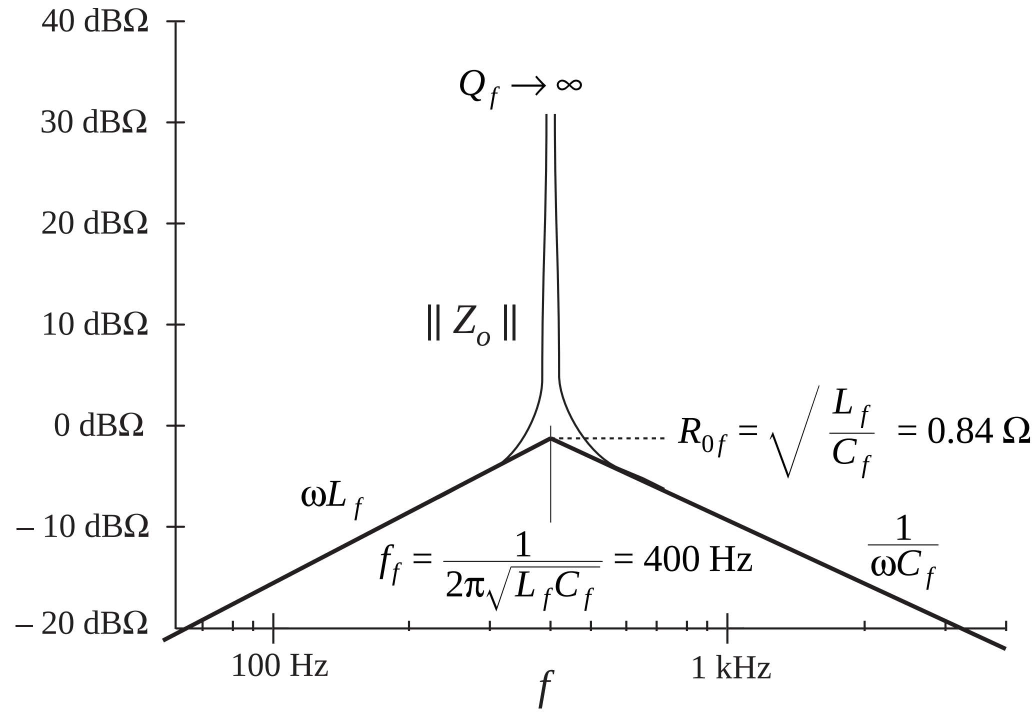
Hence,

$$Z_N(s) = \frac{\left(-\dfrac{V_g \hat{d}(s)}{D}\right)}{\left(I\hat{d}(s)\right)} = -\frac{R}{D^2}$$

Z_o of undamped input filter



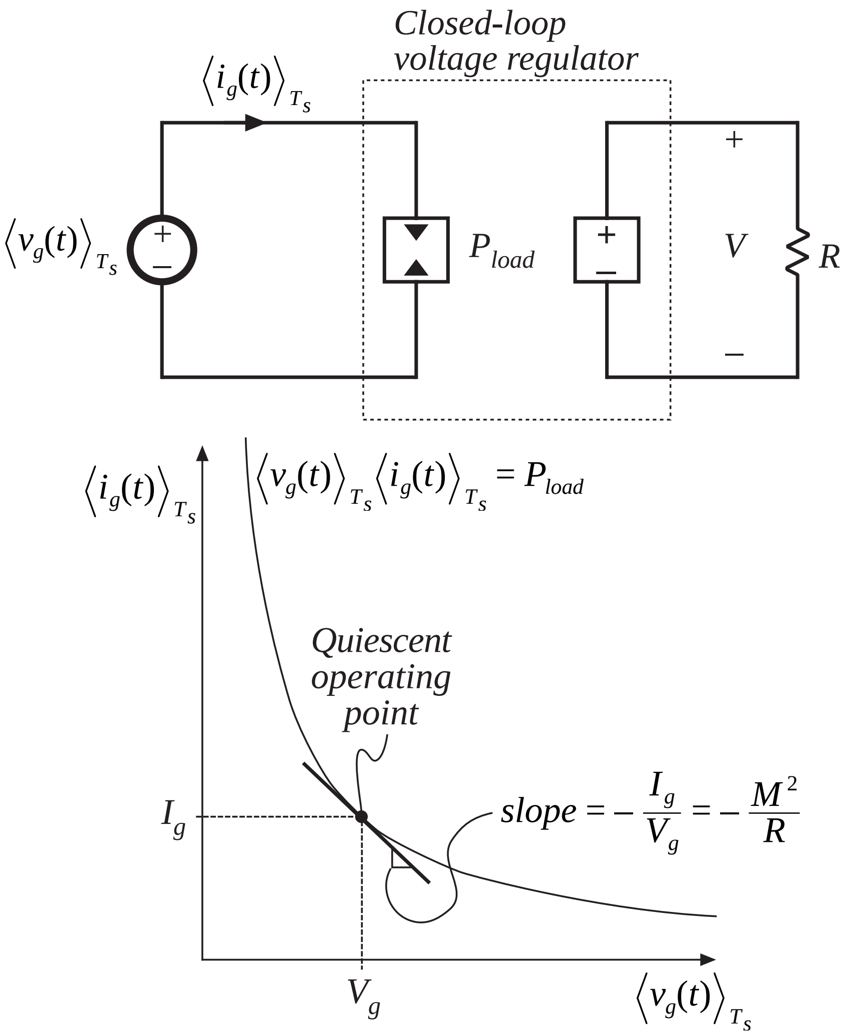
$$Z_o(s) = sL_f \| \frac{1}{sC_f}$$



No resistance, hence poles are undamped (infinite Q-factor).

In practice, losses limit Q-factor; nonetheless, Q_f may be very large.

When the output voltage is perfectly regulated



- For a given load characteristic, the output power P_{load} is independent of the converter input voltage
- If losses are negligible, then the input port i-v characteristic is a power sink characteristic, equal to P_{load}:

$$\langle v_g(t)\rangle_{T_s}\langle i_g(t)\rangle_{T_s} = P_{load}$$

- Incremental input resistance is negative, and is equal to:

$$-\frac{R}{M^2}$$

(same as dc asymptote of Z_N)

Negative resistance oscillator

It can be shown that the closed-loop converter input impedance is given by:

$$\frac{1}{Z_i(s)} = \frac{1}{Z_N(s)} \frac{T(s)}{1 + T(s)} + \frac{1}{Z_D(s)} \frac{1}{1 + T(s)}$$

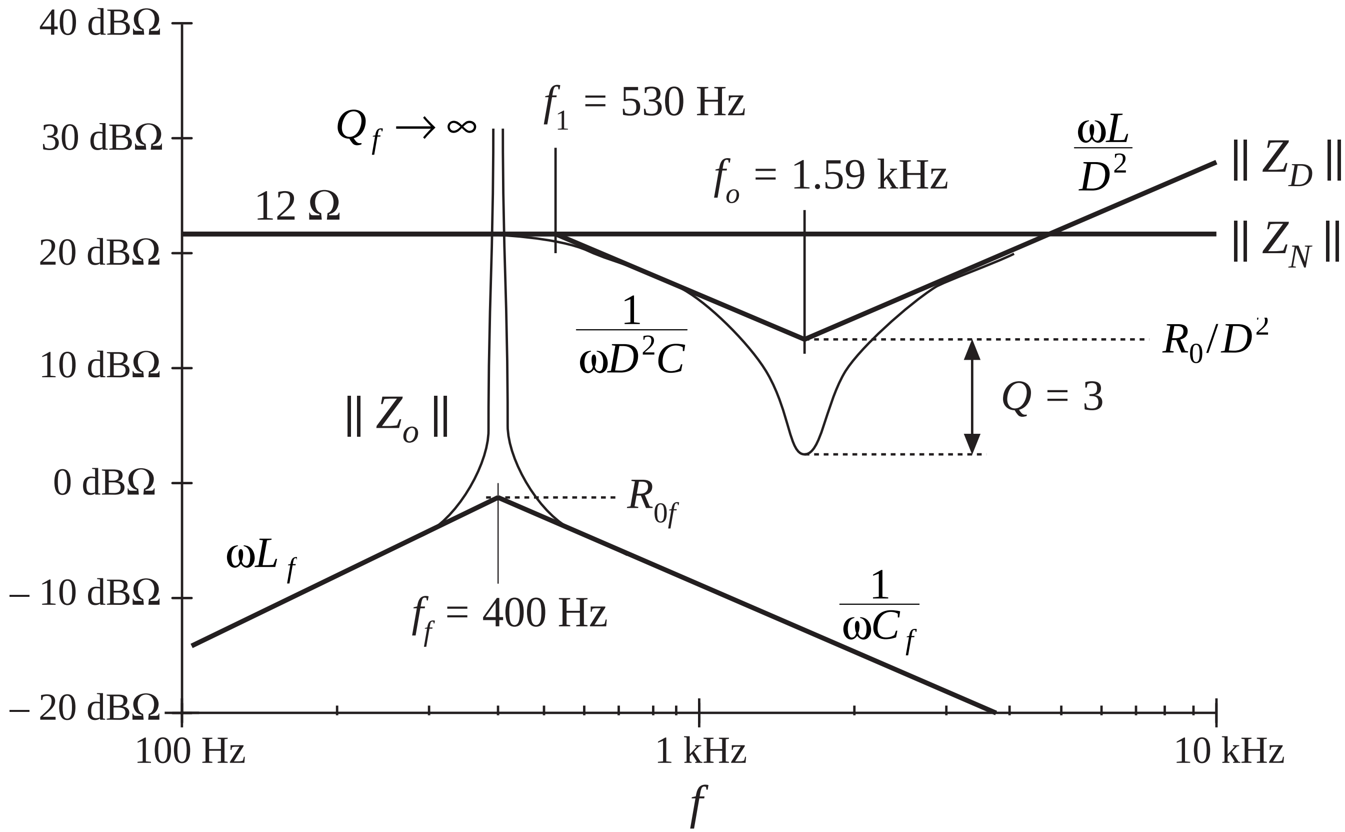
where $T(s)$ is the converter loop gain.

At frequencies below the loop crossover frequency, the input impedance is approximately equal to Z_N, which is a negative resistance.

When an undamped or lightly damped input filter is connected to the regulator input port, the input filter can interact with Z_N to form a *negative resistance oscillator*.

Design criteria

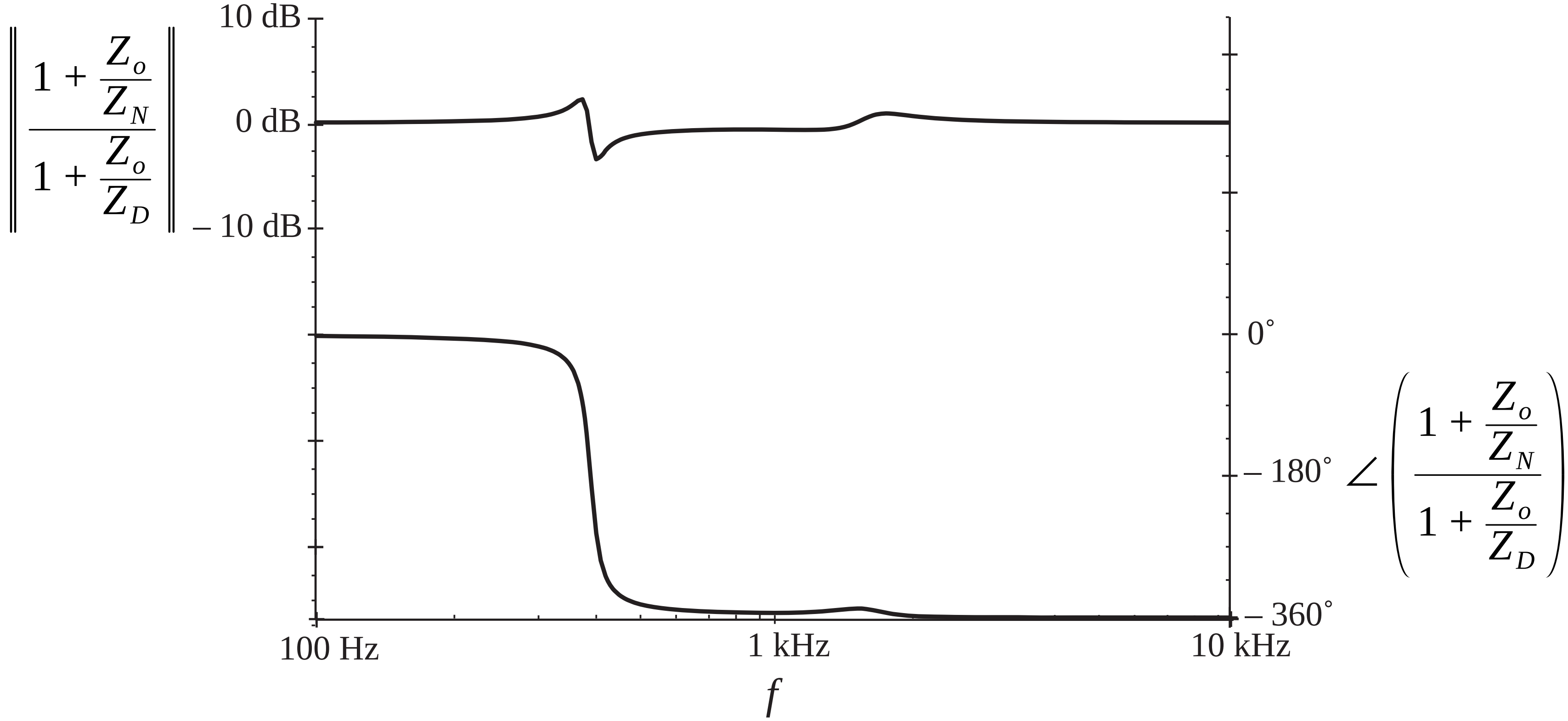
$$\left\| Z_o \right\| \ll \left\| Z_N \right\|, \quad \text{and}$$
$$\left\| Z_o \right\| \ll \left\| Z_D \right\|$$



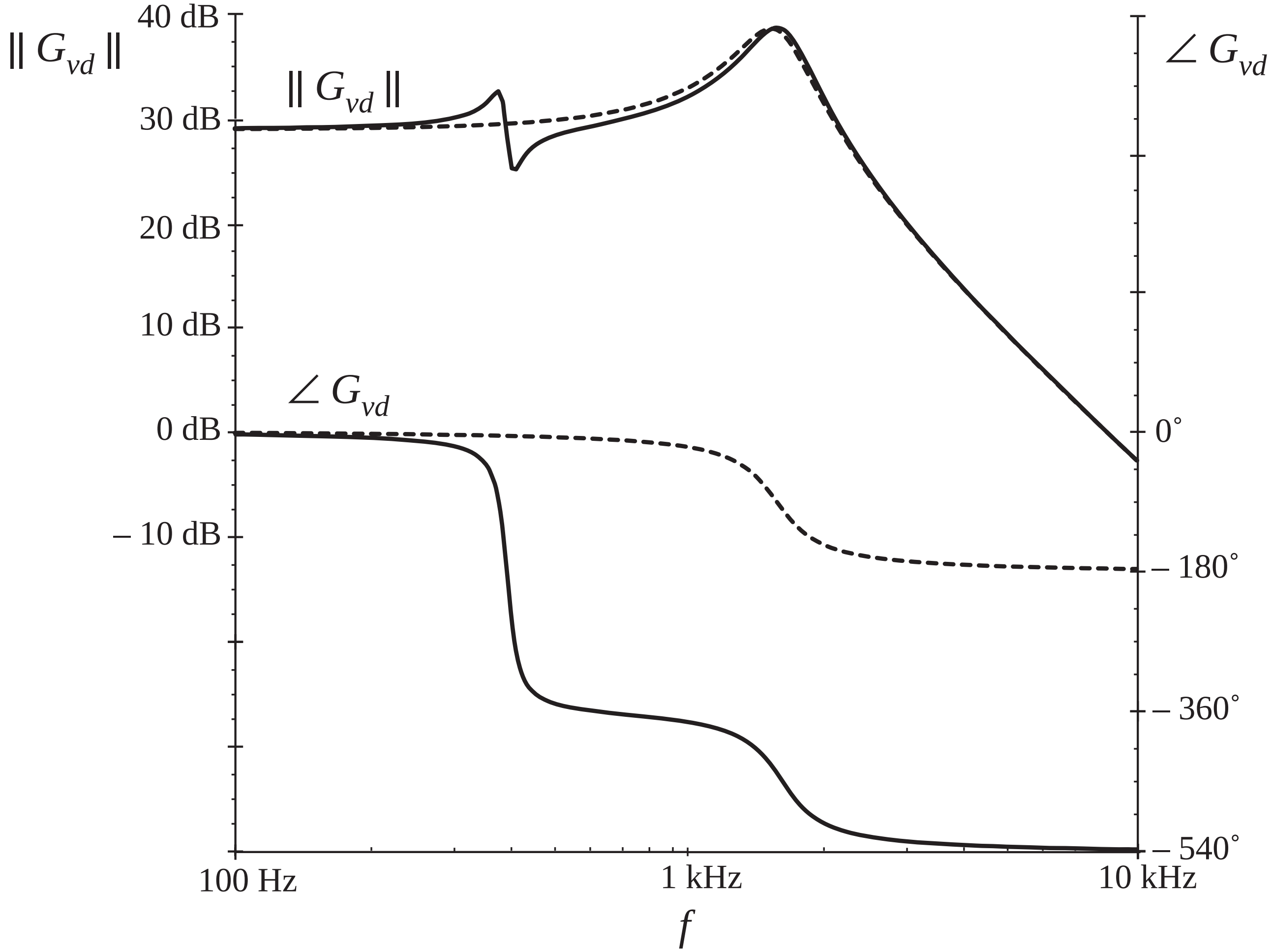
Can meet inequalities everywhere except at resonant frequency f_f.

Need to damp input filter!

Resulting correction factor



Resulting transfer function

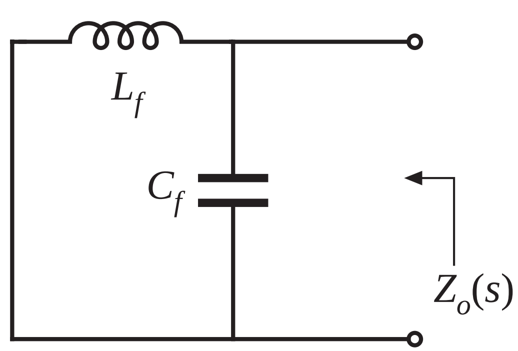


Dashed lines: no input filter

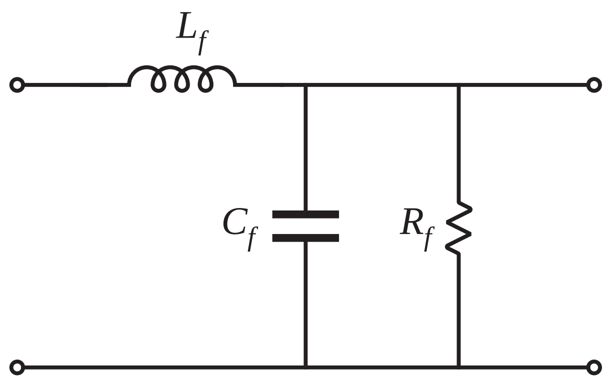
Solid lines: including effect of input filter

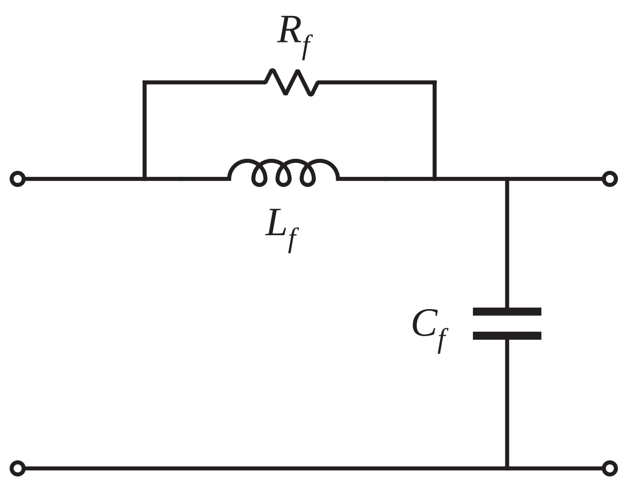
10.3.2 Damping the input filter

Undamped filter:



Two possible approaches:

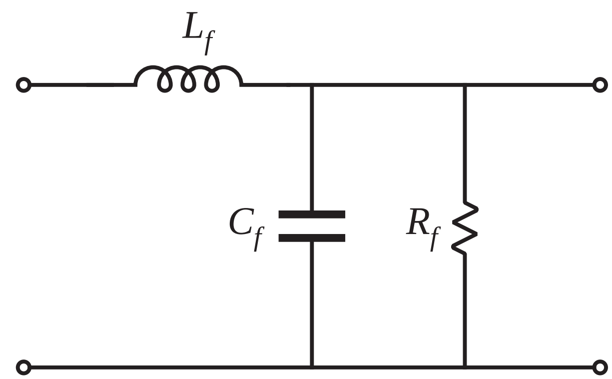




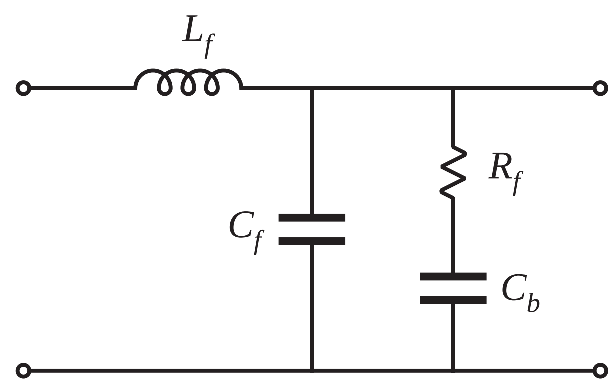
Addition of R_f across C_f

To meet the requirement $R_f \ll \| Z_N \|$:

$$R_f \ll \frac{R}{D^2}$$



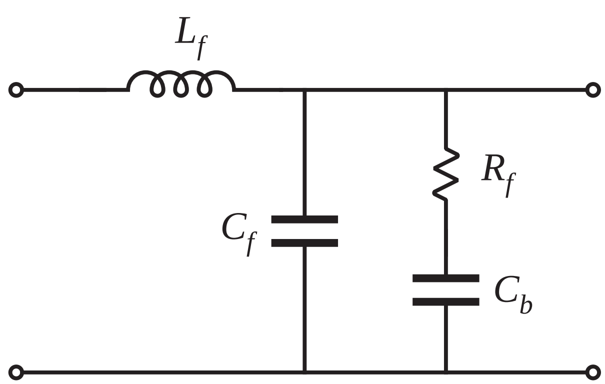
The power loss in R_f is V_g^2 / R_f, which is larger than the load power!



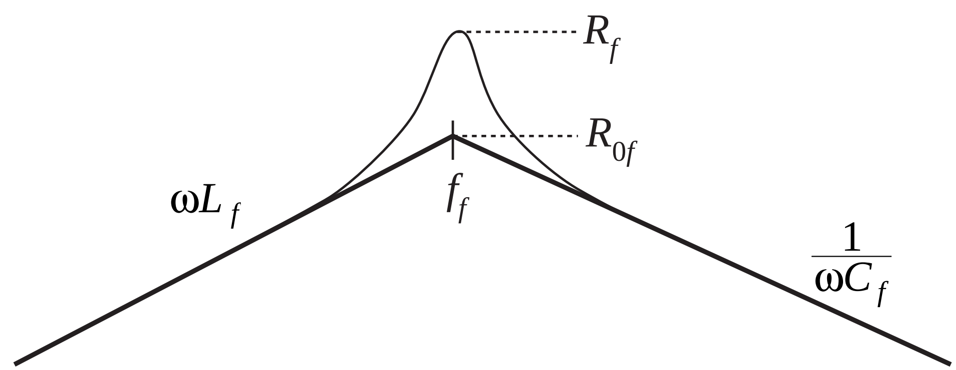
A solution: add dc blocking capacitor C_b.

Choose C_b so that its impedance is sufficiently smaller than R_f at the filter resonant frequency.

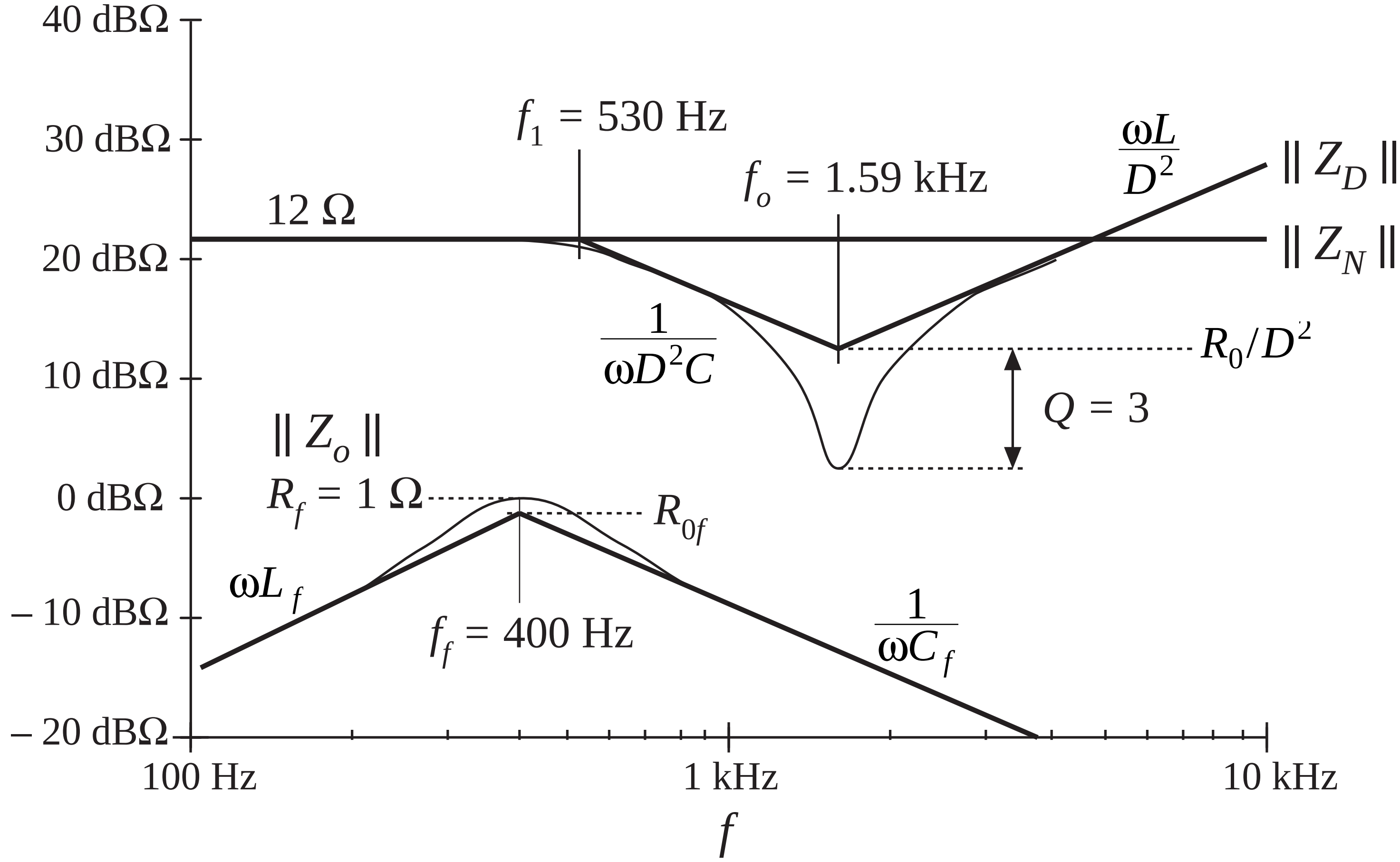
Damped input filter



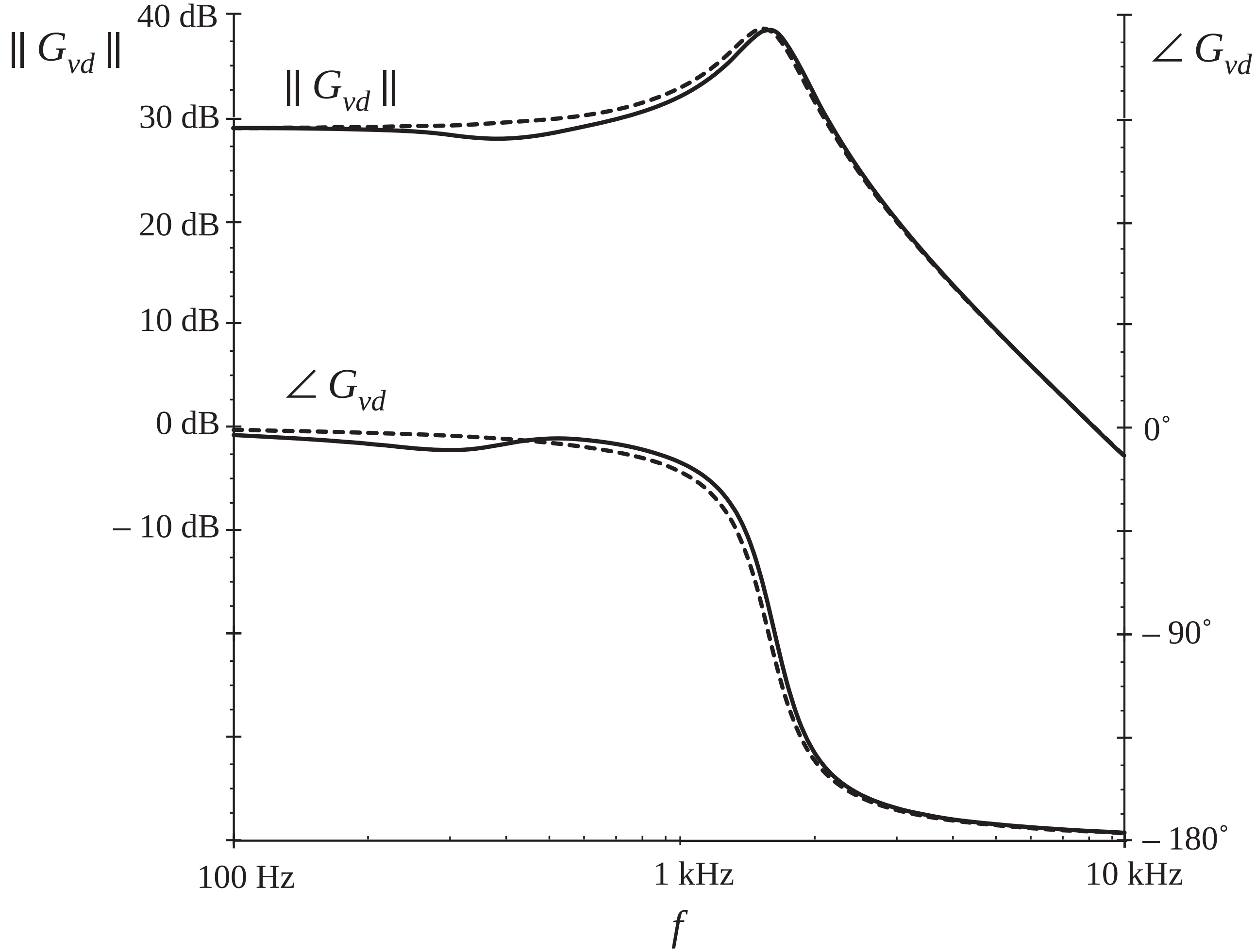
$\| Z_o \|$, with large C_b



Design criteria, with damped input filter



Resulting transfer function

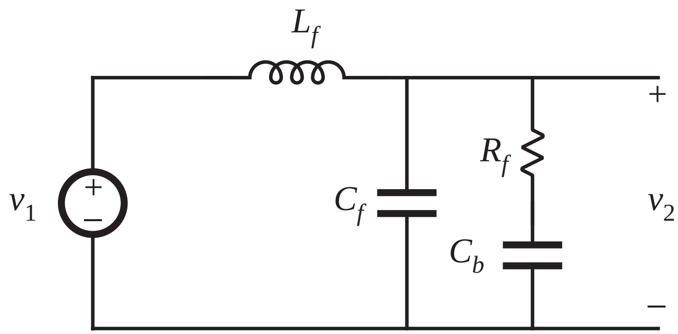


Dashed lines: no input filter

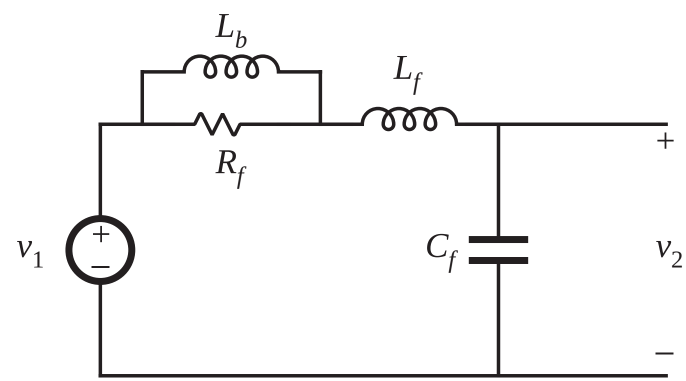
Solid lines: including effect of input filter

10.4 Design of a Damped Input Filter

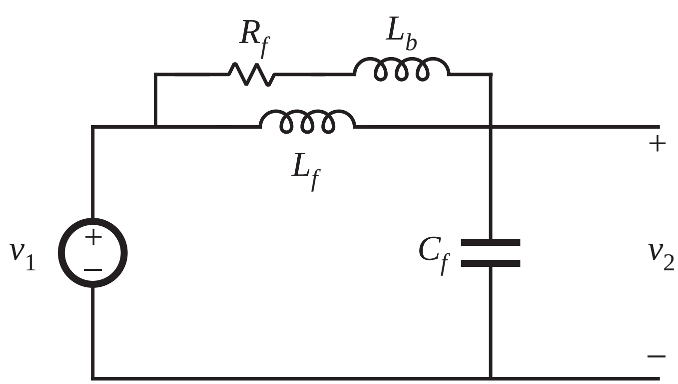
R_f–C_b Parallel Damping



R_f–L_b Series Damping

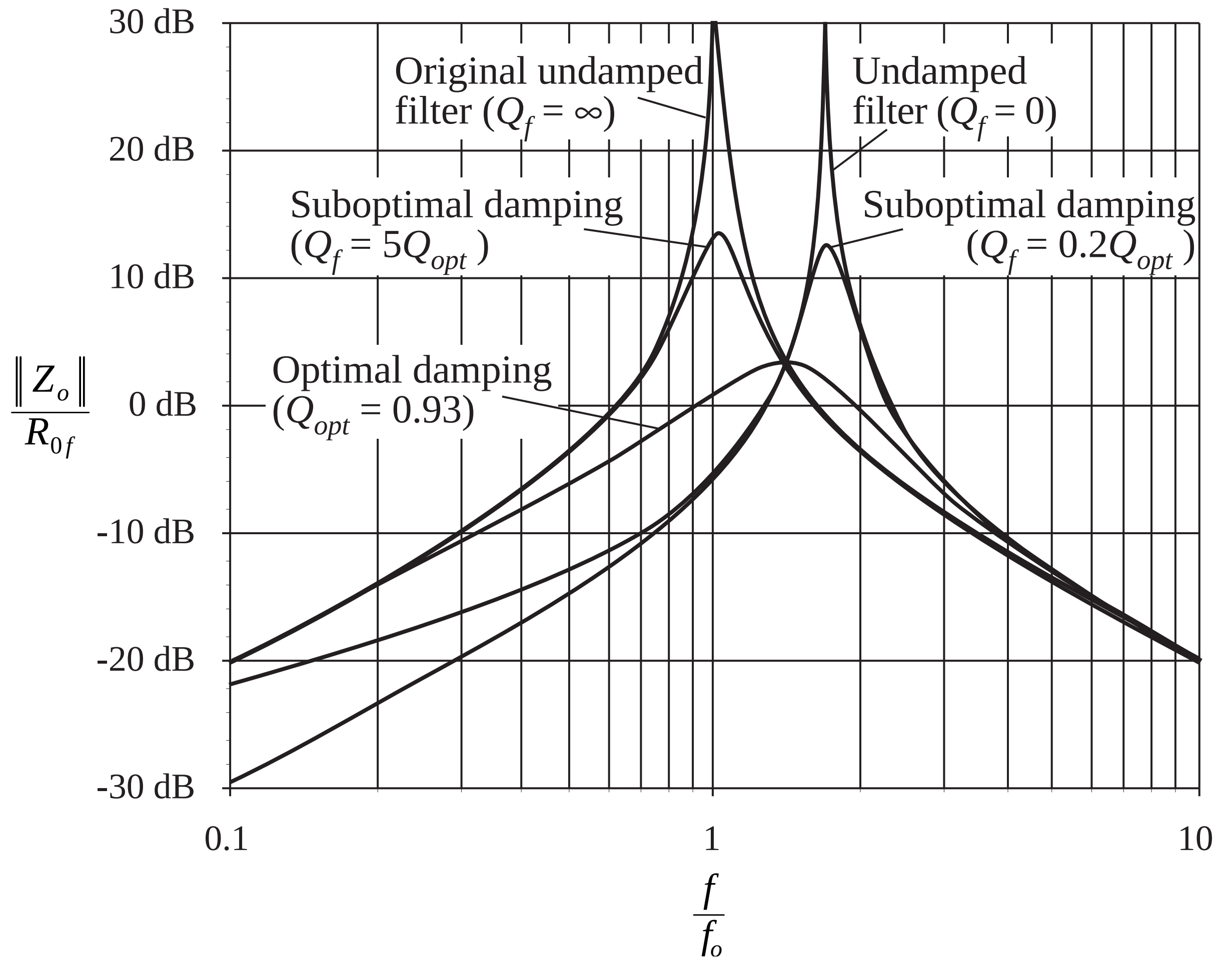


R_f–L_b Parallel Damping



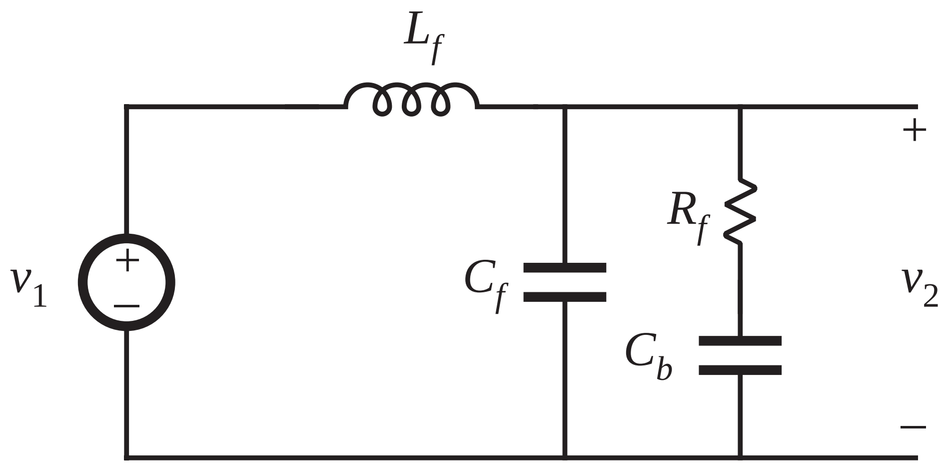
- Size of C_b or L_b can become very large
- Need to optimize design

Dependence of $\| Z_o \|$ on R_f
R_f–L_b Parallel Damping



For this example,
$n = L_b/L = 0.516$

10.4.1 R_f–C_b Parallel Damping



- Filter is damped by R_f
- C_b blocks dc current from flowing through R_f
- C_b can be large in value, and is an element to be optimized

Optimal design equations
R_f–C_b Parallel Damping

Define $n = \dfrac{C_b}{C_f}$

The value of the peak output impedance for the optimum design is

$$\| Z_o \|_{\mathrm{mm}} = R_{0f} \frac{\sqrt{2(2+n)}}{n}$$

where R_{0f} = characteristic impedance of original undamped input filter

Given a desired value of the peak output impedance, can solve above equation for n. The required value of damping resistance R_f can then be found from:

$$Q_{opt} = \frac{R_f}{R_{0f}} = \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}}$$

The peak occurs at the frequency

$$f_m = f_f \sqrt{\frac{2}{2+n}}$$

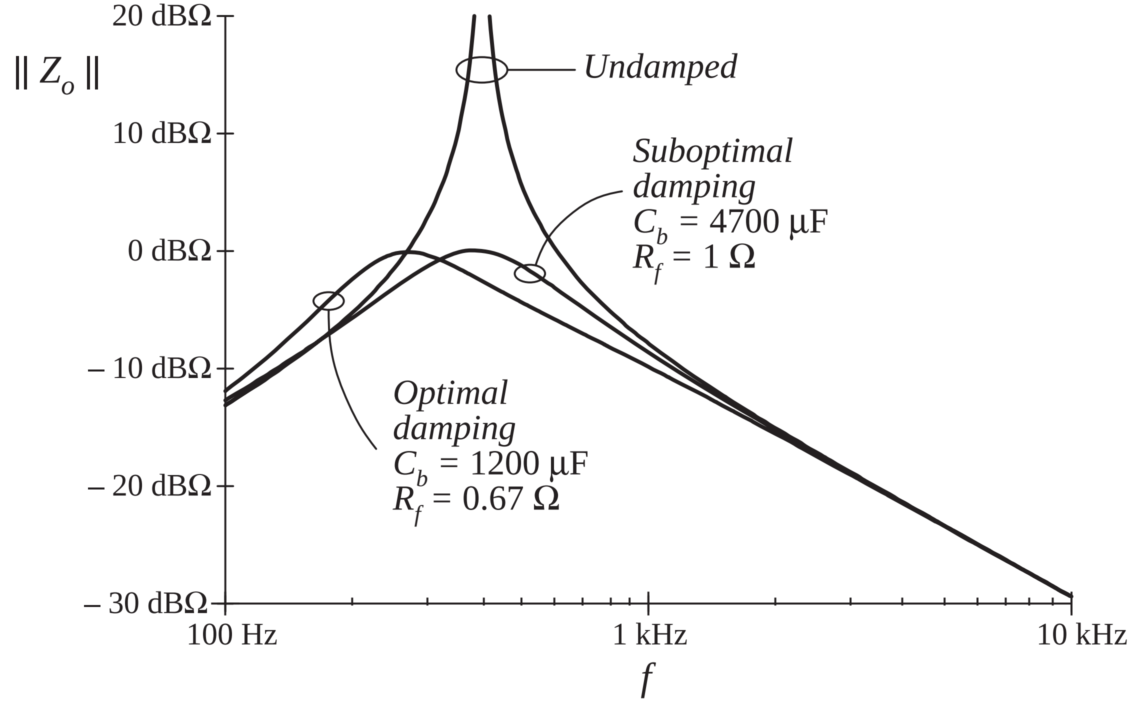
Example

Buck converter of Section 10.3.2

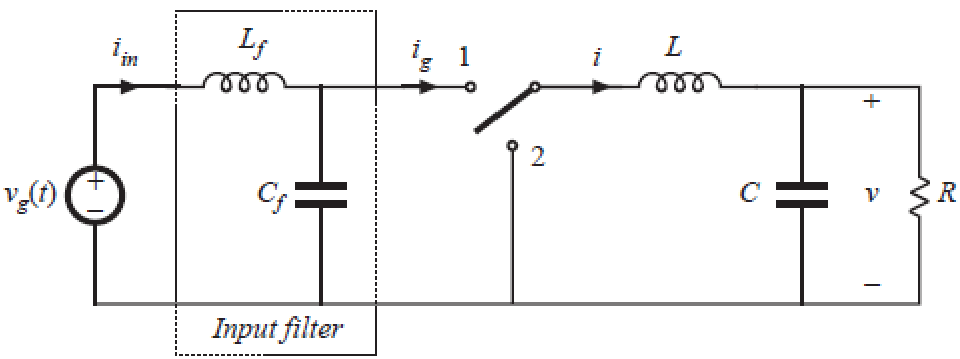
$$n = \frac{R_{0f}^2}{\| Z_o \|_{\mathrm{mm}}^2} \left(1 + \sqrt{1 + 4 \frac{\| Z_o \|_{\mathrm{mm}}^2}{R_{0f}^2}} \right) = 2.5 \qquad R_f = R_{0f} \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} = 0.67\ \Omega$$

Comparison of designs

Optimal damping achieves same peak output impedance, with much smaller C_b.



SIMULINK SIMULATION BUCK CONVERTER INPUT FILTER STUDY



$V_g = 28$ V

V = 12 V

$P_{out} = 100$ W

$f_{sw} = 100$ kHz

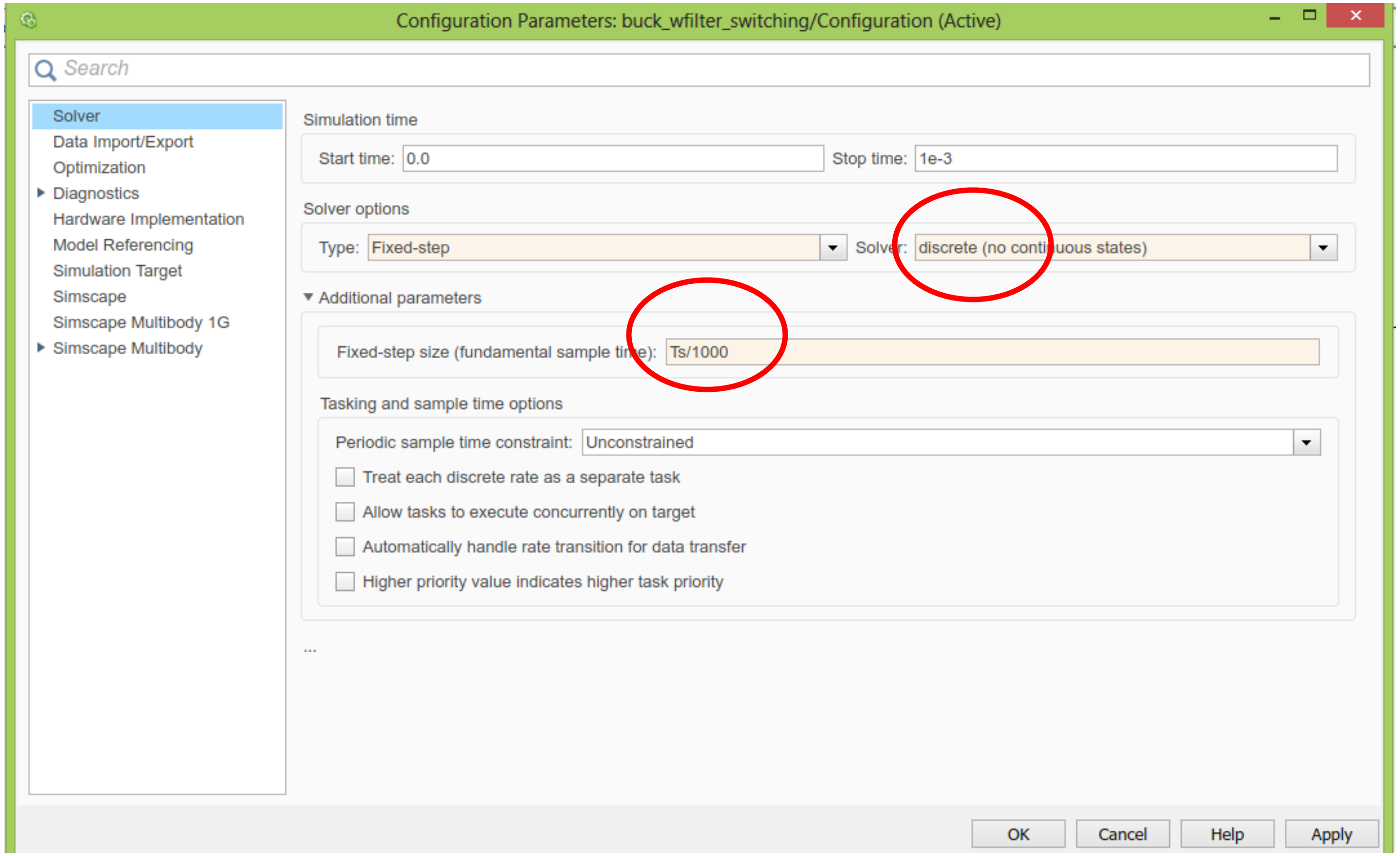
$L_{out} = 79.602$ uH

$C_{out} = 5.2083$ uF

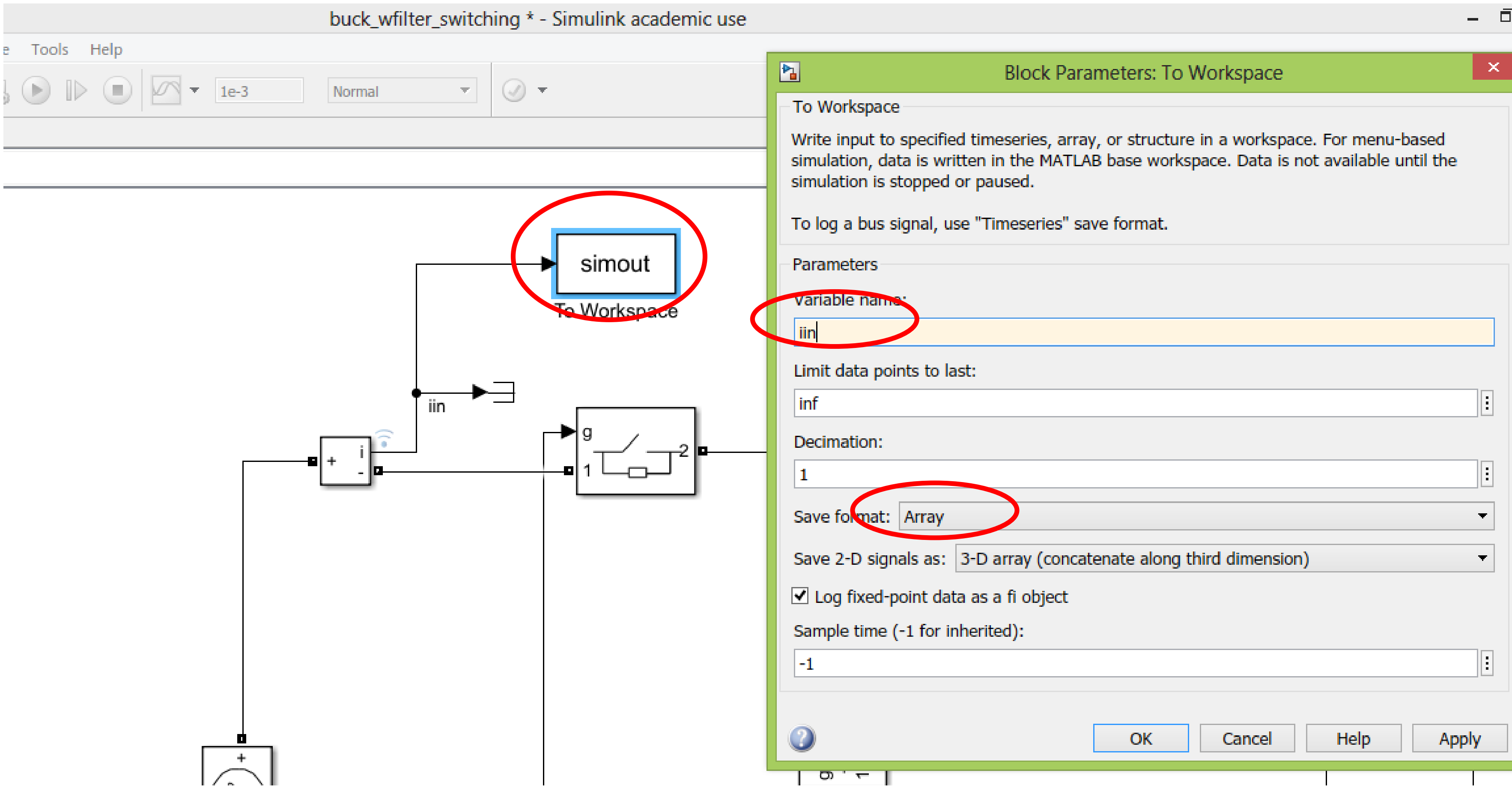
There are two mfiles and 1 simulink file

- dft_code_importingsimulink.m
  - This file pulls in a variable from work space to perform DFT
- buck_switching_filter.m
  - This is your file to set up the simulation
- buck_wfilter_switching
  - Simulink file

Run without Filter - Setup to run fixed time step (Ts/1000)



Output input current to workspace – add simout block – name variable “iin”



Fill in mfile inputs for DFT run

Editor - C:\Users\jvr2131\Desktop\APLcourse\module7\matlab\dft_code_importingsimulink.m

buck_switching_filter.m | dft_code_importingsimulink.m | +

This file can be opened as a Live Script. For more information, see Creating Live Scripts.

```
%clear all
close all
clc

% File to run DFT on time domain signals for Power Electronics Analysis Set
% up to import data from simulink
%% Fill in the inputs here!

dT = ;                            % Sample time from fixed step simulation
steady_state_time = ;           % Define steady state time
tend = ;                          % Simulation end time
ig_t = ;                           % ig_t is the input variable from the workspace

%%
ig_t = ig_t(steady_state_time/dT:end-1);      % Pulling out steady state result only
% time vector
t=[dT*(steady_state_time/dT-1):dT:tend-dT];        % Recreated

% Plot DFT of signal
fsamplefreq = 1/dT;
IG_T=fft(ig_t);                                    % Take DFT of time domain signal
lengthdft = length(IG_T);                          % Calculate size of DFT result
```

Run file – Confirm steady state