Input Filter Discussion and Design:

Recall the last lecture we talked about input filter design. The idea behind an input filter is to prevent the input current generated from the switching converter containing very high frequency harmonics from getting back onto the input source. By attenuating the switching harmonics that are present in the converter input current waveform, the input filter allows compliance with regulations that limit conducted electromagnetic interference (EMI).

We desire that the added input filter, typically designed last after the controller, does not alter the control to output transfer function, $G_{vd}(s)$, significantly as to result in an instability. Middlebrooks extra value theorem, derived in the appendix of Erickson, allows the new control to output transfer function, $G_{vdnew}(s)$, to be written in terms of impedance and the old control to output transfer function, $G_{vdold}(s)$:

$$G_{vdnew}(s) = G_{vdold}(s) \underbrace{\frac{\left(1+\frac{Z_o(s)}{Z_N(s)}\right)}{\left(1+\frac{Z_o(s)}{Z_D(s)}\right)}}_{correctionfactor} \tag{1.1}$$

If the following inequalities hold true, then the addition of an input filter has minimum effect on the control to output transfer function of the converter analyzed without an input filter. This is the desire.

$$\begin{aligned} \|Z_o(s)\| &\ll \|Z_N(s)\|, and \\ \|Z_o(s)\| &\ll \|Z_D(s)\| \end{aligned} \tag{1.2}$$

Let's quickly review what "impedance" really means:

Consider the following circuit:

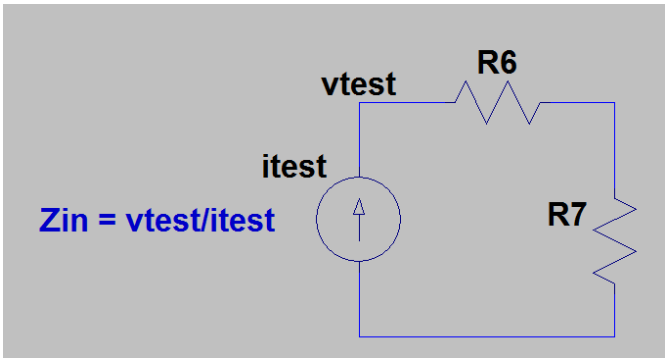

Figure 1 Impedance Example Circuit 1

Impedance is a voltage divided by a current and has the notation "Z". The impedance is usually defined with respect to a location. In this example, we want to know the input impedance, Zin, looking from left into the circuit. This can be done by inserting a current test source, *itest*, to be

injected into the terminal for which we want to know the impedance. Using KVL/KCL we can derive the impedance as follows:

$$\begin{aligned} itest\left(R_6+R_7\right) &= vtest \\ Z_{in} &= \frac{vtest}{itest} = R_6+R_7 \end{aligned} \tag{1.3}$$

Now consider the next example:

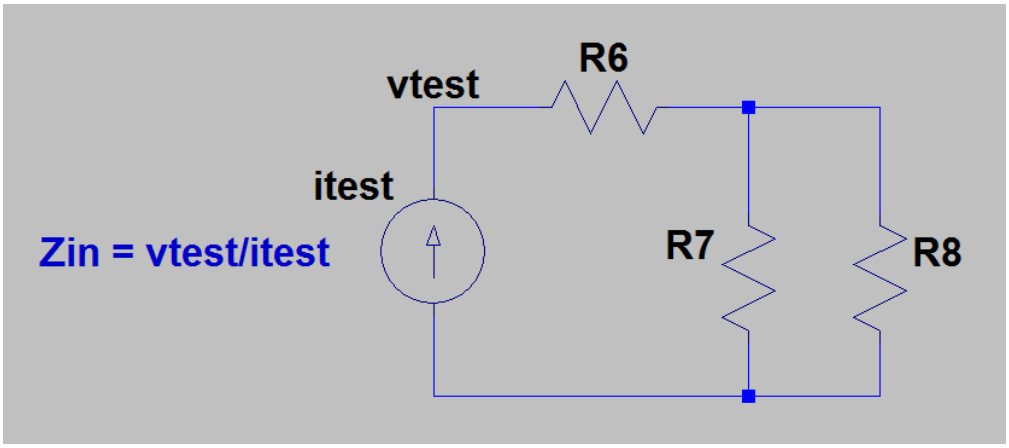

Figure 2 Impedance Example Circuit 2

Using KVL/KCL:

$$\begin{aligned} itest\left(R_6+R_7\left\|R_8\right.\right) &= vtest \\ Zin &= \frac{vtest}{itest} = \left(R_6+R_7\left\|R_8\right.\right) \\ Zin &= R_6+\frac{R_7R_8}{R_7+R_8} \end{aligned} \tag{1.4}$$

Now let's consider the impedance of the following circuit which has Ls and Cs:

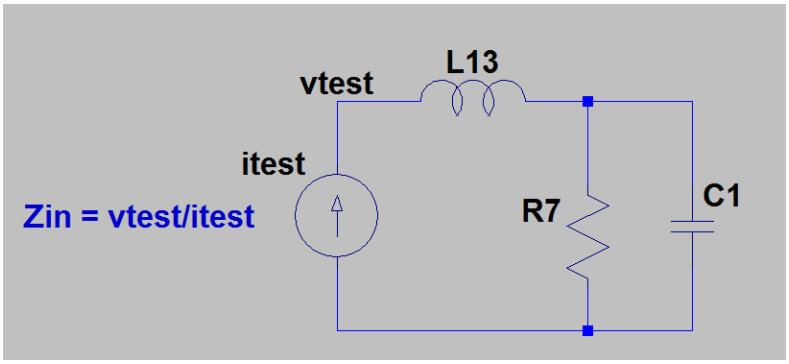

Figure 3 Impedance Example Circuit 3

After replacing the L13 and C1 by their effective impedances (sL13 and 1/sC1) respectively:

$$Zin = \frac{vtest}{itest} = \left(sL_{13} + R_7 \left\| \frac{1}{sC_1} \right. \right)$$

$$Zin = \left(sL_{13} + \frac{R_7 \left(\frac{1}{sC_1} \right)}{R_7 + \frac{1}{sC_1}} \right) \tag{1.5}$$

The impedances used in the *correction factor* from (1.1) are defined from the small signal circuits of the converter and the input filter:

$$Z_D(s) = Z_i(s)\Big|_{\hat{d}(s)=0} \tag{1.6}$$

$$Z_N(s) = Z_i(s)\Big|_{\hat{v}(s) \to 0} \tag{1.7}$$

Where $Z_i(s)$ is defined as the converter small signal input impedance looking into the converter small signal circuit equivalent circuit from the input source terminals.

This is somewhat of a confusing notation. Let's explain through an example. Consider the small signal model of a buck converter without an input filter (review if necessary this derivation before continuing)

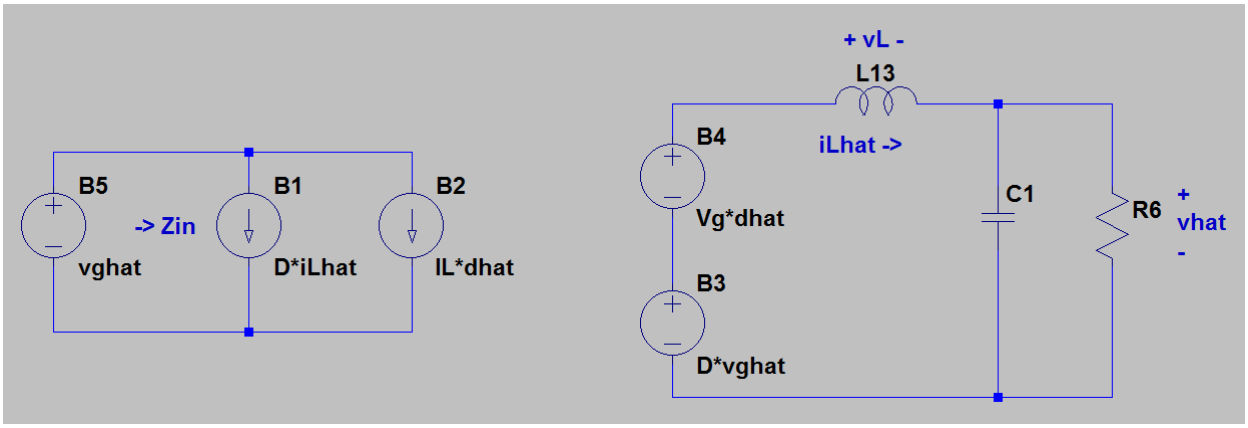

Figure 4 Buck Small Signal Model without input filter

In this case we want to define the input impedance relationships looking into the converter. This means we look from the right side of the independent input source voltage $\hat{v}_g(s)$ so we inject a test source, *itest*, at the input terminals of the small signal model where the independent source $\hat{v}_g(s)$ would reside and derive the input impedance transfer functions. The following circuit is used to determine $Z_D(s)$.

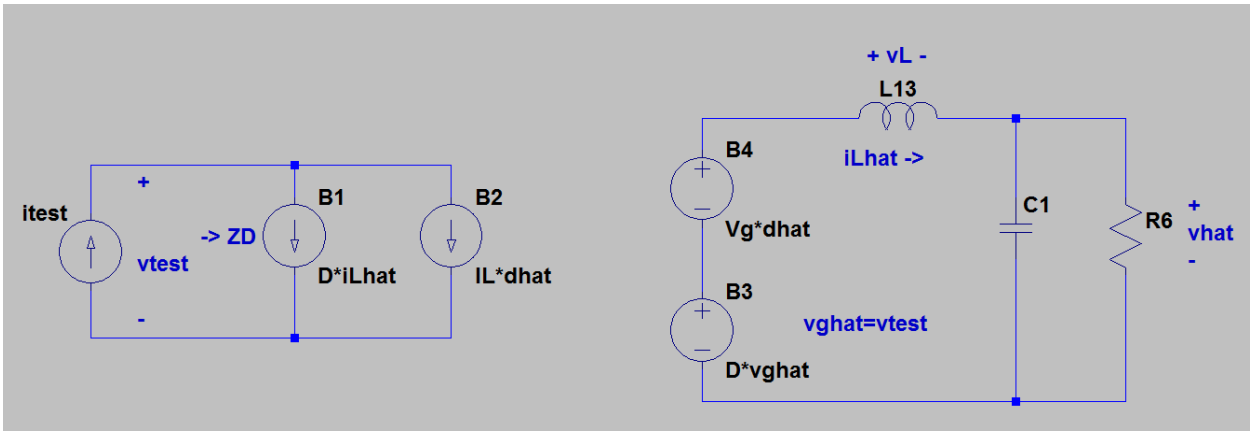

Figure 5 Buck small signal model ZD(s) formulation

First we zero out the control duty cycle $\hat{d}(s)$ as defined in (1.6).

By KVL/KCL:

$$itest(s) = D\hat{i}_L(S) \tag{1.8}$$

$$D\hat{v}_g(s) = \hat{i}_L(s)\left(sL_{13} + \left(R_6 \| \frac{1}{SC_1}\right)\right) \tag{1.9}$$

$$D\hat{v}_g(s) = \hat{i}_L(s)\left(sL_{13} + \frac{R_6\frac{1}{SC_1}}{R_6 + \frac{1}{SC_1}}\right) \tag{1.10}$$

Since the impedance is defined at the input terminals of the small signal circuit:

$$\hat{v}_g(s) = vtest(s) \tag{1.11}$$

Solving (1.8)-(1.11):

$$Z_D(s) = \frac{R_6\left(1 + s\frac{L_{13}}{R_6} + s^2 L_{13}C_1\right)}{D^2\left(1 + s\cdot R_6\cdot C_1\right)} \tag{1.12}$$

Now let's derive the impedance , $Z_N(s)$. We must assume when deriving $Z_N(s)$ that our controller is perfect with infinite gain and bandwidth such that the duty cycle $\hat{d}(s)$ can be adjusted to whatever it has to be to maintain zero output disturbance, i.e. $\hat{v}(s) = 0$. For this to be true, the voltage drop of across the capacitor, C1 and resister, R6 has to be 0. This means the

current through the parallel impedance has to be zero. This dictates that the current through the inductor, $\hat{i}_L(s) = 0$. And since $\hat{i}_L(s) = 0$, this implies that the voltage across the inductor $\hat{v}_L(s) = 0$. Make sure you understand this before going forward!

With that said, let's redraw the circuit with those assumptions.

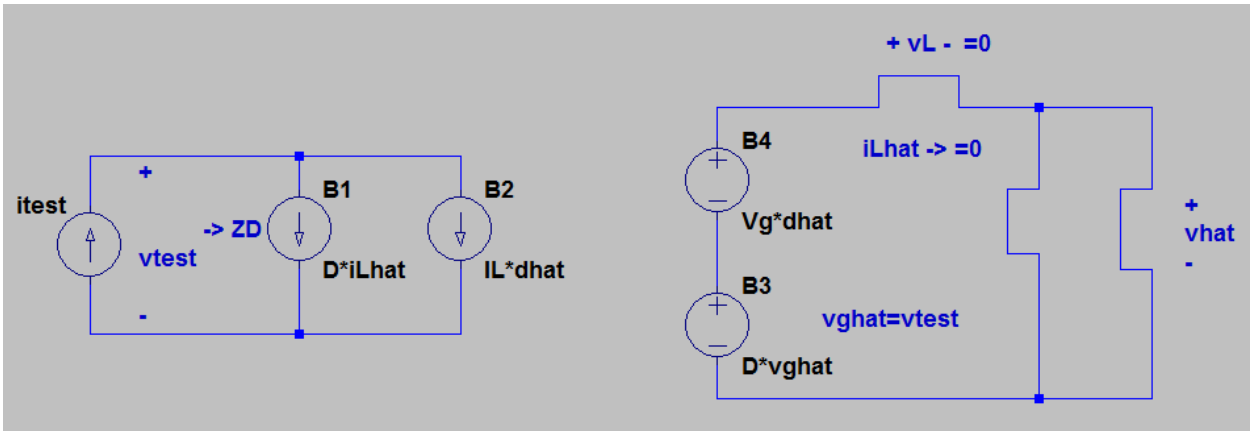

Figure 6 Buck Small signal circuit with vhat(0) nulled to zero ZD(s) formulation

KVL and KCL:

$$\hat{itest}(s) = I_L \hat{d}(s) \tag{1.13}$$

$$-D\hat{v}_g(s) - \mathrm{V}_g \hat{d}(s) = 0 \tag{1.14}$$

$$\hat{v}_g(s) = \hat{vtest}(s) \tag{1.15}$$

Solving (1.13)-(1.15)

$$Z_N(s) = \frac{\hat{vtest}(s)}{\hat{itest}(s)} = -\frac{V_g}{I_L D} \tag{1.16}$$

In a buck converter the large signal inductor current, I_L is given as:

$$I_L = \frac{V}{R_6} \tag{1.17}$$

Where V is the large signal output voltage across R6 in steady state. We also know in steady state for a buck converter:

$$V = DV_g \tag{1.18}$$

Solving (1.16)-(1.18):

$$Z_N(s) = \frac{vtest(s)}{itest(s)} = -\frac{R_6}{D^2} \tag{1.19}$$

Let's assume we will use an LC filter for the input filter. The output impedance $Z_o(s)$ can be derived from the following circuit:

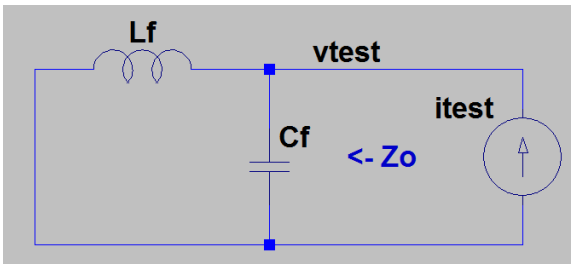

Figure 7 Input Filter Output Impedance test circuit

In this case we are looking into the output terminals from right to left. The independent source that would connect to the left side of L13 by superposition is set to zero. You may want to review this from general circuits if you need a reminder on what to do with independent voltage and current sources.

By KVL/KCL:

$$itest(s)\left(sL_{13} \| \frac{1}{sC_1}\right) = vtest(s) \tag{1.20}$$

$$Z_o(s) = \frac{vtest(s)}{itest(s)} = \left(\frac{sL_{13}\dfrac{1}{sC_1}}{sL_{13} + \dfrac{1}{sC_1}}\right) = \frac{sL_{13}}{s^2 L_{13}C_1 + 1} \tag{1.21}$$

The resonant frequency is given as:

$$f_f = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{1.22}$$

The filter characteristic impedance is given as:

$$R_{of} = \sqrt{\frac{L_f}{C_f}} \tag{1.23}$$

This input filter has infinite Q and would certainly not meet the inequality constraints given by (1.2). Three main damping strategies for this filter are given in Erickson section **10.4**. Please read and review this section.

We now have derived all the impedance relationships required to analyze a buck converter. The overall **closed loop input impedance**, $Z_i(s)$ is given by:

$$\frac{1}{Z_i(s)} = \frac{1}{Z_N(s)} \frac{T(s)}{1+T(s)} + \frac{1}{Z_D(s)} \frac{1}{1+T(s)} \tag{1.24}$$