

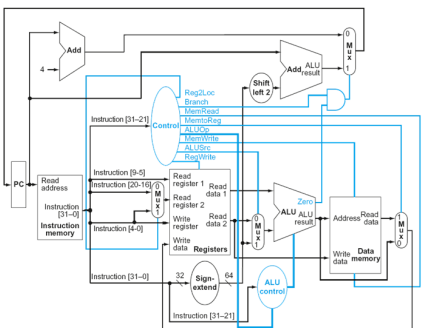
Midterm 2 Results for Julia Nelson

Score for this quiz: 19 out of 100
Submitted Dec 2 at 1:15pm
This attempt took 72 minutes.

Unanswered

Question 1

0 / 20 pts



Consider the instruction LDUR X2, [X3, #48] which uses the above datapath.

(a) What is the output of sign-extend (in hex)?

(b) What is the value of ReadRegister1 (in decimal or binary)?

(c) What is the value of ALUSrc?

(d) What are the values of MemRead and MemWrite?

Your Answer:

Question 2

10 / 20 pts

Consider a processor without pipelining that has the following stage latencies: IF 200 ps, ID 100 ps, EX 100 ps, MEM 200 ps and WB 100 ps. We wish to build a new processor with a five-stage pipeline based on the non-pipelined processor.

(a) What is the clock cycle time of the new pipelined processor?

(b) What is the ideal speed up of the pipelined processor over the non-pipelined one? Assume that no bubbles will need to be inserted in the pipeline.

(c) Why will the actual speedup be less than the above ideal one?

Your Answer:

a)

NON-Pipelined cycle time = 200+100+100+200+100 = 700ps

Pipelined cycle time = MAX(200,100,100,200,100) = 200ps

c) we can split the longest stages of the pipeline up to decrease cycle time.

Unanswered

Question 3

2 / 20 pts

Consider the following instructions executed in a pipeline with full forwarding support. Identify the value of which register is forwarded from a stage of an instructions to a stage of a subsequent instruction. (Completely impossible example: "The value of X5 is forwarded from the IF stage of instruction 1 to the WB stage of instruction 2.") No pipeline execution diagram is required, but sketching one in your notes may be helpful.

1: LDUR X20, [X19, #0]

2: LDUR X21, [X19, #8]

3: ADD X22, X21, X20

4: SUB X23, X23, X22

Your Answer:

Unanswered

Question 4

0 / 10 pts

One form of speculation is to load before completing outstanding stores.

(a) Describe what must be true for this technique to be correct.

(b) What would happen if the speculation were wrong?

Your Answer:

Unanswered

Question 5

7 / 30 pts

Consider the following assembly code.

LDUR X2, [X0, #16]

SUB X3, X1, X2

STUR X3, [X0, #24]

LDUR X4, [X0, #40]

ADD X5, X1, X4

STUR X5, [X0, #64]

(a) Add NOP instructions to the code above so that it will run correctly on a pipeline without forwarding, but WB write/read in the same cycle. (A pipeline execution diagram is not needed for this problem. Sketching it may help, but it does not need to be submitted.)

(b) Optimize the code execution by re-arranging the instructions to get the same correct result faster. (No need to prove that your solution is optimal, but it should be faster than the given code.)

Your Answer: