

OPCODES IN NUMERICAL ORDER BY OPCODE

Instruction Mnemonic	Format	Width (bits)	Opcode		Shamt Binary	11-bit Opcode Range (1)	
			Binary			Start (Hex)	End (Hex)
B	B	6	000101			0A0	0BF
FMULS	R	11	00011110001	000010		0F1	
FDIVS	R	11	00011110001	000110		0F1	
FCMPS	R	11	00011110001	001000		0F1	
FADDS	R	11	00011110001	001010		0F1	
FSDBS	R	11	00011110001	001110		0F1	
FMULD	R	11	00011110011	000010		0F3	
FDIVD	R	11	00011110011	000110		0F3	
FCMPD	R	11	00011110011	001000		0F3	
FADD	R	11	00011110011	001010		0F3	
FSDUD	R	11	00011110011	001110		0F3	
STURB	D	11	00111000000			1C0	
LDURB	D	11	00111000010			1C2	
B.cond	CB	8	01010100			2A0	2A7
STURH	D	11	01111000000			3C0	
LDURH	D	11	01111000010			3C2	
AND	R	11	10001010000			450	
ADD	R	11	10001011000			458	
ADDI	I	10	1001000100			488	489
ANDI	I	10	1001001000			490	491
BL	B	6	100101			4A0	4BF
SDIV	R	11	10011010110	000010		4D6	
UDIV	R	11	10011010110	000011		4D6	
MUL	R	11	10011011000	011111		4D8	
SMULH	R	11	10011011010			4DA	
UMULH	R	11	10011011110			4DE	
ORR	R	11	10101010000			550	
ADDS	R	11	10101011000			558	
ADDIS	I	10	1011000100			588	589
ORRI	I	10	1011001000			590	591
CBZ	CB	8	10110100			5A0	5A7
CBNZ	CB	8	10110101			5A8	5AF
STURW	D	11	10111000000			5C0	
LDURSW	D	11	10111000100			5C4	
STURS	R	11	10111100000			5E0	
LDURS	R	11	10111100010			5E2	
STXR	D	11	11001000000			640	
LDXR	D	11	11001000010			642	
EOR	R	11	11001010000			650	
SUB	R	11	11001011000			658	
SUBI	I	10	1101000100			688	689
EORI	I	10	1101001000			690	691
MOVZ	IM	9	110100101			694	697
LSR	R	11	11010011010			69A	
LSL	R	11	11010011011			69B	
BR	R	11	11010110000			6B0	
ANDS	R	11	11101010000			750	
SUBS	R	11	11101011000			758	
SUBIS	I	10	1111000100			788	789
ANDIS	I	10	1111001000			790	791
MOVK	IM	9	111100101			794	797
STUR	D	11	11111000000			7C0	
LDUR	D	11	11111000010			7C2	
STURD	R	11	11111100000			7E0	
LDURD	R	11	11111100010			7E2	

(1) Since I, B, and CB instruction formats have opcodes narrower than 11 bits, they occupy a range of 11-bit opcodes, e.g., the 6-bit B format occupies 32 (2^5) 11-bit opcodes.

IEEE 754 FLOATING-POINT STANDARD

$(-1)^s \times (1 + \text{Fraction}) \times 2^{(\text{Exponent} - \text{Bias})}$
where Single Precision Bias = 127,
Double Precision Bias = 1023

IEEE Single Precision and Double Precision Formats:

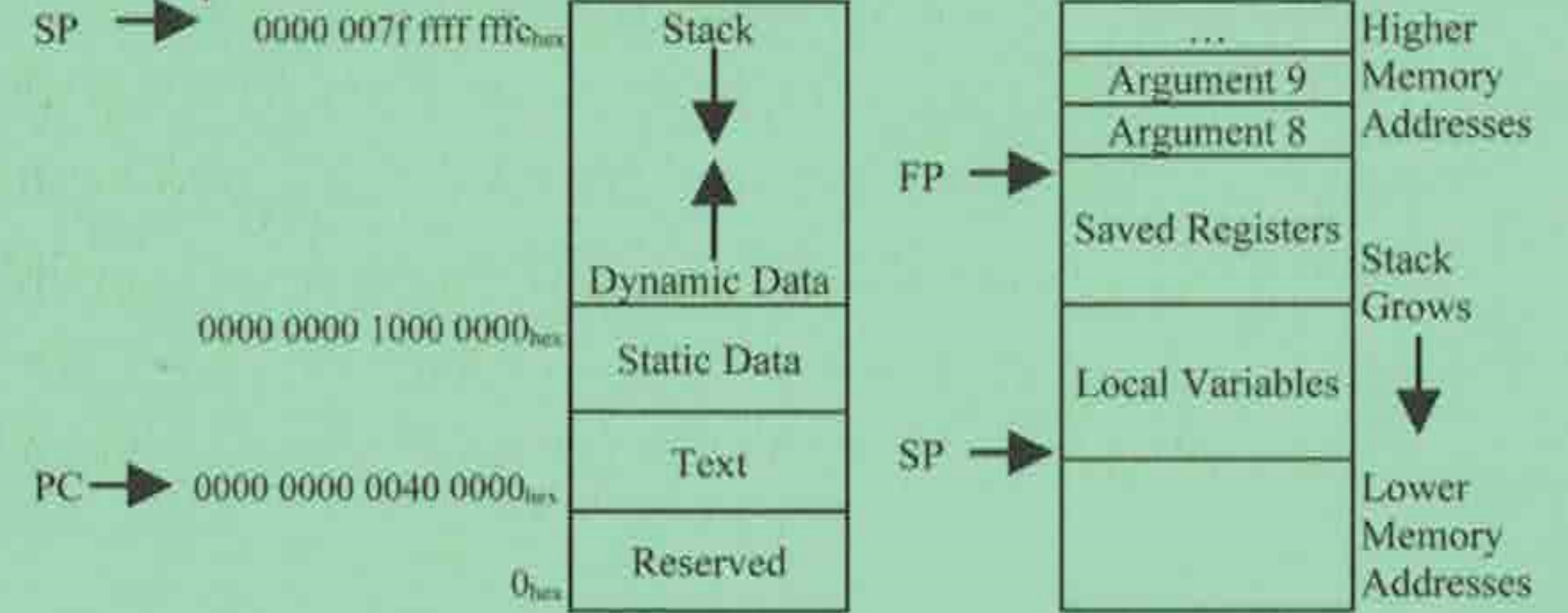
S	Exponent	Fraction
31	30	23 22
63	62	52 51

IEEE 754 Symbols

Exponent	Fraction	Object
0	0	± 0
0	$\neq 0$	$\pm \text{Denorm}$
1 to MAX - 1	anything	$\pm \text{F1. Pt. Num.}$
MAX	0	$\pm \infty$
MAX	$\neq 0$	NaN

S.P. MAX = 255, D.P. MAX = 2047

MEMORY ALLOCATION



DATA ALIGNMENT

Double Word							
Word				Word			
Halfword		Halfword		Halfword		Halfword	
Byte	Byte	Byte	Byte	Byte	Byte	Byte	Byte
0	1	2	3	4	5	6	7

Value of three least significant bits of byte address (Big Endian)

EXCEPTION SYNDROME REGISTER (ESR)

Exception Class (EC)	Instruction Length (IL)	Instruction Specific Syndrome field (ISS)
31	26	25 24
		0

EXCEPTION CLASS

EC	Class	Cause of Exception	Number	Name	Cause of Exception
0	Unknown	Unknown	34	PC	Misaligned PC exception
7	SIMD	SIMD/FP registers disabled	36	Data	Data Abort
14	FPE	Illegal Execution State	40	FPE	Floating-point exception
17	Sys	Supervisor Call Exception	52	WPT	Data Breakpoint exception
32	Instr	Instruction Abort	56	BKPT	SW Breakpoint Exception

SIZE PREFIXES AND SYMBOLS

SIZE	PREFIX	SYMBOL	SIZE	PREFIX	SYMBOL
10^3	Kilo-	K	2^{10}	Kibi-	Ki
10^6	Mega-	M	2^{20}	Mebi-	Mi
10^9	Giga-	G	2^{30}	Gibi-	Gi
10^{12}	Tera-	T	2^{40}	Tebi-	Ti
10^{15}	Peta-	P	2^{50}	Pebi-	Pi
10^{18}	Exa-	E	2^{60}	Exbi-	Ei
10^{21}	Zetta-	Z	2^{70}	Zebi-	Zi
10^{24}	Yotta-	Y	2^{80}	Yobi-	Yi
10^{-3}	milli-	m	10^{-15}	femto-	f
10^{-6}	micro-	μ	10^{-18}	atto-	a
10^{-9}	nano-	n	10^{-21}	zepto-	z
10^{-12}	pico-	p	10^{-24}	yocto-	y