Julia Nelson

Homework 1

"I pledge my honor that I have abided by the Stevens Honor System"

1.5

P1 —> (3 GHz, 1.5 CPI)
P2 —> (2.5 GHz, 1.0 CPI)
P3 —> (4 GHz, 2.2 CPI)

a.

Instructions / Second = Clock Rate / CPI

P1 => $3.0GHz/1.5CPI = (3.0 * 10^9)/1.5 = 2 * 10^9 Instructions/Second$
P2 => $2.5GHz/1.0CPI = (2.5 * 10^9)/1.0 = 2.5 * 10^9 Instructions/Second$
P3 => $4.0GHz/2.2CPI = (4.0 * 10^9)/2.2 = 1.82 * 10^9 Instructions/Second$

P2 has the highest performance

b.

# Cycles = (Clock Cycles / Second) * Time = Clock Rate * Time
# Instructions = (Instructions / Second) * Time {used IPS's from above}
Time = 10 seconds

P1 =>
#Cycles = $3GHz * 10s = 3 * 10^{10}$
#Instructions = $(2.0 * 10^9 IPS) * 10s = 2.0 * 10^{10}$
P2 =>
#Cycles = $2.5GHz * 10s = 2.5 * 10^{10}$
#Instructions = $(2.5 * 10^9 IPS) * 10s = 2.5 * 10^{10}$
P3 =>
#Cycles = $4.0GHz * 10s = 4.0 * 10^{10}$
#Instructions = $(1.82 * 10^9 IPS) * 10s = 1.82 * 10^{10}$

c.

Reduce time by 30% & Increase CPI by 20%
Execution Time * (1.0 - 0.30) = (# Instructions * (CPI * 1.2)) / New Clock Rate

New Clock Rate = Old Clock Rate * (1.2 / 0.7)

P1 =>

$$NewClockRate = 3.0GHz * (1.2/0.7) = 5.14GHz$$

P2 =>

$$NewClockRate = 2.5GHz * (1.2/0.7) = 4.28GHz$$

P3 =>

$$NewClockRate = 4.0GHz * (1.2/0.7) = 6.86GHz$$

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Homework 1

1.6

a.

Time =(# Instructions * CPI) / Clock Rate

Class A = 10^6 * 10% = 1 * 10^5 Instructions executed
Class B = 10^6 * 20% = 2 * 10^5 Instructions executed
Class C = 10^6 * 50% = 5 * 10^5 Instructions executed
Class D = 10^6 * 20% = 2 * 10^5 Instructions executed

Processor 1

$Time = (10^5 + (2 * 10^5 * 2) + (5 * 10^5 * 3) + (2 * 10^5 * 3)/(2.5 * 10^9) = 10.4 * 10^{-4}$ s

Global CPI = (10.4 * 10^{-4})* (2.5 * 10^9) / 10^6 = 2.6 CPI

Processor 2

$Time = (10^5 * 2) + (2 * 10^5 * 2) + (5 * 10^5 * 2) + (2 * 10^5 * 2)/(3 * 10^9) = 6.66 * 10^{-4}$ s

Global CPI = (6.66 * 10^{-4})* (3 * 10^9) / 10^6 = 2.0 CPI

b.

Processor 1

Clock Cycles = (1 * 10^5) + (2 * 10^5 * 2) + (5 * 10^5 * 3) + (2 * 10^5 * 3) = 26 * 10^5

Processor 2

Clock Cycles = (2 * 10^5) + (2 * 10^5 * 2) + (5 * 10^5 * 2) + (2 * 10^5 * 2) = 20 * 10^5

1.7

a.

clock cycle time = 1ns
CPI = CPU Clock Cycle / Instruction Count

CPI of A = (1.1s / (1.0 * 10^{-9}s * 1.0 * 10^9)) = 1.1
CPI of B = (1.5s / (1.2 * 10^{-9}s * 1.0 * 10^9)) = 1.25

b.

P1 Clock Cycle Time = B Instruction Count * B CPI
P2 Clock Cycle Time = A Instruction Count * A CPI

$$\Rightarrow \frac{1.2 * 10^9 * 1.25}{1.0 * 10^9 * 1.1} = 1.36$$

Because it is 1.36, B's code is the one running faster by 1.36 times or 36% faster than A's

c.

A execution time = 10^9 * 1.1
B execution time = 1.2 * 10^9 * 1.25
New execution time = 6.0 * 10^8 * 1.1

A execution time /New execution time = (10^9 * 1.1) / (6.0 * 10^8 * 1.1) = 1.67
B execution time/New execution time = (1.2 * 10^9 * 1.25) / (6.0 * 10^8 * 1.1) = 2.27
The New is 67% faster than A and 127% faster than B

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Homework 1

1.8

1.8.1

Average Capacity Load of Pentium 4 Prescott Processor

Dynamic Power = 1/2 * Capacity Load * V^2 * F
=> 2 * DP / (V^2 * F) = Capacity Load
=> Capacity Load = 2 * 90W / ((1.25 V^2) * (3.6GHz))
=> (2 * 90)/ ((1.25^2 V) * (3.6 * 10^9))
Capacity Load = 3.2 * 10^{-8} Farad

Average Capacity Load of Core i5 Ivy Bridge Pentium Processor

Dynamic Power = 1/2 * Capacity Load * V^2 * F
=> 2 * DP / (V^2 * F) = Capacity Load
=> Capacity Load = 2 * 40W / ((0.9 V^2) * (3.4GHz))
=> (2 * 40)/ ((0.9^2 V) * (3.4 * 10^9))
Capacity Load = 2.9 * 10^{-8} Farad

1.8.2

Pentium 4 Prescott Processor

% of Total dissipated power (by static) = 10W /(10W + 90W) = 0.10 = 10%
Static to Dynamic Ratio = 10W / 90W = 0.111

Core i5 Ivy Bridge Pentium Processor

% of Total dissipated power (by static) = 30W /(30W + 40W) = 0.4286 = 42.9%
Static to Dynamic Ratio = 30W / 40W = 0.75

1.8.3

voltage reduced by 10% for each
Total Dissipated Power = V * leakage
Power = V * A(current)

Pentium 4 Prescott Processor

10W + 90W = 1.25V * leakage current
100W / 1.25V = leakage current
leakage current = 80A

100W * 0.9 = (1.25 * x)V * 80A
(90W / 80A) / 1.25 = xV
x = 0.9

Voltage should be reduced by 10% to maintain same leakage

Core i5 Ivy Bridge Pentium Processor

30W + 40W = 0.9V * leakage current
70W / 0.9V = leakage current
leakage current = 77.78 A

70W * 0.9 = (0.9 * x)V * 77.78A
(63W / 77.78A) / 0.9 = xV
x = 0.8999 roughly = 0.9

Julia Nelson

Homework 1

Voltage should be reduced by roughly 10% to maintain same leakage

1.10 wafer 1 = 15cm wafer 2 = 20cm

1.10.1

Yield = $1 / (1 + \text{Defect Rate} * (\text{Die Area } 1 / 2))^2$

Wafer 1

Die Area 1 = $\frac{\text{Wafer Area 1}}{\text{Die Count 1}} = \frac{3.14 * (7.5\text{cm}^2)}{84} = 2.104\ \text{cm}^2$

Yield 1 = $1 / (1 + 0.020 * (2.103745/ 2))^2 = 0.9592$

Wafer 2

Die Area 2 = $\frac{\text{Wafer Area 2}}{\text{Die Count 2}} = \frac{3.14 * (10\text{cm}^2)}{100} = 3.14\ \text{cm}^2$

Yield 2 = $1 / (1 + 0.31 * (3.14 / 2))^2 = 0.9093$

1.10.2

Cost per Die 1

= Cost per Wafer 1 / (dies per wafer * Yield 1)

= 12/ (84 * 0.9592) = 0.14893 = 0.15

Cost per Die 2

= Cost per Wafer 2 / (dies per wafer * Yield 2)

= 15/ (100 * 0.9093) = 0.16496 = 0.17

1.10.3

Increased dies per wafer by 10%

Increased defects per area unit by 15%

Wafer 1

New Die Area = wafer area / dies per wafer =

New Yield =

Wafer 2

New Die Area =

New Yield =

1.11

1.11.1

execution Time = Instruction Count * CPI * Clock Cycle Time

$750s = 2.389 * 10^{12} * CPI * 0.333 * 10^{-9}$

CPI = 0.9427594 = 0.943

1.11.2

SPEC Ratio = CPU Time of Reference / CPU time of Measured

SPEC Ratio = 9650s/750s = 12.86666 = 12.87

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Homework 1

1.11.3

Instructions = ($2.389 * 10^{12} * 10 / 100$) + ($2.389 * 10^{12}$) = $2.6279 * 10^{12}$

New CPU Time = Instruction Count * Clock Cycle Time * CPI

= ($2.6279 * 10^{12} * 0.943 * 0.333 * 10^{-9}$)

= 825.2 s

825.2s - 750s = 75.21 second Increase in CPU Time

1.11.4

Instructions = ($2.389 * 10^{12} * 10 / 100$) + ($2.389 * 10^{12}$) = $2.6279 * 10^{12}$

CPI = 1.05 * 0.943 = 0.99015 = 0.99

New CPU Time = Instruction Count * Clock Cycle Time * CPI

= ($2.6279 * 10^{12} * 0.99015 * 0.333 * 10^{-9}$)

= 866.47 s

866.47 s - 750 s = 116.47 second Increase in CPU Time