

# DW\_bc\_1

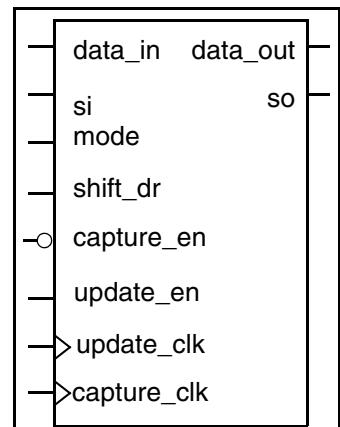
## Boundary Scan Cell Type BC\_1

Version, STAR and Download Information: [IP Directory](#)

### Features and Benefits

- IEEE Standard 1149.1 compliant
- Synchronous or asynchronous scan cells with respect to `tck`
- Supports the standard instructions: EXTEST, SAMPLE/PRELOAD, and BYPASS
- Supports the optional instructions INTEST, RUNBIST, CLAMP, and HIGHZ

### Revision History



### Description

DW\_bc\_1 is a boundary scan cell that can be used as a system input cell or as an output cell. When used as an input cell, DW\_bc\_1 provides control over the inputs to the core logic of the IC. When used as an output cell, DW\_bc\_1 provides control over the IC output signals. The Boundary Scan Description Language (BSDL) description of this cell is of type BC\_1 described in the BSDL package STD\_1149\_1\_1990.

The DW\_bc\_1 cell can be synchronous or asynchronous with respect to `tck` (Test Clock system pin), depending on the port connections.

The `mode` signal gives the Test Access Port (TAP) instructions control of the boundary scan cell.

**Table 1-1 Pin Description**

| Pin Name    | Width | Direction | Function   |
|-------------|-------|-----------|--|
| capture_clk | 1 bit | Input     | Clocks data into the capture stage   |
| update_clk  | 1 bit | Input     | Clocks data into the update stage  |
| capture_en  | 1 bit | Input     | Enable for data clocked into the capture stage, active low   |
| update_en   | 1 bit | Input     | Enable for data clocked into the update stage, active high   |
| shift_dr    | 1 bit | Input     | Enables the boundary scan chain to shift data one stage toward its serial output ( <code>tdo</code> )                  |
| mode        | 1 bit | Input     | Determines whether <code>data_out</code> is controlled by the boundary scan cell or by the <code>data_in</code> signal |
| si          | 1 bit | Input     | Serial path from the previous boundary scan cell   |
| data_in     | 1 bit | Input     | Input data   |

**Table 1-1 Pin Description (Continued)**

| Pin Name | Width | Direction | Function                                   |
|----------|-------|-----------|--|
| data_out | 1 bit | Output    | Output data                                |
| so       | 1 bit | Output    | Serial path to the next boundary scan cell |

**Table 1-2 Synthesis Implementations**

| Implementation Name | Function        | License Feature Required           |
|---------------------|-----------------|------------------------------------|
| str                 | Synthesis model | DesignWare or Test-IEEE-STD-1149-1 |

**Table 1-3 Simulation Models**

| Model                       | Function                             |
|-----------------------------|--------------------------------------|
| DW04.DW_BC_1_CFG_SIM        | Design unit name for VHDL simulation |
| dw/dw04/src/DW_bc_1_sim.vhd | VHDL simulation model source code    |
| dw/sim_ver/DW_bc_1.v        | Verilog simulation model source code |

[Table 1-4](#) lists the required values of the mode signal for each of the TAP instructions that DW\_bc\_1 supports.

**Table 1-4 Mode Signal Generation for DW\_bc\_1**

| Instruction    | Mode for Input Cell | Mode for Output Cell |
|----------------|---------------------|----------------------|
| EXTEST         | 1                   | 1                    |
| SAMPLE/PRELOAD | 0                   | 0                    |
| INTEST         | 1                   | 1 <sup>a</sup>       |
| CLAMP          | X                   | 1                    |
| RUNBIST        | X                   | 1 <sup>a</sup>       |
| BYPASS         | 0                   | 0                    |

- a. If you do not want these instructions to drive the output pins with pre-loaded data held in the boundary scan register, then these instructions are not needed to determine the state of the mode signal. Instead, the instruction must be added to the output enable logic to force every system output pin to an inactive drive state.

[Table 1-5](#) lists the connections for asynchronous boundary scan chains.

**Table 1-5 Port Connections for Asynchronous Boundary Scan Chains**

| DW_bc_1 Port Name | Connection   |
|-------------------|--|
| capture_clk       | clock_dr from TAP controller   |
| update_clk        | update_dr from TAP controller  |
| capture_en        | Logic zero   |
| update_en         | Logic one  |
| shift_dr          | shift_dr from TAP controller   |
| mode              | Mode generation logic  |
| si                | so from previous boundary scan cell                                  |
| data_in           | System input pin for input cells or IC output logic for output cells |
| data_out          | IC input logic for input cells or system output pin for output cells |
| so                | si of next boundary scan cell  |

[Table 1-6](#) lists the connections for synchronous boundary scan chains.

**Table 1-6 Port Connections for Synchronous Boundary Scan Chains**

| DW_bc_1 Port Name | Connection   |
|-------------------|--|
| capture_clk       | tck from system pin  |
| update_clk        | tck_n from system pin  |
| capture_en        | sync_capture_en from TAP controller                                  |
| update_en         | sync_update_dr from TAP controller                                   |
| shift_dr          | shift_dr from TAP controller   |
| mode              | Mode generation logic  |
| si                | so from previous boundary scan cell                                  |
| data_in           | System input pin for input cells or IC output logic for output cells |
| data_out          | IC input logic for input cells or system output pin for output cells |
| so                | si of next boundary scan cell  |

## Related Topics

- [Application Specific – JTAG Overview](#)
- [DesignWare Building Block IP User Guide](#)

## HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW_bc_1_inst is
  port (inst_capture_clk : in std_logic; inst_update_clk : in std_logic;
        inst_capture_en : in std_logic; inst_update_en : in std_logic;
        inst_shift_dr   : in std_logic; inst_mode      : in std_logic;
        inst_si         : in std_logic; inst_data_in  : in std_logic;
        data_out_inst   : out std_logic; so_inst       : out std_logic );
end DW_bc_1_inst;

architecture inst of DW_bc_1_inst is
begin
  -- Instance of DW_bc_1
  U1 : DW_bc_1
  port map (capture_clk => inst_capture_clk,
            update_clk => inst_update_clk, capture_en => inst_capture_en,
            update_en => inst_update_en, shift_dr => inst_shift_dr,
            mode => inst_mode, si => inst_si, data_in => inst_data_in,
            data_out => data_out_inst, so => so_inst );
end inst;

-- pragma translate_off
configuration DW_bc_1_inst_cfg_inst of DW_bc_1_inst is
  for inst
    end for; -- inst
end DW_bc_1_inst_cfg_inst;
-- pragma translate_on
```

## HDL Usage Through Component Instantiation - Verilog

```
module DW_bc_1_inst(inst_capture_clk, inst_update_clk, inst_capture_en,
                     inst_update_en, inst_shift_dr, inst_mode, inst_si,
                     inst_data_in, data_out_inst, so_inst );

    input inst_capture_clk;
    input inst_update_clk;
    input inst_capture_en;
    input inst_update_en;
    input inst_shift_dr;
    input inst_mode;
    input inst_si;
    input inst_data_in;
    output data_out_inst;
    output so_inst;

    // Instance of DW_bc_1
DW_bc_1
    U1 (.capture_clk(inst_capture_clk), .update_clk(inst_update_clk),
         .capture_en(inst_capture_en), .update_en(inst_update_en),
         .shift_dr(inst_shift_dr), .mode(inst_mode), .si(inst_si),
         .data_in(inst_data_in), .data_out(data_out_inst), .so(so_inst) );
endmodule
```

## Revision History

For notes about this release, see the [DesignWare Building Block IP Release Notes](#).

For lists of both known and fixed issues for this component, refer to the [STAR report](#).

For a version of this datasheet with visible change bars, click [here](#).

| Date           | Release       | Updates   |
|----------------|---------------|---|
| June 2025      | DWBB_202506.0 | Updated date and version; no technical changes  |
| September 2024 | DWBB_202409.0 | Updated date and version; no technical changes  |
| December 2023  | DWBB_202312.0 | Updated date and version; no technical changes  |
| January 2019   | DWBB_201806.5 | <ul style="list-style-type: none"><li>■ Updated example in “<a href="#">HDL Usage Through Component Instantiation - VHDL</a>” on page 4</li><li>■ Added this Revision History table and the document links on this page</li></ul> |

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