Measurement of De-assertion Threshold of Power-on-Reset Circuits

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***Abstract* - A test circuit for measuring the de-assertion threshold of a Power-on-Reset (POR) circuit is presented. With the help of the test circuit, POR de-assertion voltage can be measured without requiring a dedicated analog pad or a supply voltage higher than the POR supply voltage. The test circuit does not impact the normal mode of operation of POR and the area and power overhead due to the addition of the test circuit are minimal. The test circuit has been designed and simulated in 28nm CMOS technology. The simulation results show that the maximum error in de-assertion threshold measurement is less than +/- 0.5%.**

Keywords- power on reset; de-assertion threshold, low power analog

I. INTRODUCTION

A Power on reset (POR) circuit is used to keep the sequential elements such as flip-flops in a system-on-chip (SoC) in a known stage (either set or reset) till the power supply is reached to a desirable level [1], [2]. Generally during the power supply ramp-up, the output of the POR remains low and it goes high when the power supply reaches a pre-determined level. The power supply voltage level at which the POR output goes high (i.e. de-asserts) is called de-assertion threshold [3]. Fig. 1 shows a conventional POR circuit and Fig. 2 shows its waveforms. In Fig.1, the de-assertion threshold of the POR is decided by the ratio of the resistors R1, R2; drain to source resistance (R_{ds}) of the NMOS chain and the threshold voltage (V_t) of the NMOS transistor MN1. It is clear from Fig. 2 that the POR output, por_b remains low till the POR supply voltage, vdd_por crosses the designed de-assertion threshold which in this case is 667mV. Generally, the POR de-assertion threshold is characterized on a test chip before integrating in the SoC. For this, the POR output is exposed to an analog test pad. During characterization, the POR supply is ramped-up and the supply voltage level at which the POR output transitions to high is measured. Having a dedicated analog pad in an SoC for POR testing increases the system cost and is not a preferred solution. Another method is to poll the change in the output of a test flip-flop which gets its reset from the POR and changes its output from low to high when the POR de-asserts. In 28nm CMOS technology, the minimum core supply voltage for the SoC is 0.9V and in order to properly initialize the flip-flops in a known stage, the POR de-assertion threshold must be kept in the range of 0.6V-0.8V. However, the SoC core logic remains non-functional at 0.8V supply and is not able to poll the output of the test flip-flop.

To overcome this issue, a separate constant power supply is used for the SoC to function while the POR supply is ramped-up to measure the de-assertion threshold. This requires a dedicated supply pad for POR power supply which is again not a preferred solution. Although in the literature, many POR designs are available but there is hardly any reference available which provides a solution for the POR de-assertion threshold measurement. There are some references available to measure the brown-out threshold [5, 6] but those are not applicable directly to measure the de-assertion threshold. This paper presents a test circuit for POR de-assertion threshold measurement in an SoC without requiring a dedicated analog or supply pad. The paper consists of four sections. Section II provides the details of the proposed test circuit. Section III covers the simulation results and finally, section IV provides the conclusion.

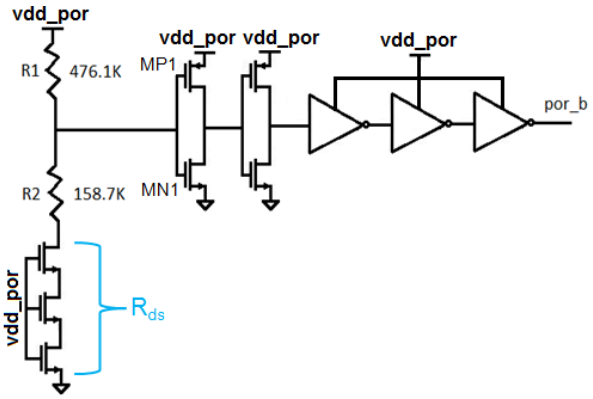

Fig. 1 Conventional POR

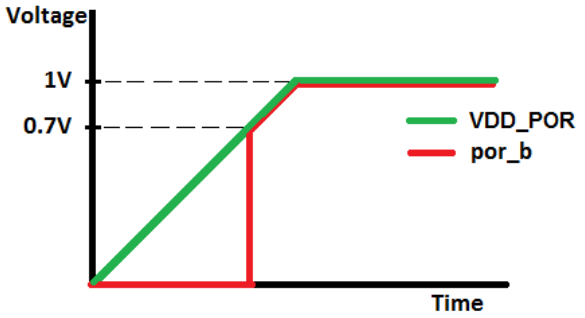

Fig. 2 Waveforms of conventional POR circuit

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II. PROPOSED TEST CIRCUIT

Fig. 3 shows the block diagram of the test circuit. It should be noted that the test circuit is generic in nature and can be used with any type of POR circuit. In the foregoing analysis, the conventional POR circuit shown in Fig. 1 has been taken for the sake of illustration. In Fig. 3, vdd is the main power supply of the SoC and the POR supply voltage, vdd_por is derived by using a resistor divider, composed of R_1 and R_2 and a fuse circuit, such as a laser fuse circuit. The value of R_1 and R_2 must be chosen in such a way so that the resistor divider is capable of sourcing the POR circuit current without impacting the voltage at vdd_por. In the test mode, the fuse is configured as a short for those chips in which the POR de-assertion threshold is to be measured. In the functional mode, the fuse remains as an open circuit and the voltage at vdd_por is equal to vdd. In the test mode, the fuse is shorted and the voltage at vdd_por is given by (neglecting the fuse resistance)

$$v(vdd\_por) = \frac{R_2}{R_1 + R_2} * vdd \qquad (1)$$

As shown in Fig. 3, taking R_1= 345.5Ω and R_2=691Ω, equation (1) gives,

$$vdd\_por = \frac{vdd}{1.5} \qquad (2)$$

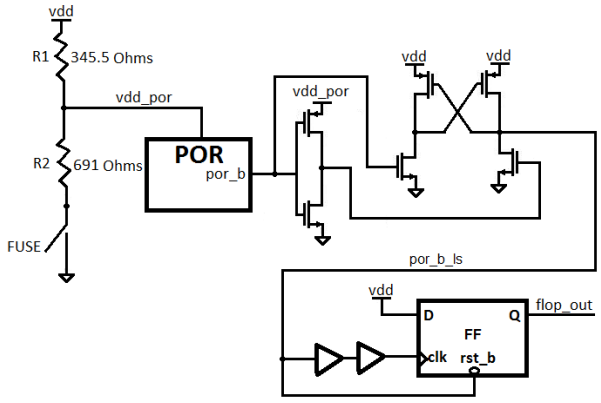

Fig 3 Proposed test circuit

The POR circuit under test consumes about 2µA current from its supply and due to this, there is less than 1mV change in vdd_por voltage as compared to the value given by equation (2). If the loading from the POR circuit under test is high, the value of R_1 and R_2 should be further reduced to minimize the loading impact. The output of the POR is level shifted to vdd with the help of a cross-coupled level shifter. The level shifted output, por_b_ls is directly connected to the reset pin of the flip-flop (FF). A delayed version of por_b_ls is connected to the clk pin of flip-flop. By applying the delayed por_b_ls signal at the clk pin, it is ensured that there will be no contention at the flip-flop output. The data pin, d of the flip-flop is tied to vdd. The output of the flip-flop, flop_out is polled by SoC logic to establish a change in its state.

In order to measure the de-assertion threshold of POR, vdd is ramped up from 0V. As shown in Fig. 4, initially por_b_ls will be low, forcing the flip-flop in reset state (i.e. flop_out is low). As vdd starts ramping up, vdd_por also starts increasing as per equation (1). When vdd_por crosses the de-assertion threshold of the POR (667mV), por_b and por_b_ls transition to vdd_por and vdd respectively. A high transition on por_b_ls brings the flip-flop out of the reset state and flop_out transitions to vdd. It is clear from Fig. 4 that at POR de-assertion, vdd is 1V which is sufficient for SoC to function and poll the change in state of flop_out from low to high.

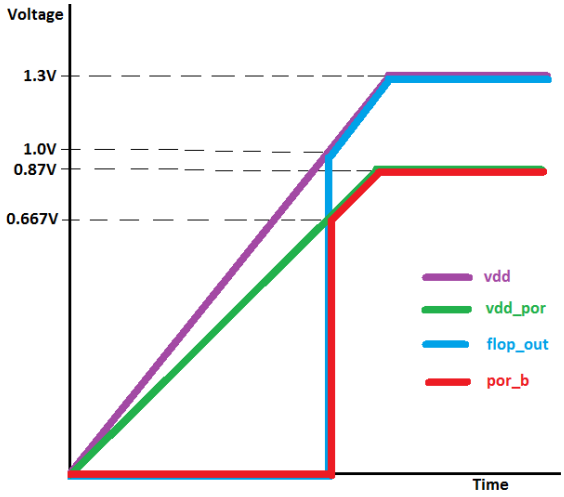

Fig. 4 Waveforms of the proposed test circuit

The vdd voltage level at which flop_out goes high is measured on the tester. The actual de-assertion threshold of the POR can then be calculated using equation (2). Fig. 5 shows a flow chart for de-assertion threshold characterization.

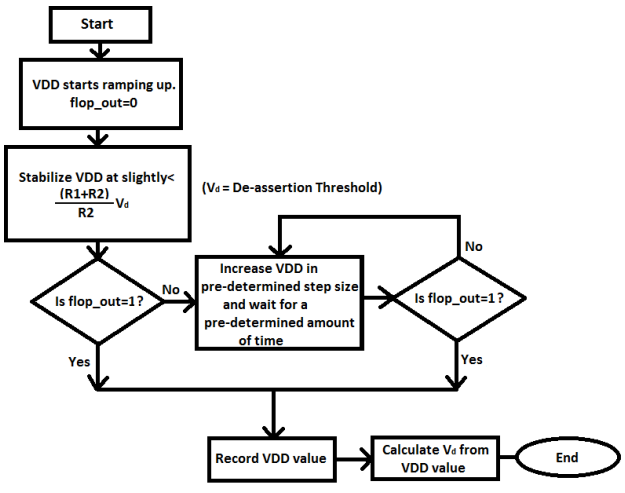

Fig. 5 Flowchart for de-assertion threshold characterization

III. SIMULATION RESULTS

The test circuit was implemented in 28nm CMOS process. For simulations, vdd is ramped-up from 0V to 1.3V and temperature variation is taken from -40C to 125C. The process corners are taken as typ-typ(TT), fast-fast(FF), slow-slow(SS), slow-fast(SF) and fast-slow(FS). The target de-assertion threshold at typical process, voltage and temperature (PVT) corner is 667mV. Fig. 6 shows the transient simulation waveforms of the proposed test circuit across all process and temperature corners in the test mode (fuse shorted). In this case, the vdd voltage range in which flop_out goes high is from 872mV to 1200mV. From this range, the de-assertion threshold range calculated using equation (2) comes out to be from 581.3mV to 800mV.

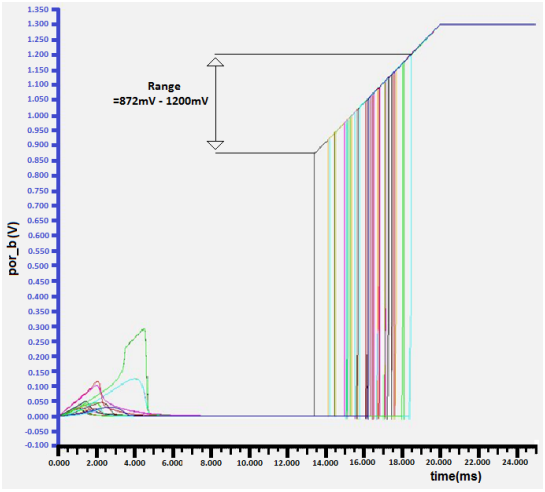

Fig. 6 POR de-assertion threshold in test mode (fuse shorted)

Fig. 7 shows the transient simulation waveforms of the proposed test circuit across all process and temperature corners in the functional mode (fuse open). The de-assertion threshold range obtained is from 583.8mV to 797.7mV which is very close to the range obtained through test mode using equation (2).

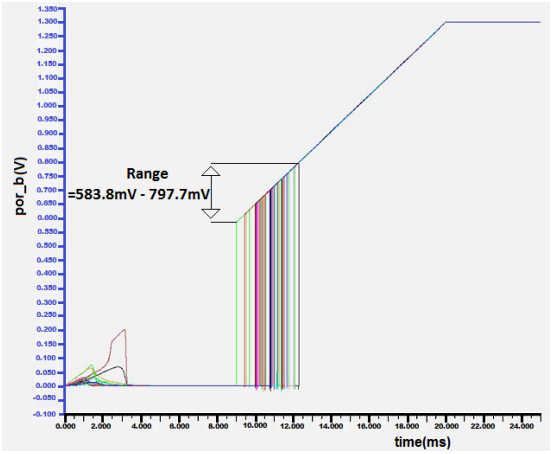

Fig. 7 POR de-assertion in functional mode (fuse open)

Fig. 8 shows the transient simulation waveforms of flop_out. The supply voltage range for flop_out transition remains the same ie. 872mV to 1200mV. Table 1 shows the extrapolated de-assertion threshold obtained from test mode (using equation 2) and simulated de-assertion threshold across different MOSFET and resistance process corners and temperature. It is clear from Table 1 that maximum error between the extrapolated and simulated de-assertion threshold values is less than 0.5% which proves the functionality of the proposed test circuit.

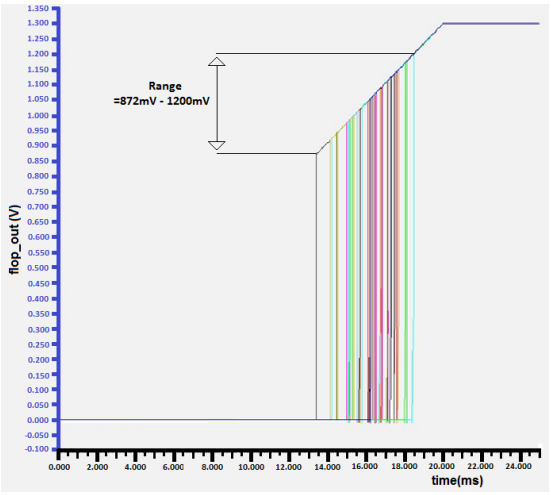

Fig. 8 Transient waveforms of flop_out

IV. CONCLUSION

A test circuit to measure POR de-assertion threshold is presented. It does not require a dedicated analog pad or a supply pad for de-assertion threshold characterization. The test circuit is fuse programmable and generic in nature and can be used with any kind of POR circuit, without having any impact on the functionality of the POR circuit.

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Table 1 Error between simulated and extrapolated de-assertion threshold across process and temperature corners

MOSFET Process Corner	Resistance Process Corner	Temp (°C)	De-assertion Threshold (Test Mode)(mV)	Extrapolated De-assertion Threshold (Test mode)(mV)	Simulated De-assertion Threshold (Functional mode)(mV)	error(mV)	% error
tt	ss	-40	1052	701.33	698.2	3.13	0.45
tt	ss	27	1008	672	672	0	0.00
tt	ss	125	940.5	627	628.6	-1.6	-0.25
tt	tt	-40	1087	724.67	722.2	2.47	0.34
tt	tt	27	1051	700.67	701.1	-0.43	-0.06
tt	tt	125	991.6	661.07	663	-1.93	-0.29
tt	ff	-40	1137	758	756	2	0.26
tt	ff	27	1111	740.67	741.8	-1.13	-0.15
tt	ff	125	1065	710	712.3	-2.3	-0.32
ff	ss	-40	983.6	655.73	654.8	0.93	0.14
ff	ss	27	942.2	628.13	629	-0.87	-0.14
ff	ss	125	872	581.33	583.8	-2.47	-0.42
ff	tt	-40	1019	679.33	678.9	0.43	0.06
ff	tt	27	984.9	656.6	657.7	-1.1	-0.17
ff	tt	125	922.7	615.13	617.9	-2.77	-0.45
ff	ff	-40	1070	713.33	712.8	0.53	0.07
ff	ff	27	1045	696.67	698.6	-1.93	-0.28
ff	ff	125	995.2	663.47	666.9	-3.43	-0.51
ss	ss	-40	1115	743.33	739.8	3.53	0.48
ss	ss	27	1073	715.33	715	0.33	0.05
ss	ss	125	1008	672	673.2	-1.2	-0.18
ss	tt	-40	1150	766.67	763.9	2.77	0.36
ss	tt	27	1116	744	743.7	0.3	0.04
ss	tt	125	1060	706.67	708	-1.33	-0.19
ss	ff	-40	1200	800	797.7	2.3	0.29
ss	ff	27	1176	784	784.3	-0.3	-0.04
ss	ff	125	1134	756	757.9	-1.9	-0.25
sf	ss	-40	1090	726.67	725.1	1.57	0.22
sf	ss	27	1045	696.67	697	-0.33	-0.05
sf	ss	125	974.6	649.73	651.5	-1.77	-0.27
sf	tt	-40	1124	749.33	748.2	1.13	0.15
sf	tt	27	1086	724	724.9	-0.9	-0.12
sf	tt	125	1024	682.67	684.4	-1.73	-0.25
sf	ff	-40	1172	781.33	780.5	0.83	0.11
sf	ff	27	1144	762.67	763.7	-1.03	-0.13
sf	ff	125	1093	728.67	731.4	-2.73	-0.37
fs	ss	-40	1018	678.67	676.4	2.27	0.34
fs	ss	27	979.4	652.93	653	-0.07	-0.01
fs	ss	125	917.2	611.47	612.9	-1.43	-0.23
fs	tt	-40	1056	704	702	2	0.28
fs	tt	27	1025	683.33	683.5	-0.17	-0.02
fs	tt	125	971.7	647.8	649.6	-1.8	-0.28
fs	ff	-40	1110	740	738.4	1.6	0.22
fs	ff	27	1090	726.67	727.7	-1.03	-0.14
fs	ff	125	1050	700	702.5	-2.5	-0.36