Power Control Flow

Driving Innovations™

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Outline

- Terminology
- System block diagram
- Power domain
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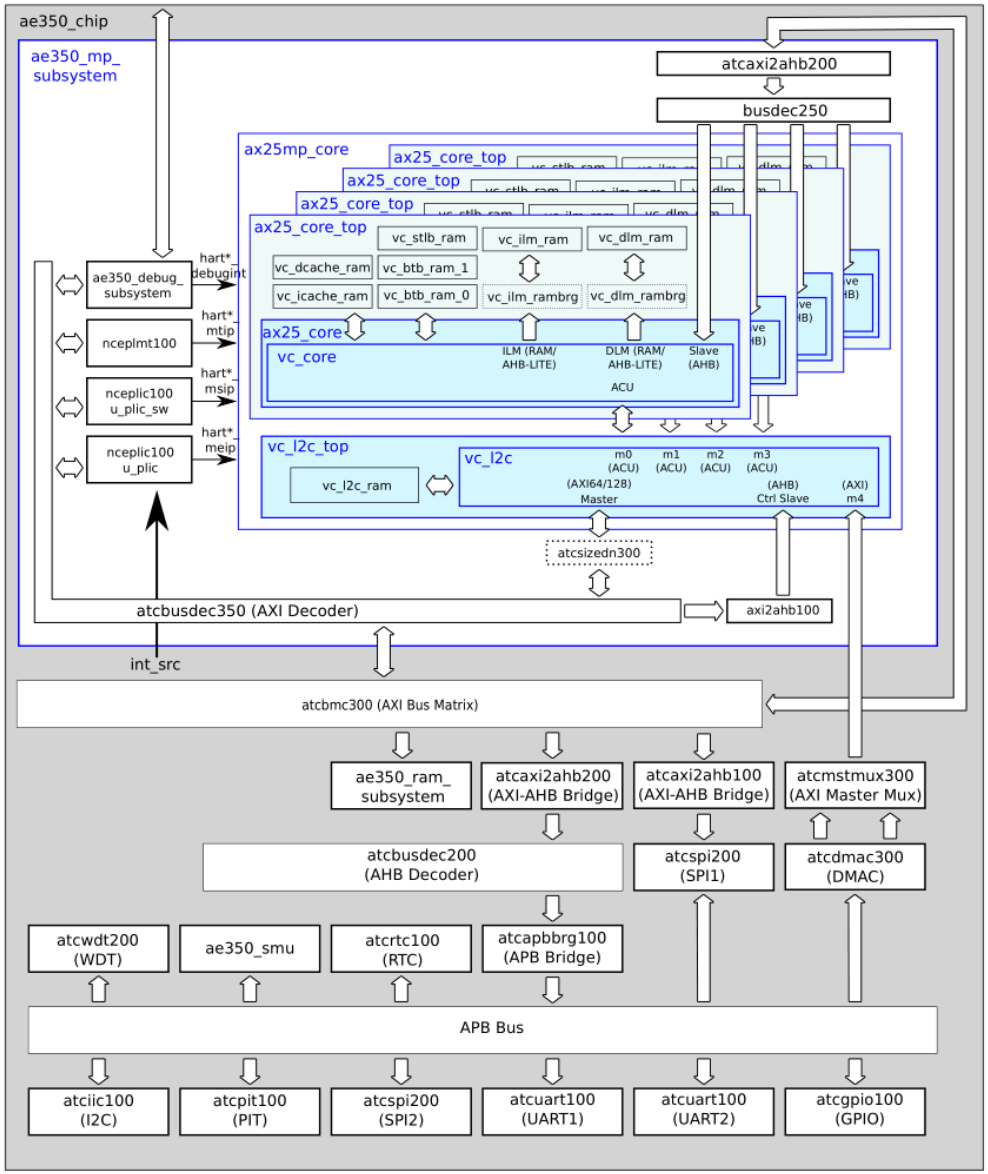
- Power off sequence
- Power on sequence
- Architecture state backup and recovery

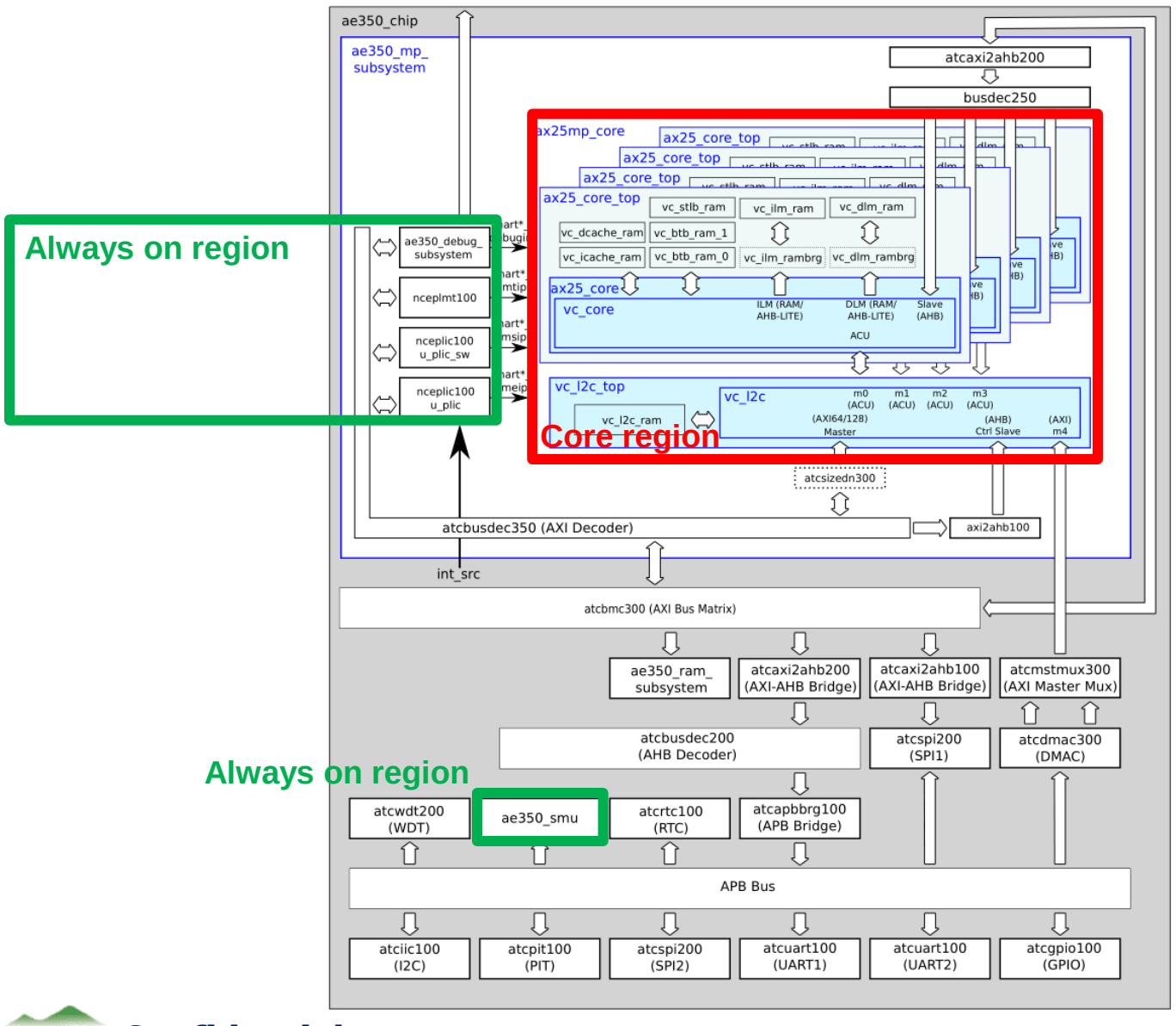
Terminology

- SMU: System Management Unit
- WFI: Wait for interrupt instruction in RISC-V
- BTB: Branch target predictor
- STLB: Shared Translation Lookaside Buffer
- ILM: Instruction local memory
- DLM: Data local memory
- PMP: Physical Memory Protection
- HPM: High Performance Monitor

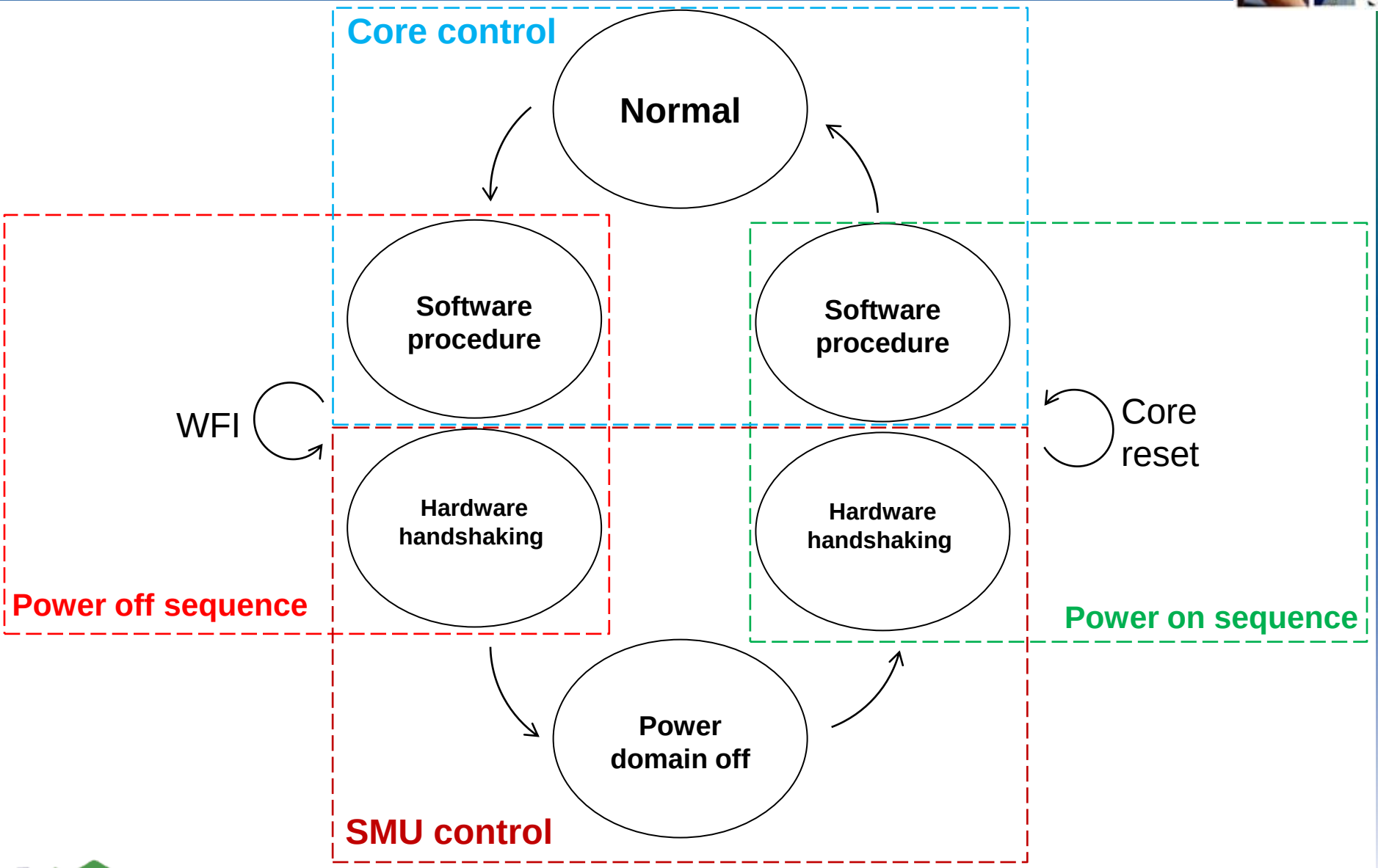
System block diagram



Power domain



System overall flow for power off



Power on sequence

- Hardware handshaking by SMU
  - Assert reset signal for core/memory/L2
  - Assert core*n*_reset_vector to restore program
  - Enable power/clock switch for core/memory/L2 region
  - Disable isolation/retention cell
  - De-assert reset signal for core/memory/L2
- Software procedure by Core
  - Redirect PC to software restore program
    - Software restore CSR/RF/FRF status from RAM
  - Restore interrupt-enable bit (mie) and handle pending interrupt
  - Redirect PC to previous program sequence

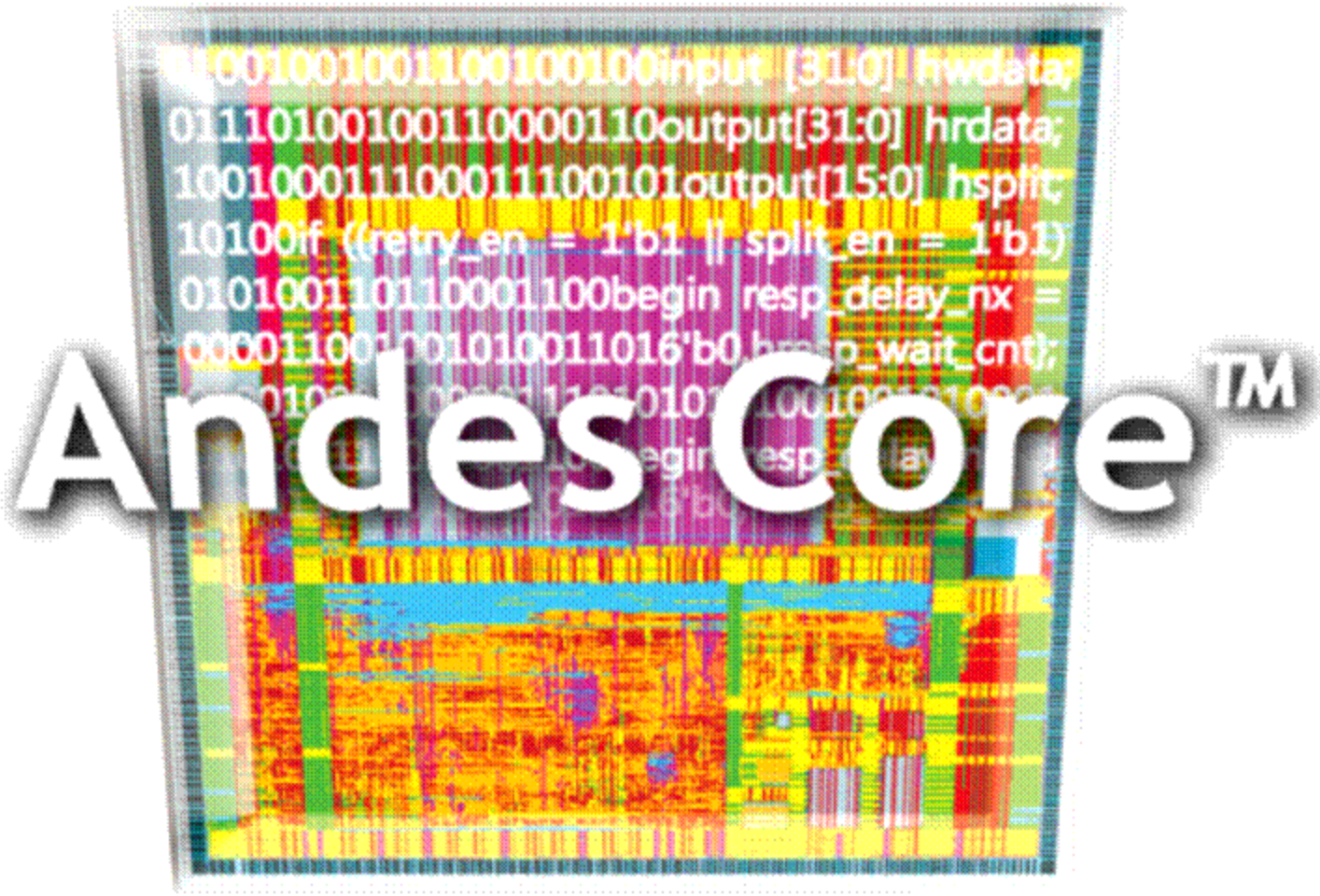
Power off sequence

- Software procedure by Core
  - Disable interrupt-enable bit (mie)
  - Execute FENCE.I for writeback dirty cache line in D-Cache
  - Execute L2 flush command for L2 shutdown
  - Program save CSR/RF/FRF status and resume PC to RAM
  - Execute WFI
- Hardware handshaking by SMU
  - Waits core_wfi_mode asserted from core
  - Enables isolation/retention cell
  - Disable power/clock switch for Core/Memory region

Architecture state backup and recovery

- Baseline RV32/64 register file (x1 ~ x31)
- Floating point RVF/D register file (f0 ~ f31)
- CSRs (Total about 200 CSRs)
  - Status CSRs
  - Trap CSRs
  - PMP CSRs
  - HPM CSRs
  - Debug CSRs
  - AndeStarV5 CSRs

Thank You!



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Thank You!