Power Control Sequencing

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Power-control (power-gating) sequencing ensures that a region of an IC is safely powered down or up, avoiding glitches, excessive leakage, or bus contention. Here's a clear breakdown:

🔌 Power-Down (No Retention)

Typical sequence to shut off a non-retentive power domain:

1. **Flush** pending transactions (bus/IO activity).
2. **Stop clocks** to that block (reduces leakage).
3. **Assert isolation**, clamping outputs to safe values via isolation cells.
4. **Assert reset**, so the block re-initializes cleanly on next power-up.
5. **Assert power-gate signal**, turning off the power switch transistor.

⚡ Power-Up (No Retention)

Sequence to restore power:

1. **De-assert power-gate**, reapplying supply voltage.

2. (Optional) **Phased power-on** of subdomains to limit inrush current.
3. **De-assert reset**, initiating clean start.
4. **De-assert isolation**, reconnecting outputs.
5. **Restart clocks**, synchronized to avoid glitches or timing jumps.

🔁 With Retention

If state must be preserved, extra steps are included:

- **Power-Down**: After isolation, **assert save** to retention flops before power-off.
- **Power-Up**: After de-gating power, use **restore** control to reload state from retention storage.

This avoids full reinitialization and speeds up wake-up.

Core Components

- **Clock stop/gating** significantly reduces dynamic power.
- **Isolation cells** prevent floating outputs from leaking into active blocks.
- **Retention registers** hold state across power-off cycles, using “save” and “restore” signals.

Why it Matters

- **Prevents leakage and crowbar currents** when outputs float.
- **Manages inrush current** by sequencing power, avoiding sudden load spikes.
- **Ensures clean startup**, avoiding unpredictable behavior on wake.
- **Supports fast wake-up** via retention saves.

Example Timing Waveform

This aligns with the bullet-point steps above.

Summary Table

Step Power-Down Power-Up 1 Flush De-assert power-gate 2 Stop clocks Phased power on (opt) 3 Assert isolation De-assert reset 4 Assert reset De-assert isolation 5 Power-gate signal Restart clocks

(With retention: "save" happens after isolation, and "restore" happens after power-on.)

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