JTAG Boundary Scan

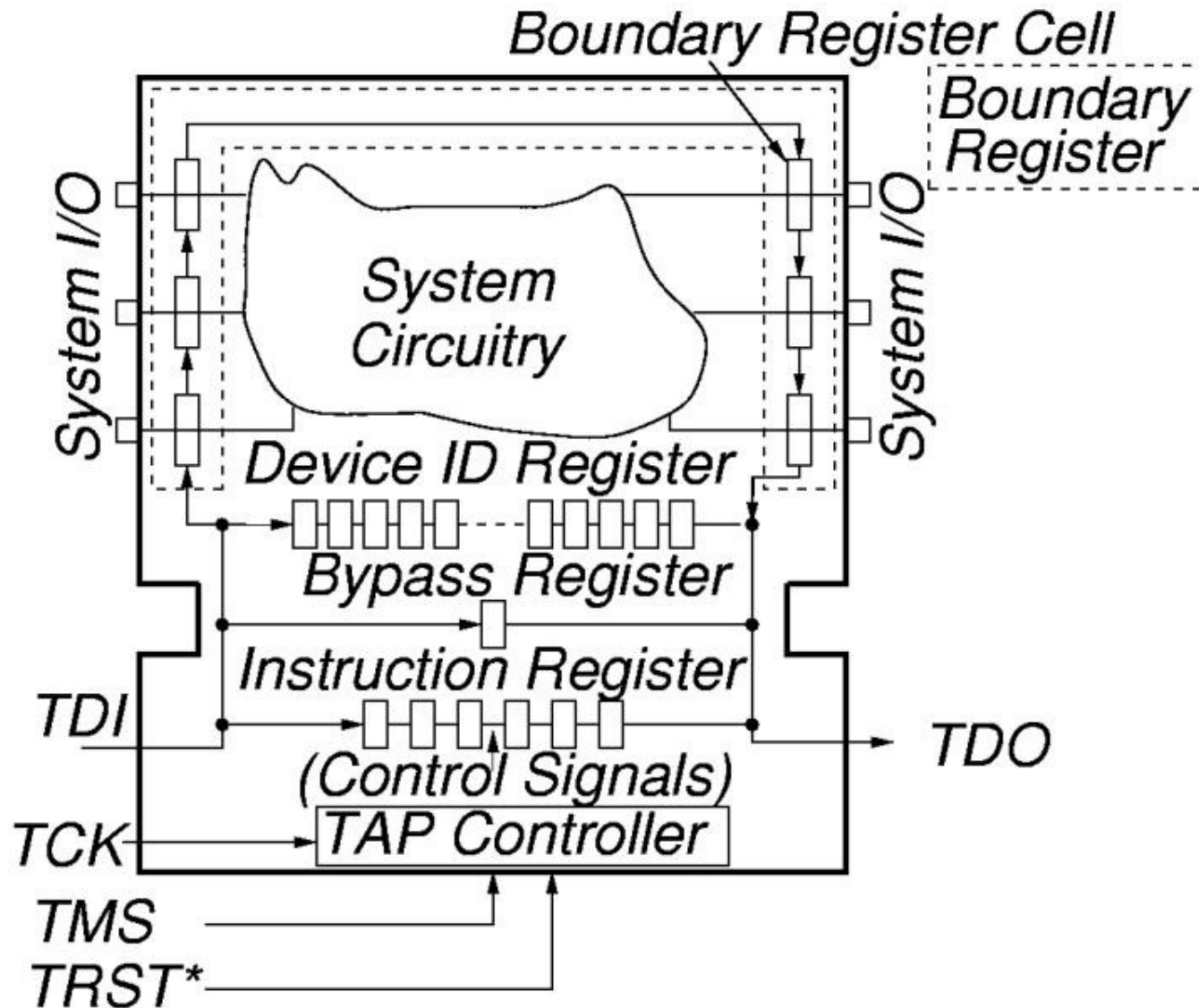# IEEE 1149.1 JTAG
Boundary Scan Standard

- Motivation
- Bed-of-nails tester
- System view of boundary scan hardware
- Elementary *scan cell*
- *Test Access Port* (TAP) controller
- *Boundary scan* instructions
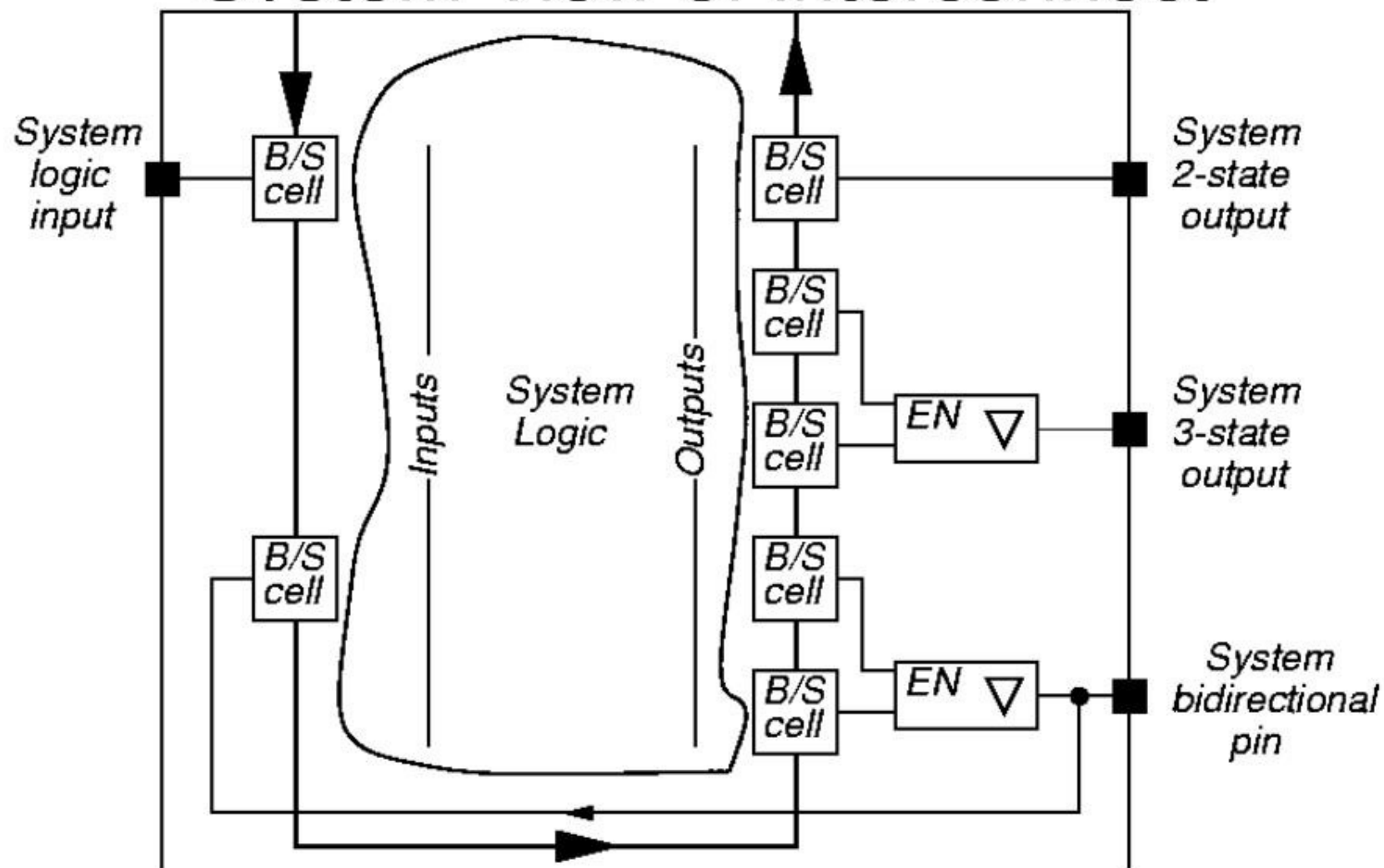- Summary

Motivation for Standard

- ***Bed-of-nails printed circuit board* tester gone**
  - We put components on both sides of PCB & replaced DIPs with flat packs to reduce inductance
    - Nails would hit components
  - Reduced spacing between PCB wires
    - Nails would short the wires
  - PCB Tester must be replaced with built-in test delivery system -- JTAG does that
  - Need standard System Test Port and Bus
  - Integrate components from different vendors
    - Test bus identical for various components
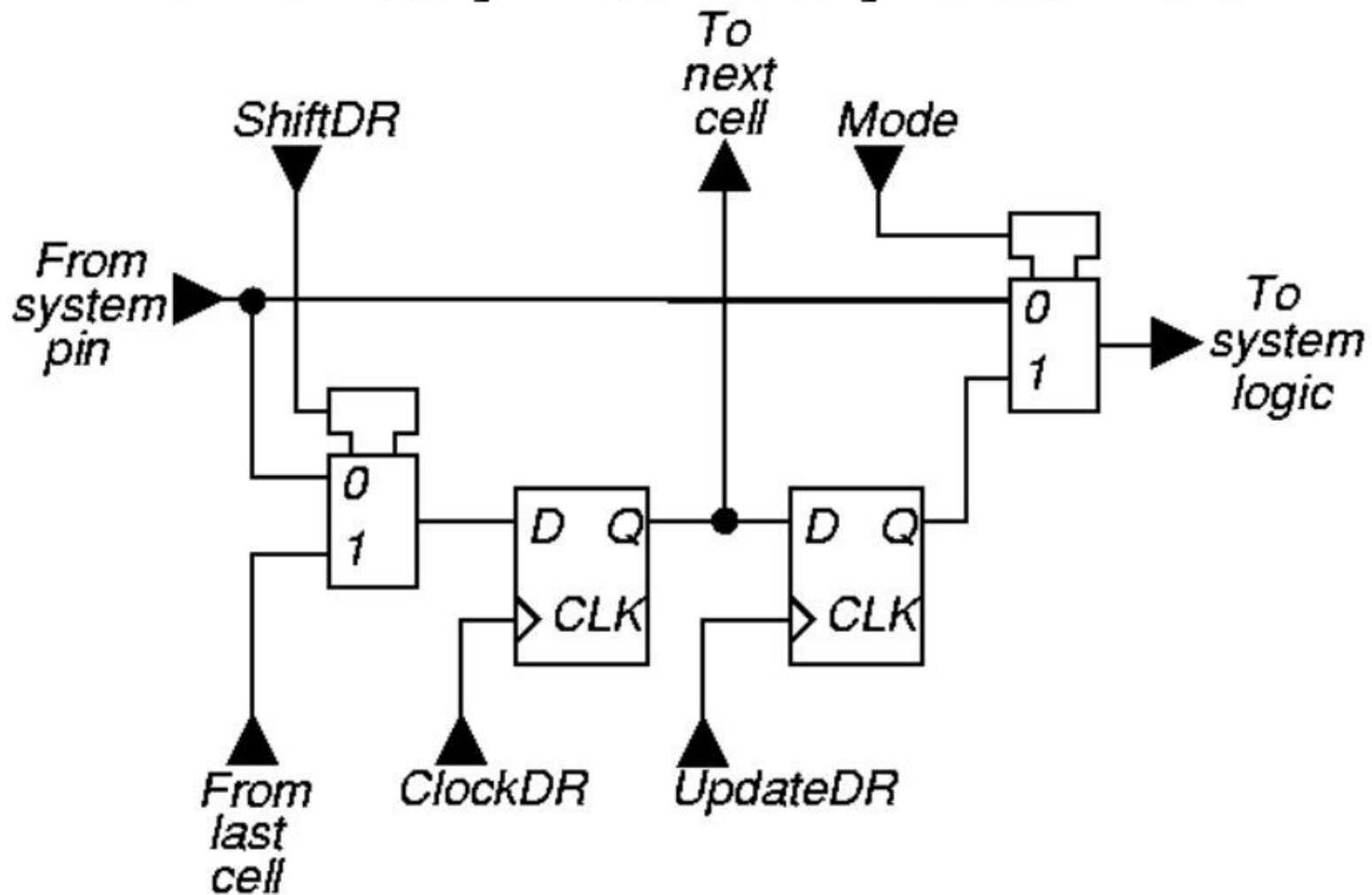   - One chip has test hardware for other chips

System Test Logic

Boundary Register Cell

Boundary Register

Boundary Register Cell

System I/O

System Circuitry

Device ID Register

Bypass Register

Instruction Register

(Control Signals)

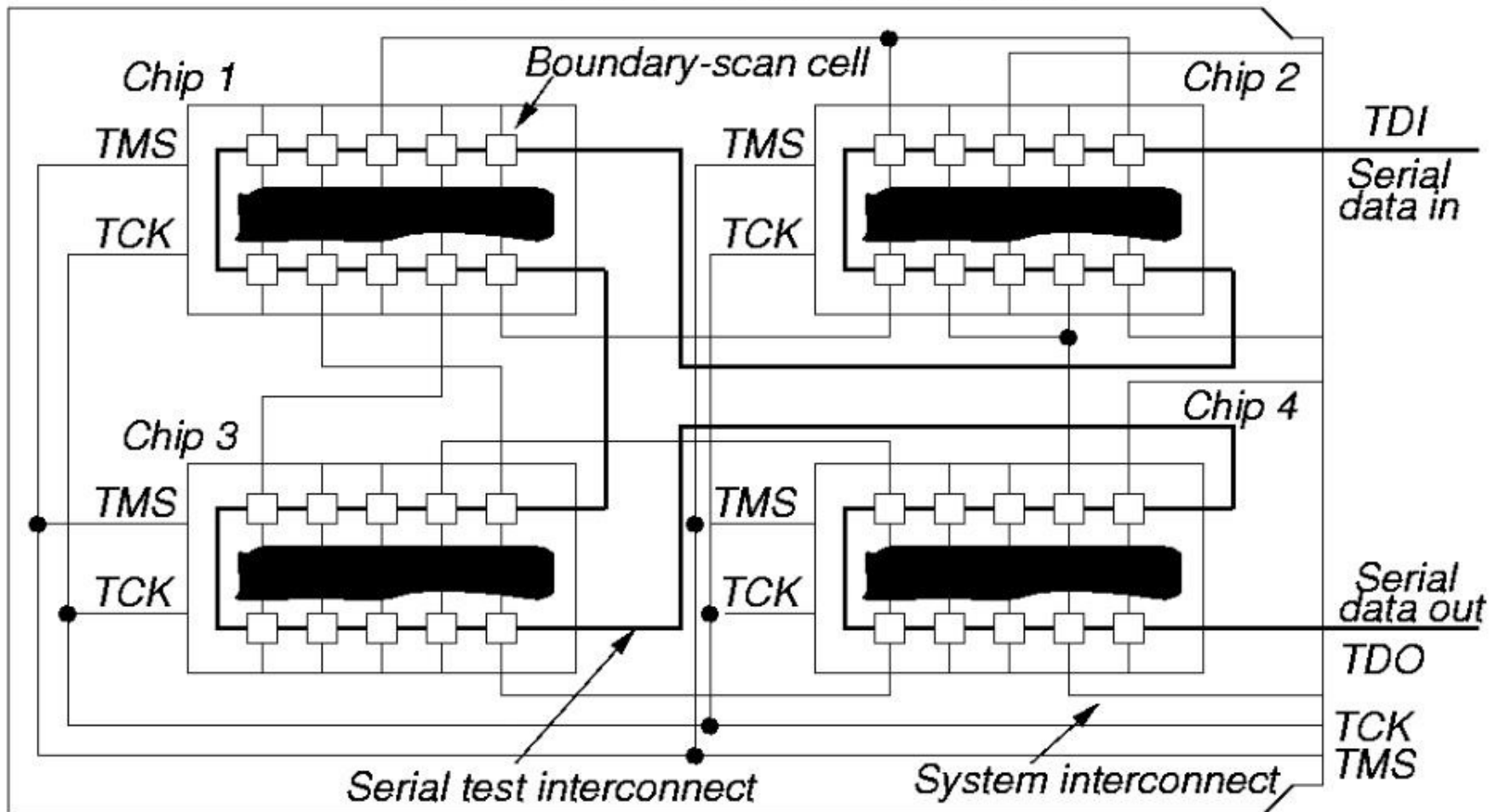TAP Controller

System I/O

TDI

TDO
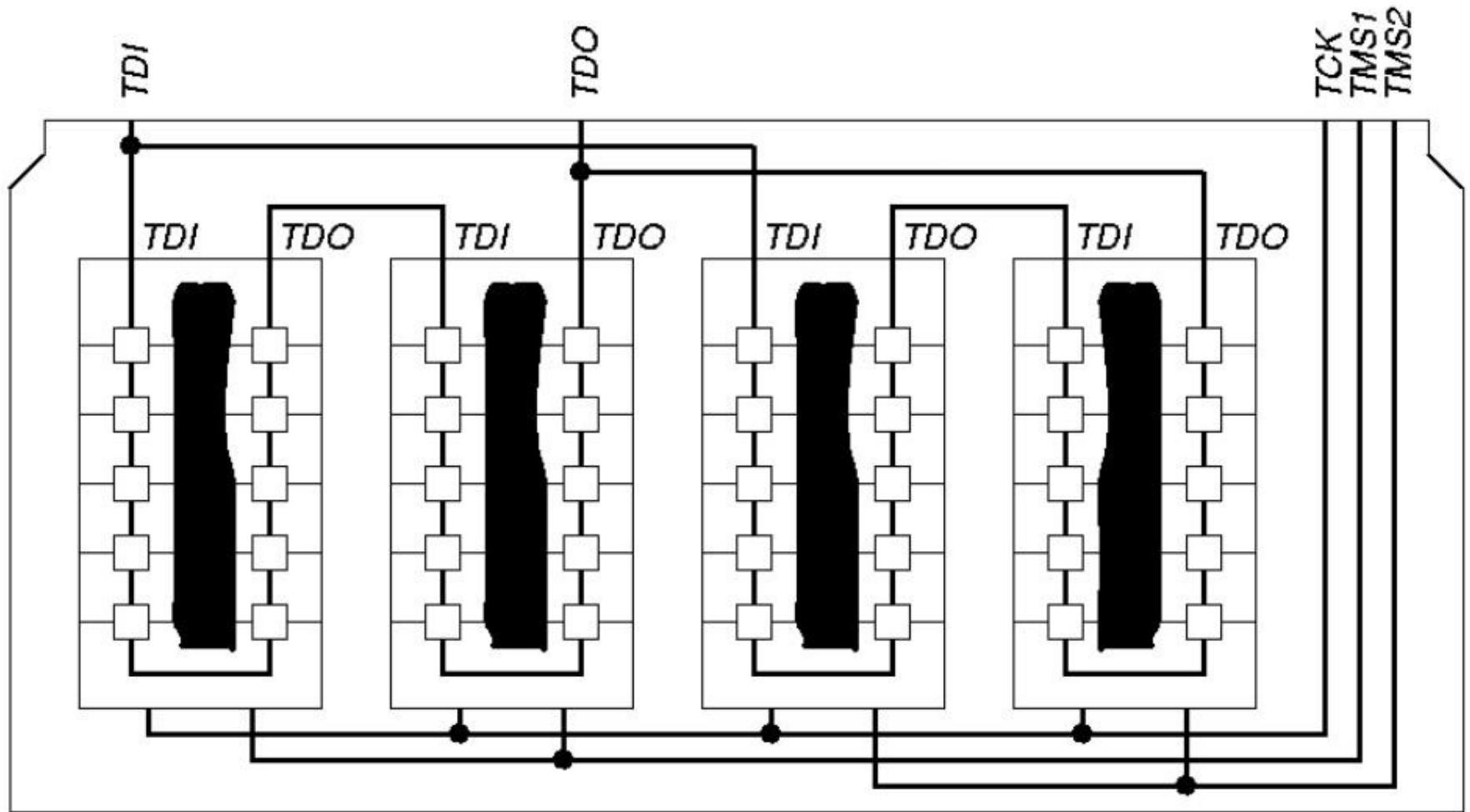
TCK

TMS

TRST*

System View of Interconnect

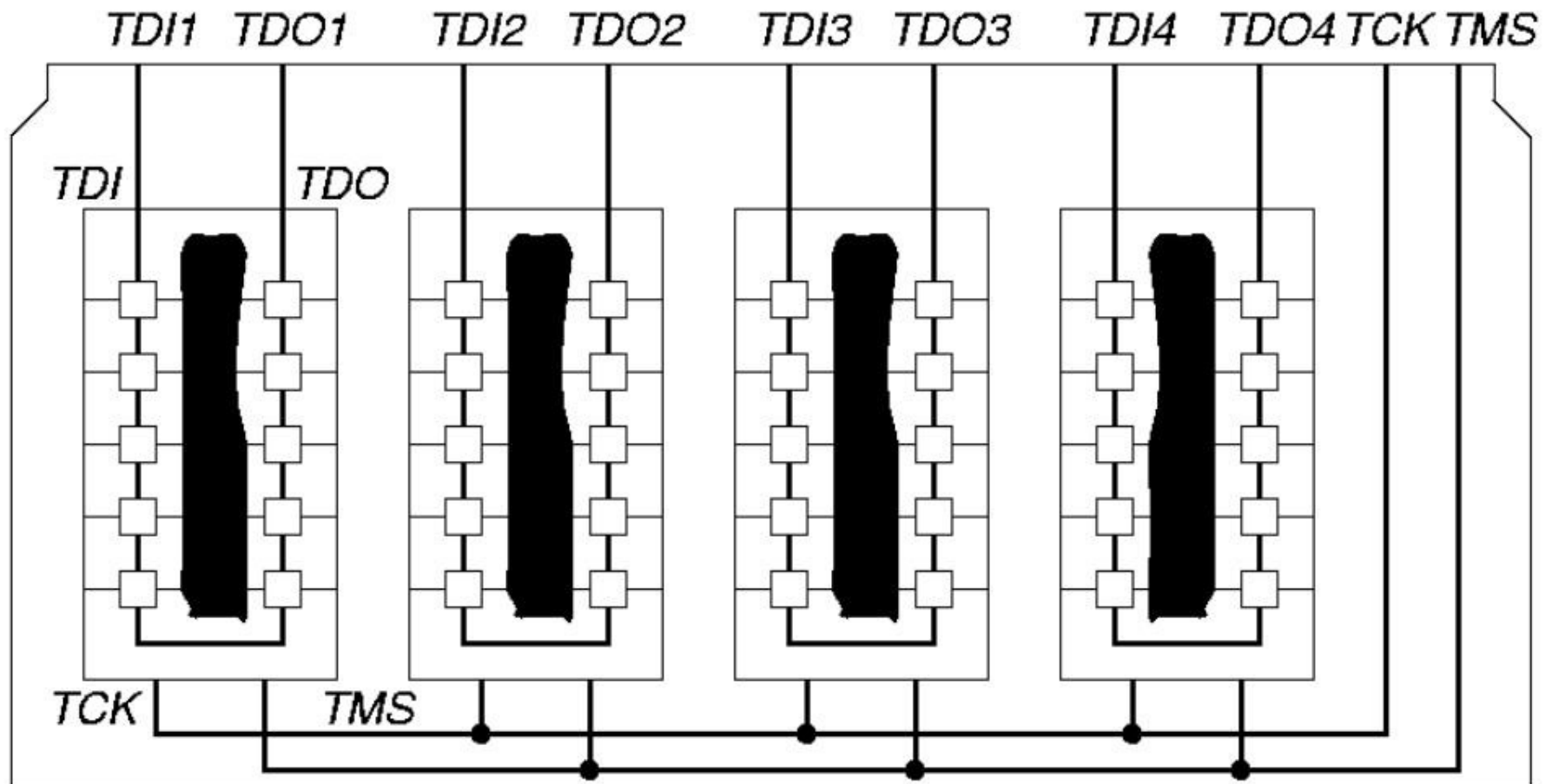# Elementary Boundary Scan Cell

Serial Board Scan

Parallel Board Scan

Independent Path Board Scan

Tap Controller Signals

- *Test Access Port* (TAP) includes these signals:
  - *Test Clock Input* (*TCK*) -- Clock for test logic
    - Can run at different rate from system clock
  - *Test Mode Select* (*TMS*) -- Switches system from functional to test mode
  - *Test Data Input* (*TDI*) -- Accepts serial test data and instructions -- used to shift in vectors or one of many test instructions
  - *Test Data Output* (*TDO*) -- Serially shifts out test results captured in boundary scan chain (or device ID or other internal registers)
  - *Test Reset* (*TRST*) -- *Optional* asynchronous TAP controller reset
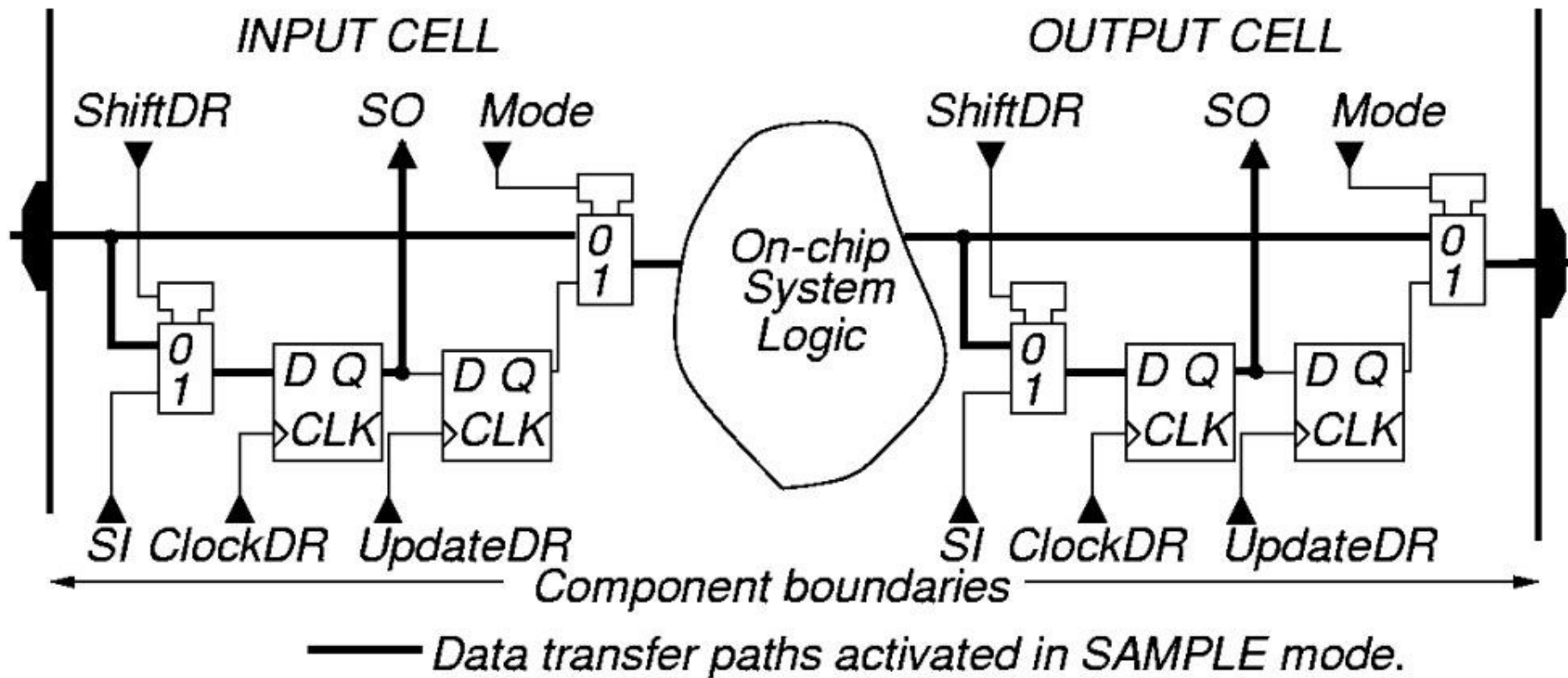
Boundary Scan Instructions:

<u>Sample/Preload</u>:
Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
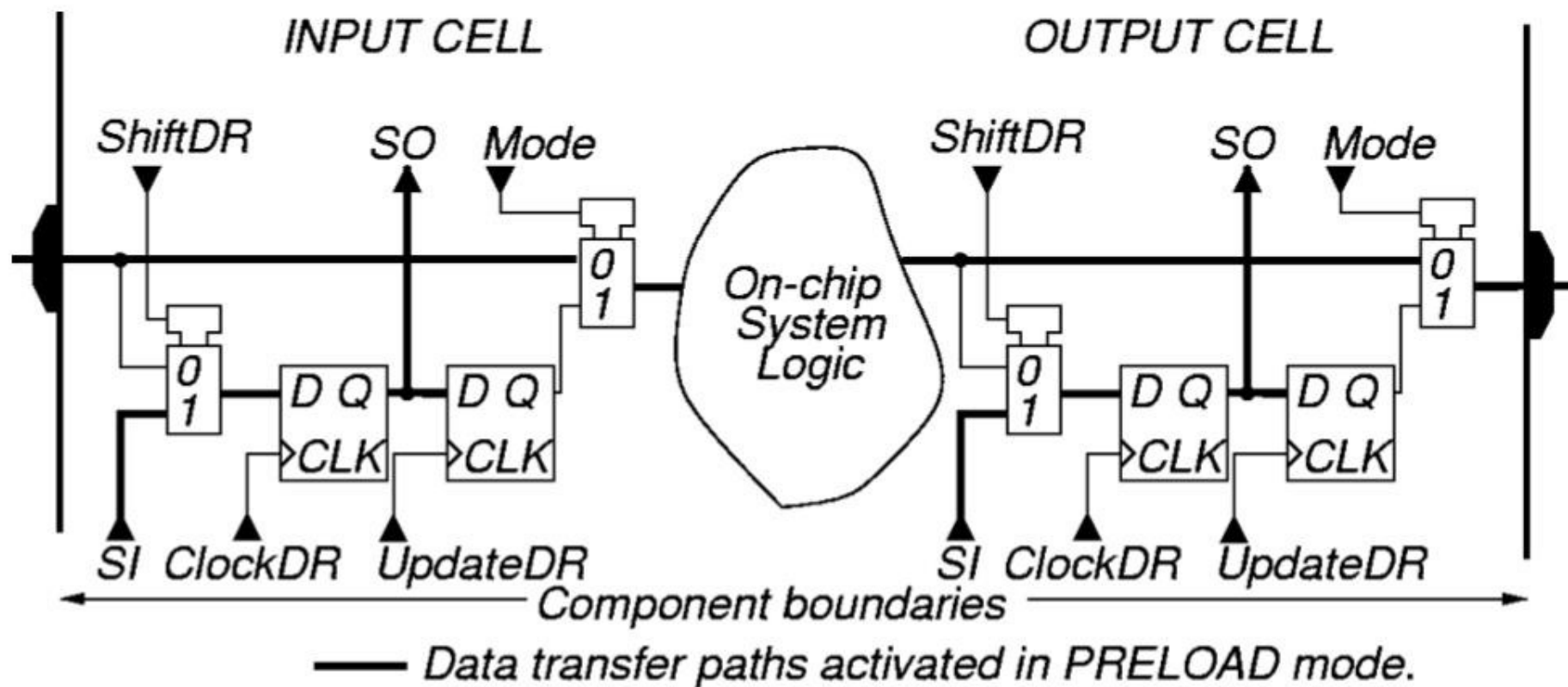
SAMPLE / PRELOAD Instruction -- SAMPLE

Purpose:

1. **Get snapshot of normal chip output signals**
2. **Put data on bound. scan chain before next instr.**

INPUT CELL   OUTPUT CELL

ShiftDR   SO   Mode   ShiftDR   SO   Mode

On-chip System Logic

SI ClockDR UpdateDR   SI ClockDR UpdateDR

Component boundaries

Data transfer paths activated in SAMPLE mode.

SAMPLE / PRELOAD Instruction -- *PRELOAD*

INPUT CELL

OUTPUT CELL

ShiftDR   SO   Mode

ShiftDR   SO   Mode

On-chip System Logic

0 1
0 1

D Q >CLK
D Q >CLK

D Q >CLK
D Q >CLK

SI ClockDR UpdateDR

SI ClockDR UpdateDR

Component boundaries

—— Data transfer paths activated in PRELOAD mode.

EXTEST Instruction

■ **Purpose: Test off-chip circuits and board-level interconnections**

Data transfer paths activated in EXTEST mode.

INTEST Instruction

- **Purpose:**
  1. **Shifts external test patterns onto component**
  2. **External tester shifts component responses out**

INPUT CELL   OUTPUT CELL

ShiftDR   SO   Mode   ShiftDR   SO   Mode

On-chip
System
Logic

SI ClockDR UpdateDR   SI ClockDR UpdateDR

Component boundaries

—— Used for first phase of INTEST

—·—·— Used for second phase of INTEST

—— Not used in the INTEST testing mode

RUNBIST Instruction

- **Purpose: Allows you to issue BIST command to component through JTAG hardware**

- **Optional instruction**

- **Lets test logic control state of output pins**
  1. **Can be determined by pin boundary scan cell**
  2. **Can be forced into high impedance state**

- **BIST result (success or failure) can be left in boundary scan cell or internal cell**

  - **Shift out through boundary scan chain**

- **May leave chip pins in an indeterminate state (reset required before normal operation resumes)**

CLAMP Instruction

- **Purpose: Forces component output signals to be driven by boundary-scan register**

- **Bypasses the boundary scan chain by using the one-bit *Bypass Register***

- **Optional instruction**

- **May have to add RESET hardware to control on-chip logic so that it does not get damaged (by shorting 0's and 1's onto an internal bus, etc.)**

IDCODE Instruction

- **Purpose: Connects the component device <u>identification register serially</u> between *TDI* and *TDO***
  - **In the *Shift-DR* TAP controller state**
- **Allows board-level test controller or external tester to read out component ID**
- **Required whenever a JEDEC identification register is included in the design**

Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
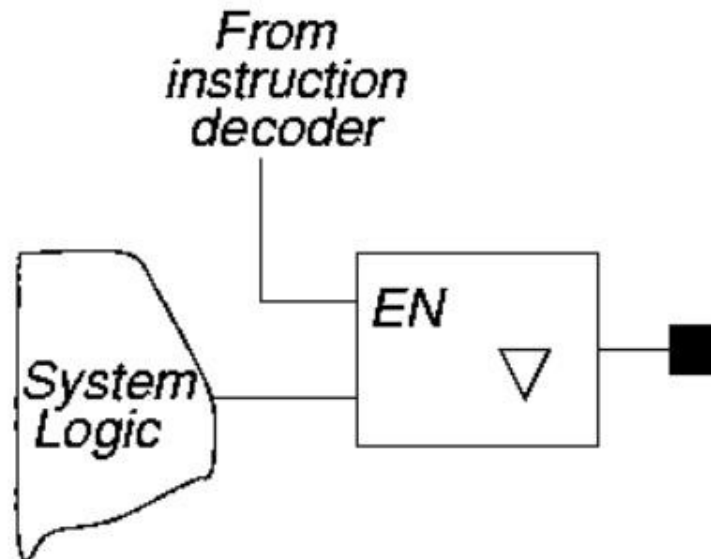
USERCODE Instruction

- ## Purpose:

Selects the USERCODE register and places it between TDI and TDO, allowing the USERCODE to be serially shifted out of TDO.
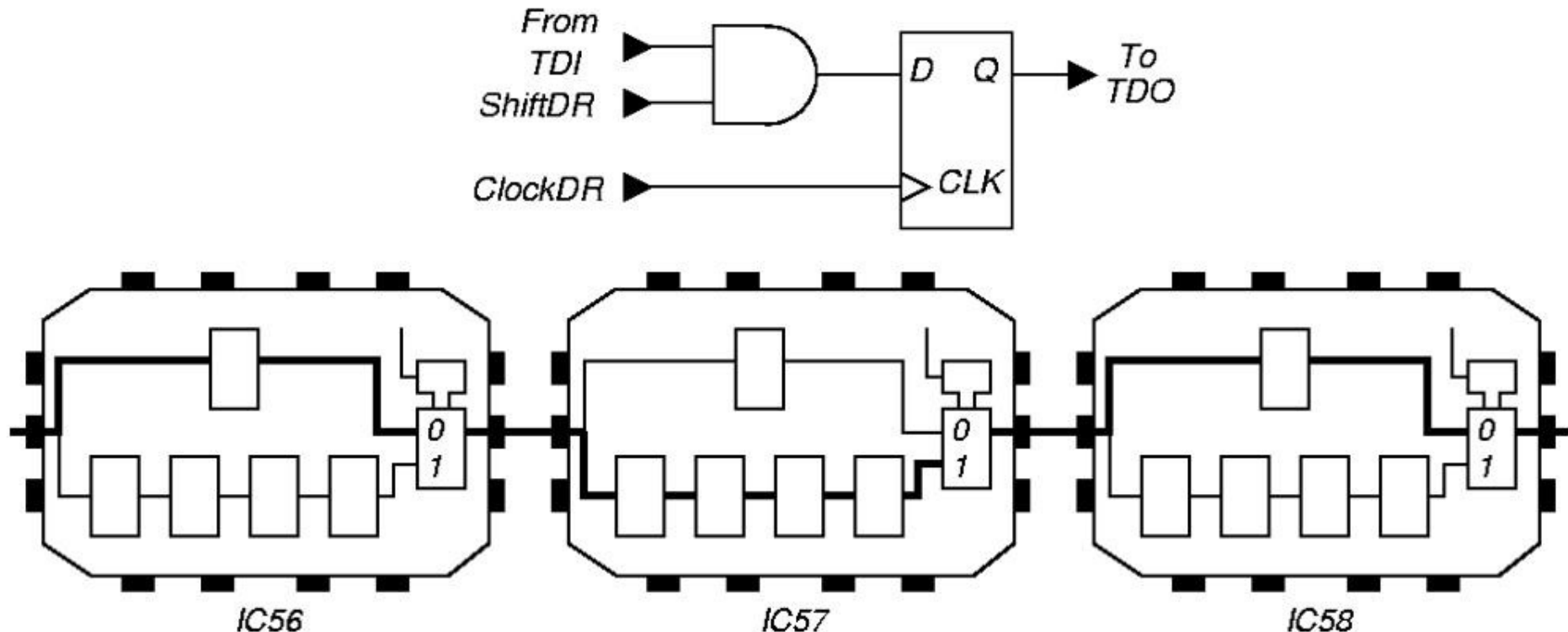
HIGHZ Instruction

- **Purpose: Puts all component output pin signals into high-impedance state**

- **Control chip logic to avoid damage in this mode**

- **May have to reset component after *HIGHZ* runs**

- **Optional instruction**

From
instruction
decoder

EN

System
Logic

BYPASS Instruction

- **Purpose:** A device's boundary scan chain can be skipped using the BYPASS instruction, allowing the data to pass through the bypass register. This allows efficient testing of a selected device without incurring the overhead of traversing through other devices.

Optional / Required Instructions

Instruction	Status
BYPASS	Mandatory
CLAMP	Optional
EXTEST	Mandatory
HIGHZ	Optional
IDCODE	Optional
INTEST	Optional
RUNBIST	Optional
SAMPLE / *PRELOAD*	Mandatory
USERCODE	Optional

Summary

- **Boundary Scan Standard has become absolutely essential --**
  - **No longer possible to test printed circuit boards with _bed-of-nails_ tester**
  - **Not possible to test multi-chip modules at all without it**
  - **Supports BIST, external testing with Automatic Test Equipment, and boundary scan chain reconfiguration as BIST pattern generator and response compacter**
  - **Now getting widespread usage**

IEEE Std. 1149.1 TAP Controller State Machine

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