设为首页 收藏本站 答讯 论坛 大讲堂 人才网 直播 博客 充值/Recharge 排行 分享 任务 全部帖20 在线咨询 jnjn0022 | 🚰 手机号码绑定 | 我的 | 设置 | 消息 | 提醒(1) | 退出 EETOP诚邀线上 消息 积分: 127 | 用户组: 蓝领工人 minglang822 P.CN 新听众 系统提醒(1) 搜帖子 搜标题 请输入搜索内容 EDA资源使用讨论 VCS安装后使用问题 俗源共享 国 爱 | | | | | | | | | | | | 返回列表 见习生 杏麦· 8618 | 同信· 8 VCS安装后使用问题 [复制链接] 发贴收入 10 信元 仄 发表于 2019-1-13 09:33:10 | 只看该作者 ▶ 1# 电梯直达 □ حز -附件收入 0 信元 下载支出 13 信元 如题,楼主在成功安装并破解VCS后,尝试使用了一下示例工程直接make, 但却遇到了如下问题: 注册时间 2018-11-20 最后登录 2020-1-28 在线时间 5 小时 发消息 01. vcs -full64 \ 02. -cpp g++-4.8 \ 03. -cc gcc-4.8 \ 04. -sverilog \ 05. -debug\_all \ 06. -1 com.log \ 07. -f rtl.lst 08. \*\*\* Using c compiler gcc-4.8 instead of cc ... Chronologic VCS (TM) Version M-2017.03-SP2\_Full64 -- Sat Jan 12 17:40:16 2019 10. Copyright (c) 1991-2017 by Synopsys Inc. 11. 12. ALL RIGHTS RESERVED 13. 14. This program is proprietary and confidential information of Synopsys Inc. 15. and may be used and disclosed only as authorized in a license agreement 16. controlling such use and disclosure. 17. 18. Parsing design file './timescale.v' 19. Parsing design file './AndOr.v' 20. Parsing design file './SR.v' 21. Parsing design file './XorNor.v' 22. Parsing design file './Intro Top.v 23. Parsing design file './TestBench.v' 24. Top Level Modules: 25. TestBench TimeScale is 1 ns / 100 ps 26. Starting vcs inline pass... 28. 1 unique modules to generate 29. However, due to incremental compilation, no re-compilation is necessary. make[1]: Entering directory '/home/alan/Desktop/Verilog\_Project/code/lab01\_instroduction/csrc' rm -f \_csrc\*.so pre\_vcsobj\_\*.so share\_vcsobj\_\*.so ld -shared -o .//../simv.daidir//\_csrc0.so objs/amcQw\_d.o rm -f \_csrc0.so 34. if [ -x ../simv ]; then chmod -x ../simv; fi  $35. \quad \text{g++-4.8} \quad \text{-o ../simv} \quad \text{-Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath=-./simv.daidir/ -Wl,-rpath$ rpath='\$ORIGIN'/simv.daidir//scsim.db.dir -rdynamic \_\_2331\_archive\_1.so \_prev\_archive\_1.so \_csrc0.so SIM\_l.o \_csrc0.so rmapats\_mop.o rmapats.o rmar.o rmar\_nd.o rmar\_llvm\_0\_1.o rmar\_llvm\_0\_0.o /home/alan/Desktop/Synopsys/vcs/linux64/lib/libzerosoft rt stubs.so /home/alan/Desktop/Synopsys/vcs/linux64/lib/libvirsim.so /home/alan/Desktop/Synopsys/ycs/linux64/lib/liberrorinf.so /home/alan/Desktop/Synopsys/ycs/linux64/lib/libsnpsmalloc.so /home/alan/Desktop/Synopsys/vcs/linux64/lib/libvcsnew.so /home/alan/Desktop/Synopsys/vcs/linux64/lib/libsimprofile.so /home/alan/Desktop/Synopsys/vcs/linux64/lib/libuclinative.so /home/alan/Desktop/Synopsys/vcs/linux64/lib/vcs\_tls.o -Wl,-whole-archive

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论坛



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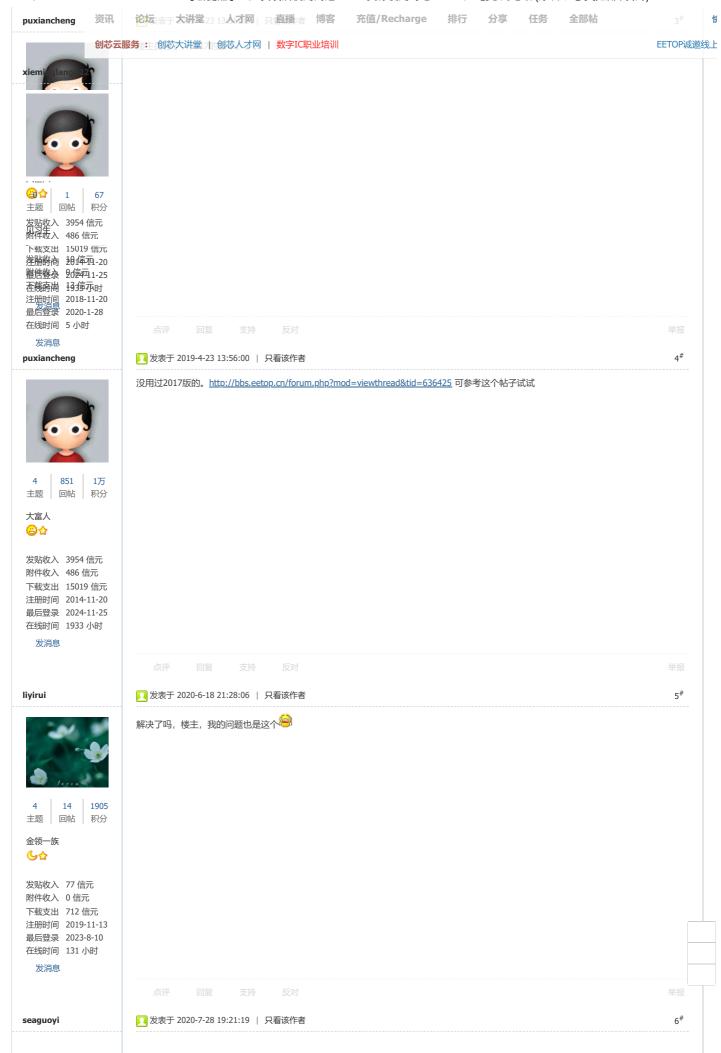
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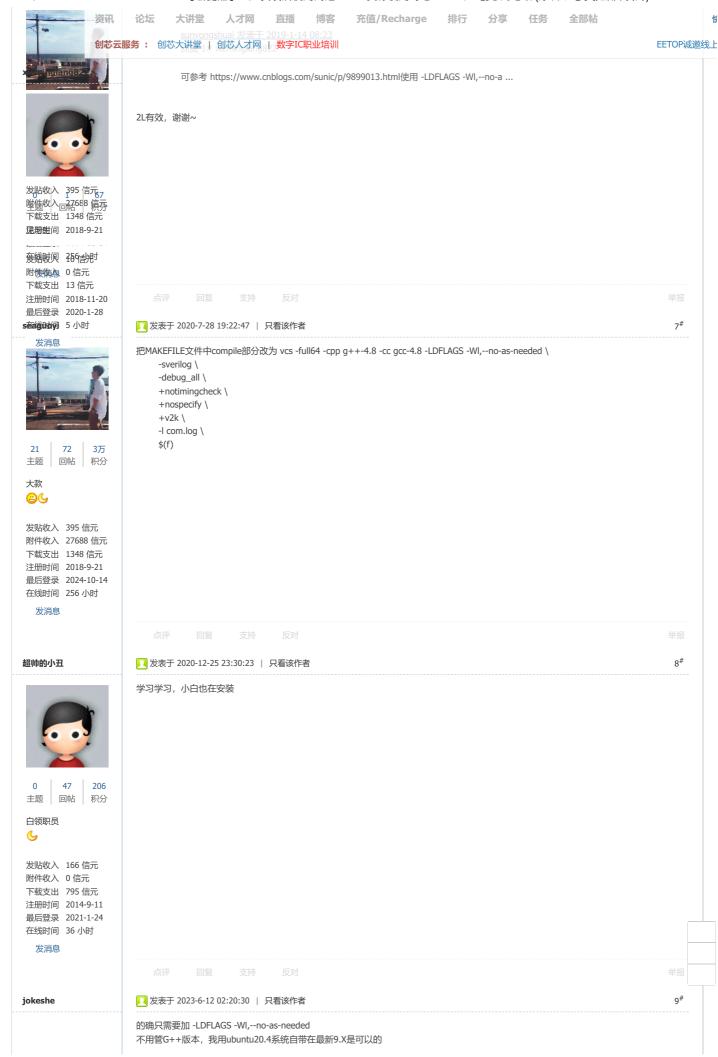
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