Task #5253

Status	Open	**Department**	RD_VLSI
Create Date	2025/07/18 14:15	**Assigned To**	rd-vlsi-support rd
Due Date		**Collaborators**	rd-vlsi-support rd, Abner Chang, 劉美華 Liu

[Presales-AMD]D45/D45-SE PPA using tsmc 16FFC 7.5T

2025/07/18 14:15 May Liu

Hi RD-VLSI:

AMD wants to know D45/D45-SE PPA based on tsmc 16FFC 7.5T, but on tsmc server, there is only tsmc 16FFC 9T. We need backend team to install tsmc 16FFC 7.5T library on the server.

Thanks

May

2025/07/18 14:16 Task Created From Thread Entry May Liu

This Task was created from Ticket **#28835**

2025/07/18 14:29 Eric Sheng-Ching Yiu

Add Abner into collaborators.

Hi Abner,
Please be informed that SA needs tsmc 16FFC 7.5T library for PPA evaluation, please install the required libraries, thanks.

Eric Yiu

2025/07/18 15:10 Abner Chang

Hi, May :

We do have 16FFC 7.5T standard cell libraries (SVT/LVT/ULVT) as below :

1. tcbn16ffcllbwp7d5t16p96cpd_0p72vm40c (SVT)
2. tcbn16ffcllbwp7d5t16p96cpdlvt_0p72vm40c (LVT)
3. tcbn16ffcllbwp7d5t16p96cpdulvt_0p72vm40c (ULVT)

Please check with customer whether the voltage is 0.72v and gate length is 16nm or not.

BR,
Abner

2025/07/19 15:07 May Liu

Hi Abner:

AMD wants to use TSMC 16nm and have a very slow target frequency (like 100MHz), but they have a strict area goal. I wonder if we have typical corner library for 16FFC 7.5T.

We will use tcbn16ffcllbwp7d5t16p96cpd_0p72vm40c (SVT) to do the synthesis first.

Thanks

May

2025/07/21 09:02 Abner Chang

Hi, May :

We do have TT corner libraries under the same SSGNP corner.

Please see below for the TT corner libraries we have installed :

SVT/LVT/ULVT:

tt0p75v25c

tt0p75v85c

tt0p8v25c

tt0p8v85c

tt1v25c

tt1v85c

Please let me know if above voltage and temperature are not compiled with customer's requests.

BR,

Abner

2025/07/21 16:37 May Liu

Hi Abner:

Thanks for your reply.

We are now using tt0p8v85c for synthesis and below is our setting.

```
set tech_lib tcbn16ffcllbwp7d5t16p96cpdssgnp0p72vm40c
set operating_cond ssgnp0p72vm40c
set tech_lib_tc tcbn16ffcllbwp7d5t16p96cpdtt0p8v85c
set operating_cond_tc tt0p8v85c
set tech_lib_path /datavault/TSMCHOME/digital/Front_End/timing_power_noise/NLDM/tcbn16ffcllbwp7d5t16p96cpd_100d
set loading_cell BUFFD1BWP7D5T16P96CPD
set driving_cell BUFFD1BWP7D5T16P96CPD
set max_trans 0.400
set dont_use_cells [list SDF* SED* GSDF* DEL* CKAN2D* CKBD* CKMUX2D* CKND* CKNR2D* CKOR2D* CKXOR2D* DCCK* *OPT* *D0BWP*]
set wire_load_group WireAreaForZero

#mem_lib_path:    Path to memory library cells.
#mem_cond:        Memory macro file name suffix. Specify the file name
#                 suffix for searching the target memory library files in the
#                 memory path. The matched memory macro library file will
#                 be used for the synthesis.
set memory_lib_path /datavault/sram/tsmcn16/db
set mem_cond ssgnp0p72v0p72vm40c
set mem_cond_tc tt0p8v0p8v85c
```

Thanks

May

2025/07/21 17:17 Abner Chang

Hi, May:
These settings should be OK.
Please let me know if there is any question or issue.

BR,
Abner

2025/07/22 14:51 May Liu

Hi Abner:

Our customer also wants to know the PPA at core_clk frequency 800Mhz, what will be the library suggestion if we cannot achieve timing using tcbn16ffcllbwp7d5t16p96cpd_0p72vm40c (SVT)/tt0p8v85c without increasing too much area?

Thanks

May

2025/07/22 16:34 Abner Chang

Hi, May :
I need to know what kind of WNS path types are (R2R/R2M/M2R/I2R/R2O/...).
Can you please give me the timing report path location
(using tcbn16ffcllbwp7d5t16p96cpd_0p72vm40c (SVT)@800MHz) ?
I will analyze the report then give you the feedback.

BR,
Abner

2025/07/22 16:55 May Liu

Hi Abner:

Sure, I will give you the path once I've finished the synthesis.

Thanks for your help

May

2025/07/22 17:47 May Liu

Hi Abner:

The synthesis result for 800 Mhz is at

```
/NOBACKUP/atctsm/maylu751/AMD/D45_SE/d45-se/andes_ip/kv_core/syn/reports_0722.1536
```

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/d45-se/andes_ip/kv_core/syn/reports_0722.1536

It seems that timings are met but have reported some long paths.

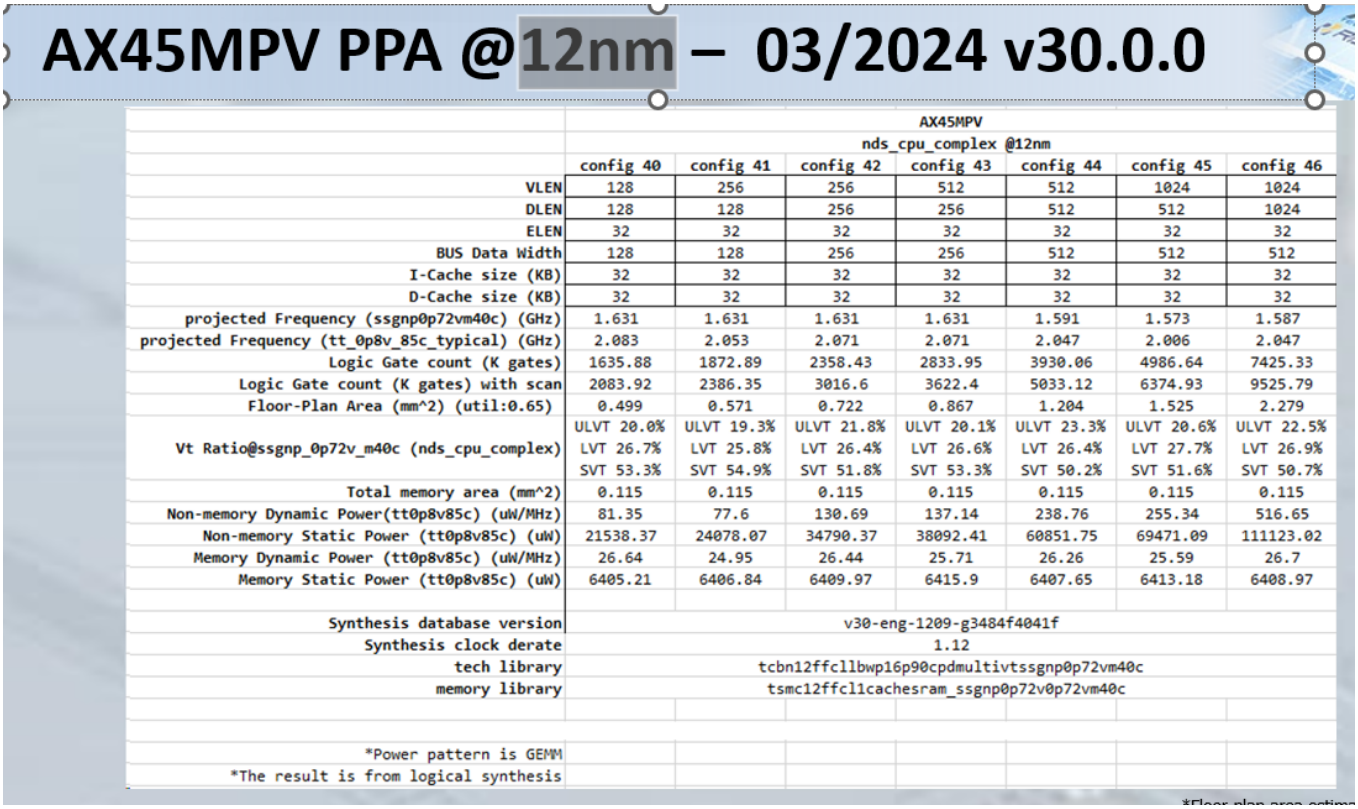
Please help to check, thanks

May

2025/07/24 08:33 May Liu

2025/08/22 07:57
Hi Abner:

We want to use 16 9T library to run the synthesis, and we want to use multi-vt for synthesis like 12nm in the company profile



AX45MPV PPA @12nm – 03/2024 v30.0.0

	AX45MPV nds_cpu_complex @12nm						
	config 40	config 41	config 42	config 43	config 44	config 45	config 46
VLEN	128	256	256	512	512	1024	1024
DLEN	128	128	256	256	512	512	1024
ELEN	32	32	32	32	32	32	32
BUS Data Width	128	128	256	256	512	512	512
I-Cache size (KB)	32	32	32	32	32	32	32
D-Cache size (KB)	32	32	32	32	32	32	32
projected Frequency (ssgnp0p72vm40c) (GHz)	1.631	1.631	1.631	1.631	1.591	1.573	1.587
projected Frequency (tt_0p8v_85c_typical) (GHz)	2.083	2.053	2.071	2.071	2.047	2.006	2.047
Logic Gate count (K gates)	1635.88	1872.89	2358.43	2833.95	3930.06	4986.64	7425.33
Logic Gate count (K gates) with scan	2083.92	2386.35	3016.6	3622.4	5033.12	6374.93	9525.79
Floor-Plan Area (mm^2) (util:0.65)	0.499	0.571	0.722	0.867	1.204	1.525	2.279
Vt Ratio@ssgnp_0p72v_m40c (nds_cpu_complex)	ULVT 20.0% LVT 26.7% SVT 53.3%	ULVT 19.3% LVT 25.8% SVT 54.9%	ULVT 21.8% LVT 26.4% SVT 51.8%	ULVT 20.1% LVT 26.6% SVT 53.3%	ULVT 23.3% LVT 26.4% SVT 50.2%	ULVT 20.6% LVT 27.7% SVT 51.6%	ULVT 22.5% LVT 26.9% SVT 50.7%
Total memory area (mm^2)	0.115	0.115	0.115	0.115	0.115	0.115	0.115
Non-memory Dynamic Power(tt0p8v85c) (uW/MHz)	81.35	77.6	130.69	137.14	238.76	255.34	516.65
Non-memory Static Power (tt0p8v85c) (uW)	21538.37	24078.07	34790.37	38092.41	60851.75	69471.09	111123.02
Memory Dynamic Power (tt0p8v85c) (uW/MHz)	26.64	24.95	26.44	25.71	26.26	25.59	26.7
Memory Static Power (tt0p8v85c) (uW)	6405.21	6406.84	6409.97	6415.9	6407.65	6413.18	6408.97
Synthesis database version	v30-eng-1209-g3484f4041f						
Synthesis clock derate	1.12						
tech library	tcbn12ffcllbwp16p90cpdmultivtssgnp0p72vm40c						
memory library	tsmc12ffcl1cachesram_ssgnp0p72v0p72vm40c						
*Power pattern is GEMM							
*The result is from logical synthesis							

Do we have all svt/lvt/ulvt for 16nm 9T poly pitch 90nm ssgnp0p72vm40c?
thanks!

May

2025/07/24 13:58 Abner Chang

Hi, May :

No, we only have LVT, please see below :

tcbn16ffcllbwp16p90lvtssgnp0p72vm40c

Please let me know if you need SVT and ULVT then I will have download.

2025/07/24 14:08 Yung-Ching Hsiao

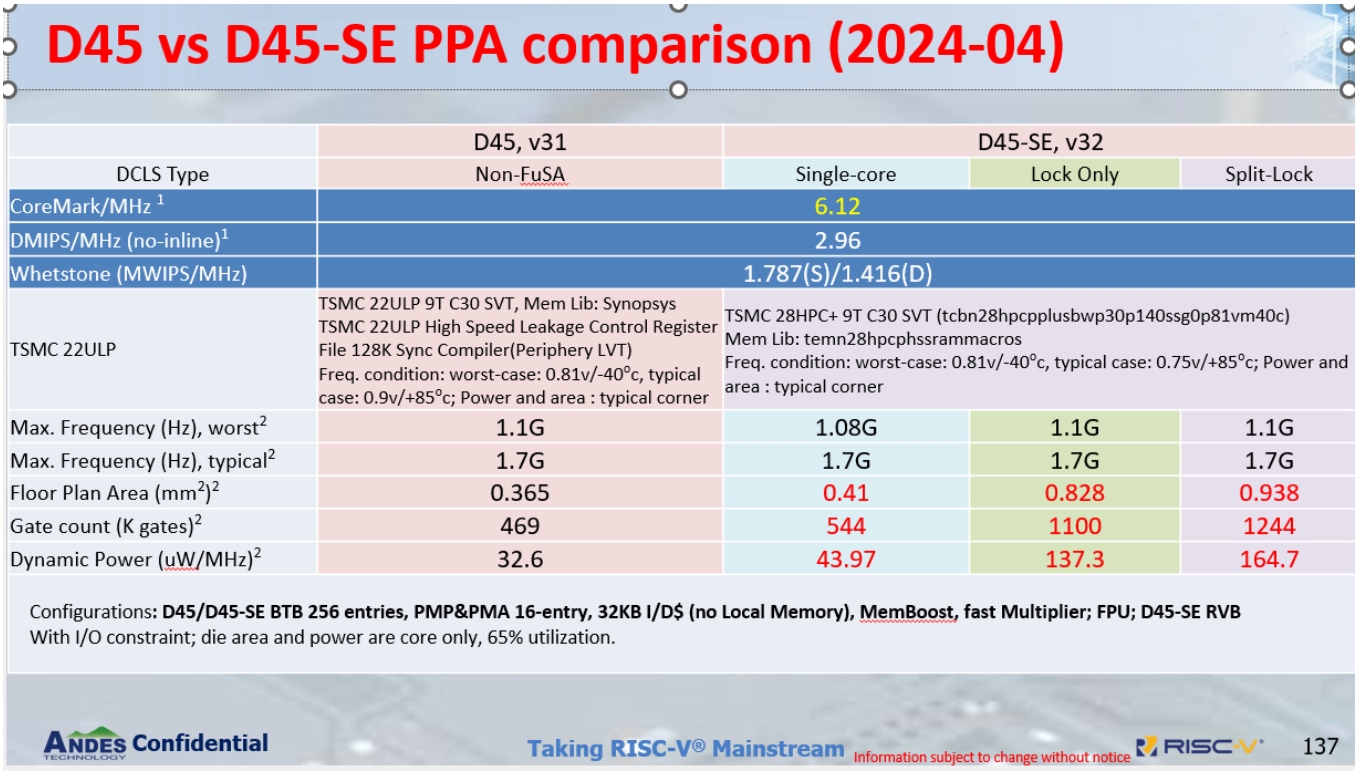
ULVT is something specific to advanced nodes at/below 7nm.

2025/07/24 15:35 May Liu

Hi Yung-Ching and Abner:

Thanks for the update. Currently we are using 16nm 7.5 T SVT (tcbn16ffcllbwp7d5t16p96cpd_0p72vm40c (SVT)) to run D45-SE PPA and can only achieve 800Mhz.

We have tried 16nm 9T ffc+ (tcpn16ffpluslbwp16p90ssgnp0p63vm40c) but the timing got worse. Since in the company profile, D45-SE can achieve 1.1G in 28nm



D45 vs D45-SE PPA comparison (2024-04)

	D45, v31	D45-SE, v32		
DCLS Type	Non-FuSA	Single-core	Lock Only	Split-Lock
CoreMark/MHz [1]	6.12			
DMIPS/MHz (no-inline)[1]	2.96			
Whetstone (MWIPS/MHz)	1.787(S)/1.416(D)			
TSMC 22ULP	TSMC 22ULP 9T C30 SVT, Mem Lib: Synopsys TSMC 22ULP High Speed Leakage Control Register File 128K Sync Compiler(Periphery LVT) Freq. condition: worst-case: 0.81v/-40°c, typical case: 0.9v/+85°c; Power and area : typical corner	TSMC 28HPC+ 9T C30 SVT (tcbn28hpcpplusbwp30p140ssg0p81vm40c) Mem Lib: temn28hpcphssrammacros Freq. condition: worst-case: 0.81v/-40°c, typical case: 0.75v/+85°c; Power and area : typical corner		
Max. Frequency (Hz), worst[2]	1.1G	1.08G	1.1G	1.1G
Max. Frequency (Hz), typical[2]	1.7G	1.7G	1.7G	1.7G
Floor Plan Area (mm²)[2]	0.365	0.41	0.828	0.938
Gate count (K gates)[2]	469	544	1100	1244
Dynamic Power (uW/MHz)[2]	32.6	43.97	137.3	164.7

Configurations: **D45/D45-SE BTB 256 entries, PMP&PMA 16-entry, 32KB I/D$ (no Local Memory), MemBoost, fast Multiplier; FPU; D45-SE RVB**
With I/O constraint; die area and power are core only, 65% utilization.

So we want to try Multi-vt for 16nm 7.5 T and 9T and need RD to install SVT and ULVT for 16 nm 9T (tcbn16ffcllbwp16p90lvtssgnp0p72vm40c)

I wonder if the voltage needs to be the same with 28 nm in order to compare. Current 16nm is 0.72v and 28nm uses 0.81v.

Thanks

May

2025/07/24 16:51 Yung-Ching Hsiao

tcpn16ffplusllbwp16p90ssgnp0p63vm40c is 16FF+, not 16FFC+. FFC/FFC+ are newer nodes. We do not have FFC+ libraries so Abner has to help checking it. But it may be likely that TSMC does not have the libraries for FFC+ - they may leverage thirdparty vendors for such libraries. TSMC claimed +10% perf over 16FFC so we can use 16FFC numbers as proxy: https://semiwiki.com/semiconductor-manufacturers/tsmc/8149-2019-tsmc-technology-symposium-review-part-i/

On the other hand, why don't you use tcbn16ffcllbwp16p90ssgnp0p72v0c? tcbn16ffcllbwp16p90cpdssgnp0p675vm40c is a library with special "CPD" treatments. It seems to be 30% slower.

2025/07/24 16:59 May Liu

Hi Yung-Ching:

Thanks for your reminder. Do you mean the libraries with "cpd" in them result in lower frequency?

We definitely will try tcbn16ffcllbwp16p90ssgnp0p72v0c.

Thanks

May

2025/07/24 17:27 Yung-Ching Hsiao

yes, you can check the rise_time for unit sized buffer in the library. I asked Abner to find out what CPD means - but not sure if we can get the info.

2025/07/25 11:31 May Liu

Hi Abner:

Please install the SVT and ULVT library for tcbn16ffcllbwp16p90lvtssgnp0p72vm40c and tcbn16ffcllbwp16p90ssgnp0p9vm40c for higher voltage.

Thanks

May

2025/07/28 12:46 Abner Chang

Hi, May :

Libraries were installed:

```
 364 tcbn16ffcllbwp16p90ssgnp0p72vm40c  : TSMC 16FFC 9T gate_length 16nm poly_pitch 90nm CPD -40C
 365 tcbn16ffcllbwp16p90ssgnp0p9vm40c   : TSMC 16FFC 9T gate_length 16nm poly_pitch 90nm CPD -40C
makatau.atctsm02$ list_tech_lib  tcbn16ffcllbwp16p90ulvtssgnp
 388 tcbn16ffcllbwp16p90ulvtssgnp0p72vm40c : TSMC 16FFC 9T ULVT gate_length 16nm poly_pitch 90nm CPD -40C
 389 tcbn16ffcllbwp16p90ulvtssgnp0p9vm40c  : TSMC 16FFC 9T ULVT gate_length 16nm poly_pitch 90nm CPD -40C
```

Please have a check and let me know if there is any issue or question.

BR,
Abner

2025/07/28 15:50 Abner Chang

Hi, May :

Please see below from TSMC's feedback about CPD question:

CPD here means "CPODE" (Continuous Poly On Diffusion Edge) , no CPD means it's "PODE" (Poly On Diffusion Edge), CPODE is slight compact than PODE which means CPODE area is smaller.

Please let me know if there is any question.

BR,
Abner

2025/07/28 21:21 May Liu

Hi Abner:

Thanks for installing the libraries, we will use them to set up multi-voltage synthesis environment.

May

2025/07/31 08:57 May Liu

Hi Abner:

We have done synthesis for D45-SE split-lock mode with FP64 using 3 different libraries and below are the results

Library 1

2025/08/22 07:57

[illegible]

We have found that the dynamic power for library 2 (16 nm 9t,0.72v -40c) is relatively small compared with the other two libraries. We want to confirm if this is caused by higher percentage in ULVT. The logs

and reports for three libraries are listed below:

Library 1 :

log: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/logs_0728.1854

reports: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/reports_0728.1854

Library2:

log:/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/logs_0729.1102

reports: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/reports_0729.1102.multivt1600mhz

Library3:

log: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/logs_0730.1559

reports: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/reports_0730.1559

Thanks

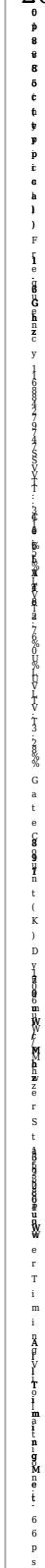
May

2025/08/01 21:00 May Liu

Hi Abner:

Thanks for helping us review the logs. The power was incorrect in the previous thread because libraries were not imported correctly while reporting power. After modifying report_tc_power.tcl, below are the latest results:

Library1



Path and reports paths:

2025/08/22 07:57

Library 1 :

log: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/logs_0801.1648

reports: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/reports_0801.1648

Library 2:

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/d45-se/andes_ip/kv_core/syn/logs_0801.1317

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/d45-se/andes_ip/kv_core/syn/reports_0801.1317

Library3:

log: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/logs_0801.1119

reports: /NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/reports_0801.1119

Thanks

May

2025/08/05 17:20 Abner Chang

Hi, May :

There are three feedback from my checks :

1. I checked and compared synthesis log files and found there is below discrepancy :

The .leakage_power_effort in Library 1 is low but in Library 2 and Library 3 are high

2. And I also found the driving_cell and loading_cell between Library 1 and Library 2/Library 3 are different:

In Library 1 they are: loading_cell/driving_cell : BUFFD1BWP16P90LVT

In Library 2 and Library 3 they are : loading_cell/driving_cell : [list BUFFD1BWP16P90 BUFFD1BWP16P90LVT BUFFD1BWP16P90ULVT]

This will make synthesis tool pick up the worst case (showed by default_emulate_libset_max) which is BUFFD1BWP16P90 (SVT) for external_driver :

'external_driver' = lib_pin:default_emulate_libset_max/tcbn16ffcllbwp16p90ssgnp0p72vm40c/BUFFD1BWP16P90/Z

Suggest use same loading_cell/driving_cell as in Library 1 which is BUFFD1BWP16P90LVT to keep loading_cell/driving_cell the same for power correlation checks.

3. I can't find read_tcf in Library 2 and Library 3 when executing report_tc_power.tcl:

In logs_0801.1648/genus.log , there are below two reading tcf files during report_tc_power.tcl:

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/netlist_0801.1648/ae350_scpu_cluster_subsystem1.tcf

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/netlist_0801.1648/ae350_scpu_cluster_subsystem2.tcf

However I can't find them in logs_0801.1317/genus.log and logs_0801.1119/genus.log

Please have a check and fix.

2025/08/07 22:13 May Liu

Hi Abner:

Thanks for pointing out that write_tcf should not have the option "-hierarchical" which caused the Asserted percentage not to achieve 100%. However I wanted to compare three power results with three options of write_tcf:

```
write_tcf ${DESIGN} > ${output_path}/${DESIGN}${itr}.tcf
write_tcf -hierarchical ${DESIGN} > ${output_path}/${DESIGN}${itr}_hier.tcf
write_tcf -computed ${DESIGN} > ${output_path}/${DESIGN}${itr}_comp.tcf
```

But the power seems to be the same for these three tcf. I'm not sure if this is normal or not.

Below is the path for logs and reports:

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/logs_0806.1711

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/reports_0806.1711

Scripts I've modified:

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/script_rc/d45se.tcl

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/script_rc/report_tc_power.tcl

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/script_rc/report_tc_power_comp.tcl

/NOBACKUP/atctsm/maylu751/AMD/D45_SE/D45_SplitLock_fp64/d45-se/andes_ip/kv_core/syn/script_rc/report_tc_power_hier.tcl

Thanks

May

2025/08/14 10:12 May Liu

Hi All:

Just a short update on this task.

1. Abner uses D45-SE run flow to check the influences on power using different write_tcf parameters. He will also change the power pattern from dhrystone to maximum power case for core since the toggle rate for dhrystone is fairly low.

2. We will also try to integrate the maximum power case into RTL customer package.

Thanks

May

2025/08/18 13:56 Abner Chang

Hi, May :
I did synthesis with more writ_tcf options (-pin -hport; with -computed and -hierarchical there are total 16 combinations) and the results are almost the same which doesn't make sense to me.
I have filed Cadence support ticket : Case #46920645
Will keep you posted.

BR,
Abner

2025/08/20 13:13 Abner Chang

Hi, May :

After phone call with Cadence Genus AE, the conclusion is no matter which options (computed, hierarchical, include_hports, pin) we use Genus always annotates those unasserted objects automatically therefore the power numbers are the same across different options.

The reason why Genus has different options to write out tcf file is because some customers will use other power analysis tool (like PrimePower) to report power which means they want to control the contents of tcf file and let tool to annotate those unasserted objects by tool's algorithm.

As we are IP vendor and we always use Genus for getting PPA number therefore we can forget about these options.

Even though Cadence AE suggests us use -computed option to generate tcf file but I don't think we need to honor as the file size will be big.

Please let me know if there is any question.

BR,
Abner

2025/08/22 15:05 May Liu

Hi All:

Thanks for all the support, we will close this task. Below is the summary:

1. D45/D45-SE can achieve 1.4 GHz using tcbn16ffcllbwp16p90ssgnpop72vm40c multi-voltage SVT/LVT/ULVT(FPU: DP,Multiplier:Fast, I/D cache 16KB, D45-SE: split-lock)

2. Don't need to set all SVT/LVT/ULVT for loading_cell/driving_cell in multi-voltage environment. Pick SVT for power worst case, LVT for better case.

3. There are three parameters for write_tcf

3.1 write_tcf

3.2 write_tcf -hierarchy

3.3 write_tcf -computed --> this will result in 100% asserted rate.

Although 3.1 and 3.2 does not result in 100% asserted rate, the uncomputed will be complete during read_tcf

The above parameters for other power tools (ex: Prime Time), if we use the same tool (Genus) to calculate power, the result will be the same.

4. Check Toggle rate for TCF:

Add the below line after read_tcf to check toggle rate of the power pattern:

```
applet load check_toggle_quality
redirect $report_path/check_toggle_quality.rpt {check_toggle_quality -all}
```

Thanks

May

2025/08/22 15:07 May Liu

Typo in the previous message:

write_tcf -hierarchy -->write_tcf -hierarchical