

# **AndeStar V5**

# **BFLOAT16 Conversion**

# **Extension**

Document Number      v0.5

Date Issued            2019-10-22

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## Revision History

Rev.	Revision Date	Revised Content
<b>0.5</b>	2019/10/22	Added NAN processing steps for VFWCVT.S.BF16 and FCVT.S.BF16 instructions. (Section 3.1.1, 3.2.1)
<b>0.4</b>	2019/8/21	Changed vfncvt.bf16.s to be defined for SEW=16, not SEW=32.
<b>0.3</b>	2019/8/16	Added intrinsic functions for scalar conversion instructions.
<b>0.2</b>	2019/8/14	Added scalar conversion instructions and configuration register bit.
<b>0.1</b>	2019/8/13	Initial release.

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## Typographical Convention Index

Document Element	Font	Font Style	Size	Color
Normal text	Georgia	Normal	12	Black
Command line, source code or file paths	Lucida Console	Normal	11	Indigo
VARIABLES OR PARAMETERS IN COMMAND LINE, SOURCE CODE OR FILE PATHS	LUCIDA CONSOLE	BOLD + ALL-CAPS	11	INDIGO
Note or warning	Georgia	Normal	12	Red
<a href="#">Hyperlink</a>	Georgia	<u>Underlined</u>	12	Blue

## 1. Introduction

This specification defines vector and scalar floating-point conversion instructions to convert between the BFLOAT16 floating-point data in a vector or scalar register and the IEEE-754 32-bit single-precision floating-point data in a vector or scalar register.



## 2. Instruction Summary

This section summarizes the added floating-point conversion instructions in the BFLOAT16 conversion extension.

### 2.1. Instruction Operation Summary

Table 1. BLOAT16 Vector Conversion Instructions

No.	Mnemonic	Instruction	Operation
1	vfwcvt.s.bf16 vd, vs // defined for SEW=16	Vector widening conversion from BFLOAT16 to SP.	vd[i].H[1] = vs[i]; vd[i].H[0] = 0;
2	vfnvcvt.bf16.s vd, vs // defined for SEW=16	Vector narrowing conversion from SP to BFLOAT16.	vd[i] = V_SP_TO_BF16(vs[i])

Table 2. BLOAT16 Scalar Conversion Instructions

No.	Mnemonic	Instruction	Operation
1	fcvt.s.bf16 frd, frs	Scalar conversion from BFLOAT16 to SP.	frd.H[1] = frs.H[0]; frd.H[0] = 0; frd = Nan-Boxing(frd.W[0])
2	fcvt.bf16.s frd, frs	Scalar conversion from SP to BFLOAT16.	frd.H[0] = S_SP_TO_BF16(frs.W[0]); frd = Nan-Boxing(frd.H[0]);

## 2.2. Instruction Encoding Summary

### 2.2.1. Vector Extension

Figure 1. vfwcvt.s.bf16 instruction encoding (SEW=16)

31	25	24	20	19	15	14	12	11	7	6	0
0000000	vs	00000	100	vd	Custom-2 1011011						

Figure 2. vfncvt.bf16.s instruction encoding (SEW=16)

31	25	24	20	19	15	14	12	11	7	6	0
0000000	vs	00001	100	vd	Custom-2 1011011						

### 2.2.2. Scalar Extension

Figure 3. fcvt.s.bf16 instruction encoding

31	25	24	20	19	15	14	12	11	7	6	0
0000000	frs	00010	100	frd	Custom-2 1011011						

Figure 4. fcvt.bf16.s instruction encoding

31	25	24	20	19	15	14	12	11	7	6	0
0000000	frs	00011	100	frd	Custom-2 1011011						

### 3. Detailed Instruction Description

#### 3.1. Andes V5 Vector BFLOAT16 Conversion Extension

This extension is present if `misa.V == 1` and `mmisc_cfg.BF16CVT == 1` (`mmisc_cfg2.BF16CVT` for RV32).

##### 3.1.1. VFWCVT.S.BF16 (Vector BF16 to 32-bit SP Conversion)

**Type:** Vector BFLOAT16 conversion extension

**Format:**

31	25	24	20	19	15	14	12	11	7	6	0
0000000	vs	00000	100	vd	Custom-2 1011011						

**Syntax:** VFWCVT.S.BF16 vd, vs

**Purpose:** Convert BFLOAT16 data to single-precision floating-point (SP) data.

**Description:** This instruction converts BFLOAT16 data in vector register “vs” to single-precision floating-point (SP) data and writes the result to vector register “vd”. This instruction is not masked.

This instruction is only defined for SEW=16. When this instruction is executed, if SEW is not 16, an illegal instruction exception will be generated.

**Operations:**

```

if (vs[i] != NAN) {
    vd[i].H[1] = vs[i];
    vd[i].H[0] = 0;
} else {
    vd[i] = 0x7fc00000;
}

```

**Exceptions:** Illegal instruction exception

**Privilege level:** All

**Note:**

## AndeStar V5 BFLOAT16 Conversion Extension

### 3.1.2. VFNCVT.BF16.S (Vector 32-bit SP to BF16 Conversion)

**Type:** Vector BFLOAT16 conversion extension

**Format:**

31	25	24	20	19	15	14	12	11	7	6	0
0000000	vs	00001	100	vd	Custom-2 1011011						

**Syntax:** VFNCVT.BF16.S vd, vs

**Purpose:** Convert single-precision floating-point (SP) data to BFLOAT16 data.

**Description:** This instruction converts single-precision floating-point (SP) data in vector register “vs” to BFLOAT16 data and writes the result to vector register “vd”. The rounding mode used by the conversion operation will be specified in the fcsr.frm field.

This instruction is not masked.

This instruction is only defined for SEW=16. When this instruction is executed, if SEW is not 16, an illegal instruction exception will be generated.

**Operations:**

```
vd[i] = V_SP_TO_BF16(vs[i], fcsr.frm);
```

**Exceptions:** Illegal instruction exception

**Privilege level:** All

**Note:**

## 3.2. Andes V5 Scalar BFLOAT16 Conversion Extension

This extension is present if `misa.F == 1` and `mmisc_cfg.BF16CVT == 1` (`mmisc_cfg2.BF16CVT` for RV32).

### 3.2.1. FCVT.S.BF16 (Scalar BF16 to 32-bit SP Conversion)

**Type:** RVF

**Format:**

31	25	24	20	19	15	14	12	11	7	6	0
0000000	frs	00010	100	frd	Custom-2 1011011						

**Syntax:** `FCVT.S.BF16 frd, frs`

**Purpose:** Convert BFLOAT16 data to single-precision floating-point (SP) data.

**Description:** This instruction converts BFLOAT16 data in floating-point register “frs” to single-precision floating-point (SP) data and writes the result to floating-point register “frd”.

**Operations:**

```

if (frs.H[0] != NAN) {
    frd.H[1] = frs.H[0];
    frd.H[0] = 0;
} else {
    frd.w[0] = 0x7fc00000;
}
frd = NaN-Boxing(frd.w[0]);

```

**Exceptions:**

**Privilege level:** All

**Note:**

**Intrinsic Functions:**

```
float __nds_fcvt_s_bf16(float bf16_src);
```



## 3.2.2. FCVT.BF16.S (Scalar 32-bit SP to BF16 Conversion)

**Type:** RVF

**Format:**

31	25	24	20	19	15	14	12	11	7	6	0
00000000	frs	00011	100	frd	Custom-2 1011011						

**Syntax:** FCVT.BF16.S frd, frs

**Purpose:** Convert single-precision floating-point (SP) data to BFLOAT16 data.

**Description:** This instruction converts single-precision floating-point (SP) data in floating-point register “frs” to BFLOAT16 data and writes the result to floating-point register “frd”. The rounding mode used by the conversion operation will be specified in the fcsr.frm field.

**Operations:**

```
frd.H[0] = S_SP_TO_BF16(frs.W[0], fcsr.frm);
frd = Nan-Boxing(frd.H[0]);
```

**Exceptions:**

**Privilege level:** All

**Note:**

**Intrinsic Functions:**

```
float __nds_fcvt_bf16_s(float fp32_src);
```



## 4. New and Modified Control & Status Registers

### Brief Summary

Type	Symbolic Mnemonics	CSR Address				Hex	Page
		[11:10]	[9:8]	[7:6]	[5:0]		
Modified	mmsc_cfg	11	11	11	000010	0xFC2	11
New in RV32	mmsc_cfg2	11	11	11	000011	0xFC3	13

## AndeStar V5 BFLOAT16 Conversion Extension

### 4.1.1. Misc. Configuration Register

Mnemonic Name: mmisc\_cfg

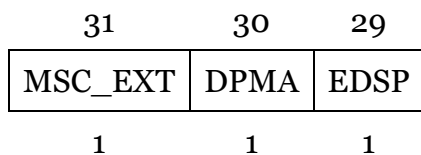
IM Requirement: Required

Access Mode: Machine

CSR Address: 0xFC2 (non-standard read only)

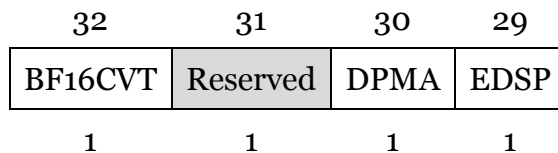
XLEN: 64 and 32

RV32:



Field Name	Bits	Description	Type	Reset	
MSC_EXT	[31]	Indicates if mmisc_cfg2 CSR is present or not.	RO	IM	
		Value			Meaning
		0			The mmisc_cfg2 CSR is not present.
		1			The mmisc_cfg2 CSR is present.

RV64:



## AndeStar V5 BFLOAT16 Conversion Extension

Field Name	Bits	Description		Type	Reset
BF16CVT	[32]	Indicates if BFLOAT16 conversion extension is supported or not.		RO	IM
		Value	Meaning		
		0	BFLOAT16 conversion extension is not supported.		
		1	BFLOAT16 conversion extension is supported.		

## AndeStar V5 BFLOAT16 Conversion Extension

### 4.1.2. Misc. Configuration 2 Register

Mnemonic Name: mmisc\_cfg2

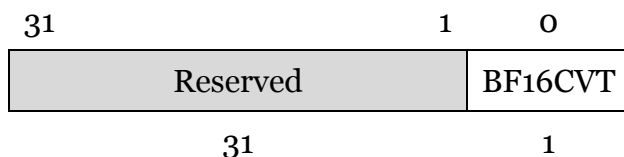
IM Requirement: mmisc\_cfg[31] == 1

Access Mode: Machine

CSR Address: 0xFC3 (non-standard read only)

XLEN: 64 and 32

RV32:



Field Name	Bits	Description	Type	Reset
BF16CVT	[o]	Indicates if BFLOAT16 conversion extension is supported or not.	RO	IM
		Value		
		0		
		1		
		Meaning		
		BFLOAT16 conversion extension is not supported.		
		BFLOAT16 conversion extension is supported.		