Jason (Wen-Jie) Li

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Summary

- ❖ 7+ years of working experience in digital IC design and team management.
- ❖ 4+ years of working experience in verification with UVM-SV/UVM-ML framework and FPGA prototyping.
- ❖ Build up the team from scratch and achieve success in silicon-proven IP and signoff.

Skills

Technology Computer Architecture, DLA, RISC-V, SoC, UVM, AMBA Protocol, IEEE 754-2019, FPU
Languages (Proficient): Verilog, C/C++, SystemVerilog (Familiar): Perl, Bash Shell, Tcl
Tools Xrun, Dc, IMC, Genus, Verdi, SimVision, HAL, SpyGalss, Superlint, Git, Jira

Work Experience

ANDES TECHNOLOGY CORPORATION **Hsinchu City, Taiwan**
Deputy Manager *2022/03 — Present*

- ❖ Project leader with 11 members in the RD-Computation Acceleration Division
  - Build up the ACCeleration (ACC) team in the RD-Computation Acceleration Division from scratch.
  - Success in silicon-proven IP, signing off with customers, and bringing the loyalty and license fee.
  - Collaborate with the hardware, algorithm, software, marketing, SA, QA, and architecture teams.
- ❖ Project: Andes Deep Learning Accelerator I400 (v1.0), I370 (v2.0/1.0), I350 (v2.0/1.1/1.0)
  - Responsible for architecture design and implementation for in-house DLA supporting SLM, LLM, ViT, CNN, RNN, and custom models with float16/int32/int16/int8 arithmetic computation.
    - ➙ Develop scalable AMBA3.0 AHB-Lite/AMBA4.0 AXI-based master DMA engine and slave port engine.
    - ➙ Develop scalable TileLink-based nested bus matrix connector and shared memory of multiple banks.
    - ➙ Develop scalable GEneral Matrix Multiplication (GEMM) from 0.125 up to 4TOPS.
    - ➙ Develop compatible Tensor Operator Set Architecture (TOSA) hardware for a more efficient ML framework.
    - ➙ Develop IEEE 754-2019-based Floating-Point Units (FPUs) with Multiply-Add-Fused (MAF) architecture.
    - ➙ Develop IEEE 754-2019-based Floating-Point Division and Square root Units (DSUs) with SRT radix-4.
    - ➙ Develop interrupt, polling, preemption, and abortion hardware control features.
    - ➙ Develop micro-command, program sequence, and scheduler for memory optimization.
    - ➙ Develop VerilogPerl language for module or top-level automatic integration and port scaling.
    - ➙ Provide AI subsystem with AndesCore and in-house platform.
  - Responsible for unit, integration, and system verification with UVM-SV/UVM-ML framework and FPGA prototyping.
    - ➙ Define verification criteria, including test plan and verification plan with dynamic and static reports.
    - ➙ Develop UVM block-level verification for DMA with AMBA4 AXI4.0 slave VIP and FPUs through UVMC/DPI-C.
    - ➙ Develop system-level verification and FPGA overnight test through C/Assembly with CMSIS-NN Library.
  - Responsible for architecture exploration and customer early evaluation.
    - ➙ Develop architecture-level performance/power/area profiler for in-house DLA estimation and correlation.

Digital IC Advanced Engineer *2019/09 -– 2022/03*

- ❖ Project: Andes Deep Learning Accelerator I320 (EA)
  - Responsible for architecture design and implementation for in-house DLA based on RISC-V coprocessor.
  - Collaborate with the compiler team to develop RISC-V ISA extensions for DLA.

Internship – VLSI *2018/07 -– 2019/09*

- ❖ Responsible for the DLA profiler under different configurations and NN models.

Education

NATIONAL TAIWAN UNIVERSITY OF SCIENCE AND TECHNOLOGY **Taipei City, Taiwan**
Master of Electronic and Computer Engineering Degree *2017/09 – 2019/09*
Advisor: Prof. Shanq-Jang Ruan
Cum. GPA: 4.04 / 4.30

TAMKANG UNIVERSITY **New Taipei City, Taiwan**
Bachelor of Electronic and Computer Engineering Degree *2013/09 – 2017/06*
Cum. GPA: 3.94 / 4.00

Publication

Li, Wen-Jie, Ruan, Shanq-Jang and Yang, Dong-Sheng, "Implementation of Energy-Efficient Fast Convolution Algorithm for Deep Convolutional Neural Networks based on FPGA," in *Electronics Letters, vol. 56, no. 10, pp. 485-488*, 2020/05/01.
https://doi.org/10.1049/el.2019.4188