

AndeShape™ ATCBUSDEC200 Design Specification

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**CONFIDENTIAL**

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**Typographical Convention Index**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Document Element | Font | Font Style | Size | Color |
| Normal | Georgia | Normal | 12 | Black |
| Code | Lucida Console | Normal | 11 | Indigo |
| USER VARIABLE | Lucida Console | ALL-CAPS | 11 | INDIGO |
| Note/Warning | Georgia | Normal | 12 | Red |
| Hyperlink | Georgia | Bold + Underlined | 12 | Blue |

# Overview

## Introduction

The ATCBUSDEC200 is designed as the AHB-Lite decoder. The AHB-Lite decoder receives AHB transactions from an upstream port and determines the downstream port(s) to send the received transactions based on the base/size information of AHB slaves.

## Features

List the features of the design:

* One internal slave to provide the base/size information of the downstream AHB slaves
* Up to 31 AHB-Lite slave ports
* Configurable base/size of each AHB slaves

## Block Diagram

ATCBUSDEC200 consists four major functional blocks: interconnect logic, and internal slave.



Figure 1. ATCBUSDEC200 Block Diagram

## Function Description

### Interconnect Logic

The interconnect logic include an address decoder and downstream-to-upstream multiplexor. The address decoder bases on the slave address base and size configuration to dispatch the upstream transaction to the appropriate slave ports. The downstream-to-upstream multiplexor dispatches the returned data of corresponsive slave to the upstream port.

### Internal Slave

The internal slave provides the base/size information of each AHB-Lite slave for software to get the configuration of each AHB-Lite slave. This internal slave is read only.

## Timing Diagram

### Write Transactions

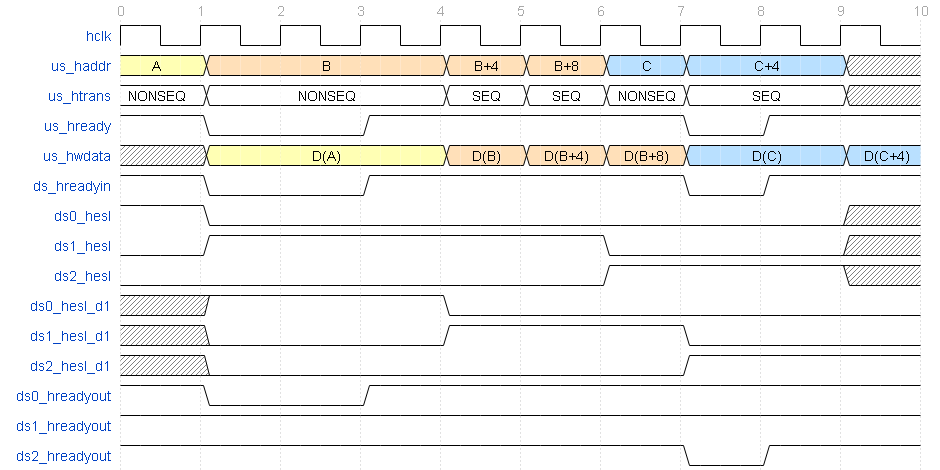


Figure 2. Write Transactions

### Read Transactions

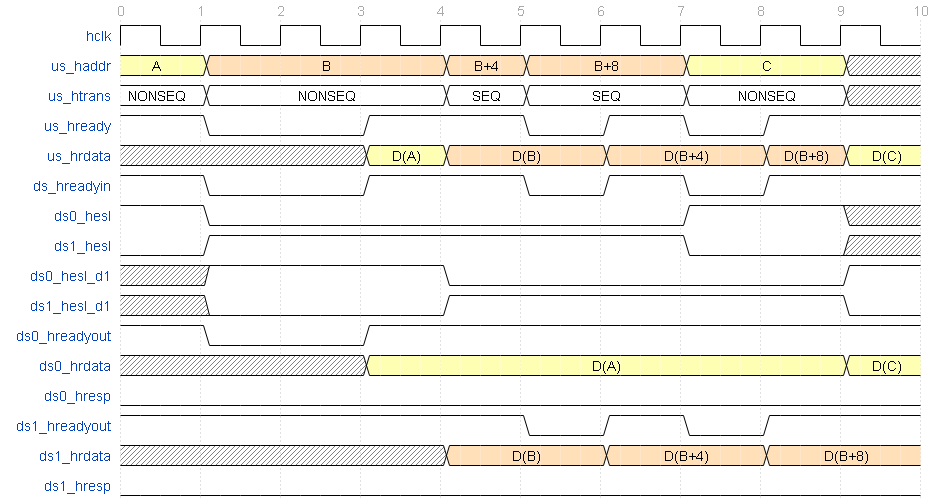


Figure 3. Read Transactions

### Write Transactions with Nonexistent Address

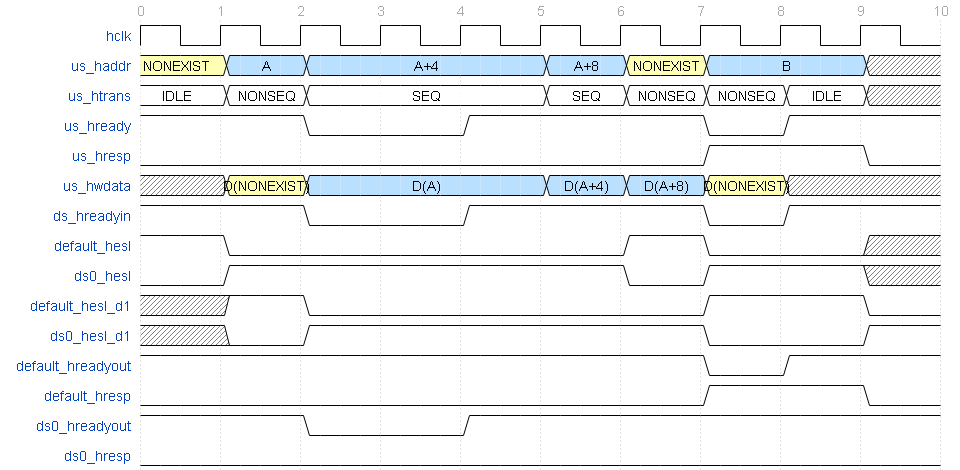


Figure 4. Write Transactions with Nonexistent Address

### Read Transactions with Nonexistent Address

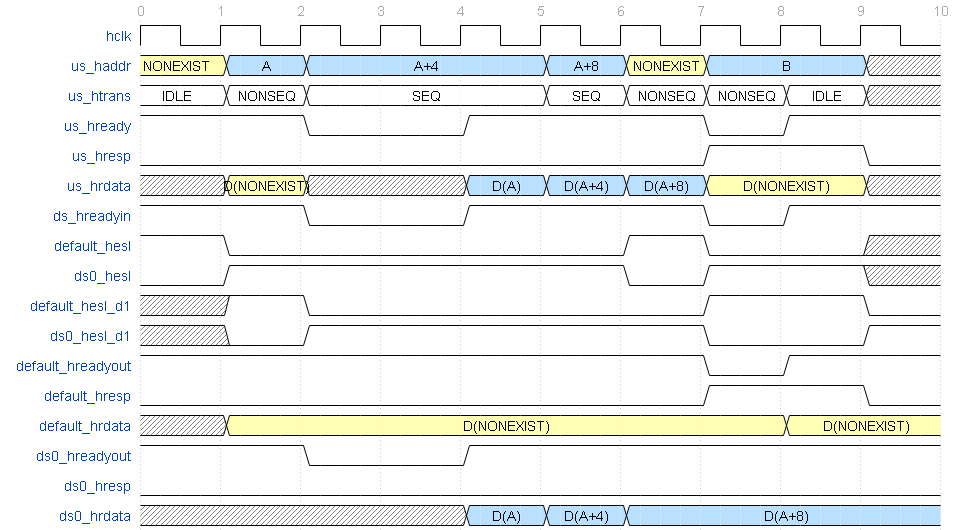
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Figure 5. Read Transactions with Nonexistent Address

## Latency

Both read and write latency is one clock cycle.

# Signal Description

Figure 6 shows the signal overview and Table 1 gives the detailed descriptions of I/O signals.



Figure 6. ATCBUSDEC200 Input/Output Ports

Table 1. ATCBUSDEC200 Signal Description

| **Signal Name** | **I/O Type** | **Description** |
| --- | --- | --- |
| **AHB-Lite Global Signals** | | |
| hclk | I | AHB-Lite bus clock |
| hresetn | I | AHB-Lite bus reset |
| **AHB-Lite Interface** | | |
| us\_haddr[ADDR\_MSB:0] | I | AHB-Lite bus address |
| us\_htrans | I | AHB-Lite transfer types |
| ds*n*\_hsel | O | This signal indicates that the current transfer is intended for the selected slave n |
| ds\_hready | O | AHB-Lite input ready for each slave. This signal and us\_hready are the same |
| ds*n*\_hrdata[DATA\_MSB:0] | I | The read data bus transfers data from the selected slave n |
| ds*n*\_hreadyout | I | This signal indicates that a transfer from the selected slave n has finished on the bus |
| ds*n*\_hresp | I | This signal indicates that the transfer status from the selected slave n |
| us\_hrdata[DATA\_MSB:0] | O | AHB-Lite read data is returned to the upstream |
| us\_hreadyout | O | AHB-Lite ready is returned to the upstream. This signal and ds\_hready are the same. |
| us\_hresp | O | AHB-Lite transfer status is returned to the upstream |

# Micro-Architecture

## ATCBUSDEC200 Block Diagram

Figure 7 shows the data path of ATCBUSDEC200.



Figure 7. ATCBUSDEC200 Block Diagram

## Default Slave

The default slave is designed to provide a response when any of the nonexistent address locations are accessed.

`ifdef ATCBUSDEC200\_OOR\_ERR\_EN

always @( posedge hclk or negedge hresetn) begin

if (~hresetn) begin

default\_hreadyout <= 1’b1;

default\_hresp <= 1’b0;

end

else if (us\_htrans[1] && default\_hsel && us\_hready) begin

default\_hreadyout <= 1’b0;

default\_hresp <= 1’b1;

end

else if (us\_hresp && ~us\_hready && default\_hsel\_d1) begin

default\_hreadyout <= 1’b1;

default\_hresp <= 1’b1;

end

else begin

default\_hreadyout <= 1’b1;

default\_hresp <= 1’b0;

end

end

`endif















# Design Configuration

## Hardware Configuration

* AHB-Lite Slave Ports

Define ATCBUSDEC200\_SLVn\_SUPPORT to enable AHB-Lite ports, where n = 1~31. For example,

`define ATCBUSDEC200\_SLV1\_SUPPORT

`define ATCBUSDEC200\_SLV15\_SUPPORT

`define ATCBUSDEC200\_SLV31\_SUPPORT

* AHB-Lite Bus Address Width

Define ATCBUSDEC200\_ADDR\_WIDTH\_24 to set the address width to 24-bit. Default address width is 32-bit.

`define ATCBUSDEC200\_ADDR\_WIDTH\_24

* AHB-Lite Bus Data Width

Define ATCBUSDEC200\_DATA\_WIDTH\_64 and ATCBUSDEC200\_DATA\_WIDTH\_128 to set the data width to 64-bit and 128-bit, respectively. Default data width is 32-bit. For example, 128-bit data width

`define ATCBUSDEC200\_DATA\_WIDTH\_64

`define ATCBUSDEC200\_DATA\_WIDTH\_128

* AHB-Lite Space Width

Define ATCBUSDEC200\_ADDR\_DECODE\_WIDTH to identify the partial address bits for AHB-Lite address decoding. For the 24-bit mode, this macro could be 11–24; for the 32-bit mode, this macro could be 21–32. For example, 4MB decoding space

`define ATCBUSDEC200\_ADDR\_DECODE\_WIDTH 22

* AHB-Lite Slave Size

Define ATCBUSDEC200\_SLVn\_SIZE (n=1~31) to identify the space size of an AHB-Lite slave based on Table 4 and Table 5 for 24-bit mode and 32-bit mode, respectively. For example, specify the space size of AHB-Lite slave #3 to be 8MB in 32-bit mode:

`define ATCBUSDEC200\_SLV3\_SIZE 4

* AHB-Lite Slave Address Offset

Define ATCBUSDEC200\_SLVn\_OFFSET (n=1~31) to identify the address offset of an AHB-Lite slave which must align on the AHB-Lite slave size. SLV0 is for the ATCBUSDEC200 internal slave. For example, suppose the size of the entire AHB-Lite bus address space is 2GB and the size of the AHB-Lite slave #3 is 8MB, specify the address offset of the AHB-Lite slave #3 to be 0x10800000:

`define ATCBUSDEC200\_ADDR\_DECODE\_WIDTH 31

`define ATCBUSDEC200\_SLV3\_SIZE 4

`define ATCBUSDEC200\_SLV3\_OFFSET `ATCBUSDEC200\_ADDR\_DECODE\_WIDTH’h10800000

* AHB-Lite Default Slave Error Response

Define ATCBUSDEC200\_OOR\_ERR\_EN to identify that the default slave returns two-cycle ERROR response to upstream when decoding nonexistent address which is a NONSEQUENTIAL or SEQUENTIAL transfer. If this macro is not defined, it always returns OK response.

`define ATCBUSDEC200\_OOR\_ERR\_EN

## Local Parameters

* ATCBUSDEC200 ID Number

PRODUCT\_ID = 24’h000320

* ATCBUSDEC200 Reversion Major

REV\_MAJOR = 4’h0

* ATCBUSDEC200 Reversion Minor

REV\_MINOR = 4’h0

# Programming Model

## Summary of Registers

### Internal Slave

Internal slave provide the ID number of ATCBUSDEC200, reversion number and the information of base/size for each slave. The following table shows that the information corresponds to address. All of these fields are read only.

RO: Read Only

Table 2. ATCBUSDEC200 Internal Slave Summary

|  |  |  |
| --- | --- | --- |
| Address | Type | Description |
| +0x00 | RO | ATCBUSDEC200 ID and reversion number |
| +0x04~0x1C | - | Reserved |
| +0x20~0x98 | RO | Offset/size of slave 1~31 |

## Register Description

### ATCBUSDEC200 ID Number and Reversion Number (0x00)

Table 3. ATCBUSDEC200 ID Number and Reversion Number

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Bit | Type | Description | Reset |
| Reserved | HDATA\_MSB:32 | - | - | - |
| ID | 31:8 | RO | ATCBUSDEC200 ID number | PRODUCT\_ID |
| RevMajor | 7:4 | RO | Major revision number | REV\_MAJOR |
| RevMinor | 3:0 | RO | Minor revision number | REV\_MINOR |

### Offset/Size of Slave 1~31 (0x20 + (n-1) \* 0x4)

Table 4. Offset/Size of Slave 1~31 in 24-bit mode

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Bit | Type | Description | Reset |
| Reserved | 31:M | - | M= ATCBUSDEC200\_ADDR\_DECODE\_WIDTH | - |
| Offset | M-1:10 | RO | AHB-Lite slave address offset | Hardware Configurable |
| Reserved | 9:4 | - | - | - |
| Size | 3:0 | RO | Size of the slave address space:  0x0: Invalid slave  0x1: 1K  0x2: 2K  0x3: 4K  0x4: 8K  0x5: 16K  0x6: 32K  0x7: 64K  0x8: 128K  0x9: 256K  0xA: 512K  0xB: 1M  0xC: 2M  0xD: 4M  0xE: 8M  0xF: Reserved | Hardware Configurable |

Table 5. Offset/Size of Slave 1~31 in 32-bit mode

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Bit | Type | Description | Reset |
| Reserved | 31:M | - | M= ATCBUSDEC200\_ADDR\_DECODE\_WIDTH | - |
| Offset | M-1:20 | RO | AHB-Lite slave address offset | Hardware Configurable |
| Reserved | 19:4 | - | - | - |
| Size | 3:0 | RO | Size of the slave address space:  0x0: Invalid slave  0x1: 1M  0x2: 2M  0x3: 4M  0x4: 8M  0x5: 16M  0x6: 32M  0x7: 64M  0x8: 128M  0x9: 256M  0xA: 512M  0xB: 1G  0xC: 2G  0xD~0xF: Reserved | Hardware Configurable |

## Programming Sequence

N/A