Horizontal Counter

On Pang (HSEL = 0) $\overline{HRST}$ goes active on HCNT 511 and resets to value HCNT 0.
The number of horizontal pixels in a line is 511−0+1 = 512.
Else when HSEL = 1, $\overline{HRST}$ goes active on HCNT 448 and resets to value HCNT 64.
The number of horizontal pixels in a line is 448−64+1 = 385

H[8..0]

Active between HCNT 384 to 511

Vertical Counter

V[8..0]

On Pang (VSEL = 1) $\overline{VRST}$ goes active on VCNT 391 and resets to value VCNT 120 (-391).
The number of vertical lines in a frame is 391−120+1 = 272

Else if VSEL = 0, $\overline{VRST}$ goes active on VCNT 385 and resets to value 126. The number of vertical lines in a frame is 385−126+1 = 260.

Active between 112−127 or 368−383

High 128 to 135

Vertical Counter Reset

385

391

Horizontal Counter Reset

Acive for one HCLK period after HCNT 447 or 511.

CLK Divided

$\overline{HRST2}$ is synchronised to CLK.
Stays active for one CLK period.

Horizontal Blanking

$\overline{HSEL}$ = 0
$\overline{HBLK}$ active when HCNT is 456−71 (rolls over at 511).
for 511−456+1+71−0+1 = 128 pixels.

H: 384−511

$\overline{HSEL}$ = 1
$\overline{HBLK}$ active when HCNT is 392−134. HCNT resets at 448 to 64. Total blanked pixels is 134−64+1+448−392+1 = 128 pixels.

H: 0−127

L: 392−134

Vertical Blanking

$\overline{VSEL}$ = 0
$\overline{VBLK}$ active when VCNT is 126−143 or 368−385
Total blanked lines 36.

$\overline{VSEL}$ = 1
$\overline{VBLK}$ active when VCNT is 120−135 or 376−391
Total blanked lines 32.

VSEL = 1 normal for Pang

Composite Sync

Low between 480 to 511

$\overline{HSEL}$ = 0
HSYNC high when HCNT is 480−511

$\overline{HSEL}$ = 1
HSYNC high when HCNT is 432−464

$\overline{VSEL}$ = 0
VSYNC high when VCNT 120−127 or 384−391

$\overline{VSEL}$ = 1
VSYNC high when vertical counter is 388−391

HCLK divided

Div by 4

Div by 8

$\overline{HLD}$ active at HCNT 497

CNTEN Connected to VCC on pang

XOR

Clk edge Detector

Fixed at GND in Pang

The Schematics have been analyzed from a die picture by InfoSecDJ.
The chip is identified as:

NEC
65006−103

It is a uPD65000 (CMOS−2) series, 3−micron gate array.
− 528 Basic Cells
− 12 Columns, 44 Rows

Timing

File: timing.kicad_sch

Ulf Skutnabba, twitter: @skutis77

Sheet: /
File: dl−010d−103.kicad_sch

Title: Capcom DL−010D−103

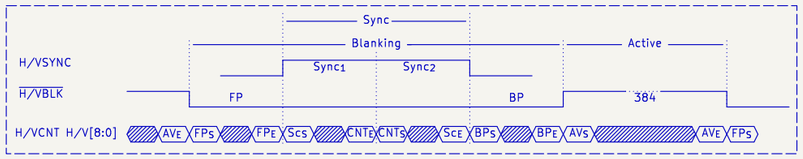
Size: A3	Date: 2025−09−18	Rev:
KiCad E.D.A. 8.0.9		Id: 1/2

HSEL	1	0
FP_S,$\overline{HBLK}_S$	392	456
FP_E	431	479
Sc_S	432	480
CNT_E	447	511
CNT_S	64	0
Sc_E	79	31
BP_S	80	32
BP_E,$\overline{HBLK}_E$	135	71
AV_S	136	72
AV_E	391	455
Total pixels	384	512
Active pixels	256	384
Blank pixels	128	128
Front Porch	40	24
$Sync_1$	16	32
$Sync_2$	16	32
Sync	32	64
Back Porch	56	40

Horizontal/Vertical Counter Abbreviations

AV_S, AV_E: Active Video Start/End
FP_S, FP_E: Front Porch Start/End
BP_S, BP_E: Back Porch Start/End
CNT_S, CNT_E: Horizontal/Vertical Counter Start/Stop
Sc_S, Sc_E: Horizontal/Vertical Sync Start/Stop

Active: Active video signal, AV = AV_E−AV_S+1
Blanking: Blank video signal
Sync: Synchronizing video signal
FP: Front Porch, FP = FP_E−FP_S+1
BP: Back Porch
Sync = $Sync_1$ + $Sync_2$



VSEL	0	1
FP_S,$\overline{VBLK}_S$	382	376
FP_E	383	387
Sc_S	384	388
CNT_E	385	391
CNT_S	126	120
Sc_E	127	123
BP_S	128	124
BP_E,$\overline{VBLK}_E$	143	135
AV_S	144	136
AV_E	381	375
Total lines	260	272
Active lines	238	240
Blank lines	36	32
Front Porch	2	12
$Sync_1$	2	4
$Sync_2$	2	4
Sync	4	8
Back Porch	16	12

HSEL = 0, VSEL = 1 is used on all games on the Capcom/Mitchell platform.

Total pixels: 512
Active pixels: 384
Blanked pixels: 128
Pixel clock: 8Mhz
Hsync frequency: 15.625kHz
Vertical lines: 272
Blanked lines: 32
Vsync frequency: 57.44485Hz

Sheet: /Timing/
File: timing.kicad_sch

Title:

Size: A3	Date: 2025-09-18	**Rev:**
KiCad E.D.A. 8.0.9		Id: 2/2