Analog and Mixed-signal Circuit Design and Techniques for Bioelectrical Signals

by

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ABSTRACT

The study of cellular functionality and response has been used for decades to better understand the workings of the body. Electrodes connected through biocompatible interfaces to analog or digital circuits permit researchers to gain better insight into the functionality and interconnectivity of cellular networks. With the fast development of very-large-scale integration circuit fabrication and design techniques, the measurement of electrical properties, such as capacitance and impedance of biological materials, can improve sensitivities, accuracy, and dynamic range through more diverse sensing techniques. Capacitance sensing can be used in various types of sensing and measurement applications.

Most biomolecules have high affinity to attach to a surface coated by specific receptor molecules. If the type of molecule coated on a surface as a receptor is known and there is binding observed, then the molecules that bound to the surface can be determined. This results in a surface capacitance change that can be measured. Molecules, cells, and proteins have different impacts on the change in capacitance. In addition, different cell types may also provide different capacitances. Since the cells usually change slowly, the induced capacitance changes are also slow. Thus, the detected signal from the capacitance sensing setup is typically a small signal at very low frequencies.

In this dissertation, a switched-capacitor based capacitance sensor design chip including a temperature sensing circuit, a bandgap reference and various testing structures is presented. Circuit analysis, simulation verification, implementation and testing plans are presented. In addition, a three stage amplification circuit for

HL-1 cardiac cells action potential measurement has been implemented and tested. A phase detector circuit for cardiac array measurement has been designed and simulation verified. A sigma-delta analog-to-digital-converter and a sigma-delta digital-to-analog-converter have been simulation verified.

Acknowledgement

I would like to express my sincere gratitude to my dissertation supervisor, Dr. Jennifer Blain Christen, for her advice, her friendship, and her insight, throughout the entire duration of my research on this dissertation. I thank her for providing me this invaluable opportunity to work on an interesting and challenging project.

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CHAPTER 1

INTRODUCTION

1.1. Motivation

The study of cellular functionality and response has been used for decades to better understand the workings of the body. Biological signals can be directly measured using microelectrodes. Metal electrodes have been used successfully for measurements in biological environments for decades [4]. Advances in microfabrication in the 1980s allowed for the development of microelectrode sensing arrays that are similar in size to cells. Current techniques allow for the examination of a single cell or a population of cells through the use of microelectrode arrays as passive elements of sensing systems [5]. Electrodes connected through biocompatible interfaces to analog or digital circuits permit researchers to gain better insight into the functionality and interconnectivity of cellular networks [6]. With the fast development of VLSI circuit fabrication and design techniques, the measurement of electrical properties, such as capacitance and impedance of biological materials, can improve sensitivities, accuracy, and dynamic range through more diverse sensing techniques. Capacitance sensing can be used in various types of sensing and measurement applications. For example, capacitance change occurs when chemical or voltage change causes charges to move in and out of the cell membranes through ion channels [7]. For healthy cells, when there is no triggering, the charges are constrained inside membranes; the measured capacitance at the surface of the membrane is nearly constant. When cells are compromised, charge leakage from ion channels and the movement of charge will result in changes to

membrane capacitance change. This leakage indicates that the cells are not in their normal healthy condition. Most biomolecules have high affinity to attach to a surface coated by specific receptor molecules, such as streptavidin-biotin binding, which was first utilized in histo-chemical research in the mid-1970s [8] [9]. If the type of molecule coated on a surface as a receptor is known and there is binding observed, then the molecules that bound to the surface can be determined. This results in a surface capacitance change that can be measured. Molecules, cells, and proteins have different impacts on the change in capacitance. For example, the base capacitance of the receptor molecules and the surface that cells can attach to, would be on the order of pF or more, while the change of capacitance due to the binding of the cells is usually much smaller, typically in a range from several fF to several pF. In addition, different cells may also provide different capacitance change. Since the cells usually change slowly, the induced capacitance changes are also slow. Thus, the detected signal from the capacitance sensing setup is typically a small signal at very low frequencies.

1.2. Overview

A good capacitance sensor for biomedical applications should provide two key features. One is to have a large dynamic range for capacitance sensing. It has been observed that some type of cells may only change the capacitance by a very small amount, for example, on the order of fF change, while other types of cells may cause large capacitance changes, for example, on the order of pF. In order

to measure both small and large capacitance changes with one device, we need to make sure that our sensing circuit has enough dynamic range to cover all types of cells. One way to achieve this high dynamic range is to use a programmable gain in the capacitance sensing circuit, such that at the high-gain setting, we can convert a capacitance change of 0 to 10 fF to a voltage output from 0 V to 3 V. On the other hand, when the capacitance changes are large, we can use the low-gain setting to convert the capacitance change of 0 to 5 pF to the same range of voltage outputs from 0 V to 3 V. The second key feature that a capacitance sensor should have is the ability to continuously record data. This means the sensing circuit needs to have a mechanism to reset itself automatically to start from its initial state to record new data. In biomedical applications, researchers are more interested in the capacitance change over time, which requires the sensor to be able to reset itself and record the data at a frequency that can be controlled. This aspect is particularly important when the capacitance changes induced by activities of cells or other reactions are being studied, as people will be more interested in the capacitance changes over a long period of time. Temperature is also a very important parameter for biomedical experiments. For example, live cells are very sensitive to temperature change. Thus our sensor should monitor the temperature in order to correlate temperature with our measurements and data recording. Capacitance is one parameter we can use to evaluate the health of cells as long as an appropriate, constant temperature is maintained. Therefore, if the sensor can

record capacitance and temperature change over time, it will provide more useful information about cells' activities. In addition to the capacitance and temperature sensing, some cells such as cardiac cells exhibit electrical activity; they beat in solution generating electrical signals. We are interested in constructing a measurement setup that can be implemented either on printed-circuit-boards (PCB) or VLSI circuits (i.e. Lab-on-a-Chip) to measure the signal generated by cardiac cells. Based on the fact that signals from cells are usually very small with low signal-to-noise-ratio (SNR), our sensing and recording system needs to be able to amplify the useful signal and filter out the noise in the data collection. In the VLSI circuit approach, we want to integrate all functions on a small IC chip, which is a few square centimeters; analog-to-digital converter and digital-to-analog converter should be included to facilitate interface with a computer. Eventually, wireless communication will be used to transmit the digital signals out, which will allow end users to observe and record the signals from a computer screen. The advantage of a wireless connection to the chip is in the ease of the measurement.

1.3. General Approach

In order to implement the capacitance sensor, we have simulated, designed and taped out two IC chips, each with a different design. They were fully simulated using the Cadence IC 6 design tool, and the chips were taped-out in December 2008 under a process provided by Lincoln Lab, MIT. MIT fabricate a single wafer by bonding 3 stacked wafers from the IBM silicon over insulator 0.15 m process.

The most important function of the two chips is the capacitance sensing capability. This VLSI sensing circuit design has two key features. One is the programmable gain control for capacitance sensing, which sets the output signal range by programming two external input clocks. Theoretically, the design can be used to measure a large range of capacitance changes from as low as a few fF to as high as a few pF. The second key feature is the ability to record data utilizing a switched-capacitor circuit to enable discrete-time recording over long time periods; the sampling frequency can also be programmed by the same two clock inputs. An on-chip bandgap voltage reference circuit was implemented on this VLSI capacitance sensing IC to provide high quality signal reference nearly independent of the supply voltage and temperature variations. This kind of reference will help to increase the accuracy of the capacitance sensing circuit. A proportional-to-absolute-temperature (PTAT) circuit was also implemented on the same IC that can be used for temperature sensing and recording. Both the bandgap reference and the PTAT circuits have been fully simulated using pre-layout netlists, demonstrating the IC's ability to offer stable voltage reference and accurate temperature measurement in a range from -4 to 120 degrees Celsius. We were unable to simulate the post-layout netlists due to the lack of bipolar junction transistor (BJT) and resistor models in this process. This temperature sensor can work simultaneously with the capacitance sensor. Since SOI 3D technology is relatively new, some of the design models are still under development as mentioned above. Thus, test

structures of sub-circuit blocks included: BJTs, sub-blocks of bandgap reference and PTAT circuit; a constant Gm biasing circuit, a sub-block of a two stage operational amplifier; an externally biased two stages operational amplifier, a test circuit to bypass the constant Gm circuit; and transistor pairs connected in several current mirror configurations. Chapter 7 includes detailed test procedures, bond pads connection diagrams, and expected values for the anticipated testing results. Thanks to the work of David Welch, Steve Herman, and Sahana Sen, the two chips also included specially designed capacitor structures for capacitance sensing as well as resistors to heat the chip in a feedback configuration with the on-chip PTAT circuit. A printed circuit board (PCB) circuit has been designed, implemented, and tested that measures cardiac action potentials. The circuit, which uses discrete components from Texas Instruments and Linear Tech, includes the signal filtering and gain control. The filters and amplifiers on the PCBs have been tested and verified with a function generator and an oscilloscope. A phase detector circuit, a 2^{nd} order sigma delta ADC, and a 1st order sigma delta DAC have been designed. Matlab Simulink was used to simulate the 2_{nd} order sigma delta ADC. All three designs have been fully simulated and verified with the Cadence IC 5 design tool. Each of the designs will be fabricated in the 0.5μm ON Semiconductor process in early 2010.

CHAPTER 2

CAPACITANCE SENSOR

2.1. Switched-Capacitor Circuit Techniques

2.1.1. Introduction

Filters at low frequencies, e.g. for speech (audio band) or biomedical signals from cells or molecules, require large time constants. Large time constants require large capacitors and resistors that are difficult to integrate. Switched capacitors behave like resistors with large values. As a result, they allow integration of low-frequency filters without external components. This makes the design of on-chip discrete time sigma delta ADCs possible for very low frequency applications. The switched capacitor (SC) circuit has created a revolution in the realization of integrated low-pass filters for low-frequency applications. VLSI SC circuits, based on the discrete-time (DT) signal processing, were first developed to design accurate, economical analog signal processing circuits at voice-band frequencies in a fully integrated form. SC circuits provide an easy way to implement low-power, compact designs fully compatible with VLSI digital circuits. SC circuits implement large resistors accurately using a control clock signal to keep charging and discharging capacitors across their two terminals. In implementing SC circuits, RC constants can be controlled by the clock frequency and the ratio of capacitor values. Thus, SC circuits are suitable for VLSI circuit realization of high-value on-chip resistance. Another implementation of SC circuits allows them to be used to measure capacitance using discrete time techniques to record data over a long period of time. When SC circuits are implemented in this manner with user-controlled clock fre-

quencies, extremely large dynamic range circuits can be achieved. This is the technique being used in our capacitance sensor design. Our SC circuit works by charging and discharging both a sensing and reference capacitor during two non-overlapped clock phases. The periods of changing and discharging are controlled with clock signals. These cycles are repeated many times to increase the resolution of the measurements. These key ideas for the working mechanism of this capacitance sensor will be explained in details.

2.1.2. SC Circuits to Realize Large Resistances On-Chip

As previously stated, SC circuits provide a way to replace large resistors on-chip. The principle is to control the frequency of charging and discharging a capacitor to achieve an equivalent resistance value. Traditional resistors follow Ohms law, and the relationship between resistance, voltage and current can be described as $R = \frac{V_a - V_b}{I}$.

The same resistance can be achieved with a SC implementation as shown in Figure 2.1. In Figure 2.1, first we assume that switches S2, S3 are closed and switches S1, S4 are open in phase 1; in phase 2, switches S1, S4 are closed and switches S2, S3 are open. During phase 1, both sides of C are connected to ground, C discharges to ground. During phase 2, C is being charged by the different potentials at each sides. When C completes charging to a steady state, the charge on C is $Q = C(Va - Vb)$. As phase 1 and phase 2 repeat, $i_{average} = \frac{q}{T} = \frac{C}{T}(Va - Vb)$. Thus we have achieved a circuit where the capacitor and switches

have an equivalent resistance of $R_{eff} = \frac{T}{C}$ where T is the period of the clock cycle, and C is the capacitance of the capacitor.

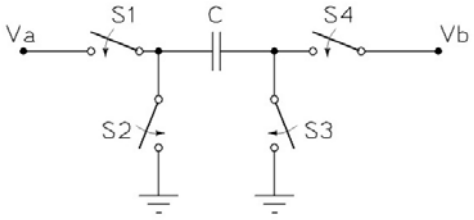

Figure 2.1. Basic Switched-Capacitor Circuit Structure

The advantage of the SC implementation is that it can achieve a large, accurate time constant $R_{eq}C_1 = T\frac{C_1}{C_2}$. The ratio of $\frac{C_1}{C_2}$ can be controlled to $\pm$0.1 % with good matching layout.

2.1.3. Non-ideal Effects of Switched-cap Circuit

Switches controlled by digital signals to act as on-state and off-state devices can be implemented with NMOS or PMOS transistors. The non-zero on-resistance of the switches will introduce noise. The desired properties of the VLSI SC circuits are: high off-resistance, low on-resistance, low switching delay between phases, minimized charge redistribution during clock transitions, and low voltage offset. The basic SC switch in CMOS is usually a single, small size NMOS (or PMOS) transistor. The non-zero on-resistance causes an effective error in the capacitance ratio. It is desirable to reduce error to less than the tolerance on capacitor matching (0.1, where T is the clock period, and C is the capacitance of the switch. Switching charge injection (also referred to clock feed through) also causes noise in SC

circuits. When the switches are turned on, charges are present under the gate to create a channel for current to flow according to the standard transistor behavior. When the switches are turned off, the charges have to go somewhere. Some of the charges end up on the input gate of a opamp circuit or another sampling or feedback capacitors, depending on the position of the switches in the SC circuit. $\Delta V = \frac{\Delta q}{C}$, where q is the charge under the gate of the switch during its on-state, and C is the capacitance of an opamp's input gate or another capacitor in the circuit. Using small switch and larger capacitor will help with charge injection, but if the switch is too small and the capacitor is too large, the required charge transfer may not have time to complete. In addition, driving large capacitors consumes more power.

2.1.4. Non-Overlapped Clock Generation Circuit

The design of our SC circuit based capacitance sensors requires an on-chip four-phase clock generation. The four-phase clock signals determine the periods of charging and discharging of a single capacitor, the cycles for the integration of charges on the feedback capacitors, and the time to reset the feedback capacitor to ground. The reset feature enables the sensor to sense and record capacitance change over time at a tunable frequency. A commonly used 2-phase non-overlapped clock generation circuit structure is shown in Figure 2.2. The actual four-phase clock generation circuit I designed is more complex, but the basic concept is the same as Figure 2.2. The non-overlapped regions of the 2-phase clock

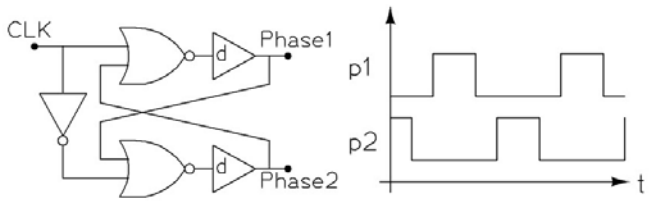

Figure 2.2. VLSI 2-phase non-overlap clock generation circuit and its waveform

are determined by the delay time elements which are the buffers. The easiest way to increase the delay time is to add more inverters in the buffer configuration as delay elements. SC circuits require phase 1 and phase 2 do not overlap to ensure functionality.

2.1.5. VLSI Sample/Hold Structures

Sample and hold (S/H) circuits are essential parts of SC circuit based sensors. Sensors only read the value from a feedback capacitor during a sampling period determined by their clock signals; during the hold period, the value should not change while the charge is being integrated on the feedback capacitor for the next sample. S/H provides this function by reading the value at a given time and storing the value before it reads new one. This idea is very important for discreet time system, as discrete systems only defined values at certain time intervals. Continuous time systems, however, have defined values at all times. One S/H circuit is shown in Figure 2.3. S/H circuits are typically used to avoid frequency response distortion caused by continuous time signal feed through effects. In S/H circuits, the output signal tracks the input signal during the sample phase, and the output holds the

previous sampled input signal value during the hold phase until the next sample phase.

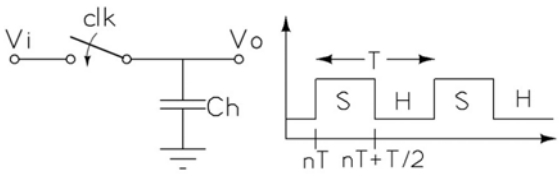

Figure 2.3. Basic sample/hold circuit [Reference, change t/2 to T]

2.2. Capacitance sensing principle

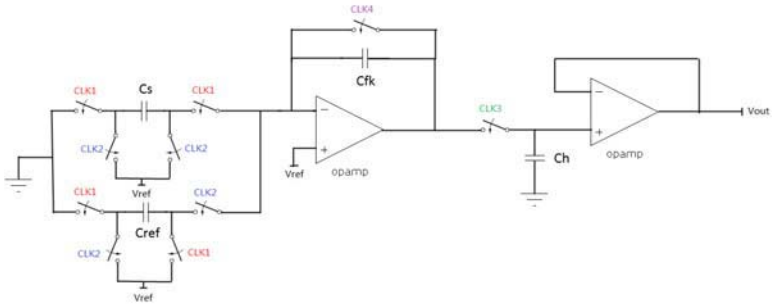

Figure 2.4. Capacitance sensor circuit diagram

We have designed a capacitance sensor circuit using each of the elements described in the sections above. The simplest explanation of our capacitance sensor is that we use the same reference voltage V_{ref} to charge both the sensing capacitor C_S and the reference capacitor C_{ref} which are designed and laid out with identical initial capacitance values C_S=C_{ref}. Capacitance change happens on the sensing capacitor. Then all the charges on the sensing capacitor are used to charge another feedback capacitor C_{fk}, and the reference capacitor C_{ref} is used to discharge the same feedback capacitor C_{fk}. If there is a capacitance difference between the

C_S and the C_{ref}, there will be some charges ΔQ left on the feedback capacitor C_{fk} after one cycle of charging and discharging, $\Delta Q = V_{ref}(C_S - C_{ref})$. We will assume the capacitance change on C_S is positive. If the charging and discharging repeat N times, the resolution of our sensor is increased N times since the total charge integrated on the feedback capacitor is $\Delta Q = N \cdot V_{ref}(C_S - C_{ref})$. For different applications, capacitance change may vary and the number of cycles N can be user-controlled with external clock signals (CLK3 and CLK4) . The dynamic range of the sensor can be optimized by choosing the right external clock signals. The relationship between the voltage output and the capacitance change ΔC on C_S can be described as $V_{out} = N \cdot \frac{V_{ref}(C_S - C_{ref})}{C_{fk}}$, V_{ref} can be provided by external voltage reference or on-chip bandgap reference voltage. This equation assumes that all components are ideal, which means that the non-zero resistance of switches, the potential offset at the S/H circuit, layout mismatch, parasitic capacitance and all other noise are not considered.

2.3. Capacitance Sensor Performance Simulation

In order to have more realistic idea of actual performance, the capacitance sensor was designed and fully simulated with transistor level components. Switches were implemented with PMOS or NMOS transistors with minimum width and length under 0.15 μm technology. The opamp used was a two stage opamp with on-chip constant Gm biasing circuit; a startup circuit was included to guarantee the working state of the current biasing circuit. The detailed circuit diagram of the opamp and

biasing circuit is included in Section 3.4. The four phase clock generation circuit will be explained on Section 2.4. The simulation environment tool used was Cadence IC 6 analog environment simulator; simulation models are from MIT/Lincoln Labs 3D SOI 0.15 μm technology, model version 3DIC 3.3.5.

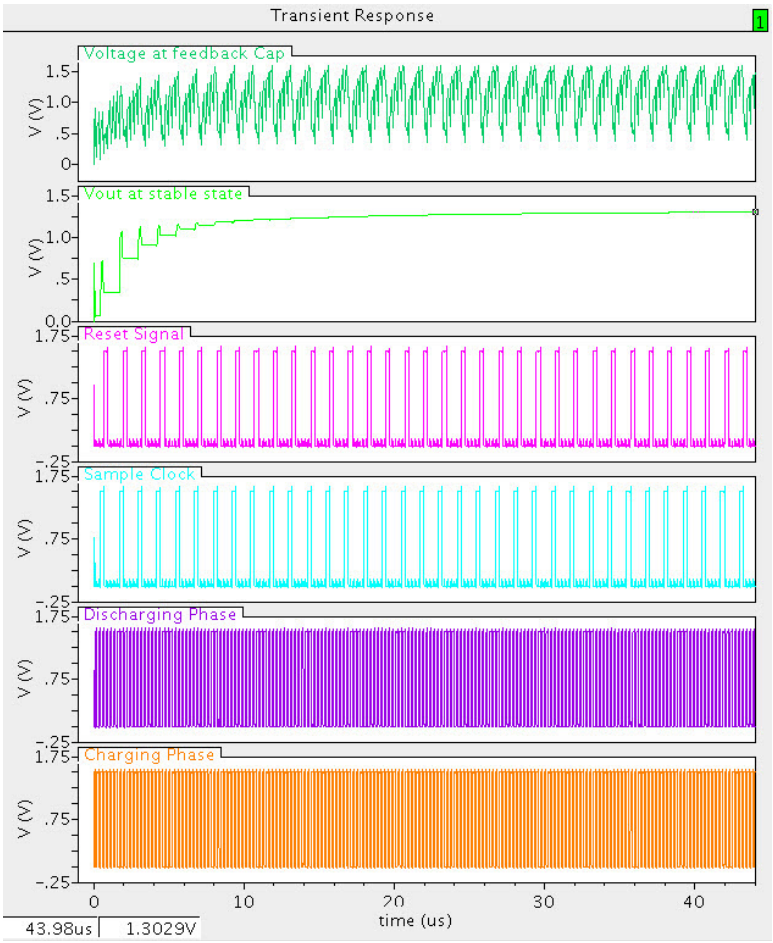

Figure 2.5. Transient Responses over more than 40 microseconds of voltage at C_{fk}, voltage at C_{out} and four clock signals (CLK4: Reset Signal, CLK3: Sample Clock, CLK2: discharging C_{fk} phase, and CLK1: charging C_{fk} phase), respectively from top to bottom.

Figure 2.5 shows that Vout (output voltage at steady state) took slightly over 10 s for the output node stabilize. From Figure 2.6, in the ”voltage at feedback cap”

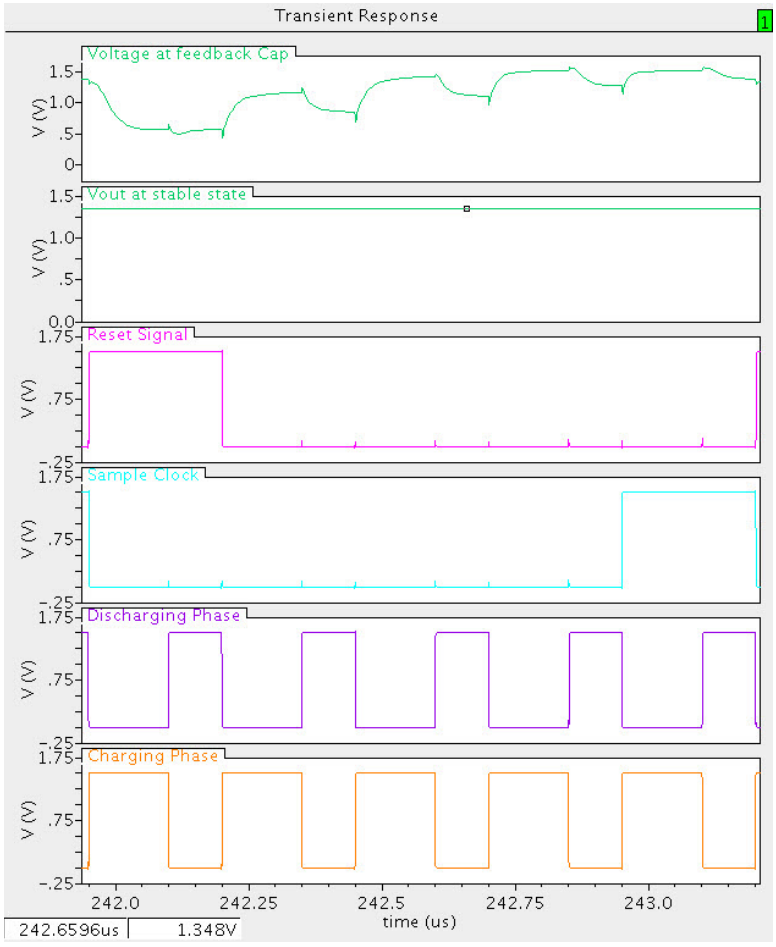

Figure 2.6. Transient Response over a shorter period, 3 complete charging and discharging cycles, with voltage at C_{fk}, voltage at C_{out} and four clock signals (CLK4: Reset Signal, CLK3: Sample Clock, CLK2: discharging C_{fk} phase, CLK1: charging C_{fk} phase), respectively from top to bottom.

waveform, 3 complete cycles of charging and discharging were simulated. The charging period started on the rising edge of the first pulse of the ”charging phase” waveform after the ”Reset Signal” goes to zero; in this figure, it was the second pulse of the ”charging phase” waveform. Right after the ”charging phase” goes to zero, ”discharging phase” goes high, which makes the curve at ”Voltage at feedback Cap” node go down. After one complete cycle of charging and discharging, a

slightly increased voltage can be seen from ”Voltage at feedback Cap” node voltage change. This difference is caused by the difference in capacitance between C_S and C_{ref} which is determined by $\Delta V = \frac{V_{ref}(C_S - C_{ref})}{C_{fk}}$. Before the ”Sample Clock” goes high, there are 3 cycles of charging and discharging which makes the total voltage change at ”Voltage at feedback Cap” node be $\Delta V = 3 \cdot \frac{V_{ref}(C_S - C_{ref})}{C_{fk}}$. The four-clock signals shown in Figure 2.5 and Figure 2.6 are all generated on-chip. For different applications, the number of cycles of charging and discharging can be accurately controlled with two external clock signals with the help of the four-phase clock generation circuit.

2.4. Four-phase Clock Generation Circuit

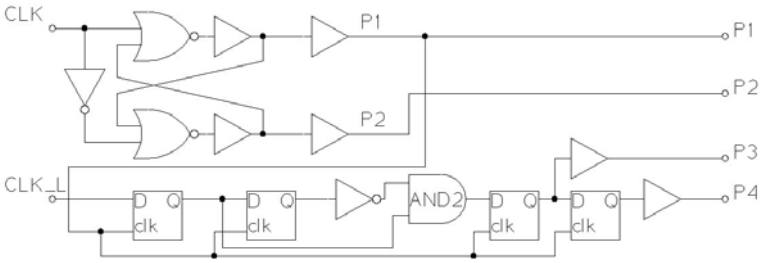

Figure 2.7. Four-phase clock generation circuit

In order to control the charging and discharging cycles for different applications, a four-phase non-overlapped clock generation circuit was designed and laid out on chip. The beauty of this design is that two external clock inputs will be evaluated with on-chip digital logic. The number of cycles is based on the equation $N = \frac{f_{CLK}}{f_{CLK\_L}}$, where f_{CLK} is the frequency of charging and discharging which determines the frequency of CLK1 and CLK2; f_{CLK_L} is the frequency of the sampling

and reset clocks which determines the frequency of CLK3 and CLK4.

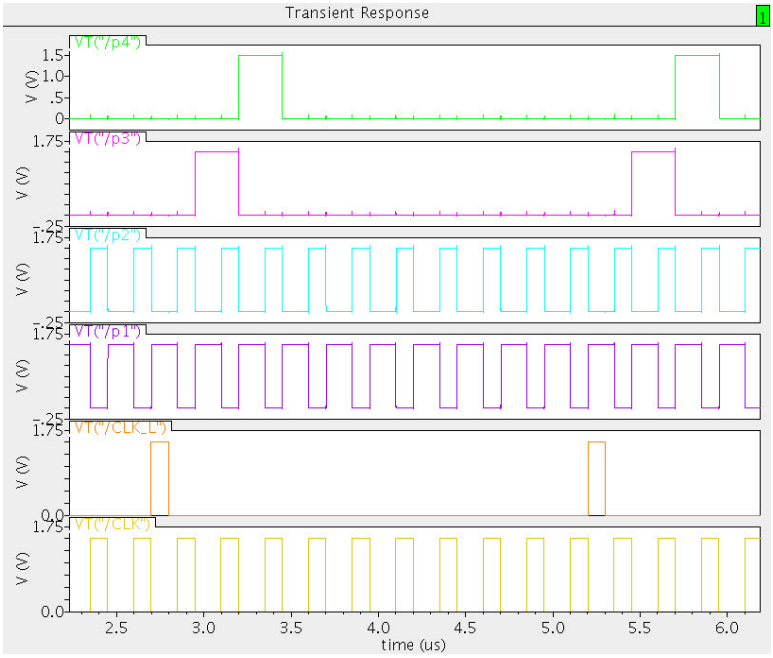

Figure 2.8. Four-phase clocks generation waveform

In Figure 2.8, the CLK waveform comes from an external high frequency clock input; the CLK_L waveform comes from an external low frequency clock input. When CLK_L signal goes from 0 to 1, the coming rising edge of P1 will set the output node Q of the first D Flip-flop to 1. Then the next rising edge of P1 will trigger the rising of P3, and P3 is just one clock delay from P3 with the P1 clock signal. From Figure 2.8, the number of cycles of charging and discharging can be controlled with the CLK_L signal.

CHAPTER 3

BANDGAP AND PTAT DESIGN

3.1. Bandgap and PTAT

3.1.1. Introduction

Designing circuits for biological interfaces requires careful analysis of the role temperature plays in the system. Physiological temperature must be maintained to keep cells alive or mimic the parameters for other biomolecular experiments. In addition, when the temperature in electrical components changes, some of the properties of the components change as well. For instance, if the temperature of a PN-junction increases, the threshold voltage decreases. Naturally occurring signals are analog and thus sensor interfaces require analog circuits. Analog circuits incorporate voltage and current references extensively. Such references should have DC values that exhibit little dependence on supply and process parameters. Thus a good reference establishes a DC voltage or current that is both supply and process independent and has a well-defined behavior with respect to temperature. There are two types of circuits that are commonly used for applications that are highly temperature dependent, PTAT (proportional to absolute temperature) circuits and bandgap references. The output of a PTAT circuit has a linear dependence on the temperature. Bandgap references have an output with very little temperature dependency. Voltage references are also key elements of both analog-to-digital and digital-to-analog converters which need high accuracy reference voltages to provide high-resolution conversions.

3.1.2. CMOS Bandgap Reference

In a Bandgap reference, an output voltage with a low sensitivity to the temperature is obtained as the sum of a forward voltage drop on a PN junction and a contribution proportional to absolute temperature (PTAT). The term with negative temperature dependence is the forward-bias of a diode (usually base-emitter junction). The PTAT term is realized by amplifying the voltage difference of two or more forward-biased diodes (usually base-emitter junctions). $V_{ref} = V_{BE} + K \cdot V_{PTAT}$ Exact cancellation of the dependence of Vref on temperature is not possible because of component tolerances and non-linear second order effects. The behavior of a PN junction voltage is described by $\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln(\frac{I_c}{I_s}) - \frac{V_T}{I_s} - \frac{E_g}{KT^2} V_T$ where V_T is the thermal voltage. We can use the components as described above to implement a circuit with a temperature independent voltage output, see Figure 3.1; this circuit is known as a bandgap reference. In figure 3.1, Q_1 is a single device, and Q_2 represents n devices in parallel. By forcing V_1 to be equal to V_2, the voltage drop on R is determined by the difference of the V_{BE} voltages of the transistors. This suggests that V_2 can serve as a temperature-independent reference with proper design. The positive temperature coefficient of the voltage difference between the PN junctions can be described by the equation below. $V_{BE1} - V_{BE2} = \Delta V_{BE} = V_T \ln(\frac{I_c}{I_s}) - V_T \ln(\frac{I_c}{nI_s}) = V_T \ln n$ In CMOS technologies, where standard bipolar transistors are not available, parasitic bipolar transistors may be used. Figure 3.2 is an example of a simple implementation of bandgap

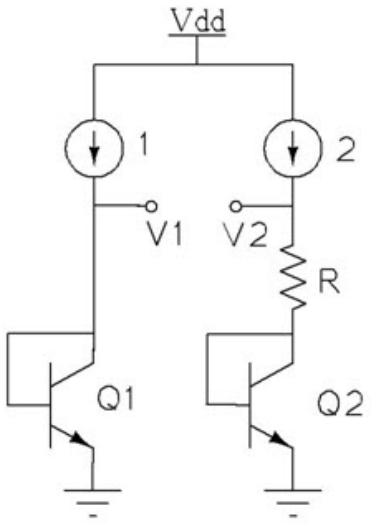

Figure 3.1. Conceptual Generation of Temperature Independent Voltage

reference and PTAT circuits.

3.1.3. A Complete Bandgap and PTAT Implementation

The bandgap voltage reference circuit was further developed by Kuijk [10] and Brokaw [11] based on the work of Widlar [12]. The most recent developments in CMOS bandgap voltage references focus on low-voltage and low-temperature-coefficient methodologies. Here from Figure 3.3, we have $V_o = V_{be1} + \frac{R_2}{R_3}\frac{kT}{q}\ln(\frac{R_2}{R_1}\frac{I_2}{I_1})$.

3.1.4. CMOS Bandgap Reference for Sub-1V Operation

As conventional bandgap reference circuit achieved a V_{REF} around 1.2V, which is the value of the energy band of silicon, as is shown in the following equation: $V_o = V_{be1} + \frac{R_2}{R_3}\frac{kT}{q}\ln(\frac{R_2}{R_1}\frac{I_2}{I_1})$ Banba et al. [13] had proposed an alternative for sub-1volt bandgap reference operation. The idea is to introduce another factor defined by the ratio of resistors that can scale down the bandgap reference voltage. If we

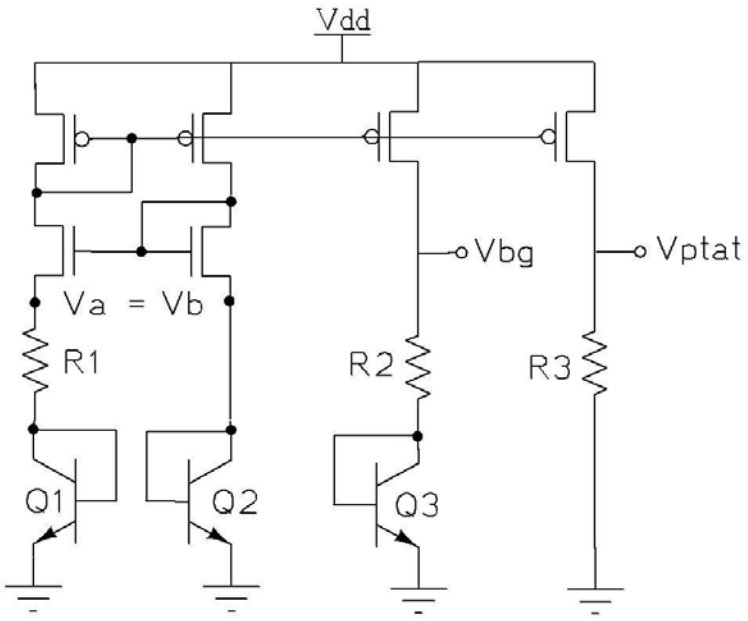

Figure 3.2. Simple implementation of Bandgap Reference and PTAT

assume the opamp in Figure 3.4 has infinite gain, the potentials at the positive and negative input nodes are the same. If we assume that R1=R2, we obtain the following equations to illustrate why this configuration can provide a sub-1V reference voltage.

$$I_{2b} = I_{1b} = \frac{Vb}{R_1}$$

$$V_{R3} = V_{pnp1x} - V_{pnpNx} = V_T \ln(\frac{I_{1a}}{I_s}) - V_T \ln(\frac{I_{2a}}{NI_s}) = V_T \ln(N\frac{I_{1a}}{I_{2a}})$$

$$I_{2a} = \frac{V_{R3}}{R_3} = \frac{V_T}{R_3} \ln(N\frac{I_{1a}}{I_{2a}}) = \frac{V_T}{R_3} \ln N$$

$$I_1 = I_2 = I_3 = I_{2a} + I_{2b} = \frac{V_T}{R_3} \ln N + \frac{V_{pnp1X}}{R_2}$$

$$V_{ref} = R_4 \cdot I_1 = \frac{R_4}{R_2}(\frac{R_2}{R_3} V_T \ln N + V_{pnp1X})$$

$$V_{bandgap\_conv} = \frac{R_2}{R_3} V_T \ln N + V_{pnp1X}$$

Since the ratio of $\frac{R_4}{R_2}$ can be controlled, it is possible to decrease the conventional bandgap voltage, around 1.2V, to a lower or even sub-1V value.

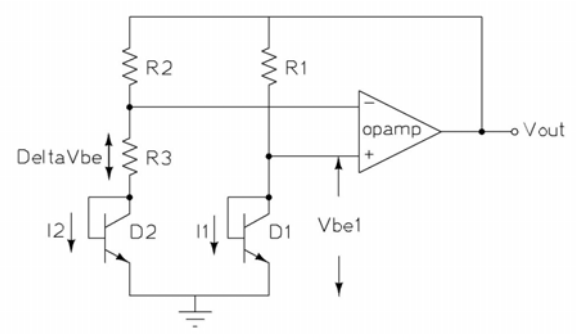

Figure 3.3. Fundamental Bandgap Circuit

3.2. Bandgap and PTAT Design in 3D SOI 0.15 μm Process

The bandgap reference and PTAT circuit have been implemented on both ICs. Various conditions including power supply variations, resistor absolute value variations have been simulated and verified. In Figure 3.6, the values of R1, R2 and R3 have been varied by +/- 20%, and simulations showed that the PTAT circuit outputs are linear and bandgap reference outputs are changing by less than 3mV total from 0 to 50 degrees C.

3.3. Opamp Design Verification at Various Conditions

Opamp Design with Constant-GM Biasing is shown in Figure 3.7

3.3.1. Power supply variation

We simulated the performance of the system under various of power supply conditions. The system was designed to use a power supply of 1.5 V. In simulations, the power supply has been varied from 1.2V to 1.8V, and the system's performance was verified. Figure 3.8 showed that opamp's DC gain and phase margin are consistent with 20% power supply variation.

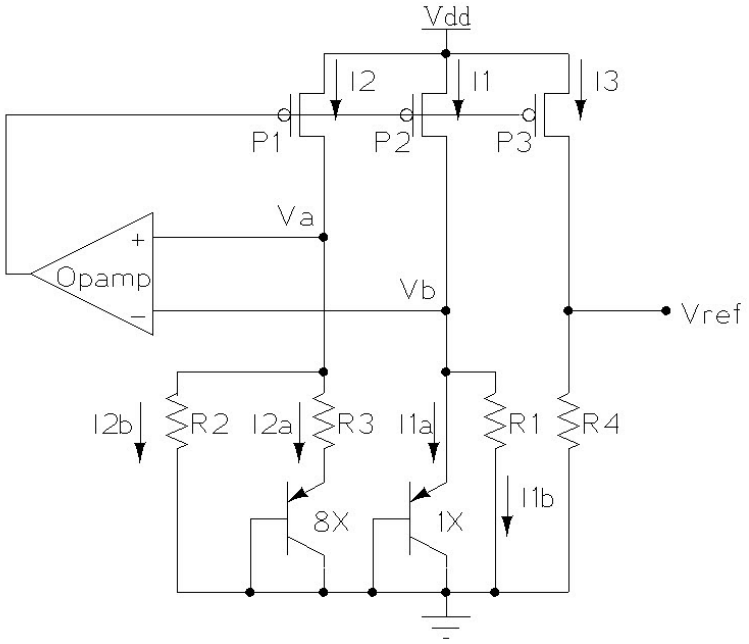

Figure 3.4. Sub-1 Volt Bandgap Reference Circuit

3.3.2. Common Mode Input Level Variation

We simulated the performance of the system under various of common mode DC levels. The system was designed to use a common mode voltage of half Vdd. In simulations, the common mode input DC level has been varied from 0.4 V to 1.1 V, and the system's performance was verified. Figure 3.9 showed that opamp's performance is consistent with a common mode DC operating voltage from 0.4 V to 1.1 V.

3.3.3. Temperature Variation

We simulated the performance of the system under various of temperature. In simulations, the temperature has been varied from 0 Degree C to 120 Degree C. Figure 3.10 showed that with temperature variation from 0 Degree C to 120 Degree

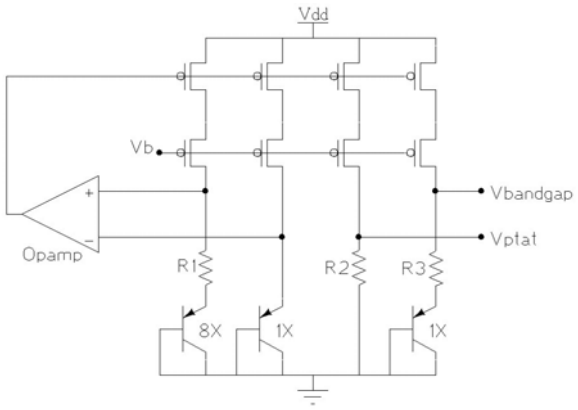

Figure 3.5. Bandgap reference and PTAT circuit diagram

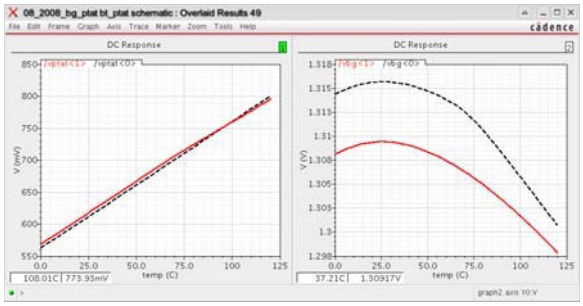

Figure 3.6. Simulation results of Bandgap reference and PTAT under resistance variations of +20% (dashed black line) and -20% (solid red line)

C, opamp's performance is consistent.

3.3.4. Resistor in Constant Gm Biasing Variation

We simulated the performance of the system under the resistor variations. The system was designed to use a resistor value of 3.5 kOhms. In simulations, the resistor value has been verified from 2.5 kOhms to 4.5 kOhms. Figure 3.11 showed that within +/- 29% variation of the resistor in constant Gm circuit, the opamp's performance is consistent.

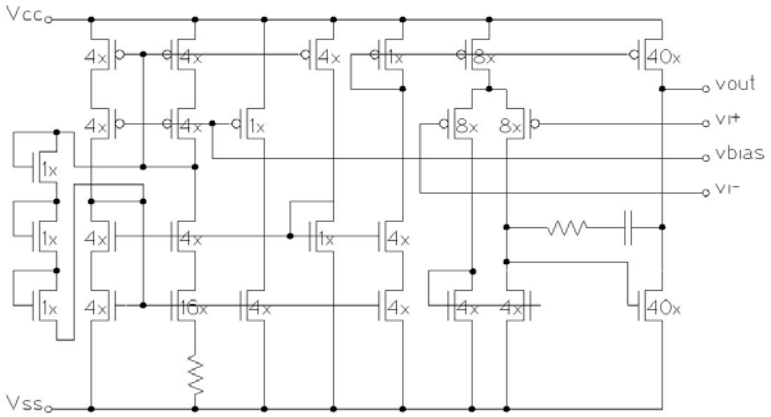

Figure 3.7. Opamp with constant Gm biasing circuit diagram

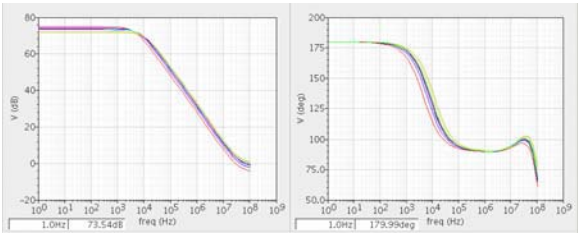

Figure 3.8. Gain and phase margin Bode plot with power supply variation

3.3.5. Compensation Capacitor Variation

We simulated the performance of the system under the compensation capacitor variations. the system was designed to use a capacitor value of 2 pF. In simulations, the compensation capacitor value has been verified from 1.5 pF to 2.5 pF. Figure 3.12 showed that with +/- 25% variation of the capacitor value, the opamp's performance is consistent.

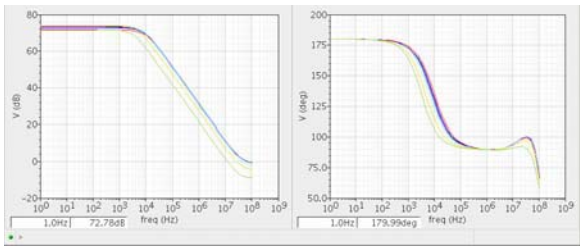

Figure 3.9. Gain and phase margin Bode plot with power supply variation

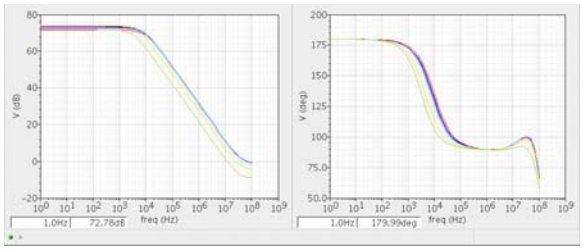

Figure 3.10. Gain and phase margin Bode plot temperature variation

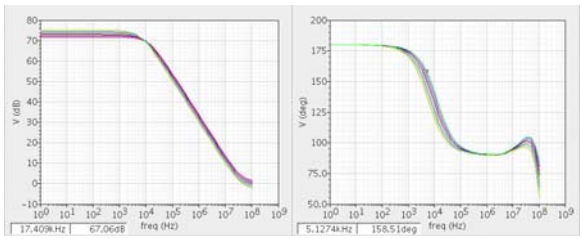

Figure 3.11. Gain and phase margin Bode plot with biasing current variation

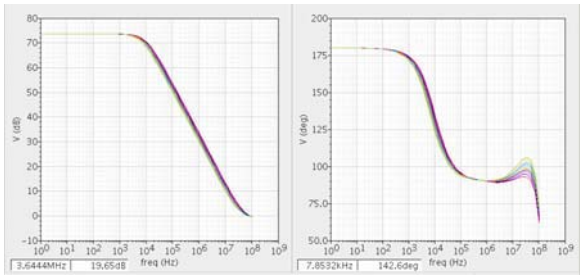

Figure 3.12. Gain and phase margin Bode plot with compensation capacitor variation

CHAPTER 4

AMPLIFICATION CIRCUIT FOR HL-1 CARDIAC CELLS ACTION POTENTIAL MEASUREMENT

4.1. Introduction

Action potentials in cardiac cells are intracellular signal across the cell membrane. When microelectrode recording methods are used, only the second derivative of the signal can be detected due to the low seal resistance between the cell and the electrode [14]. The challenge in measuring the extracellular cardiac action

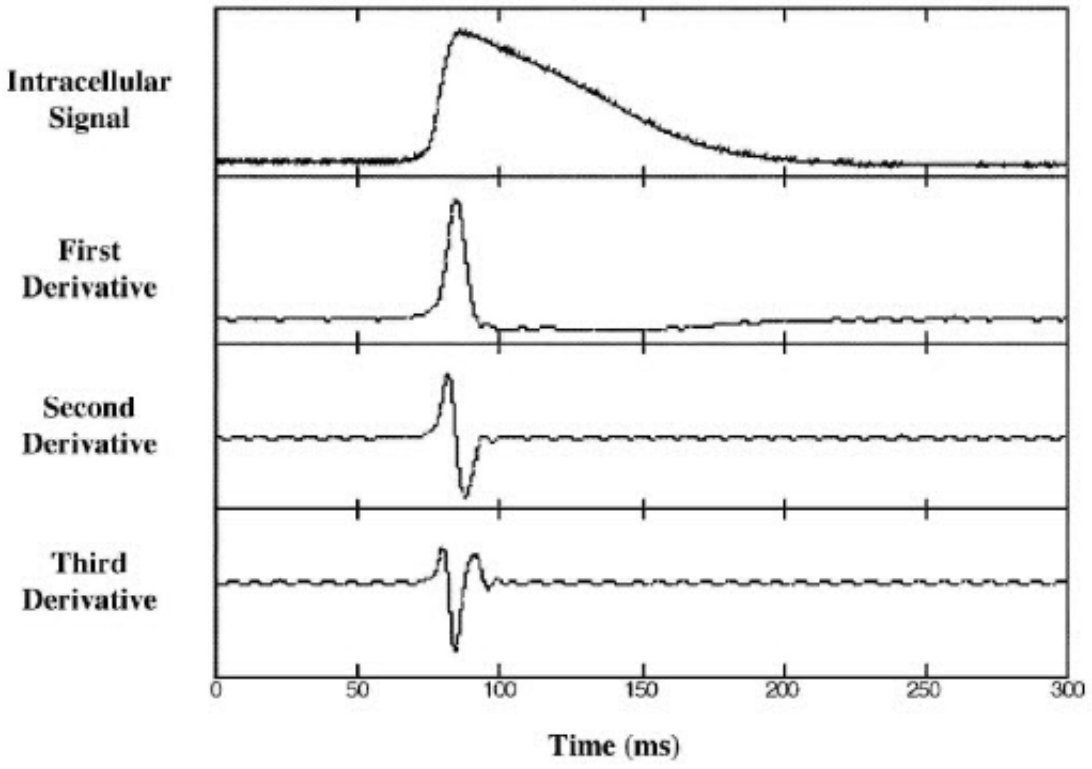

Figure 4.1. A typical HL-1 intracellular signal recorded are shown [1]

potentials is the small signal amplitude, small signal to noise ratio, and DC drift. Creating a biologically suitable interface for recording these signal is also difficult.

The extracellular action potential is 1-2mV peak-to-peak with a bandwidth of 2 kHz to 4 kHz and a signal to noise (SNR) ratio of less than 10. For low frequencies the noise floor is pushed up by the flicker noise (1/f noise), so we will include high pass filtering We therefore use a multi-stage amplification and filtering circuit shown in

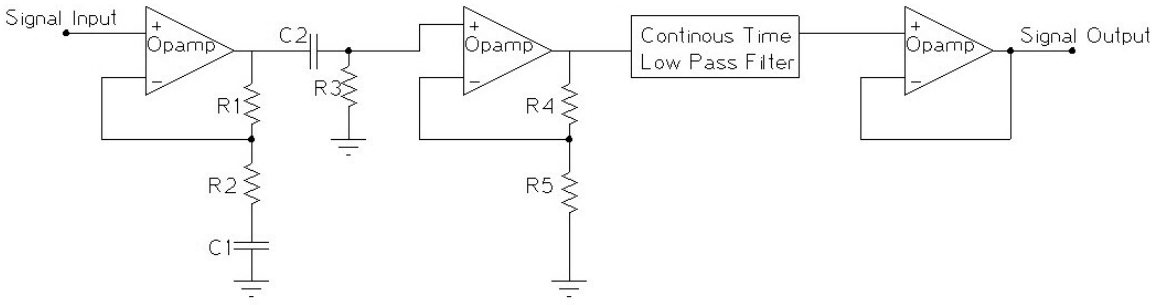

Figure 4.2. The complete amplification and filtering circuit diagram

Figure 4.2. The electrodes are directly connected to the active components in the pre-amplification stage to maintain the signal to noise ratio since initial filtering with passive devices would further decrease the SNR. Rather than using a coupling capacitor to mitigate the effects of DC drift, we use a higher SNR design and eliminate the DC drift problem by adding a capacitor between the non-inverting gain resistors and ground. In addition we add an AC coupling capacitor between the first and second gain stages to further remove DC offset. This capacitor is also part of the high pass filter after the first stage that removes frequencies below 6 Hz. The second stage of the circuit is a non-inverting amplifier with a gain of 20. This is followed by a continuous time 10th order linear phase low pass filter with a cutting frequency of 5 kHz. The continuous time filter was selected because it does not require a clocking signal for operation that would add noise to the circuit.

The final stage is a buffer for a possible low impedance load. All of the amplifiers used are LinCMOS precision chopper-stabilized op amps from Texas Instruments with a low offset voltage of $1\mu V$, a low temperature drift of less than $0.003\mu V/°C$, and a common-mode input voltage range that includes the negative rail.

4.2. Circuit Design and Testing

A custom square inch, two-layer PCB designed using PCB Artist is shown in Figure 5.2. Two instances of the circuit are included on each board. The first instance allows for both individual measurement of each stage and the complete circuit, because the stages are not connected but instead require jumpers to manually complete the connections. This allows for separate testing after each stage but also introduces additional parasitics that are not favorable for operation. The other instance contains the complete circuit without testing points. UPDATE UPDATE

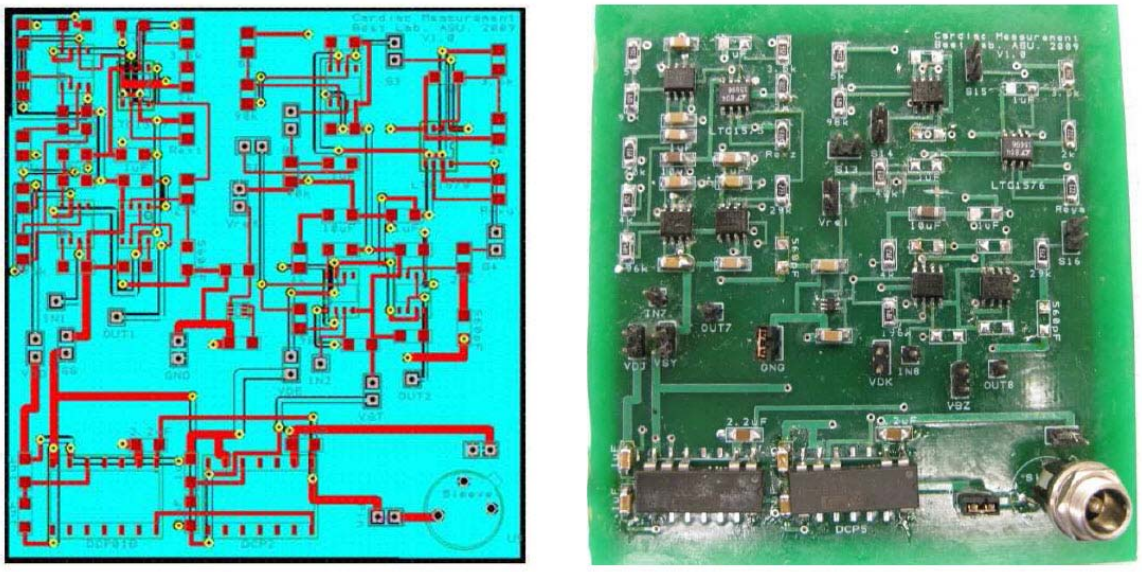

Figure 4.3. Custom designed printed circuit board layout (left) and picture (right) are shown

4.3. Discussion

I have designed and tested an amplification circuit for measuring test signals from an arbitrary function generator. The circuit performance was consistent with simulation results having expected gain and cutoff frequencies. In a multistage

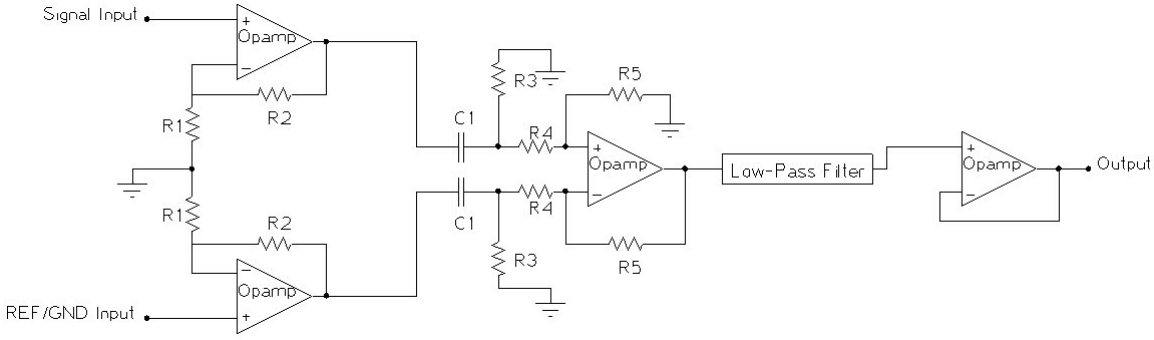

Figure 4.4. Fully differential design of amplification and filtering circuit

amplification circuit, the first stage should have a relatively low gain, around 10, because the noise in the input will be amplified as well. With a low gain first stage, we can perform the first filtering after the pre-amplification to remove noise contribution before the high-gain second stage. This will improve the overall signal-to-noise ratio since the signal experience the gain of the whole system while the noise does not. Though our current design filters the signal several times and gives a high gain on the input signal, we can further improve the resolution of our measurement circuit by implementing a fully differential design. Single-end op amps suffer from surrounding noise including induction noise. Fully differential circuits will improve the performance of the system by canceling out noise from connection wires and other parasitics in the system. Since the noise is mostly common to both input

nodes, amplifiers with good common-mode rejection ratio (CMRR) will be nearly unaffected by this type of noise. We have redesigned the circuit in a fully differential configuration with a gain of 10 at the pre-amplification stage; this will give higher resolution and better SNR performance. The schematic for the circuit is shown in Figure 4.4.

CHAPTER 5

PHASE DETECTOR FOR CARDIAC ARRAY MEASUREMENT

5.1. Phase Detector Design

5.1.1. Introduction

Phase detectors are used to detect the delay of between two signals in the time domain. Phase detectors can be used to convert delay information to a voltage. This can be accomplished by generating digital pulses when their effective pulse widths equal to the phase difference between two inputs. Usually, the output is integrated to generate a voltage representative of the delay. We have designed a phase detector that converts the delay information to a 12-bit digital output using a high frequency counter clock signal. Detailed analysis will be covered in Chapter 5.3.

5.1.2. Basic Phase Detector Circuit

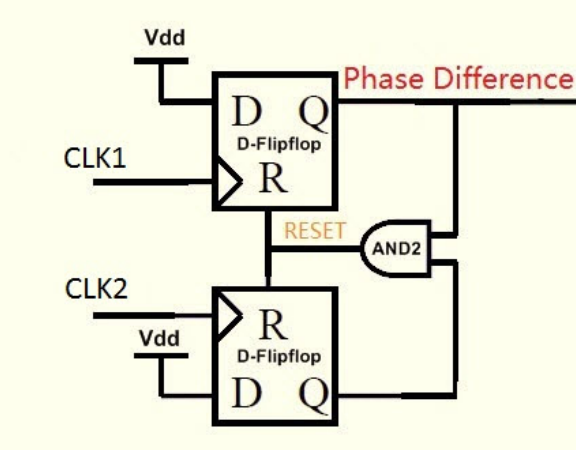

Figure 5.1. Basic phase detector with D-flip flops

Operation of such phase detector circuits can be described using timing diagrams, see Figure 5.2 If we define the two inputs of the phase detector as CLK1

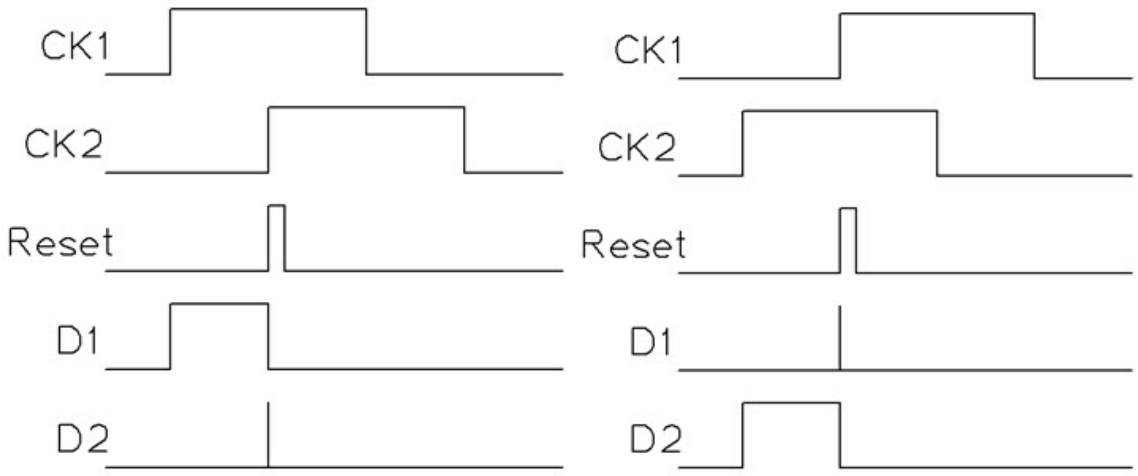

Figure 5.2. CLK1 leads CLK2(left), and CLK2 leads CLK1(right).

and CLK2 with CLK1 connecting to FF (flip flop) 1 and CLK2 connecting to FF2 (see Figure 3.3.1.1), we can describe the behavior of the system as follows. If the CLK1 leads CLK2, see Figure 5.2 (left), the output of the FF1 (D1) is first asserted to a logical 1 at the rising edge of CLK1. At the rising edge of CLK2, a reset signal Reset = 1 is generated by AND2, the AND of the two D-FFs outputs. The reset signal will then reset both D-FF to logical 0. The pulse width for FF1 (D1) at logical 1 equals the delay difference between CLK1 and CLK2. If CLK2 leads CLK1, see Figure 5.2 (right), the output of the FF2 (D2) is first asserted to logical 1 at the rising edge of CLK2. At the rising edge of CLK1, a reset signal Reset= 1 is generated by AND2, the AND of the two D-FFs outputs. The reset signal will then reset both D-FF to logical 0. The pulse width for FF2 (D2) at logical 1 equals the delay difference between CLK1 and CLK2.

5.2. Phase Detector Circuit Diagram

Signal propagation and transfer speed of action potentials contain a great deal of information that can be used to understand the properties of the cells that transfer the signals to detect the integrity of the signal path. For example, the activities of cardiac cells can be exposed to pharmaceuticals that modify their behavior. We can understand the effects of this interaction on the electrical activity of the cells by measuring the propagation of the signals. I have designed a phase detector

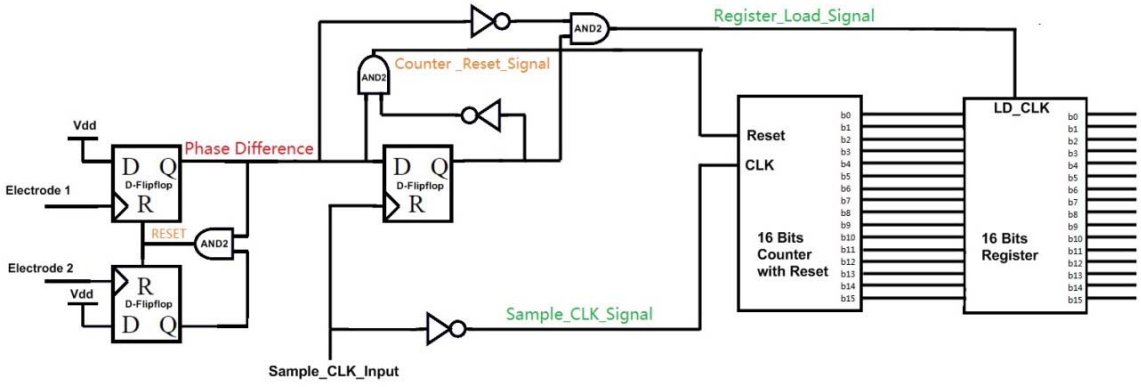

Figure 5.3. Phase detector circuit diagram

circuit to measure the propagation delay between action potentials in a array of electrodes over which cardiac cells have been cultured. In my design, in order to measure the delay between two propagation signals, I converted the delay information to a pulse. The pulse width in the time domain is the time delay between signals; here the term ”two signals” can also be thought of as one signal measured at two different points in space. If an array is built for delay measurement, any two electrodes from the array can be used to measure the propagation delay. The

pulse width which contains the delay information is then passed through digital logic. Here another external sampling clock signal will be needed. The counter was clocked by this sampling clock, and it counts the delay with a 16 bits digital output. A higher frequency sampling clock is used to measure this delay in the time domain and convert the pulse width to a digital output. The digital output is then stored in a register. Continuous measurement is possible as the counter will be reset with the next rising edge of the delay pulse.

5.3. Circuit and Application Analysis

In Figure 5.3 electrode 1 and electrode 2 are the cell responses after amplification and filtering (the filter and amplification circuit discussed in Chapter 5.3); the pulse is considered a logical 1 for the connected D-flip flop. The flip-flop directly connected to the input clock signals (CLK1, CLK2) has a positive edge triggered reset signal. The output of two D-flip flops are connected as two inputs of the NAND2 gate, and the NAND2 gate output is connected to the Reset port of two D-flip flops. We assume there is a phase difference T1 in time domain and both input clock signals CLK1 CLK2 are square pulses. We also assume CLK1 is always earlier than CLK2; this can be physically decided by our electrode configuration. The output of the D-flip flops connected from CLK1 is a square pulse with a duty cycle directly related to the T1 phase difference. We name this pulse CLK_DF. The rising edge of CLK_DF will trigger the rising of the Counter_Reset signal. Counter_Reset resets the counter. This makes the counter start counting from 0 and continues to count

until the next Counter_Reset signal goes to logical 1. The falling edge of CLK_DF will trigger the rising of Load_Signal. When the Load_Signal is set to its logical 1, the counter will transfer the counts it has at that time to the register. In Figure 5.3, a 16 bit Counter and 16 bit Register are used for counting and storing. The actual number of counts we get is decided by the Phase Difference T1 (seconds) and the frequency Fs (Hz) of sampling clock CLK_SAMPLE. $Counts = \frac{T1}{1/Fs} = T1 \cdot Fs$. The phase difference T1 is usually on the order of several milliseconds. For example, if we use the value 1ms and we choose a sampling frequency of 1 MHz,

$$Counts = 1 \times 10^{-3} \times 1 \times 10^{6} = 1000$$

; the resolution (time period of a single count) = $10^{-3}s$. We can decide the number of bits we need for the counter and register based on the expected counts. A 16 bit counter supports up to 2^{16} counts. This means if the phase difference CLK_DF= $10^{-3}s$, theoretically the maximum sampling clock we can use is 6.5M Hz, the minimum time period difference it can detect is 1.5×10^{-7} seconds. However, due to the inherent input-to-output delay, usually called Tpd (usually several nanoseconds), of the discrete components and other non-ideal effects, we may not be able to obtain this theoretic value. A more practical time difference (resolution) that can be detected with discrete components would be in the microsecond range.

5.4. Phase Detector Simulation Result with Digital Outputs

From Figure 5.4, the first phase difference pulse has 10 rising edges of the sampling clock signal within this single pulse, the digital outputs from bit 0 to bit 3

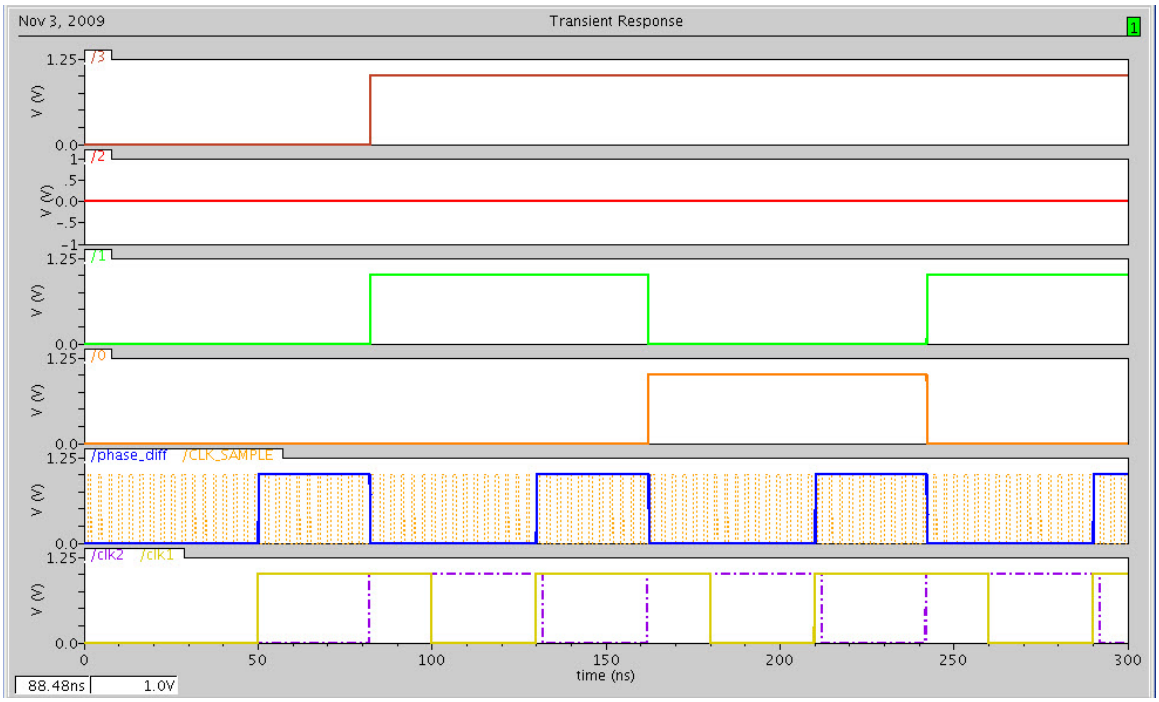

Figure 5.4. Phase detector simulation results for a typical delay time

are ”0101” which is 10 in decimal. The second phase difference pulse has 9 rising edge of sampling clock signals within this pulse period, and the digital outputs from bit 0 to bit 3 are ”1001” which is 9 in decimal. The third phase difference pulse also has an output of 10 in decimal. The simulation demonstrates that we are able to design a phase detector circuit capable of determining phase differences on the order of nanoseconds. However, as previously mentioned, implementation of the circuit with discrete components with severely decrease the time resolution of the circuit.

CHAPTER 6

SIGMA DELTA ADC AND SIGMA DELTA DAC

6.1. Sigma Delta Circuit and Sigma Delta D/A Design

Computational and signal processing tasks are now performed predominantly by digital logic. Since digital circuits are robust and can be realized by extremely small and simple structures, they can be combined to obtain very complex, accurate and fast systems. Given that the physical world properties such as temperature or capacitance remains analog, data converters are needed to interface with the digital signal processing and transmission. Data converters (both ADCs and DACs) can be classified into two main categories: Nyquist-rate and oversampled converters. In the former category, there exists a one-to-one correspondence between the input and output samples. Each input sample is separately processed, regardless of the earlier input samples; the converter has no memory. Thus, the analog signal can be converted back via Nyquist-rate DAC via this one-to-one correspondence with a reference voltage. Practical conditions restrict the matching accuracy to about 0.02%[UPDATE], and hence the effective number of bits (ENOB) to about 12. A common measure of a converter's accuracy is the signal-to-noise ratio (SNR) for a sine-wave input. SNR/dB=ENOB*6+1.76, in this case SNR is about 74dB. Nyquist-rate converters usually operate at a sampling frequency slightly higher than twice the signal bandwidth being sampled. In many applications, higher resolution and linearity are required. This can be achieved at much faster sampling rate using noise shaping. The concept of noise shaping was probably first proposed (along with the sigma delta modulation) in 1962 by Inose

et al [15]. Noise shaping is further explained below. From Figure 6.1, at relatively low frequency, Sigma Delta ADCs have the ability to achieve the highest ENOB. The reason we are interested in Sigma-Delta ADCs (Analog-to-Digital Converters)

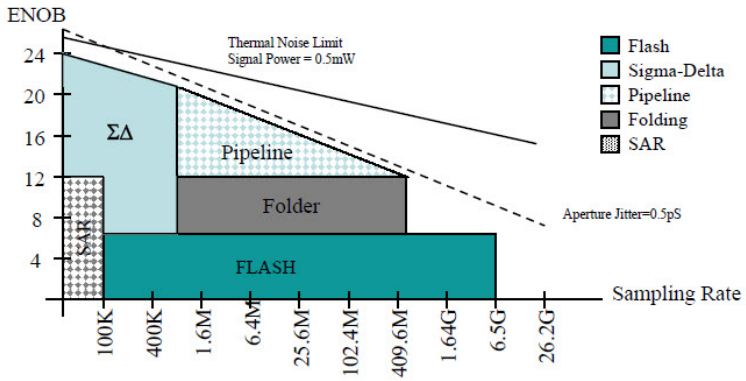

Figure 6.1. ADC's ENOB with sampling rate

is based on the fact that the signal frequencies from the action potentials of the cardiac cells or other biomedical signals is limited to several kHz. These relatively low signal frequency responses makes the architecture of Sigma Deltas appealing. The Nyquist rate ADC method creates a flat quantization noise floor (see Figure 6.2) independent of the signal bandwidth. This flat noise floor makes it difficult to achieve a high SNR. The use of Sigma Delta ADCs inherently provides quantization noise shaping giving us the power to optimize our design based on the signal bandwidth we actually observes in our experiments. Figure 6.3 demonstrates how a Sigma Delta ADC, an oversampling noise-shaping data converter, can minimize the quantization noise at the signal bandwidth and thus maximizing the SNR at the signal bandwidth. For the traditional Nyquist-rate ADC when a analog signal

is converted to digital signal, the quantization noise floor is essentially flat from DC to Fs (the sampling frequency), see Figure 6.2. With a Sigma Delta ADC for even better in band SNR, an analog loop filter can be added. This decreases the quantization noise within our band of interest at the expense of larger quantization noise power outside the band. This is the concept of ”noise-shaping” with Sigma Delta ADCs; see Figure 6.3 for the noise shaping near Fin.

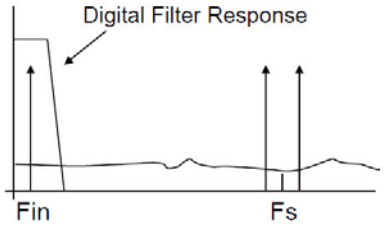

Figure 6.2. Quantization Noise without Noise Shaping [2]

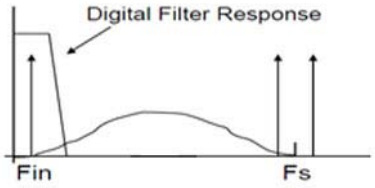

Figure 6.3. Quantization Noise with Noise Shaping [2]

6.2. Sigma Delta ADC for Low Frequency Sampling

As previously discussed, using a Sigma Delta ADC can achieve the highest ENOB in a relatively low frequency band. If we want to determine the appropriate sampling frequency for a specific application, we need to know the bandwidth of the signal that we are trying to measure. If we use a Sigma Delta ADC to measure a signal with a bandwidth of fb, we can get an OSR (over-sampling ratio) of 64 with a

sampling frequency of 128 times fb or an OSR of 128 with a sampling frequency of 256 times fb, where OSR = sampling frequency/(2*Signal Bandwidth). The signal bandwidth of action potentials for cardiac cells is limited to several kHz (ranging from 1 to 4 kHz). If we assume a signal bandwidth of 4 kHz, we obtain an OSR of 64 or 128 using a sampling frequency of 512 kHz or 1.024MHz respectively. We can determine the maximum SNR as SNRmax=6.02*N+1.76+10Log (OSR), where N is the ENOB of an ADC. With an oversampling ADC, theoretically the SNR can be increased by 10Log (OSR). If we have an OSR of 64 and 128, we can increase the SNRmax by 18dB and 36dB respectively.

6.3. 2nd order Sigma Delta ADC design

We have designed a continuous-time sigma delta ADC implemented with active-RC circuitry. The same architecture can be applied to our cardiac cell recordings with a low frequency design. Initially the system was verified with a 200 kHz sinusoidal input signal, but the system can be further optimized for low frequency applications by scaling the passive components. For testing, our circuits and sim-

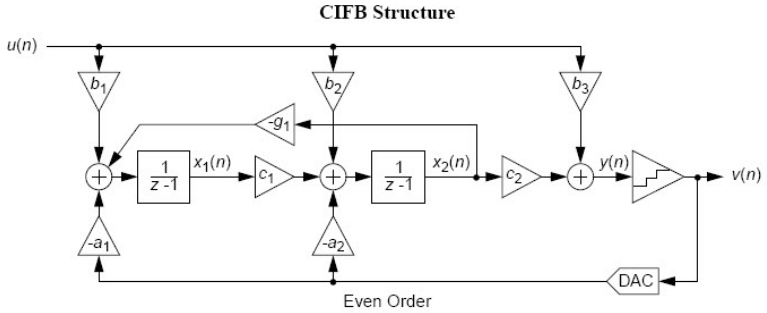

Figure 6.4. Architecture of our Sigma Delta ADC [2]

ulations were designed and conducted with a 200 kHz sinusoidal differential input (0.5 Vp-p). We achieved a SNR greater than 70dB with a sampling clock rate at an over sampling ratio of 128. The simulation environment is based on Simulink from Matlab 2009a and Cadence IC 5.141. All models used in Cadence simulations are written in VerilogA. Based on the following calculation, coefficients are obtained for the CIFB 2nd order sigma delta ADC converter architecture. The transfer function of the system is shown below with EQ representing the quantization noise.

$$[(b_1x + a_1y)\frac{k_1}{sT_s} + b_2x + a_2y]\frac{k_2}{sT_s} + E_Q = y$$

The transfer function with each fraction having a common denominantor is shown below.

$$y = \frac{b_1xk_1k_2}{s^2{T_s}^2 - a_1k_1k_2 - a_2k_2sT_s} + \frac{b_2xk_2sT_s}{s^2{T_s}^2 - a_1k_1k_2 - a_2k_2sT_s} + E_Q\frac{s^2{T_s}^2}{s^2{T_s}^2 - a_1k_1k_2 - a_2k_2sT_s}$$

The signal tranfer function comprised of the first two terms from above and the noise tranfer functions which modifies the quantization noise, EQ, are shown.

$$STF = \frac{b_1k_1k_2 + b_2k_2sT_s}{s^2{T_s}^2 - a_1k_1k_2 - a_2k_2sT_s}$$

$$NTF = \frac{s^2{T_s}^2}{s^2{T_s}^2 - a_1k_1k_2 - a_2k_2sT_s}$$

The signal bandwidth, Fb, is 200 kHz. The OSR is defined as Fs/2Fb, and we used a value of 128. This implies a sampling frequency of 51.2 MHz. The sigmal delta toolbox in Simulink can only simulate direcrete time sigma delta architecutres. Therefore, we use the z-domain signal tranfer funtion (STF) and noise tranfer funtion (NTF) for these discrete time simulations. These z-domain tranfer functions

can be converted to the s-domain through transformations [PUT EXACT NAME OF THE EQUATION]. This allows us to have the correct transfer funtions for continous time architectures. Each of the transfer funtions is shown below.

$$
\begin{aligned}
z-domainSTF &= \frac{0.21637}{z^2-1.225z+0.4415} \\
s-domainSTF &= \frac{-0.18996(s-1.713)}{s^2+0.8175s+0.3254} \\
z-domainNTF &= \frac{(z-1)^2}{z^2-1.225z+0.4415} \\
s-domainNTF &= \frac{\mathrm{s}\,(\mathrm{s}-0.19)}{(s^2+0.8175s+0.3254)}
\end{aligned}
$$

The coefficients for this architecture in the z-domain can be obtained by the sigma delta toolbox in Simulink. The coefficients in z-domain are as follow: a1= 0.2112, a2= 0.133, b1= 0.2112,b2=0, c1=0.1763,c2=5.81, g=0 By comparing the specific values obtained by transforming the z-domain STF and NTF to the s-domain with the general equations shown above, we can obtain the coefficients in the S-domain. The coefficients in s-domain are as follow: a1=-0.3254, a2=-0.8175, b1=0.3254, b2=-0.18996, k1=k2=1 Even though the coefficients are obtained, when the architecture has been implemented with active-RC circuitry, we still need to adjust those values for optimized performances. We have implemented this architecture in Cadence IC 5.141, and the initial parameters we used were obtained from the coefficients. We further adjust those values based on the VLSI requirements that capactiors and resistors for integration can not exceed certain values; however with active-RC, the ratio of capacitors and resistors can be controlled in oder

to realize the STF and NTF we are interested in. In Figure 6.5, the output from Cadence was processed in matlab and the power spectrum plot is shown.

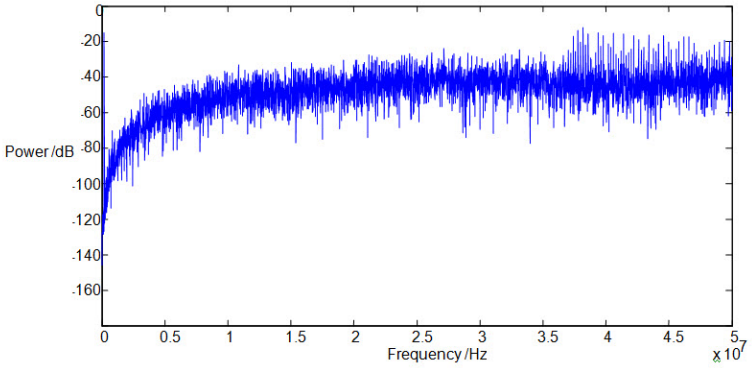

Figure 6.5. Noise shaping is shown with 200 kHz input sine wave

6.4. 1st Order Sigma Delta DAC Design

The following system diagram demonstrates how a sigma delta DAC circuit is realized. This architecture was implemented in Cadence with VerilogA models. Sigma Delta DAC can be used to convert parallel data to serial data output. For

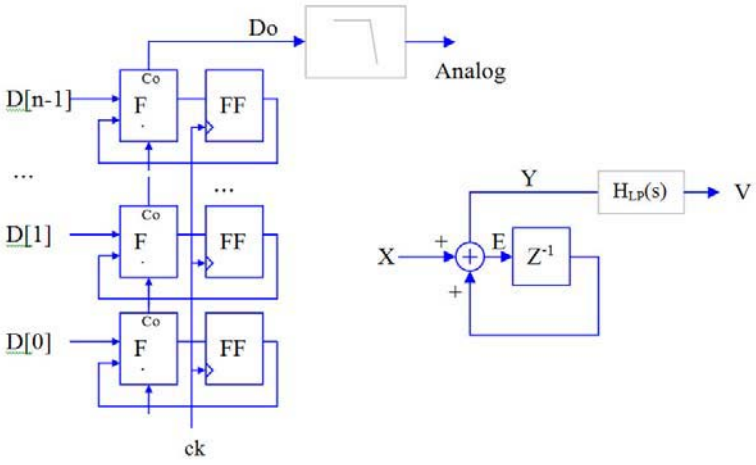

Figure 6.6. 1st order Sigma Delta DAC architecture [3]

the fist-order sigma delta DAC in Figure 6.6, z-domain SFG illustrates the design concepts. From the SFG we can obtain the transfer function below. If we solve for Y, we can obtain the complex exponential form shown.

$$X + E \cdot z^{-1} = E + Y$$

$$Y = X + E(z^{-1} - 1)$$

$$z = e^{jwt}$$

Here w is the signal bandwidth, and 1/ is the sampling frequency. We have defined the OSR as shown below, and we can write it in terms of w and t. $OSR = \frac{SamplingFrequency}{2 \times SignalBandwidth} = \frac{1/t}{2 \times 2\pi \times w} = \frac{1}{4\pi wt}$ For a Sigma Delta DAC, the OSR should be much greater than 1, so $wt << 1$. Thus we can approximate the transfer functions as follows: $Y = X + E(z^{-1} - 1) \approx X + E\sin(wt/2) \approx X$

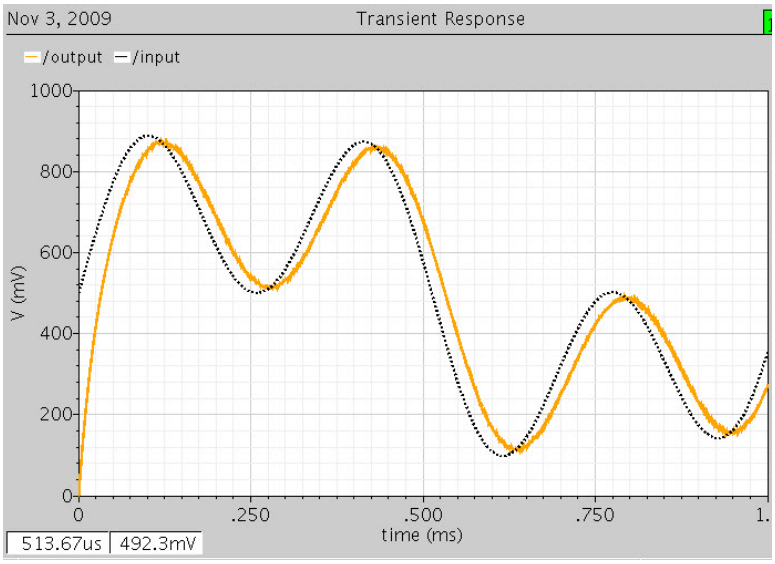

Figure 6.7. The input signal was first quantized with a 12 bit ADC and then recovered by a 1st order sigma delta DAC and a low pass filter. The output signal tracked the input signal with a phase delay. The black dashed line is the original signal input, and the solid orange line is the output from the DAC.

CHAPTER 7

CHIP OVERVIEW AND TESTING PLANS

7.1. Introduction

The capacitance sensor, bandgap reference, PTAT circuits described in chapter(s) XXX were implemented on two chips for the MIT/LL 3D process as was explained. The two chips were taped out in December 2008. Designs were made and tested with 3DIC_3.3.5 model files from MIT Lincoln Lab using IBM 0.15 μ M SOI 3D technology. The design environment is Cadence IC 6. The difference be-

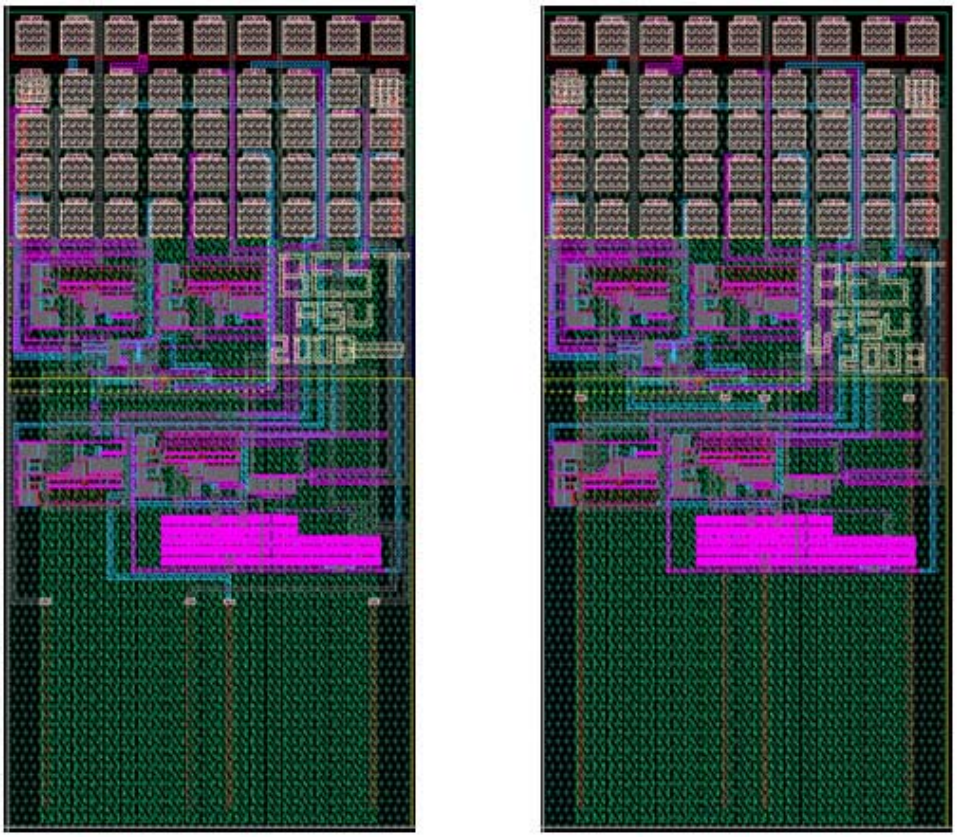

Figure 7.1. Layout of via capacitor chip (left), without via capacitor chip (right) are shown.

tween the two chips is the structure of the sensing capacitor. In the first design, the layout of the sensing capacitor is only on the top tier of the chip; the other

design uses vias to connect the sensing capacitor over two tiers. The designs are expected to sense the capacitance change when fluid or ionic solutions are applied on the surface of the chips. Post-processing in the ASU CSSER (Center for Solid State Electronics Research) facility we be performed to etch the passivation layer, removing the top glass of the dies to expose the sensing capacitor. The sensing capacitance changes without etching will be due to the fringe capacitance, and the etched capacitor will behave as a traditional parallel plate capacitor. The latter should provide a greater capacitance change; this justifies the extra processing required. Together with the capacitance sensor, both the PTAT circuit and the bandgap reference were laid out on both chips. From the PTAT circuit, we expect to measure the internal temperature of the chip. This PTAT circuit was simulated to work at a temperature range from 0 to 120 $^{\circ}C$ with a linear relationship between temperature and voltage output. The bandgap circuit has an output voltage that is within only 1mV change over a 0 to 120 $^{\circ}C$ temperature range. A two stage opamp was designed with an internal biasing circuit; the biasing circuit was implemented through constant Gm circuit. The opamp has a DC gain of 70dB. One non-overlapped clock generation circuit was laid out in order to provide the switched-cap circuit with the internal clock signal. All designs were tested with all corner conditions including power supply changes, temperature changes and possible fabrication variations on resistors and capacitors. On the bottom tier of the chips, we have a serpentine polysilicon structure which will serve as a resistive

component for the on-chip heaters. The heater covered the entire bottom tier, so it can be used to heat the whole chip. The temperature change can also be used to verify the functionality of the PTAT circuits and the bandgap reference.

7.2. Full Chip Bond Pads Naming and Testing Plans

The following figure, Figure 7.2 illustrates the location of each bond pad for both chips. The table is easily correlated with the bond pads visible in Figure 7.1 and can serve as a bonding diagram for the two chips. Since we have several rows of bond pads, we will be unable to bond the entire chip. However, many of the test structures will be tested with a probe station only. For operation we need to bond only a small subset of the bond pads.

Full chip Bond pads Definitions								
1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9
2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9
3.1	3.2	3.3	3.4	3.5	3.6	3.7	3.8	3.9
4.1	4.2	4.3	4.4	4.5	4.6	4.7	4.8	4.9
5.1	5.2	5.3	5.4	5.5	5.6	5.7	5.8	5.9

Figure 7.2. Full chip naming map

7.2.1. Capacitance Sensor Testing

The capacitance sensor is the key functional element for each of the two chips. As mentioned before, the difference of two chips is the structure of the sensing capacitor. Both designs have identical reference capacitors with an initial value of 10pF. Both designs allow the sensing capacitors to have physical contact from top tier of the chip. Bond bad 3.2 is the power supply connection with a nominal value

of 1.5 V DC; power supply voltages from 1.2 V to 1.8 V were also simulated as previous described. Bond pad 3.1 is the ground connection. Pad 4.5 is the output of capacitor sensing circuit. As a buffer circuit was laid out before this output, a low impedance load can be used for testing. Bond pads 5.1, 4.6 are for non-overlapped clock generation; pad 5.1 needs to connect to a power supply of 1.5 V for digital circuits. 4.6 is the ground for digital circuits. Two external clock signals must be correctly fed in through bond pads 5.4 and 2.5. Pad 5.4 is for the regular clock input, 30 k Hz Sine signal was used for simulation. Bond pad 2.5 is the low frequency clock input; this frequency determines the cycles of charging and discharging for capacitance sensing. This frequency may vary due to different applications. The non-overlapped clock generation circuit is described in Chapter 2.4.

7.2.2. Bandgap and PTAT Temperature Sensor Testing

The PTAT temperature circuit and bandgap reference must be tested over our temperature range of interest. For the bandgap reference, our simulations showed that its output is around 1.2 V for the temperature range from 0 to 120 $^{\circ}C$. For PTAT temperature sensor our simulation indicated linearity of the output, and at room temperature (20 $^{\circ}C$) our expected value is around 420mV. It will change slightly due to the offset caused by the fabrication variations on the resistors in the design, but the linearity will not be affected. We will conduct a calibration test with linear temperature change with 1 $^{\circ}C$ steps and accordingly record the output value from PTAT. Bond pads 3.7 and 4.9 are the power supply and ground connections.

Bond pad 2.8 is the output of bandgap reference circuit; this will be tested in the same manner as the PTAT circuit. Bond pad 3.9 is the PTAT temperature circuit's output.

7.2.3. Opamp with Biasing Circuit Testing

A constant Gm on chip biasing generation circuit provides a 10 μA current (this value may vary with temperature changes or fabrication variation). Bond pad 2.7 is the output of the constant-GM circuit; the measuring device needs to sink current to measure the output current from the constant Gm biasing circuit. Bond pad 3.8 is the input current of the Opamp; in simulation a 10 A current source was used to supply the bias current. Opamp can be tested with an external current source; bond pad 3.8 needs to be connected to this external current source. The constant Gm biasing circuit and opamp can be connected to test both together; bond pad 2.7 and 3.8 need to be connected in this test.

7.2.4. Opamp without Biasing Circuit Testing

For testing of the Opamp with an external bias, an external current source of 10 μA needs to be connected through bond pad 3.8. From the simulation, the DC gain of the opamp is around 70dB. Both AC bode plot and DC gain will be tested. In the simulation, the common mode voltage input was set to 0.75 V. Bond pads 1.5 and 1.7 are the positive and negative input nodes, respectively. Bond pad 3.3 is the single ended output of the opamp. Bond pads 2.6 and 4.8 are the ground and Vdd connections, respectively.

7.2.5. Biasing Current Circuit Testing

The constant Gm biasing circuit can be tested separately, bond pads 2.6 and 4.8 need to be set correctly; they are ground pin and Vdd power supply pin, respectively. The test structure of the Opamp without biasing shares the same Vdd and ground bond pads. In simulation, the biasing current can range from 10 to 20 μA. Bond pad 2.7 is the bias current output.

7.2.6. Bond Pad Capacitance and ESD Protection

Bond pads 1.8 and 1.9 are connected to each other without any connections to other components. They will be used to measure the capacitance of bond pads directly. Bond pads 2.2 and 2.3 are pads with ESD protections. We have implemented this structure to provide direct testing of the pad capacitance with ESD structures. In addition, we can use this structure to determine the maximum discharge voltage the ESD structures can handle.

7.2.7. Heater Connections

Bond pads 2.1 and 2.9 are the two terminals of the serpentine resistor. The resistive heating of this structure will be tested using the PTAT circuit after we have completed its testing. We will apply a voltage to one terminal and ground to the other. This will allow us to determine the heat generated by a specific input. However, for operation the resistor should be used in a feedback loop with the PTAT circuit.

CHAPTER 8

SUMMARY

8.1. Capacitance Sensor Chips

Two chips were taped out in December 2008. They included two designs of capacitance sensors, a PTAT temperature sensing circuit and a bandgap reference. The fabrication technology is provided by MIT Lincoln Lab. Each chip is fabricated by stacking and bonding three wafers. Each wafer is fabricated in the IBM 0.15 μm SOI technology. MIT will assemble the three wafers and add wafer-to-wafe vias to make connections between different layers. The chip were taped out in this 3D 0.15 μm SOI technology. We initially expected to receive the wafers in December 2009. In November 2009, MIT Lincoln Laboratory issued the problems they uncovered during their single tier testing. In order to deliver fully integrated 3D chips, they need their all process monitors behave as expected. The completion of 3D chips will be delayed to early 2010. (Describe the problem and new expected timeline.) The capacitance sensors utilized switched-cap circuits and had discrete time responses. The principle the capacitance sensors are based on is charging and discharging the capacitors, which are the sensing and reference capacitors. Inside the switched-cap circuit, the clock signals controlled the charge integrations on the feedback capacitors. This mechanism allows the circuit to detect capacitance changes from several fF to a few pF by adjusting the number of iterations. Capacitance is converted to a voltage output. From simulations, the estimated response time of the capacitance sensors is within 1 mS. PTAT temperature sensing circuit is capable of detecting a temperature ranging from 0 to 100 degree Cel-

sius. The bandgap reference has been verified to work with a temperature range from 0 to 100 degree Celsius with sub-1 mV voltage change. Both the PTAT circuit and bandgap reference were taped out on the same chip as capacitance sensor. Several additional test structures were also tapped out. They included bipolar transistor structures, current mirrors, transistors, etc. Those test structures will be used to collect information on this specific technology. Since this is a new technology many of these structures are still experimental, and models for their behavior are not available. We will utilize our test structures to aid MIT Lincoln Labs in creating models for these devices, especially the BJTs. In addition, we will use the test results to further understand the operation of our circuits.

8.2. Further Work

A circuit using discrete components was made on PCB as described in Chapter 4. It included 3 gain stages and a high order low pass filter. It has been tested to work with cardiac cells' action potential measurements. A phase detector circuit has been designed, and it will serve as a tool to detect the delay in the time domain from the signal propagation measured at two or more locations in a microelectrode array. A second order sigma delta ADC and a first order sigma delta DAC have been implemented on simulation tools. All these circuits will be implemented in another IC that will be taped out early 2010.

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