

# An ARM backend for the stage2 zig compiler

Joachim Schmidt

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# @This()

► Joachim Schmidt

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- ▶ Joachim Schmidt
- ▶ Technische Universität Darmstadt

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- ▶ Technische Universität Darmstadt
- ▶ Fun fact about me: I like pizza

# Overview

Compiler backends and stage2

ARM architecture

Live demo on a Raspberry Pi

Q & A

# What is a compiler?

# Compiling Hello World in zig

# Where did the zig compiler come from?



# Bootstrapping

# The current plan

# Backends

# von Neumann architecture

# CISC

```
export fn foo() u32 {      ...
    var x: u32 = 42;      mov     dword ptr [rbp - 8], 42
    var y: u32 = 23;      mov     dword ptr [rbp - 12], 23
    return x + y;         mov     eax, dword ptr [rbp - 8]
}                          add     eax, dword ptr [rbp - 12]
                          ...
```

<https://zig.godbolt.org/z/qoMfEK>

# RISC

```
...  
movw    r0, #42  
export fn foo() u32 {  
    var x: u32 = 42;    movw    r0, #23  
    var y: u32 = 23;    str      r0, [sp, #8]  
    return x + y;       str      r0, [sp, #4]  
}                   ldr      r0, [sp, #8]  
                   ldr      r1, [sp, #4]  
                   adds     r0, r0, r1  
...
```

<https://zig.godbolt.org/z/Mee9ro>

# ARM instruction set

- ▶ Data Processing

```
add r0, r1, #2
```

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- ▶ Memory

```
ldr r0, [sp, #4]
```



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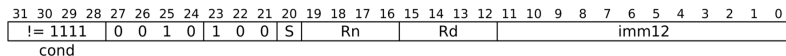
- ▶ Branching

```
b label
```

```
bx lr
```

# A brief look at the add instruction

add r0, r1, #2



**ADD (S == 0 && Rn != 11x1)**

ADD{<c>}{<q>} {<Rd>}, {<Rn>}, #<const>

Figure: Encoding of add; Source: [2]

## Condition codes

```
export fn isAnswer(x: u32) u32 {  
    return if (x == 42) 32  
           else 12;  
}  
  
mov     r1, #12  
cmp     r0, #42  
movweq  r1, #32  
mov     r0, r1  
bx      lr
```

<https://zig.godbolt.org/z/q5rP8e>

# Live demo



Figure: Source: [1]

# Q & A

- ▶ GitHub: <https://github.com/joachimschmidt557>
- ▶ Discord: joachim.schmidt557#6869
- ▶ Matrix: @joachimschmidt557:matrix.org

# References



<https://www.flickr.com/photos/rexroof/3802694376/>



[https://static.docs.arm.com/ddi0597/h/ISA\\_AAArch32\\_xml\\_v86A-2020-06.pdf](https://static.docs.arm.com/ddi0597/h/ISA_AAArch32_xml_v86A-2020-06.pdf)