1 Design of a Latch

After building the circuit and launching the simulation tool we get the following graph :

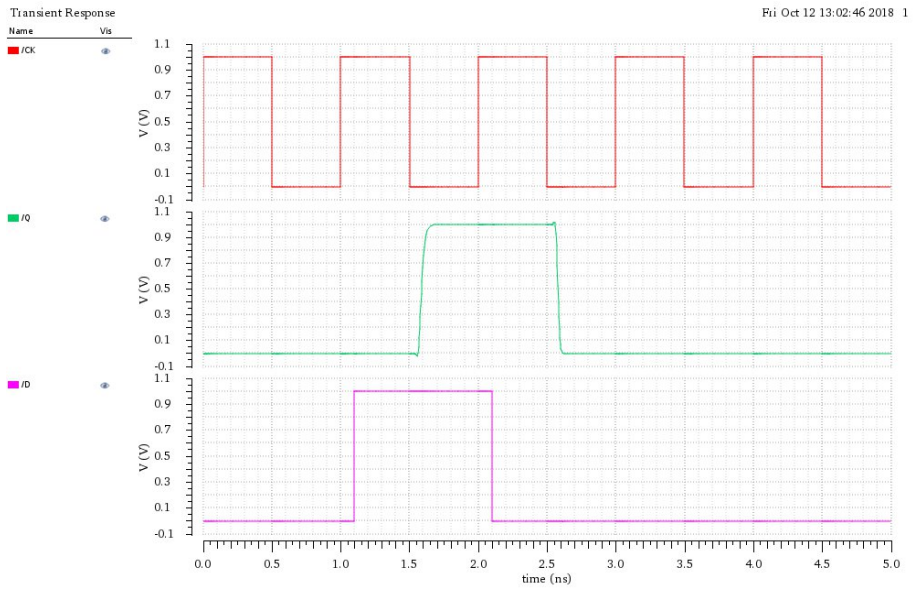

FIGURE 1 – Output graph of the latch

We can observe that in fact as expected the latch is transparent on the lower part of the clock and opaque on the high part of the clock. Thus on the first clock cycle the output stays at 0V. During the second clock cycle, the latch input goes high. During the first half of the clock the latch is still opaque and thus the output stays low and in the second part of the clock cycle, the latch becomes transparent and thus the output is pulled high. During the third clock cycle, the input goes low but as in the first half of the clock cycle the latch is opaque, the output remains high and then drops at during the second half period. After that, as the input doesn't change anymore, the output doesn't aswell.

2 Design of a Flip Flop

2.1 Functioning of the Flip Flop

During the first half of the clock, the firstlatch of the flip flop is transparent as it can be seen it the following schematic.

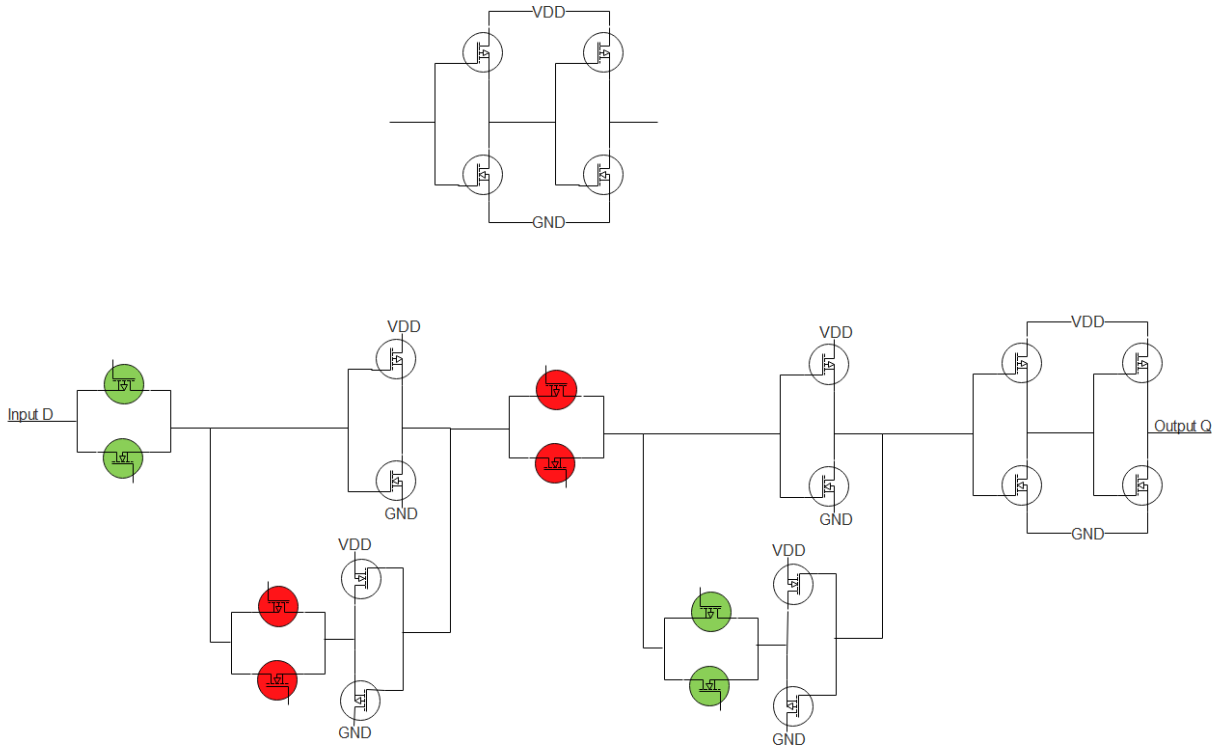

FIGURE 2 – First half of the clock cycle

During this half of the clock, the second flip flop is in it's opaque phase and thus the input is not directly propagated to the output. During the second clock half, the first latch becomes opaque and thus no further input is taken into account but the previous input can be propagated to the second latch. Durind this half cycle the second latch is transparent and thus the output is set to the value that was before in the first latch.

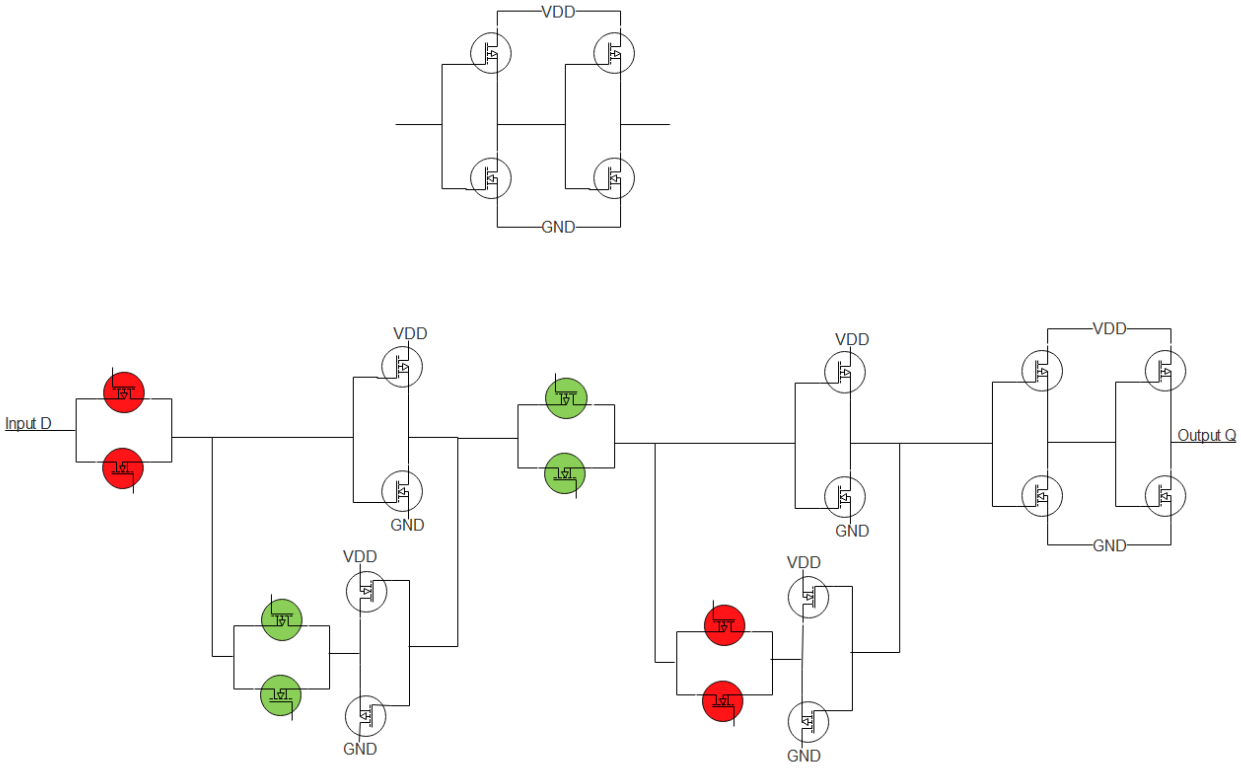

FIGURE 3 – Second half of the clock period

2.2 Simulation

After building the circuit on Cadence and simulating we get the following plot :

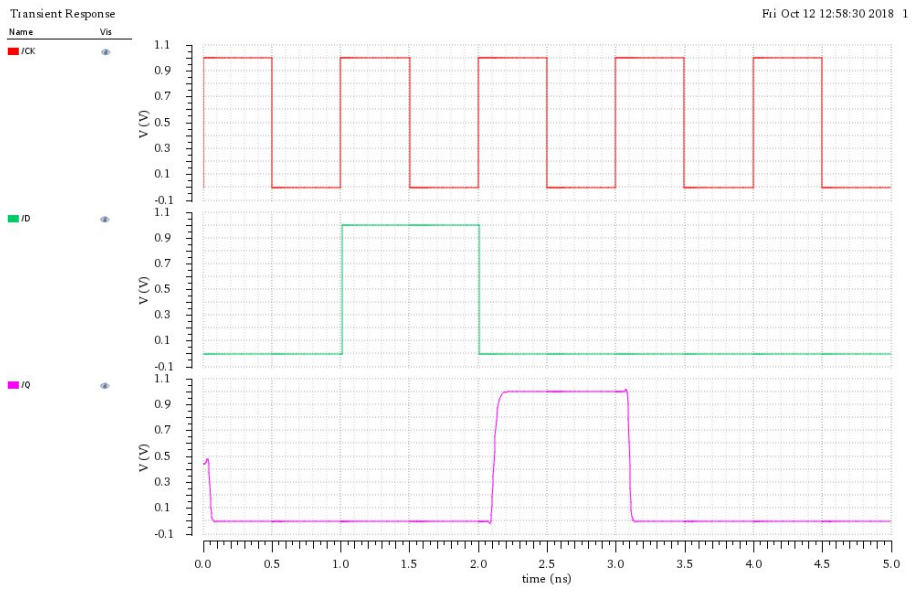

FIGURE 4 – Output graph of the Flip Flop

During the first clock cycle, the inputs stays low and thus nothing happens at the output. During the second clock cycle, the output still doesn't change but on the second half of the second clock cycle, the first latch becomes

transparent and thus it's output changes goes high. During this time, the second latch is opaque and thus the output stays low. During the first half of the third clock cycle, the first latch becomes opaque again and thus it's output stays at 1 and the second latch becomes transparent and thus the output finally goes high. During the second half of the third clock cycle, the first latch becomes transparent again and thus isn't output changes to 0 but the second latch is opaque, thus it's output stays high. Finally, during the fourth clock cycle, everything returns to zero as the previously stored 0 in the first latch is transmitted to the second latch.

The main difference between the Flip Flop and the latch is that the output will only change on the rising edge of the clock and never during clock cycles as it could happen during the transparent phase of a latch. This "accurateness" is paid for by the fact that we have to wait a lock cycle before the input reaches the output.