Introducción al Diseño Lógico (E0301)

Ingeniería en Computación

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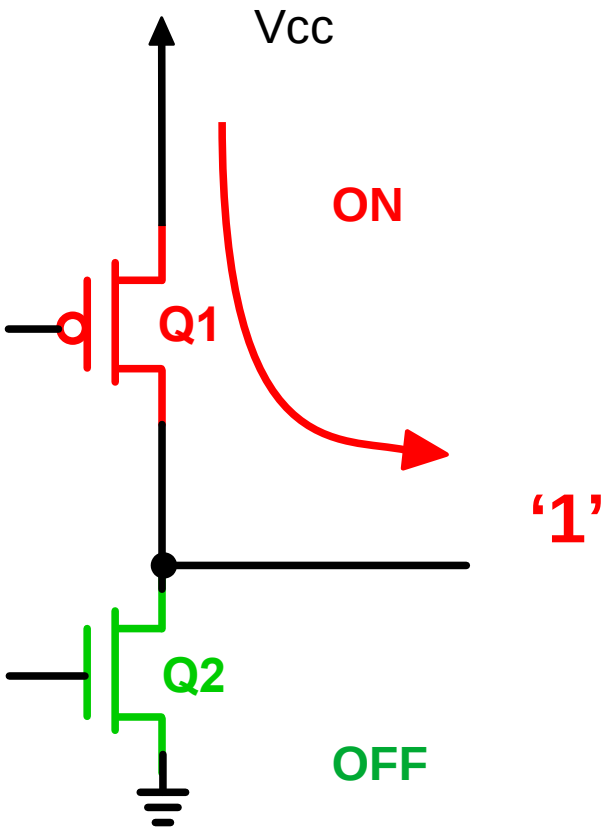
Clase 14 curso 2023

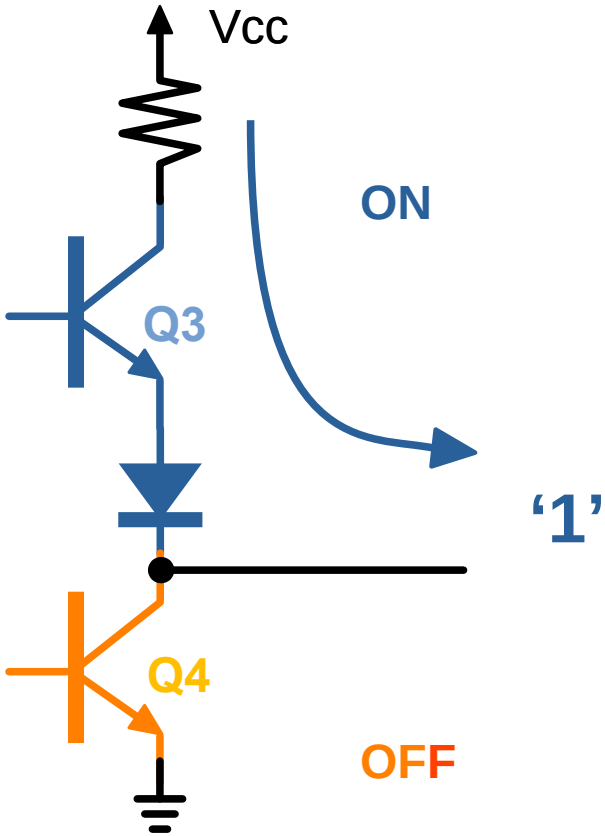
Interconexión de Dispositivos.

- Temas a tratar
  - Interconexión de salidas en CMOS y TTL
    - Totem Pole
    - Open collector
    - Open Drain
    - Three State (TRISTATE®)
  - Buses
    - I2C
    - Con Multiplexores
    - Three State
  - Celda de Memoria

Etapa de Salida “Totem Pole”

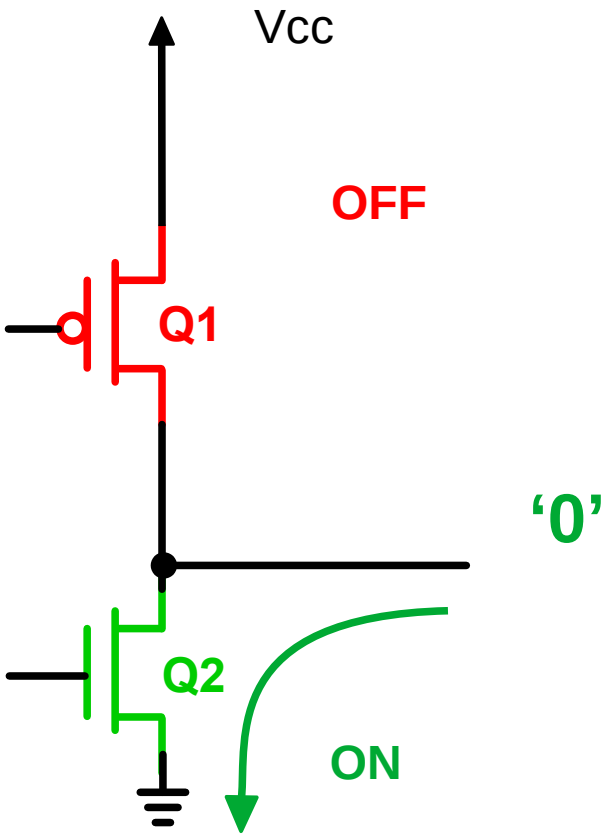


CMOS

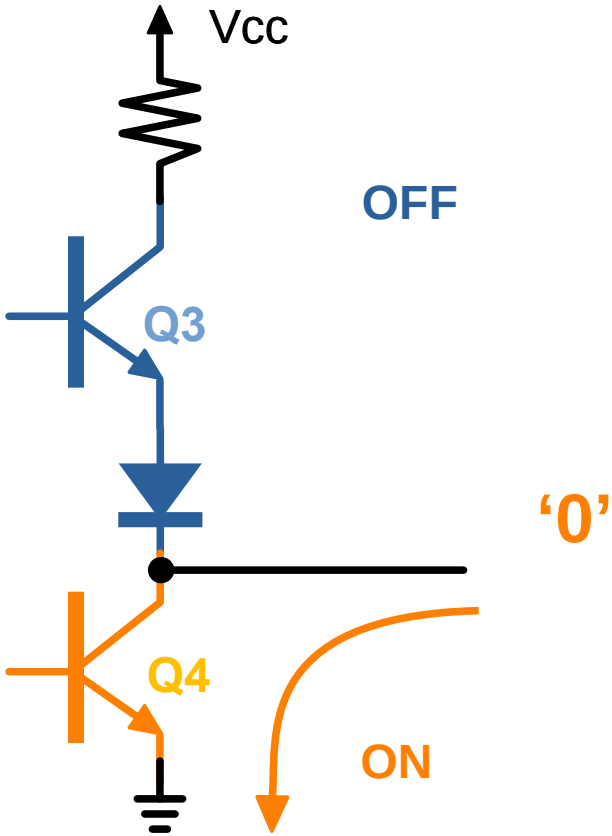


BIPOLAR

Etapa de Salida “Totem Pole”



CMOS



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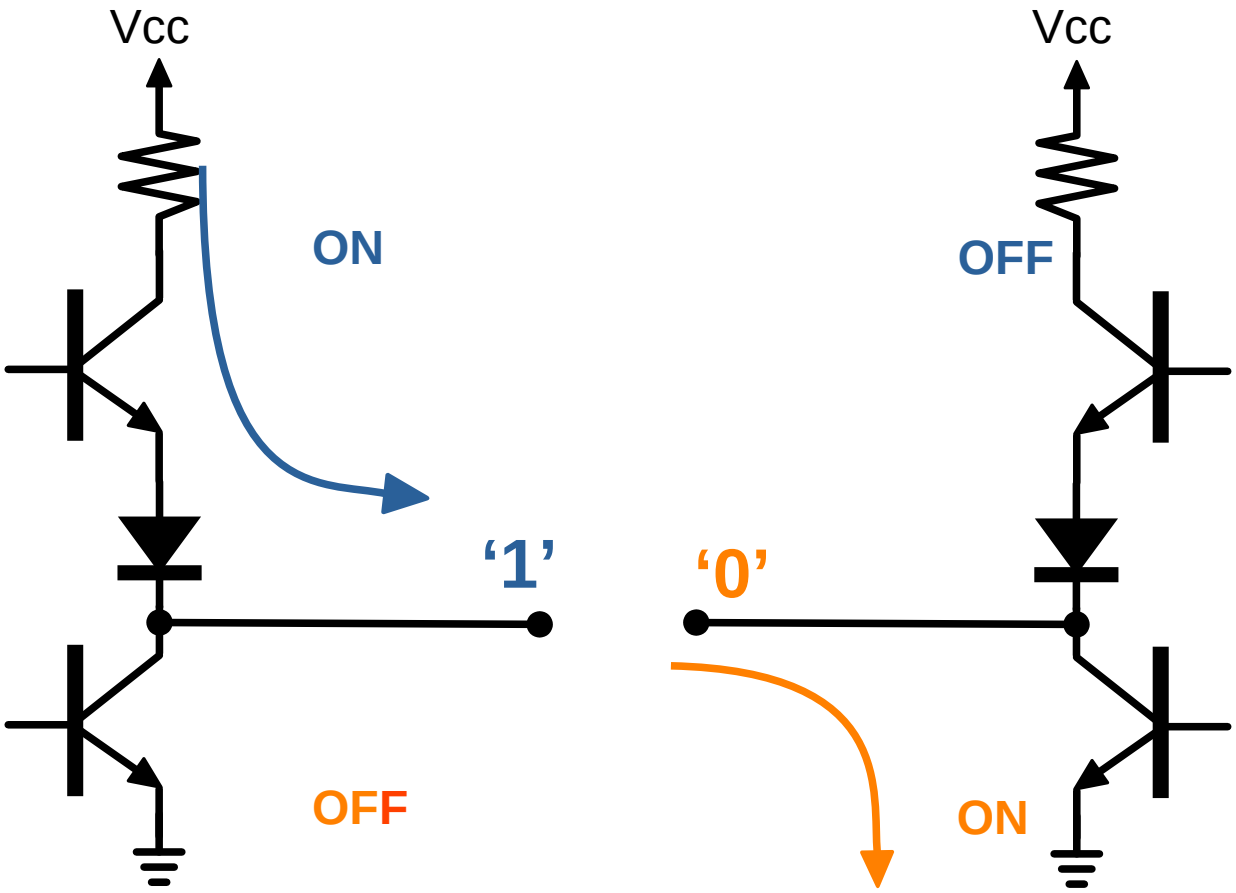
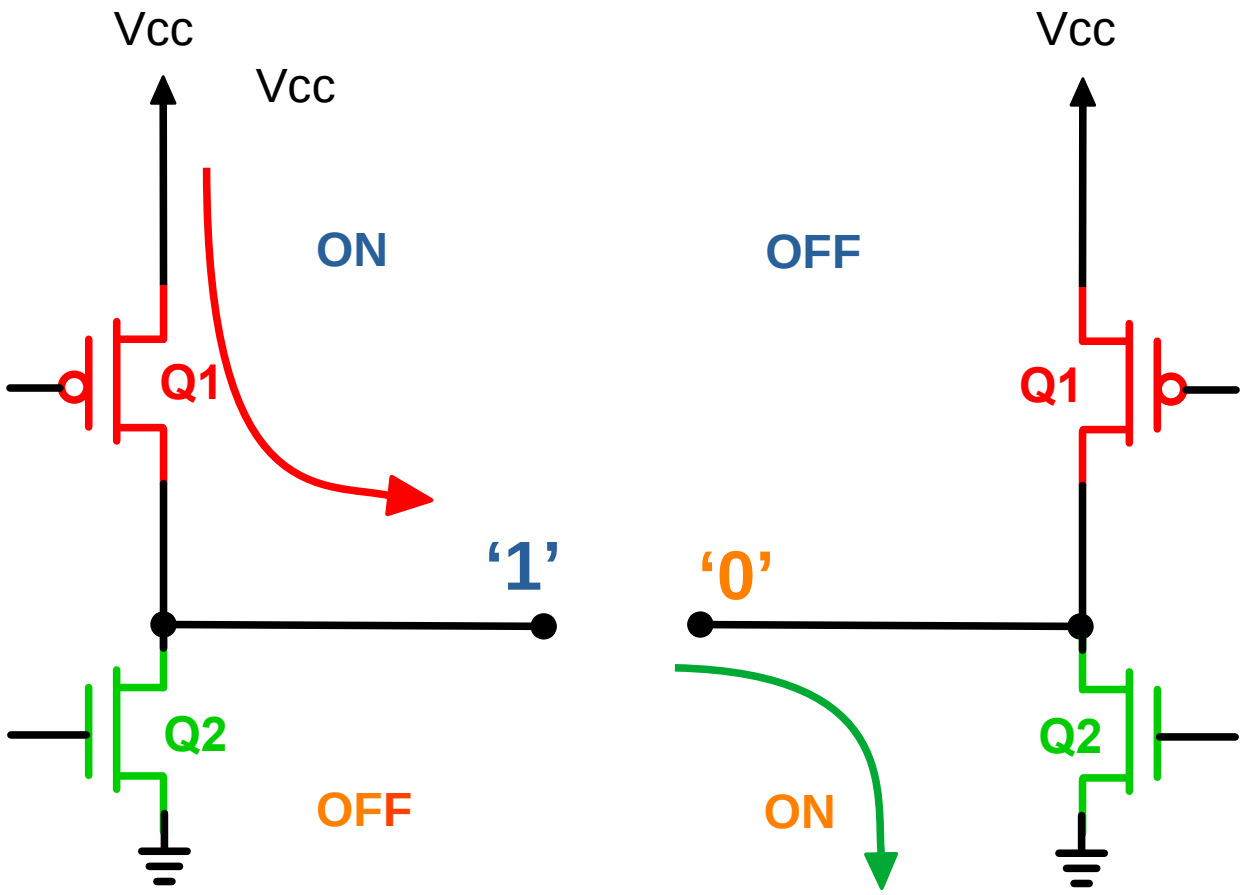
Etapa de Salida “Totem Pole”



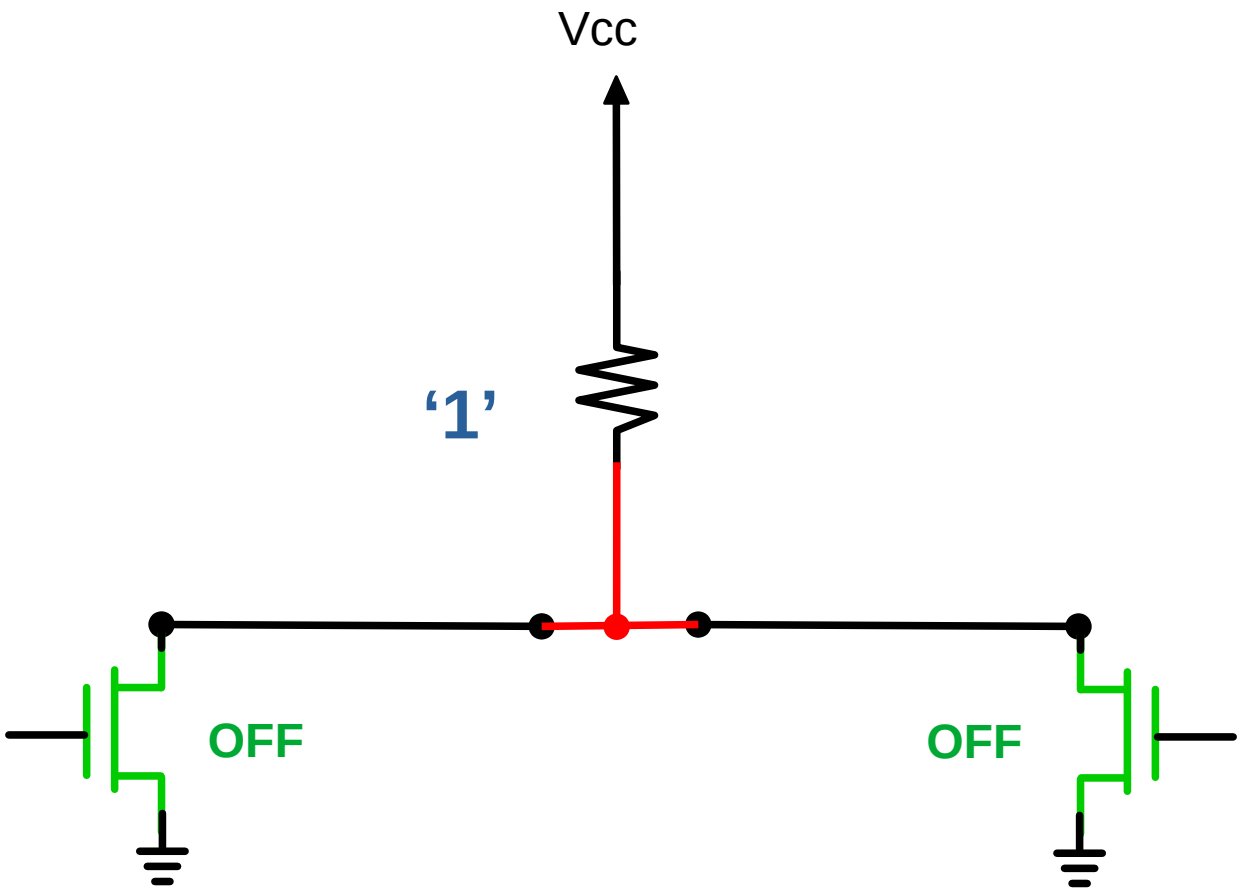
Que pasa si conectamos las salidas entre sí?

Etapa de Salida “Totem Pole”

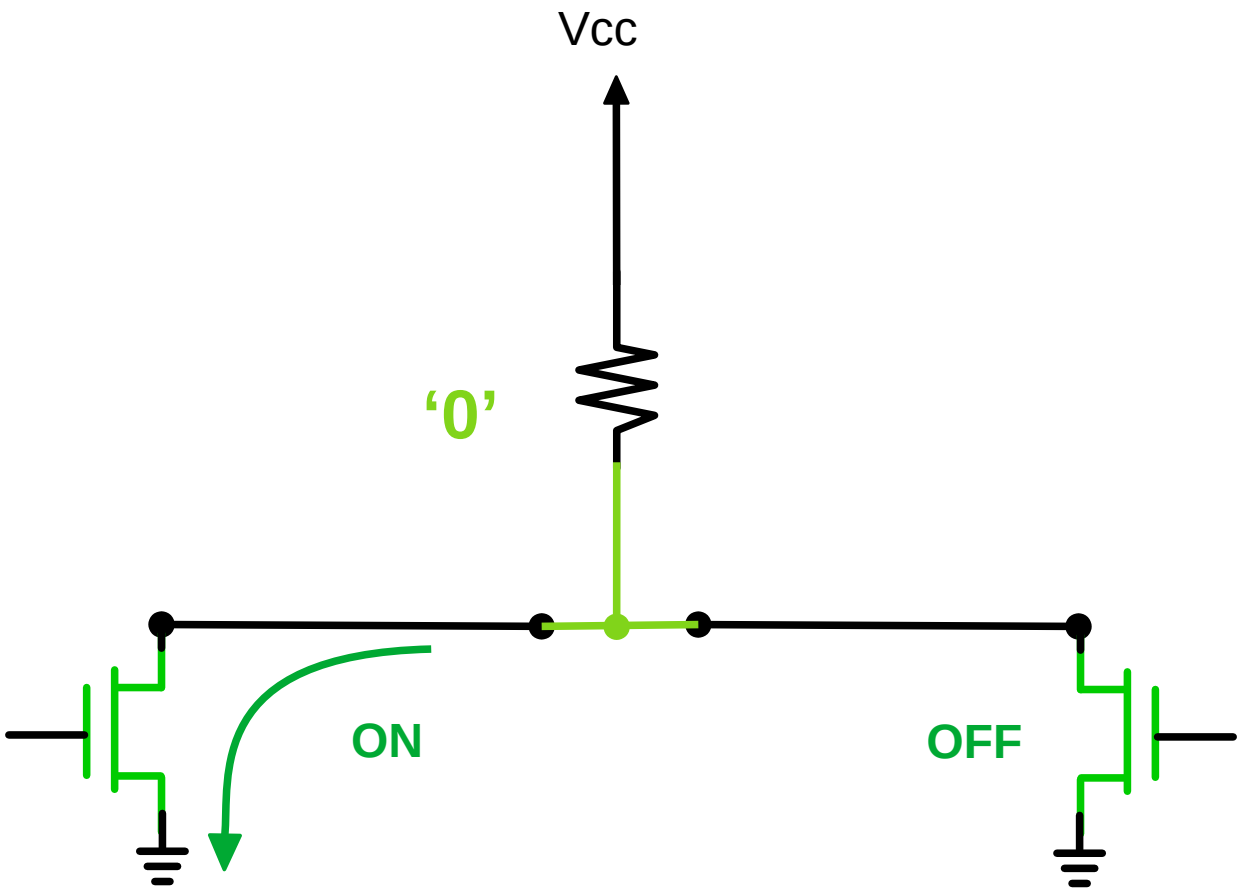


Que pasa si conectamos las salidas entre sí?

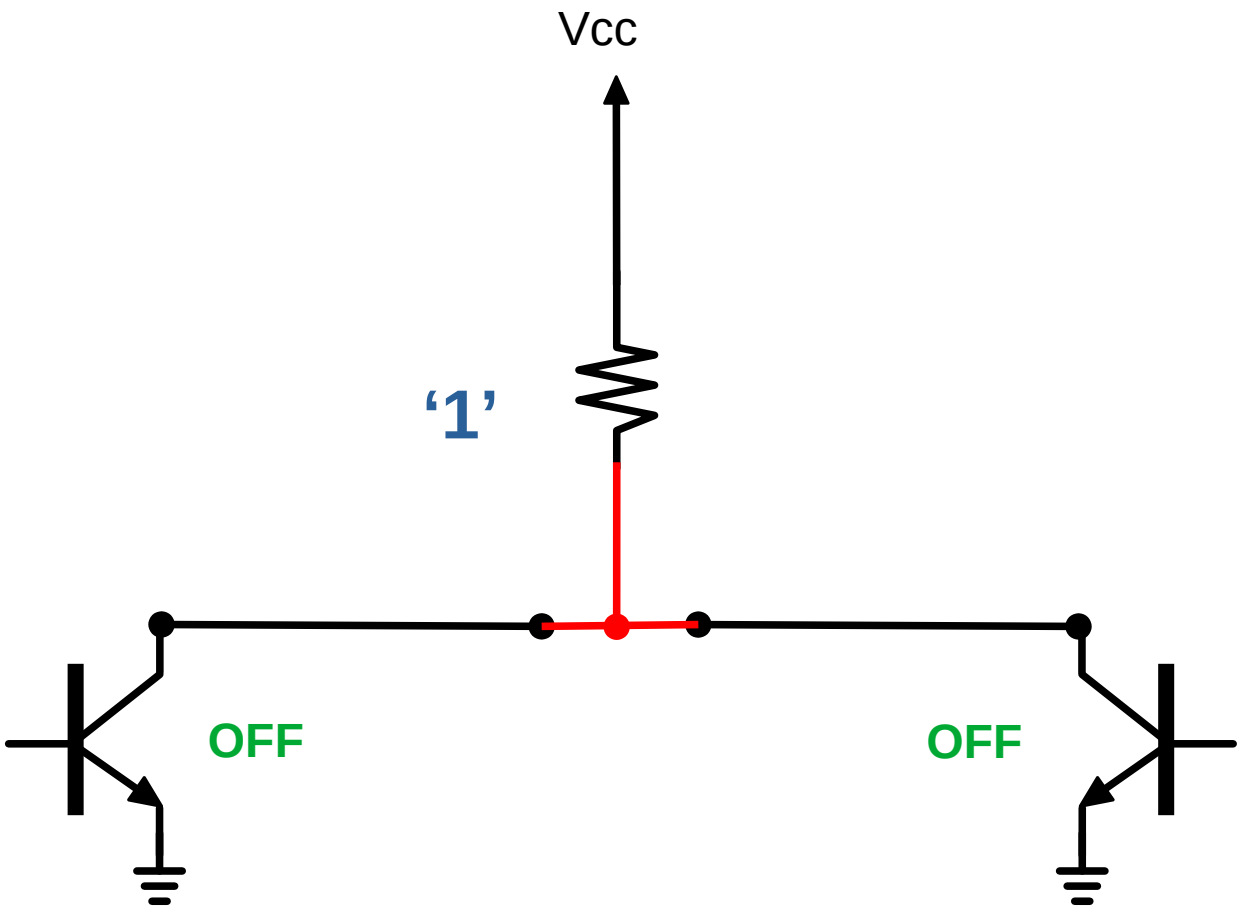
Etapa de Salida “Open Drain”



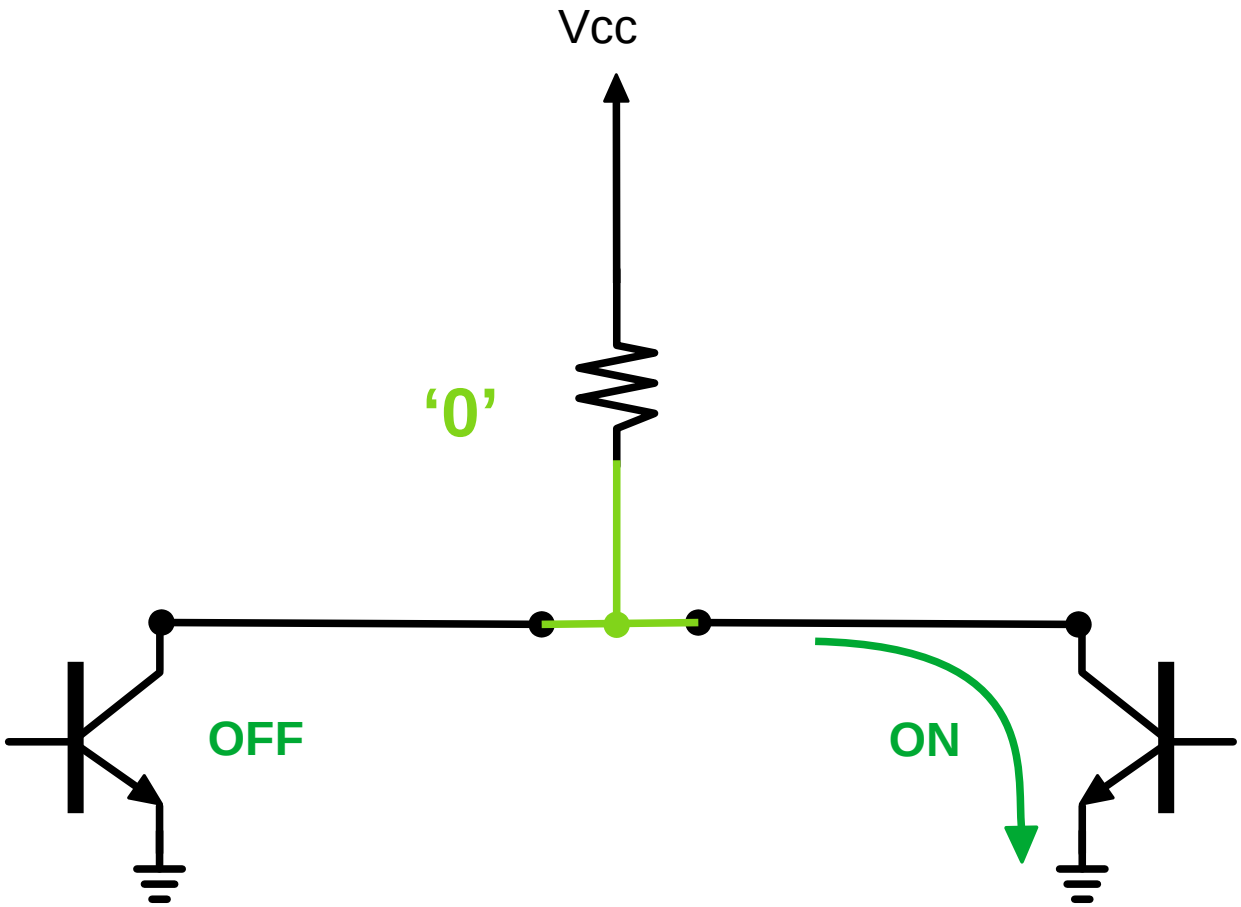
Etapa de Salida “Open Drain”



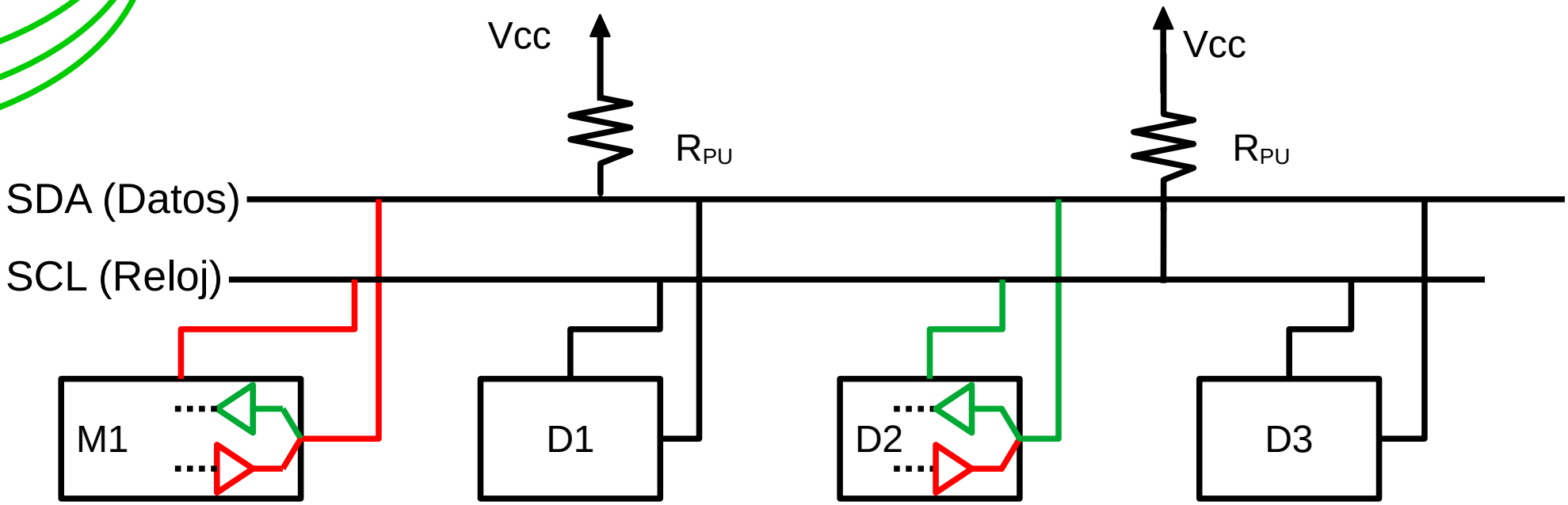
Etapa de Salida “Open Collector”



Etapa de Salida “Open Collector”



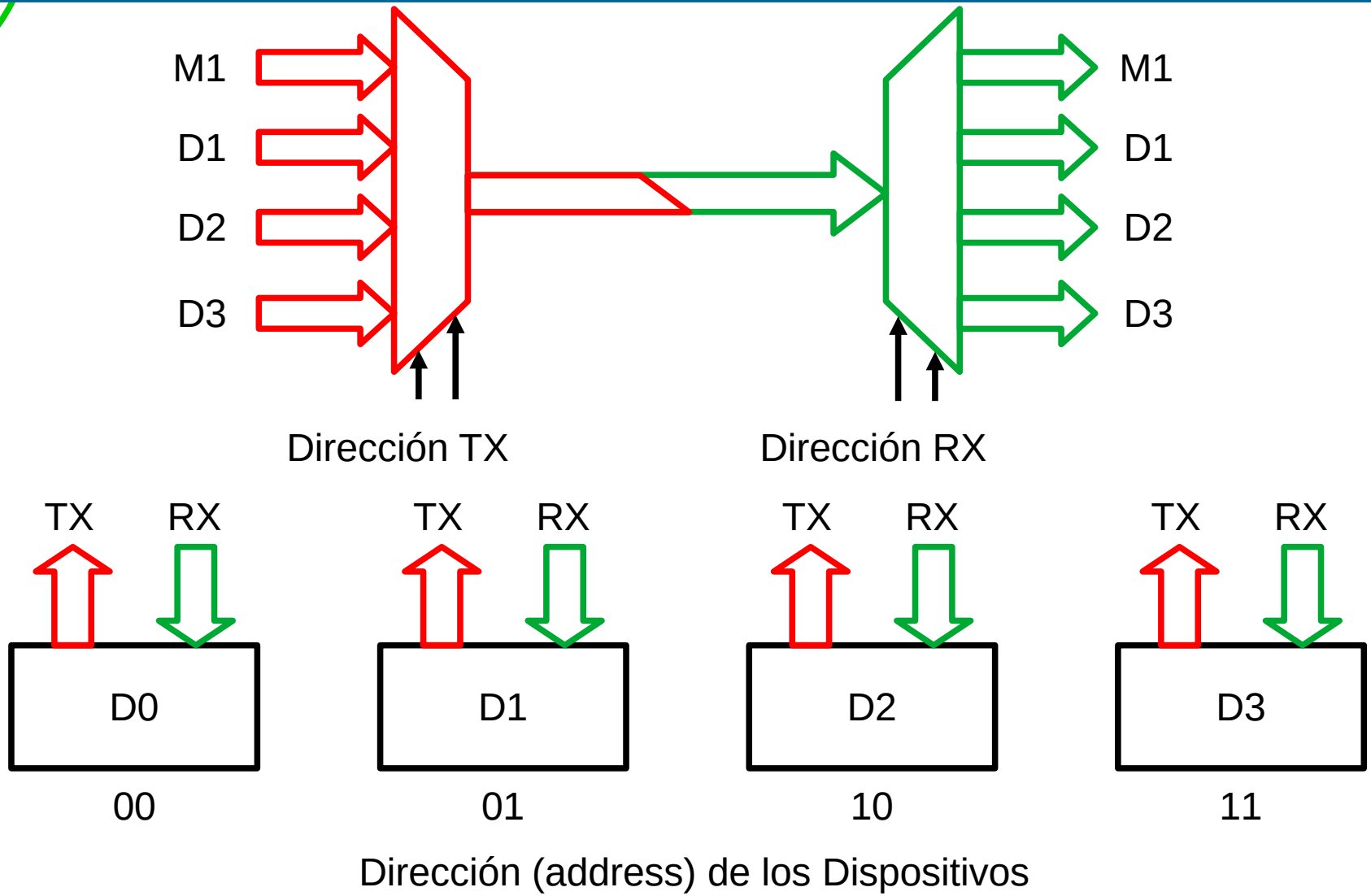
Aplicación: Bus I2C



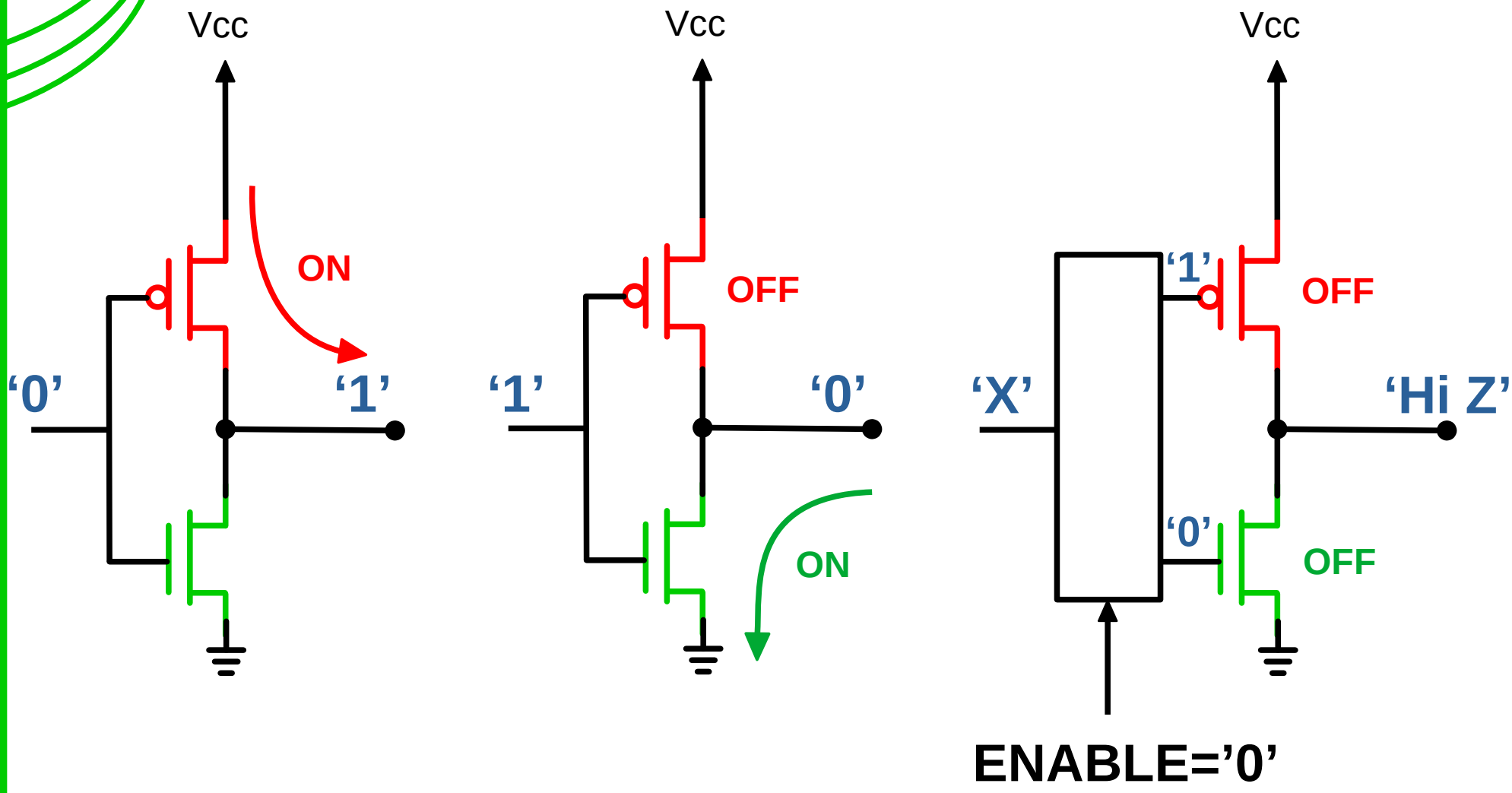
El BUS I2C es Open Collector/ Open Drain

- R_{PU} mantiene la tensión en Vcc. (ALTO)
- Cuando se activa TX en cualquier dispositivo, llevan la tensión a BAJO.
- Los cambios en SDA, se intepretan como datos si SCL esta en bajo o como inicio o fin de transmisión si SCL está en ALTO

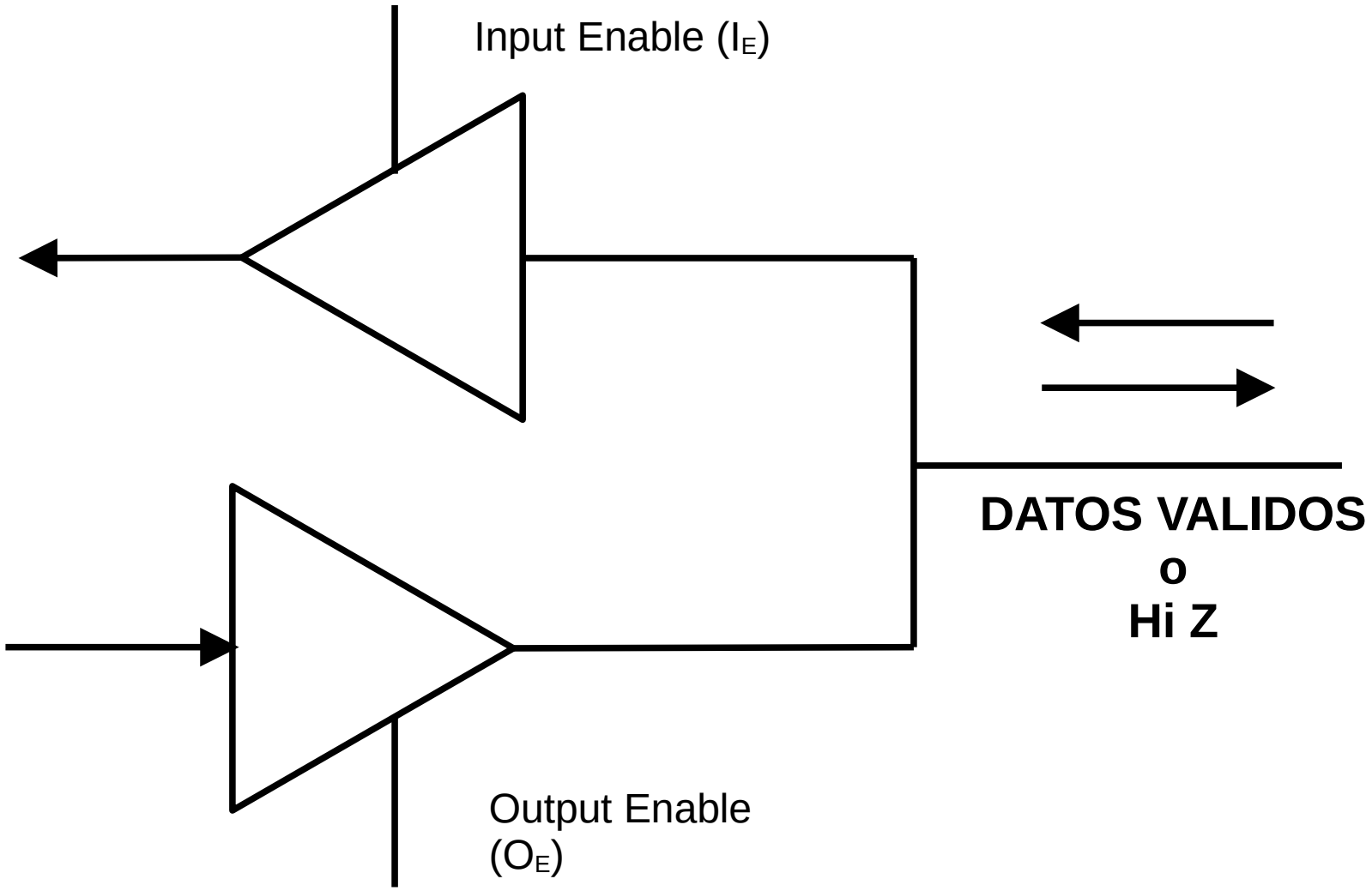
Bus basado en MUX/DEMUX



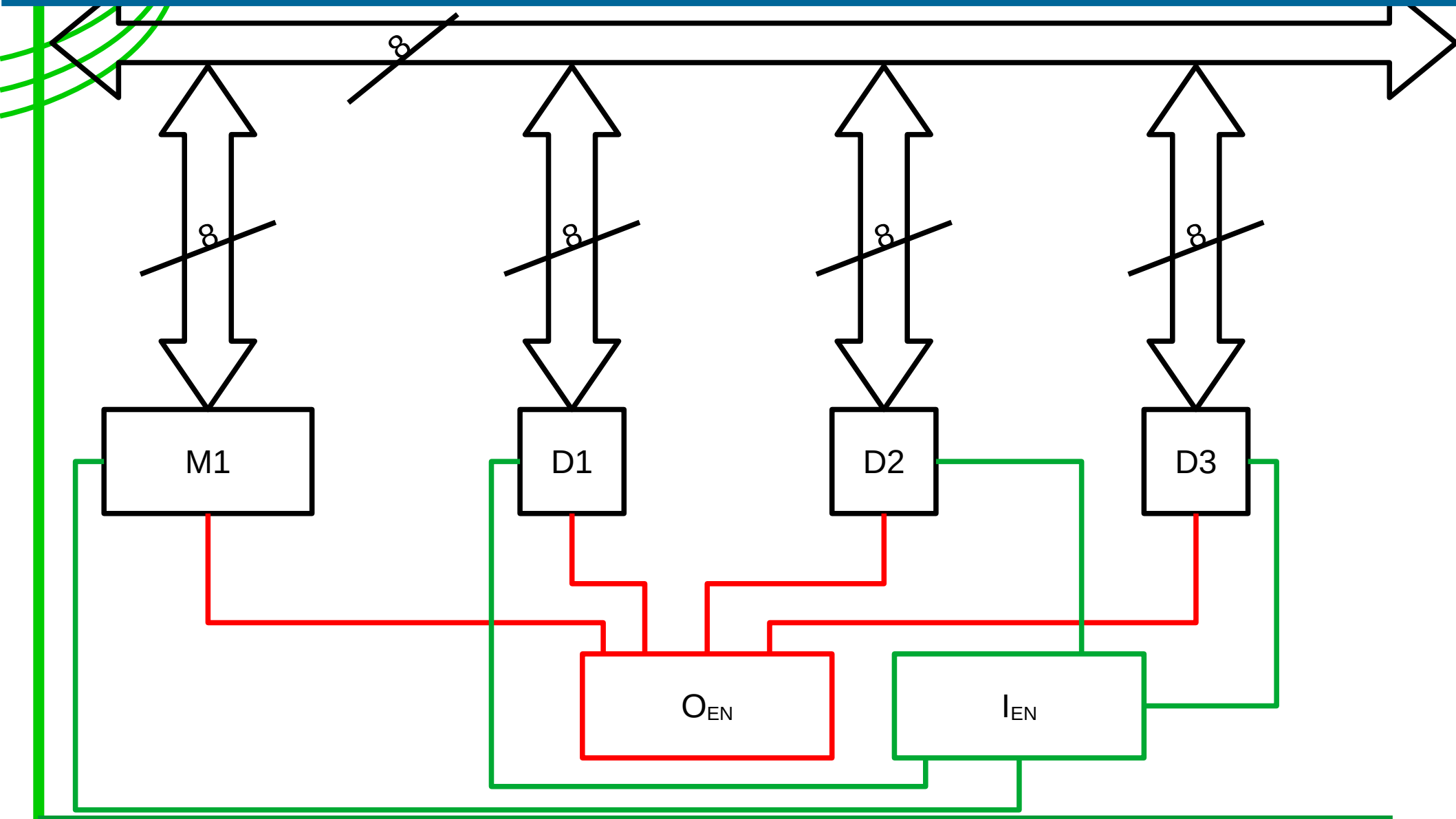
Etapa de Salida “Three -State”



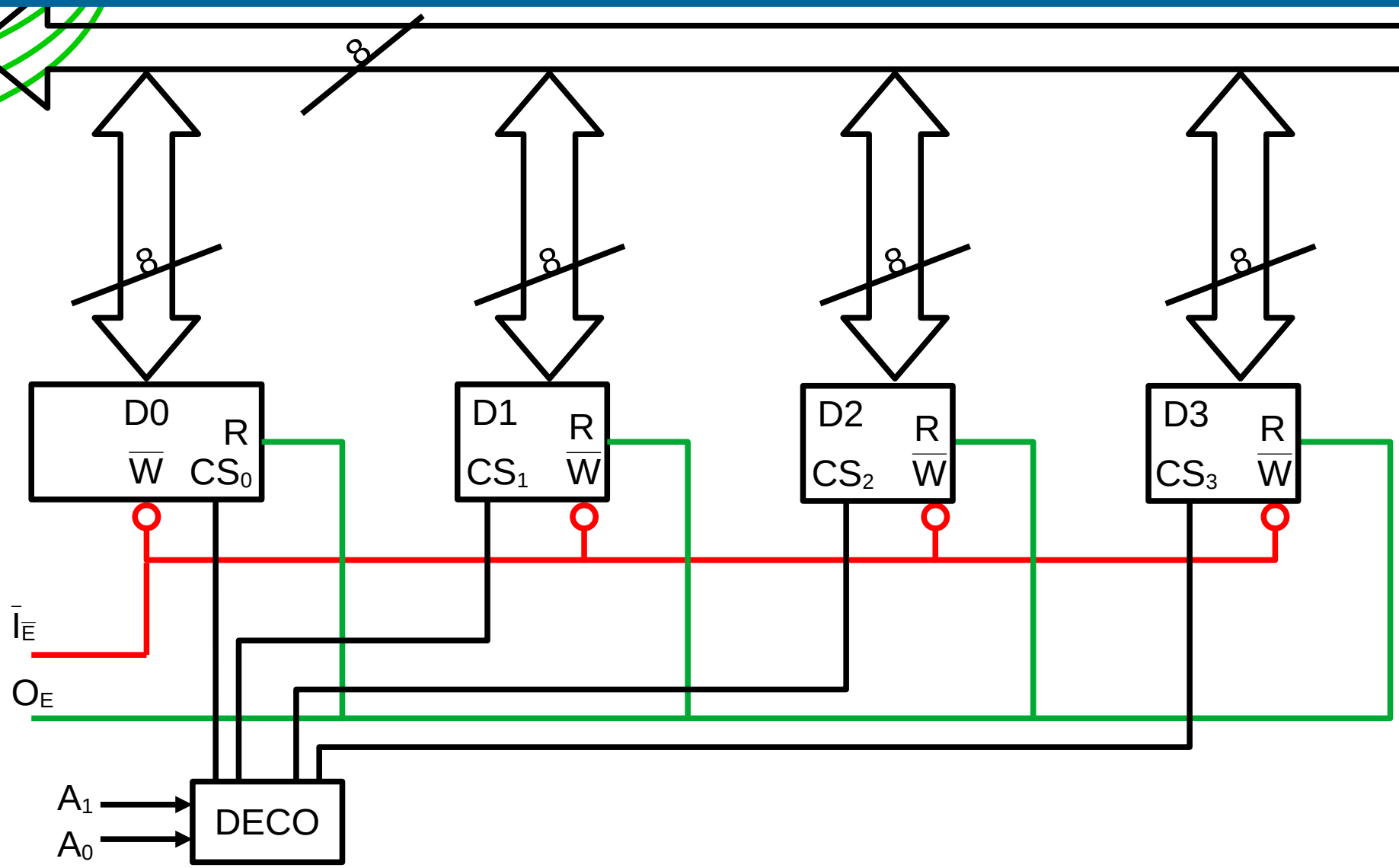
Bus bidireccional usando 3-STATE



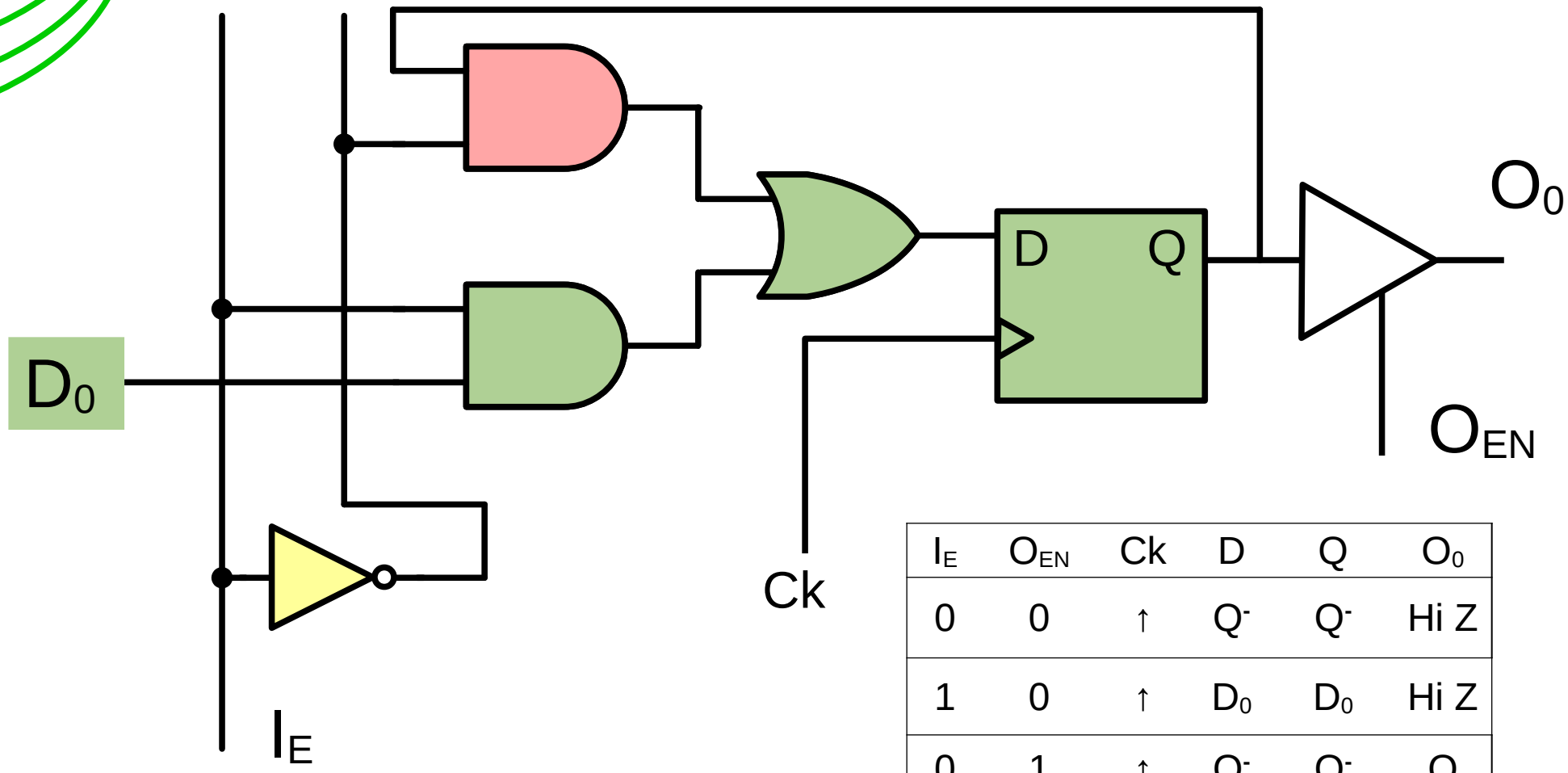
Aplicación: Bus Tristate



Aplicación: Bus Tristate



Celda Básica de Memoria



I_E	O_{EN}	Ck	D	Q	O_0
0	0	↑	Q^-	Q^-	Hi Z
1	0	↑	D_0	D_0	Hi Z
0	1	↑	Q^-	Q^-	Q
1	1	↑	D_0	D_0	Q