

UNIVERSIDADE FEDERAL DA PARAÍBA

INTRODUÇÃO À MICROELETRÔNICA

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## Atividade 5

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*Aluno:*  
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20180027213

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## 1 Inversor Tristate

Design:

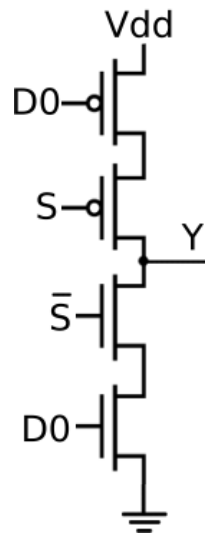


Figura 1: Diagrama esquemático em nível de transistores do inversor tristate.

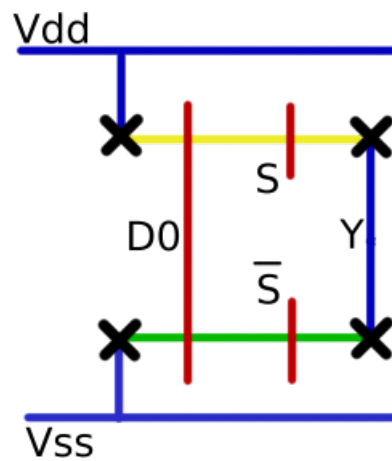


Figura 2: Diagrama de palitos do inversor tristate.

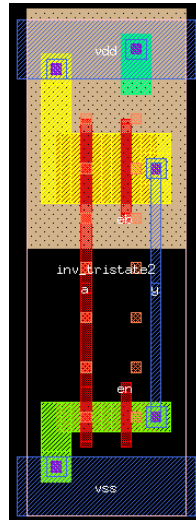


Figura 3: Layout físico do inversor tristate.

**Teste:**

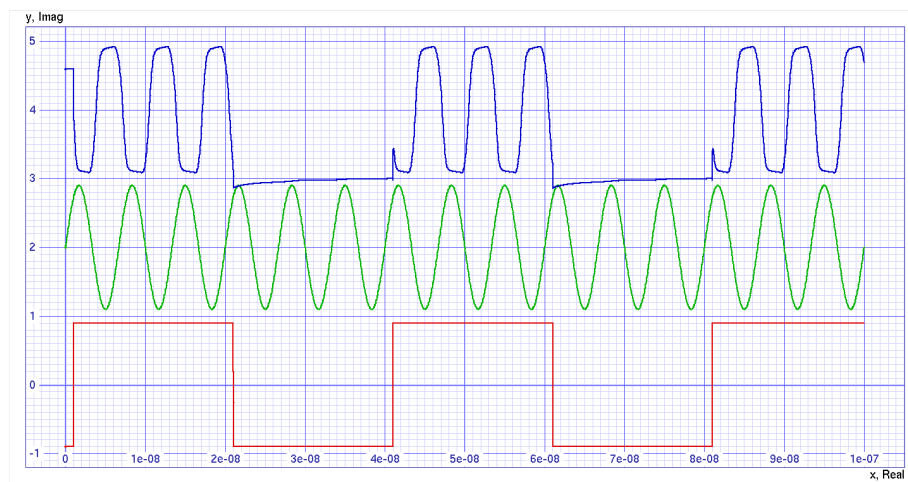


Figura 4: Simulação do funcionamento do inversor tristate.

## 2 Mux Inversor 2:1

Design:

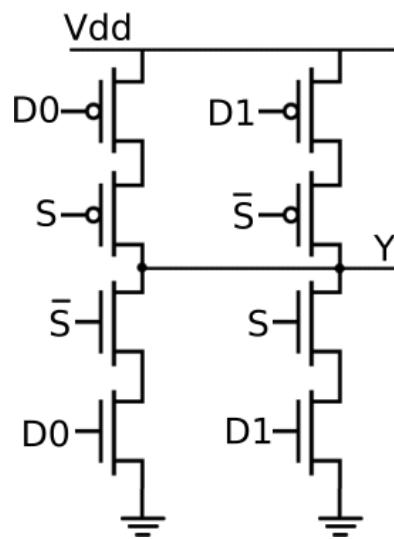


Figura 5: Diagrama esquemático em nível de transistores do mux.

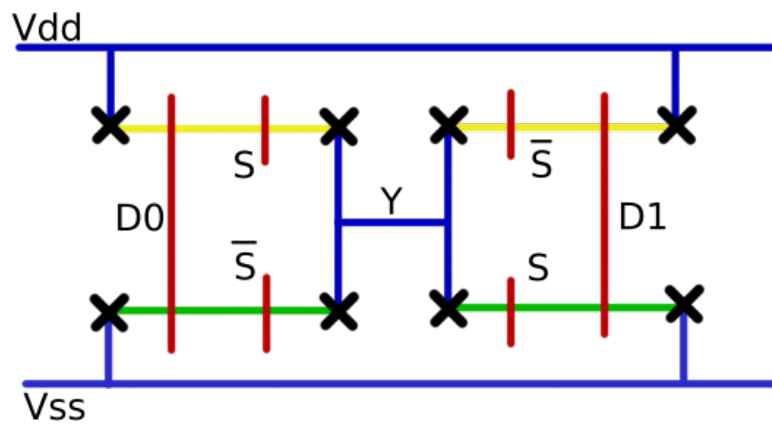


Figura 6: Diagrama de palitos do mux.

## Atividade 5

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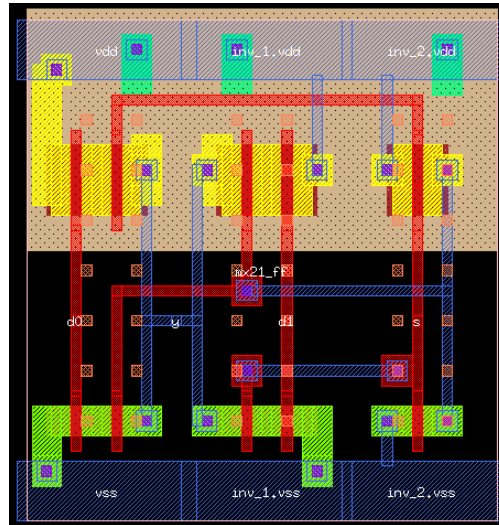


Figura 7: Layout físico do mux.

Teste:

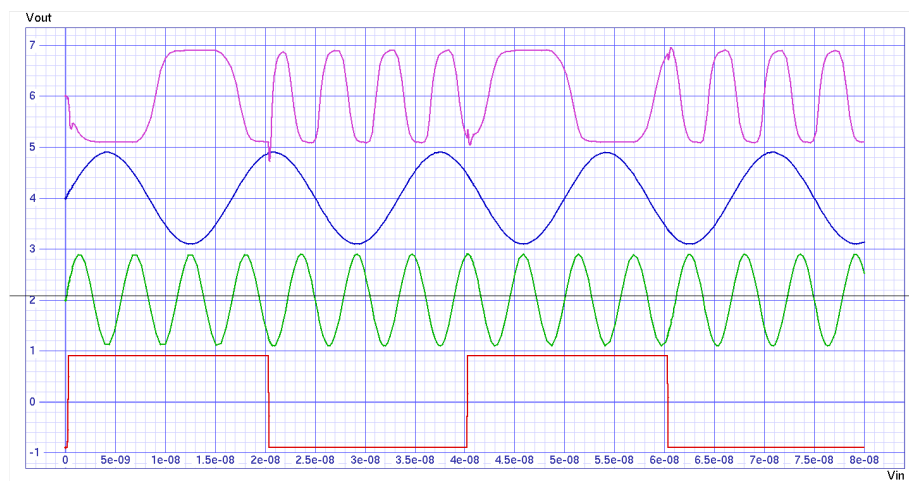


Figura 8: Simulação do funcionamento do mux.