DMCS

Computer Aided Design of Electronic Circuits

REPORT 1

EXERCISE 1 – RC CIRCUIT

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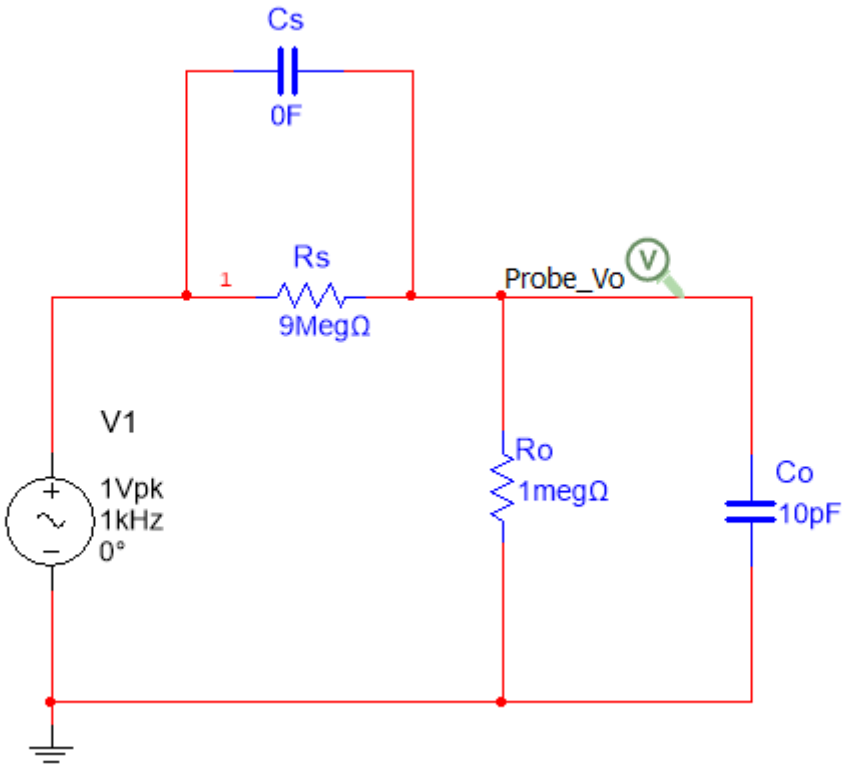
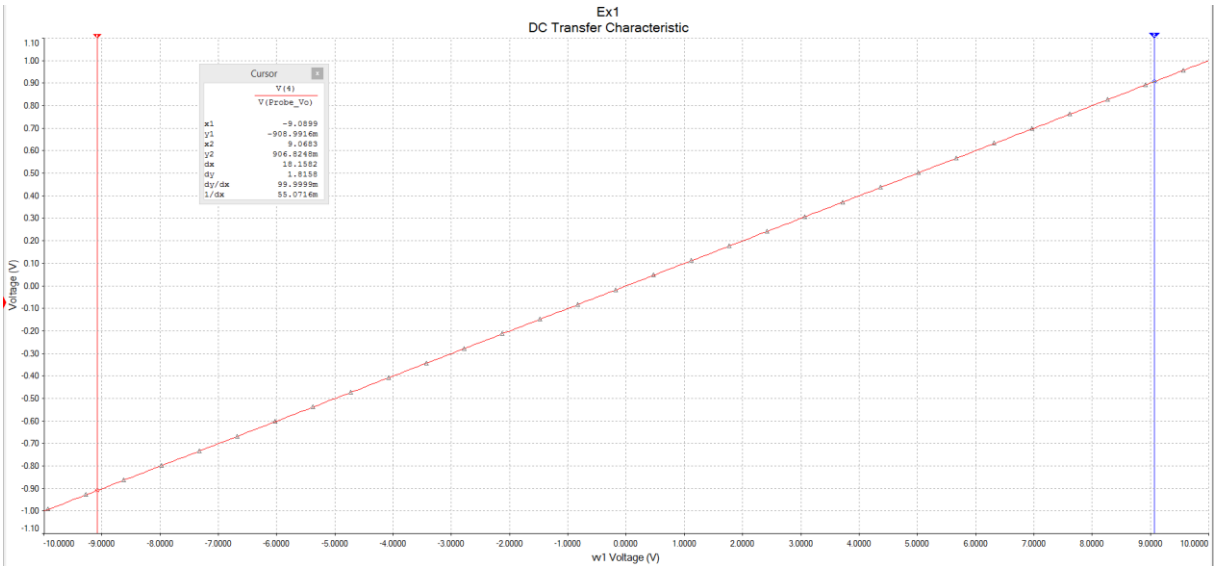


Plot 1. Circuit scheme.

DC ANALYSIS



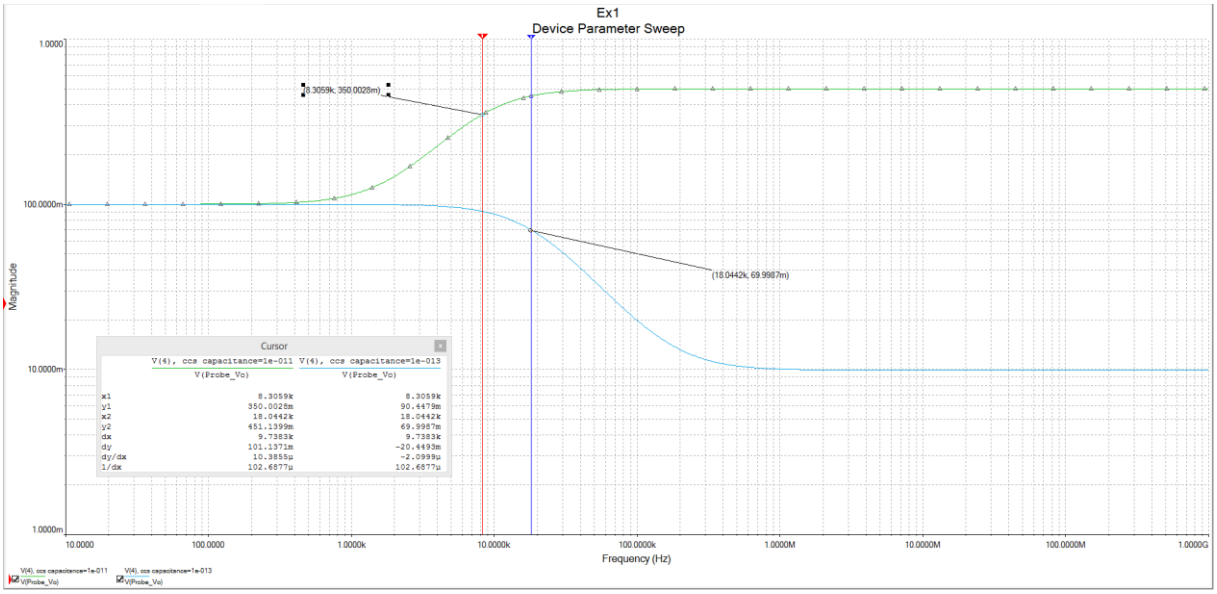
Plot 2. V_{out} as a function of V_{in}.

Voltage gain was determined graphically from the plot using cursors.

$V_{gain}=V_{out}/V_{in}$

V_{gain}=99.999m therefore V_{gain}=0.1

AC ANALYSIS



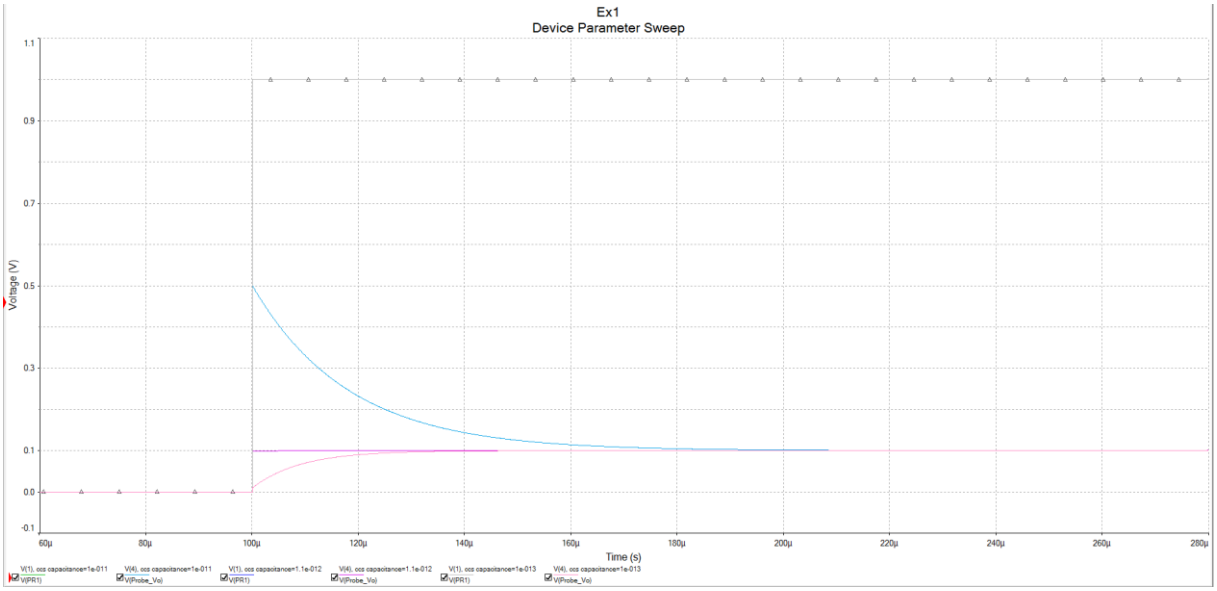
Plot 3. Ac magnitude analysis for both Cs=0.1 pF and Cs=10pF.

Capacitance Cs has an impact on magnitude analysis. The biggest Cs, the smallest cutoff frequency.

The decrease of the signal voltage to its halt value is at the -3dB and thus it specifies cutoff frequency F_{cut} that is:

0.707*100mV=70,7mV
$F_{cut=}$ 18 kHz for circuit with Cs=0.1pF

0.707*500mV=353,3mV
$F_{cut=}$8.4 kHz for circuit with Cs=10pF



Plot 4.Flat characteristics of V_{out} vs. time.

Depending on Cs value the circuit characteristic might change from low pass to high pass filter. Having exact value of Cs, the characteristic will be flat.

Cs*Rs=Co*Ro, therefore Cs= Co*Ro/Rs

Cs= 10pF*1M Ω / 9MΩ
Cs=1,1pF

Having Cs=1,1pF the characteristic will be flat.

PROJECT II

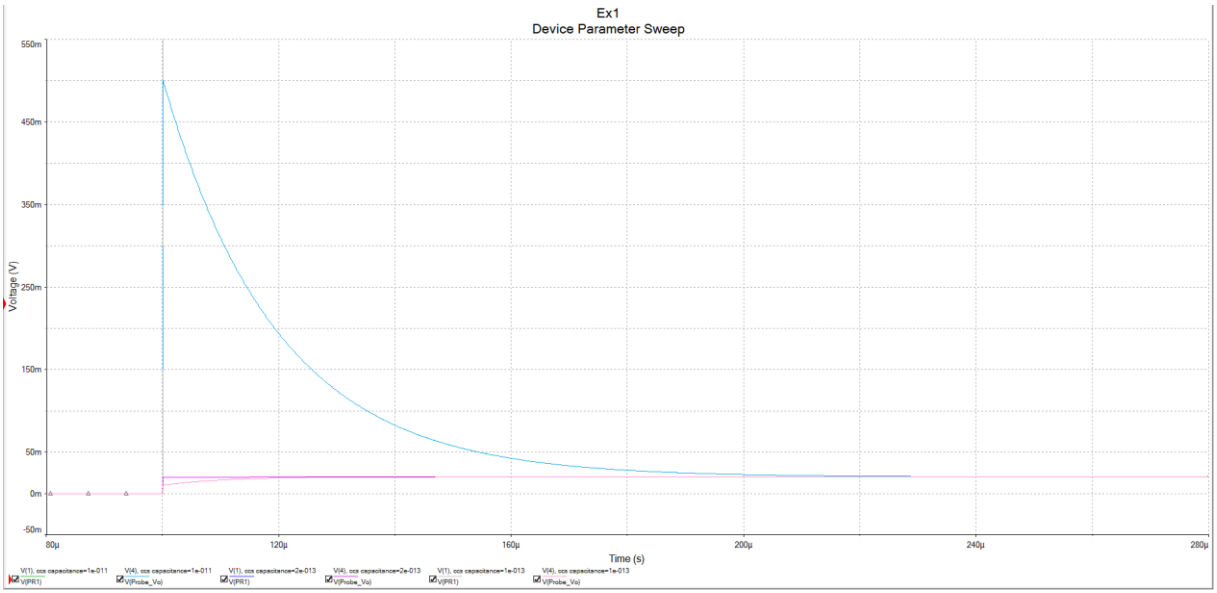
In order to get the division ratio 1:50 one need to calculate:

Cs*Rs=Co*Ro , where from the ratio we know that Rs=49MΩ

Cs=Co*Ro / Rs

Cs=10pF*1MΩ / 49MΩ

Optimal values: Cs=0,2pF and Rs=49MΩ



Plot 4. Characteristics of V_{out} vs. time for Cs=0,2 pF.