Lab 3 Practice: LEDs controller

Objective

1. Getting familiar with the LEDs, clock designs, and finite-state machines in Verilog.

Action Items

1 Lab3_practice.v (100%)

In this lab, you must design a LEDs controller. This game must be controlled by a finite-state machine (FSM) which controls the LEDs based on the switch.

a. I/O list

I/O	Connected to	Definition
clk	W5	Clock signal with the frequency of 100MHz
rst	SW15	Asynchronous positive reset signal, resetting the FSM to the **INITIAL** state
speed	SW0	Controlling the speed of LEDs
led[15:0]	LD15~LD0	Lighting up the LEDs in the sequence based on the control of the switches

b. **Finite state machine (FSM)**

The FSM may consist of an **INITIAL** state to initialize it, a **SLOW** state in which the LEDs will light up in sequence at a slower speed, and a **FAST** state in which the LEDs will light up in sequence at a faster speed. You can design your own variant instead. Note that in any state, when **rst == 1 (following the positive edge)**, the FSM will reset to the **INITIAL** state. When the **rst** goes back to 0, the FSM will operate normally.

✓ **INITIAL** state

- When entering this state, the FSM will switch to the **SLOW** state at the next cycle.
- In this state, the **LD15~LD0** are all **on**. The FSM can enter the **SLOW** state by switching the **rst** to 0. The LEDs in the **INITIAL** state:

LD15 ●●●●●●●●●●●●●●●● LD0

(● : LED on, ○ : LED off)

✓ **SLOW** state

- In this state, if the **speed** is set to 1, the FSM will go to the **FAST** state. However, if the **speed** is set to 0, the FSM will stay in the **SLOW** state.
- In this state, the LEDs will light up in sequence at the rate of **100MHz/2^{28}** 。

EX1:

At the beginning, the LEDs will light up as follows:

LD15 ●○○○○○○○○○○○○○○○ LD0

(● : LED on, ○ : LED off)

In the next cycle, the LEDs will light up as follows:

LD15○●○○○○○○○○○○○○○○○ LD0

(● : LED on, ○ : LED off)

EX2:

When the LD0 is on, the LEDs will light up as follows:

LD15○○○○○○○○○○○○○○○● LD0

(● : LED on, ○ : LED off)

In the next cycle, the LD15 will be on. Therfore, the LEDs will light up as follows:

LD15●○○○○○○○○○○○○○○○ LD0

(● : LED on, ○ : LED off)

✓ **FAST** state

- In this state, if the **speed** is set to 0, the FSM will go to the **SLOW** state. However if the **speed** is set to 1, the FSM will stay in the **FAST** state.
- In this state, the LEDs will light up in sequence at the rate of **100MHz/2^{27}** 。

EX1:

At the beginning, the LEDs will light up as follows:

- LD15 ●○○○○○○○○○○○○○○○ LD0
- (● : LED on, ○ : LED off)

In the next cycle, the LEDs will light up as follows:

- LD15○●○○○○○○○○○○○○○○○ LD0
- (● : LED on, ○ : LED off)

EX2:

When the LD0 is on, the LEDs will light up as follows:

- LD15○○○○○○○○○○○○○○○● LD0
- (● : LED on, ○ : LED off)

In the next cycle, the LD15 will be on. Therfore, the LEDs will light up as follows:

- LD15●○○○○○○○○○○○○○○○ LD0
- (● : LED on, ○ : LED off)

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c. You have to use the following template for your design:

```
module lab3_practice (
    input wire clk,
    input wire rst,
    input wire speed,
    output reg [15:0] led
     );
  /* Note that output ports can be either reg or wire.
  * It depends on how you design your module. */
  // add your design here
      endmodule
```

Attention

- ✓ DO NOT copy-and-paste code segments from the PDF materials. It may also paste invisible non-ASCII characters, leading to hard-to-debug syntax errors.