Lab 6 Practice: Dual FPGA Boards

Due Date: 2024/11/26

Objective

1. Familiarize yourself with connecting dual FPGA boards.
2. Become familiar with the I/O components on the demo board.
3. Learn to write and manage I/O constraints file.

Description

In this practice, you will connect two FPGA boards: one is Master, and the other is Slave.

Achieve the following objectives:

1. Initially, all the LEDs are turned off.
2. Only SW0 to SW7 on the Master board control LED0 to LED7 on the Slave board.
   a. Configure the LEDs on the Slave FPGA board to reflect the status of switches on the Master FPGA board. Normally, only one switch will be pulled up. For example, if the SW0 (V17) on the Master board is pulled up, the LED0 (U16) on the Slave board should turn on.
   b. If more than one switch is pulled up at any time, all LEDs (0-7) on the Slave board should be off.
   c. If all eight switches are pulled down, all LEDs (0-7) on the Slave board should be off.
3. Since 4 bits can represent at most 16 different conditions, only 4 pins are required for the connection.
4. Use DuPont wires (杜邦線) to connect two FPGA boards.
5. Select appropriate PMOD ports for the connection and create your own constraints file (.xdc file) for both the Master and Slave.
6. Use the provided template for your design:
   Notice: The data_out and data_in I/O ports are the signals used to transmit data between the two FPGA boards.

```
module lab6_practice_master (
    input wire clk,
    input wire rst,
    input wire [7:0] sw, // switches
    output wire [3:0] data_out  // data (number) to slave
);
```

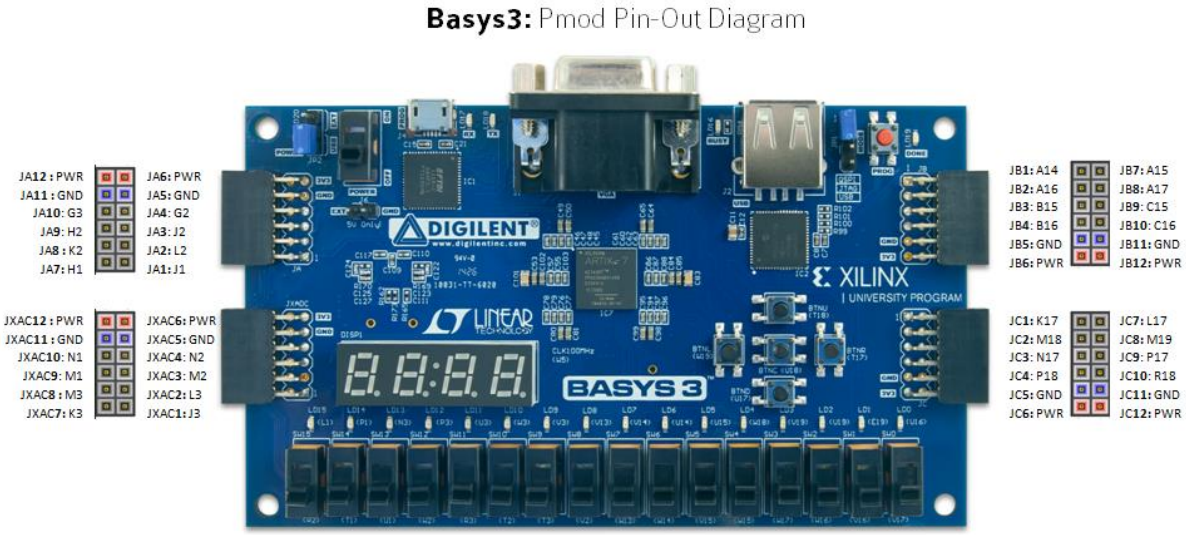
```
    // add your design here
    endmodule

    module lab6_practice_slave (
        input wire clk,
        input wire rst,
        input wire [3:0] data_in, // data (number) from master
        output wire [7:0] led // LEDs
    );

    // add your design here
    endmodule
```

Hint

- Here is the pin-out diagram for the PMOD connector for reference:



- Here is an example of a revised constraints file:

```
## Pmod Header JA
## Sch name = JA1
set_property PACKAGE_PIN J1 [get_ports {data_out[0]}]
  set_property IOSTANDARD LVCMOS33 [get_ports {data_out[0]}]
# Sch name = JA2
set_property PACKAGE_PIN L2 [get_ports {data_out[1]}]
  set_property IOSTANDARD LVCMOS33 [get_ports {data_out[1]}]
# Sch name = JA3
set_property PACKAGE_PIN J2 [get_ports {data_out[2]}]
  set_property IOSTANDARD LVCMOS33 [get_ports {data_out[2]}]
# Sch name = JA4
set_property PACKAGE_PIN G2 [get_ports {data_out[3]}]
  set_property IOSTANDARD LVCMOS33 [get_ports {data_out[3]}]
```

Attention

- This practice helps you with the following basic lab. Please make sure you completely understand it.
- Feel free to ask questions about the specification on the EECLASS forum.