

Joanne Baba

4B Computer Engineering – University of Waterloo

✉ jbaba@uwaterloo.ca
🌐 joannebaba.com
in linkedin.com/in/joannebaba
🔗 github.com/joannebaba

SKILLS

Languages Verilog, VHDL, RISC-V/ARM assembly, C/C++, Java, Kotlin, JavaScript/TypeScript, Python
Frameworks & Tools React, React Native, Flow, Jest, Android, Git
Hardware FPGAs, PCB design and assembly, STM32F401RE, TI MSP430, Raspberry Pi, Arduino Uno

WORK EXPERIENCE

Microsoft | Silicon Design Engineer

Sep – Dec 2022

- Designed RAS parity protection for **AXI** bus interface in security processor as an IP owner using **Verilog**
- Enhanced performance and security capabilities by supporting multiple outstanding **AXI** bus transactions
- Collaborated with verification and architecture teams to review design specifications and documentation

Microsoft | Silicon Design Engineer

Jan – Apr 2022

- Implemented RTL power optimization in **Verilog** for crypto IP in Microsoft **Pluton** security processor
- Reduced total power consumption in crypto IP by **93%** through active power analysis from waveforms
- Improved overall design clock gating efficiency by **100%** by increasing dynamic clock gating coverage

Sony Interactive Entertainment | Software Developer

May – Aug 2021

- Enhanced and maintained **PlayStation 5** game and application library with **React Native** and **TypeScript**
- Spearheaded development of configurable API sandbox app to facilitate early-stage debugging process
- Increased functional and component unit test coverage across multiple repositories using **Jest** and **Enzyme**

Ford Motor Company | Android Developer

Sep – Dec 2020

- Key team contributor to early-stage HMI project using **Kotlin**, **Java**, and **XML** in Android environment
- Developed large-scale framework and media app prototype while significantly reducing build time cost

Ford Motor Company | Software Developer

Jan – Apr 2020

- Enhanced vehicle settings interface in the Ford **Mustang Mach-E** using **React**, **JavaScript**, and **Redux**
- Analyzed and significantly reduced performance data by refactoring with **Flow** to remove legacy code

University of Waterloo | Embedded Design and Business Workflows Co-op

May – Aug 2019

- Created custom component footprint and schematic library in **DipTrace** by analyzing module datasheets
- Designed and fabricated an ultrasonic distance sensor PCB prototype using a **TI MSP430** microcontroller

PROJECTS

RISC-V Processor

Sep – Dec 2021

- Built **Verilog** RTL implementation of 5-stage pipelined processor for **RISC-V** instruction-set architecture
- Designed control logic and components such as memory and ALU to support multi-cycle datapath

Digital Image Processor

Jan – Apr 2021

- Implemented Kirsch edge detector algorithm to detect edges in 8-bit grayscale images using **VHDL**
- Optimized area and performance analysis using dataflow diagram with overlapping pipelined stages

AWARDS & ACHIEVEMENTS

- SIE Hackathon First Prize** – awarded **\$1500** out of **100+** teams in company-wide hackathon 2021
- Governor General's Academic Medal** – graduated with **highest overall average** of **98%** 2018

EDUCATION

University of Waterloo

Sep 2018 – Jun 2023

Candidate for Bachelor of Applied Science in Computer Engineering (BASC) – Dean's Honours List 2020-2022