Joanne Baba

BASc Computer Engineering – University of Waterloo

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SKILLS

Languages	Verilog, VHDL, RISC-V/ARM assembly, Python, C/C++, Java, Ruby, Perl
Frameworks & Tools	Git, Perforce, Verdi, PrimePower, PowerArtist
Hardware	ASIC design, static verification (lint, CDC, RDC), RTL synthesis, PCB design and assembly

WORK EXPERIENCE

AMD | Silicon Design Engineer 2

July 2023 – Present

- Implemented RTL wrapper for third-party IP interface using **Verilog** by following architecture specifications
- Contributed to zero static verification waiver initiative through **lint** and **CDC/RDC** timing analysis
- Integrated new CPUs into microprocessor subsystems leading to almost **5x** speed performance uplift
- Triaged regression failures through waveform debugging and collaboration with design verification team
- Utilized **Perl** for infrastructure, build-flow methodology, integration, and uniquification to support IP bring-up
- Automated IP configuration comparison across multiple projects through **Ruby** script development

Microsoft | Silicon Design Engineer Intern

Sep – Dec 2022

- Designed RAS parity protection for **AXI** bus interface in security processor as an IP owner using **Verilog**
- Enhanced performance and security capabilities by supporting multiple outstanding **AXI** bus transactions
- IP ownership responsibilities included micro-architecture, synthesis, lint, and code coverage review
- Collaborated with verification and architecture teams to review design specifications and documentation

Microsoft | Silicon Design Engineer Intern

Jan – Apr 2022

- Implemented RTL power optimization in **Verilog** for crypto IP in Microsoft **Pluton** security processor
- Performed power analysis using tools including Ansys **PowerArtist** and Synopsys **PrimePower** (PTPX)
- Reduced total power consumption in crypto IP by **93%** through activity factor analysis from waveforms
- Improved overall design clock gating efficiency by **100%** by increasing dynamic clock gating coverage

Sony Interactive Entertainment | Software Developer Intern

May – Aug 2021

- Enhanced and maintained **PlayStation 5** game and application library with **React Native** and **TypeScript**
- Spearheaded development of configurable API sandbox app to facilitate early-stage debugging process
- Increased functional and component unit test coverage across multiple repositories using **Jest** and **Enzyme**

PROJECTS

RISC-V Processor

Sep – Dec 2021

- Built **Verilog** RTL implementation of 5-stage pipelined processor for **RISC-V** instruction-set architecture
- Designed control logic and components such as memory and ALU to support multi-cycle datapath

Digital Image Processor

Jan – Apr 2021

- Implemented Kirsch edge detector algorithm to detect edges in 8-bit grayscale images using **VHDL**
- Optimized area and performance analysis using dataflow diagram with overlapping pipelined stages

AWARDS & ACHIEVEMENTS

- **Keysight Technologies Award** – awarded **best hardware design** for 4th year ECE capstone project 2023
- **SIE Hackathon First Prize** – awarded **$1500** out of **100+** teams in company-wide hackathon 2021
- **Governor General's Academic Medal** – graduated with **highest overall average** of **98%** 2018

EDUCATION

University of Waterloo

Sep 2018 – Jun 2023

Bachelor of Applied Science in Computer Engineering (BASc) – Dean's Honours List