## FTDI GPIO configuration

| High byte = ACBUS | | | | | | | | Low byte = ADBUS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Direction : 0 = input, 1 = output

The initial state of inputs must be set to 0.

## MPSSE pin functions

| **Pin** | **FT232H** | **FT2232H (1)** | **FT4232H (2)** | **FT2232D (3)** |
|---|---|---|---|---|
| ADBUS0 | TCK/SK | TCK/SK | TCK/SK | TCK/SK |
| ADBUS1 | TDI/DO | TDI/DO | TDI/DO | TDI/DO |
| ADBUS2 | TDO/DI | TDO/DI | TDO/DI | TDO/DI |
| ADBUS3 | TMS/CS | TMS/CS | TMS/CS | TMS/CS |
| ADBUS4 | GPIOL0 | GPIOL0 | GPIOL0 | GPIOL0 |
| ADBUS5 | GPIOL1 | GPIOL1 | GPIOL1 | GPIOL1 |
| ADBUS6 | GPIOL2 | GPIOL2 | GPIOL2 | GPIOL2 |
| ADBUS7 | GPIOL3 | GPIOL3 | GPIOL3 | GPIOL3 |
| ACBUS0 | GPIOH0 | GPIOH0 | n.a. | n.a. |
| ACBUS1 | GPIOH1 | GPIOH1 | n.a. | n.a. |
| ACBUS2 | GPIOH2 | GPIOH2 | n.a. | n.a. |
| ACBUS3 | GPIOH3 | GPIOH3 | n.a. | n.a. |
| ACBUS4 | GPIOH4 | GPIOH4 | n.a. | n.a. |
| ACBUS5 | GPIOH5 | GPIOH5 | n.a. | n.a. |
| ACBUS6 | GPIOH6 | GPIOH6 | n.a. | n.a. |
| ACBUS7 | GPIOH7 | GPIOH7 | n.a. | n.a. |

**(1)**: The FT2232H has JTAG on channels A and B, i.e. ADBUS*n* and BDBUS*n* are isofunctional.

**(2)**: The FT4232H has JTAG on channels A and B, i.e. ADBUS*n* and BDBUS*n* are isofunctional. Channels C and D (CDBUS*n* and DDBUS*n*) can only be used for RS232 or bit-bang interface.

**(3)**: On the FT2232D, MPSSE is channel A only.

## Application to OpenOCD configuration

In OpenOCD, the **ftdi_layout_init** command accepts 2 arguments, **data** and **direction**. Those are 16-bit numbers defining the initial state and the direction of the GPIO pins, respectively.

For instance, **ftdi_layout_init 0x0008 0x001b** defines:

- All ACBUS lines as inputs,
- ADBUS2 (TDO), ADBUS5, ADBUS6, and ADBUS7 as inputs,
- ADBUS0 (TCK), ADBUS1 (TDI), ADBUS3 (TMS) and ADBUS4 as outputs, with an initial state of 1 for TMS, and 0 for TCK, TDI, and ADBUS4.

# NVARCHER FTx232HL dev. board J4 connector pinout

| | | | | |
|---|---|---|---|---|
| | VTref | 1 | 2 | N.C. |
| BDBUS4: O | nTRST | 3 | 4 | GND |
| BDBUS1: O | TDI | 5 | 6 | GND |
| BDBUS3: O | TMS / SWDIO | 7 | 8 | GND |
| BDBUS0: O | TCK / SWCLK | 9 | 10 | GND |
| BDBUS5: I | RTCK | 11 | 12 | GND |
| BDBUS2: I | TDO / SWO | 13 | 14 | GND |
| BDBUS6 | nRESET | 15 | 16 | GND |
| BDBUS7 | DBGRQ | 17 | 18 | GND |
| | +5V | 19 | 20 | GND |

"*Output*" *below means signal from debug probe to target board.* "*Input*" *means signal from target board to debug probe.*

VTref = Target Voltage reference (= VDD from target board). Input.

TDI = Test Data In. Output.

TDO = Test Data Out. Output.

TCK = Test ClocK. Output.

TMS = Test Mode Select. Output.

nTRST = Test ReSeT Output, active low, optional. Used to reset the TAP controller and/or debug logic. If target board doesn't have TRST, JTAG reset is triggered with TMS and TCK signals instead.

RTCK = Return Test ClocK. Input. Specific to ARM9 and ARM11 cores.

nRESET = Reset signal sent to target board, e.g. to connect under reset. Also known as nRST or nSRST (System ReSeT). Output, active low.

DBGRQ = DeBuG ReQuest. Output, optional. Forces the target CPU to enter debug mode.

SWDIO = SWD bidirectional data I/O.

SWCLK = SWD clock. Output.

SWO = Serial Wire Output trace port. Input, optional. Not required for SWD communication.

+5V = Output.