WCH QingKe RISC-V cores summary

Core	ISA	Branch prediction	Interrupts	HPE levels	Interrupt nesting levels	VTF channels	Pipeline	Vector table mode	XW extension	Memory protection areas	Instruction cache	Floating point unit
V2A	RV32EC	static	256	2	2	2	2	address / instruction	yes	-	-	-
V2C	RV32EC_Zmmul	static	256	2	2	2	2	address / instruction	yes	-	-	-
V3A	RV32IMAC	static	256	2	2	4	3	instruction	-	-	-	-
V3B	RV32IMCB	static	256	2	2	4	3	address / instruction	yes	4	-	-
V3C	RV32IMCB	static	256	2	2	4	3	address / instruction	yes	4	-	-
V4A	RV32IMAC	BHT / BTB / RAS	256	2	2	4	3	address / instruction	-	4	-	-
V4B	RV32IMAC	BHT / BTB / RAS	256	2	2	4	3	address / instruction	yes	4	-	-
V4C	RV32IMAC	BHT / BTB / RAS	256	2	2	4	3	address / instruction	yes	4	-	-
V4F	RV32IMACF	BHT / BTB / RAS	256	3	8	4	3	address / instruction	yes	4	-	yes
V4J	RV32IMAC	BHT / BTB / RAS	256	2	2	4	3	address / instruction	yes	4	64K	-

BHT Branch History Table
BTB Branch Target Buffer
RAS Return Address Stack

HPE Hardware Prologue / Epilogue
VTF Vector Table Free interrupt response mechanism
XW Compressed instructions for self-extending byte and half-word operations

The following chart shows available MCU for each QingKe core: https://special.wch.cn/zh_cn/RISCV_MCU_Index/