Hardware/Software Codesign – Project part 2

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The video processing accelerator was implemented using Vivado HLS. Firstly, the standard data types were converted to HLS specific arbitrary precision data types, such as *ap_fixed<96,32, AP_RND, AP_SAT>* for data processing and *ap_uint* with different bit sizes for different purposes. To speed up the implementation, the HLS directive **ARRAY_PARTITION** with a factor of 64 was used to enable parallel memory access for the histogram computation. The **PIPELINE** directive was used with an Initiation Interval (II) of 2, overlapping loop iterations in a safe manner, as 1 would be too low and inefficient. These directives allowed the code to obtain much better results in terms of timing, reducing the estimated duration of a clock cycle from 8.763 ns to 6.022 ns and latency, which was reduced by approximately 19.7%. Resource utilization also improved. Apart from DSPs, all other components had a big increase in their utilization, meaning that the solution with the directives utilizes more efficiently the resources it has available to it. Figure 1 shows the results for the implementation without the HLS directives and Figure 2 the results for the implementation with the HLS directives. Both implementations had an II of 2.

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	7.00 ns	8.763 ns	0.88 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
2591	2592	22.705 us	22.714 us	2560	2560	loop rewind(delay=0 initiation interval(s))

Detail

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	584	12242	-
FIFO	-	-	-	-	-
Instance	2	124	8637	4235	-
Memory	4	-	1118	1368	0
Multiplexer	-	-	-	516	-
Register	0	-	6214	224	-
Total	6	124	16553	18585	0
Available	280	220	106400	53200	0
Utilization (%)	2	56	15	34	0

Figure 1: Results for the implementation without HLS directives

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	7.00 ns	6.022 ns	0.88 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
2605	2605	18.235 us	18.235 us	2605	2605	none

Detail

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	584	12484	-
FIFO	-	-	-	-	-
Instance	128	124	13677	19541	-
Memory	0	-	94	24	-
Multiplexer	-	-	-	7674	-
Register	20	-	35703	356	-
Total	148	124	50058	40079	0
Available	280	220	106400	53200	0
Utilization (%)	52	56	47	75	0

Figure 2: Results for the implementation with HLS directives

As for the testing of this accelerated implementation, it wasn't able to be done. Although it was tried, problems with the resolution of the available monitors (especially the active signal resolution, which led to the correct resolution of 1280x720 not being transmitted to the board, even when set to that value) didn't allow this implementation to run correctly. With this said, it would be predictable that this version would be significantly faster than the version implemented in the first part of this project, as evidenced by the results of running the synthesis with Vivado HLS in Figure 2.