

# Arquiteturas de Computadores Paralelos

# ELC139 - Programação Paralela

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2023/1

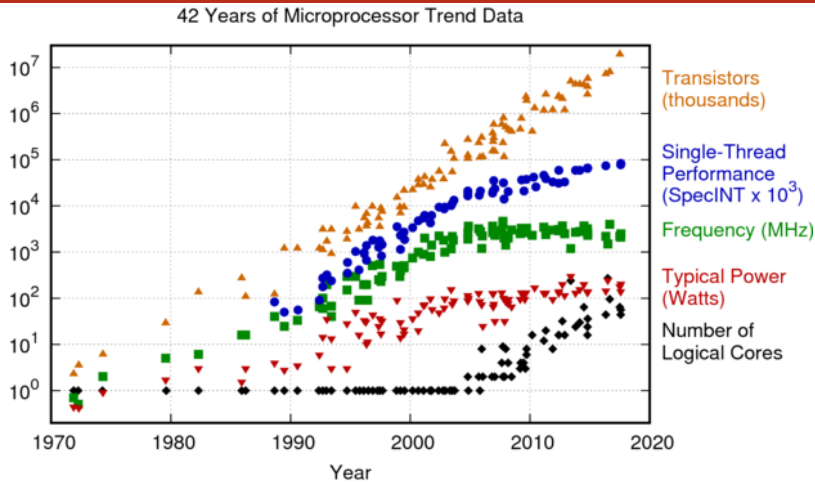
# Outline

- 1 Introdução
- 2 Taxonomia de Flynn

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# Evolução dos processadores



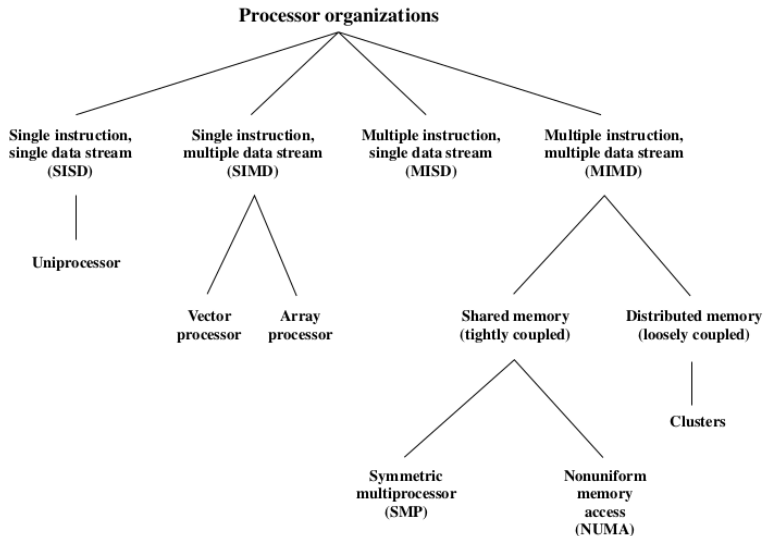
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten  
New plot and data collected for 2010-2017 by K. Rupp

# Outline

1 Introdução

2 Taxonomia de Flynn

# Taxonomia de Flynn





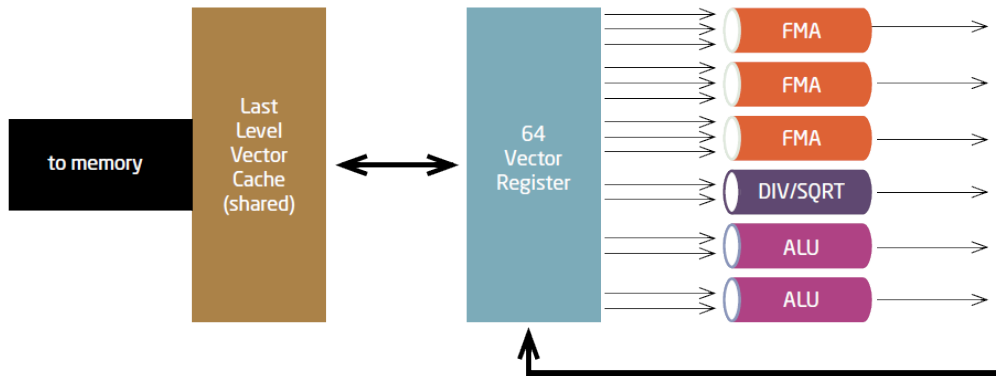
# Single instruction, multiple data (SIMD)

- O processador executa um conjunto de operações **simultaneamente** sobre múltiplos dados (matrizes ou vetores)
- Muito usada em HPC
- Exemplos de arquiteturas
  - NEC SX-Aurora TSUBASA
  - GPUs como Single Instruction Multiple Threads (SIMT)



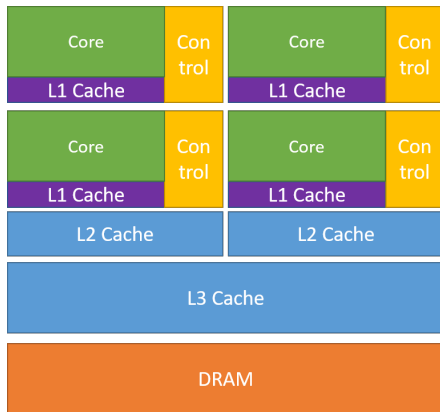
# NEC SX-Aurora TSUBASA

- Cada Vector Engine Processor pode ter até 16x cores.
- FMA - Fused multiply-add  $a*b + c$

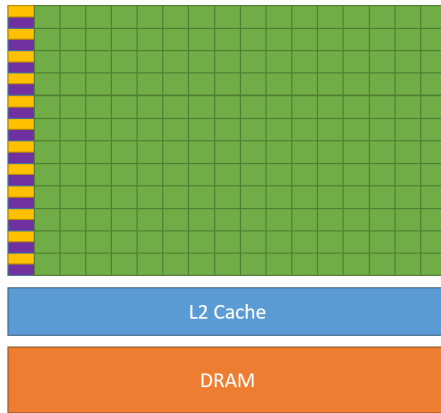


# Graphics Processing Unit (GPU)

- CPUs executam uma sequência de instruções o mais rápido possível
- GPUs executam um grande número de instruções concorrentes



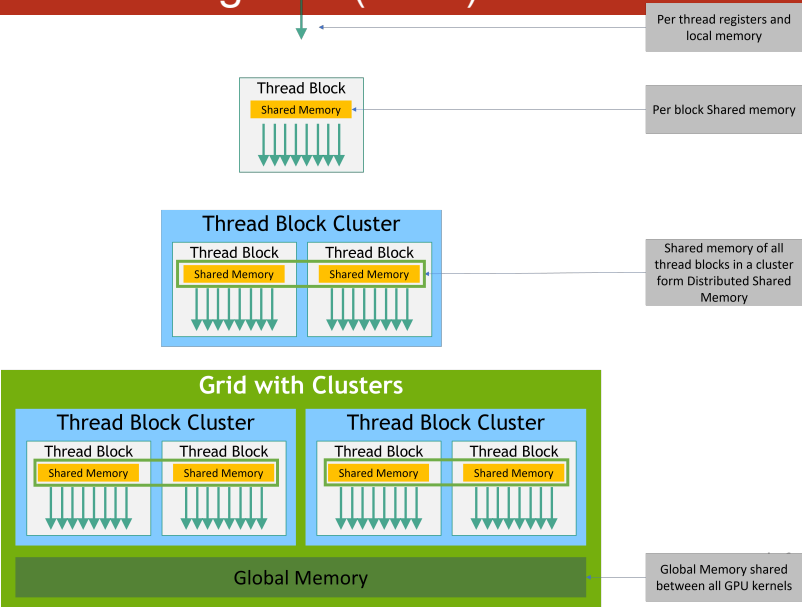
CPU



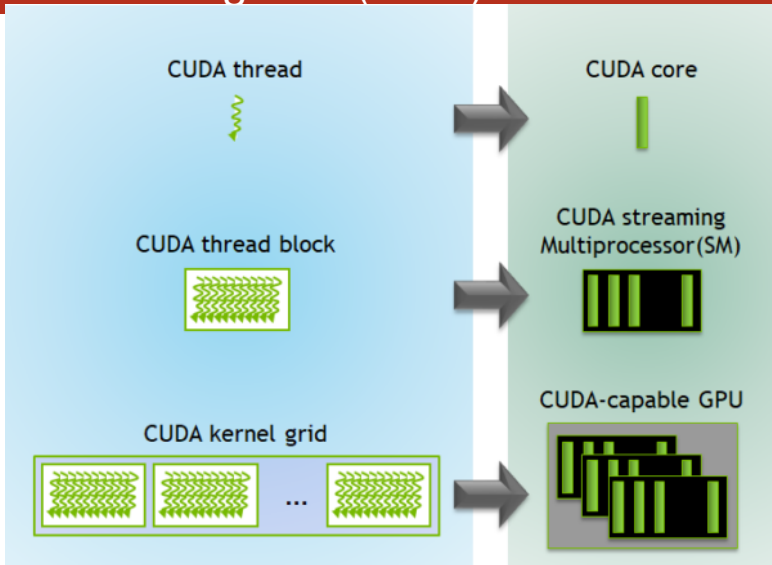
GPU

<https://docs.nvidia.com/cuda/cuda-c-programming-guide/>

# Graphics Processing Unit (GPU)

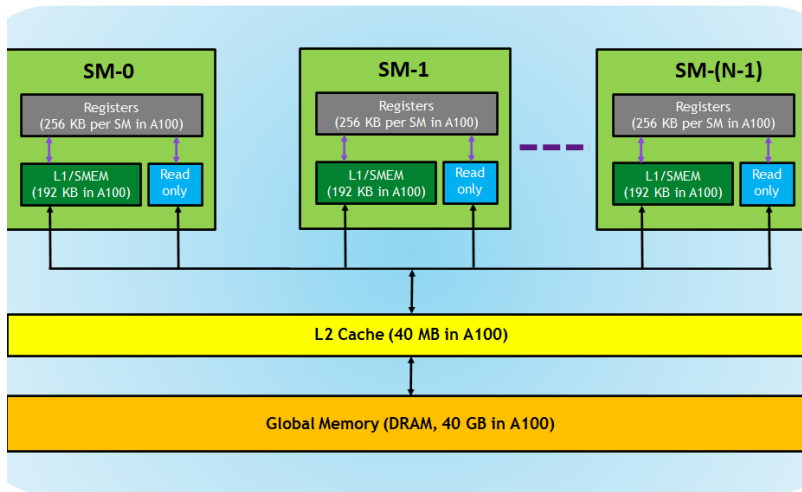


# Graphics Processing Unit (GPU)



<https://developer.nvidia.com/blog/cuda-refresher-cuda-programming-model/>

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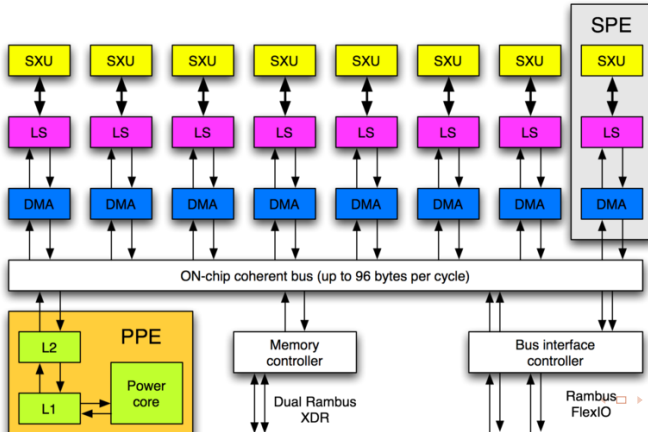
# Multiple instruction, single data (MISD)

- Múltiplas instruções operam sobre um dado de cada vez.
- Nunca desenvolvida
- Algumas vezes associado a *systolic arrays*



# IBM Cell processor

- Processador multi-core baseado no PowerPC
- 1x IBM PowerPC processing element (PPE)
- 8x synergistic processing elements (SPE)
- A movimentação de dados entre caches dependia do programador



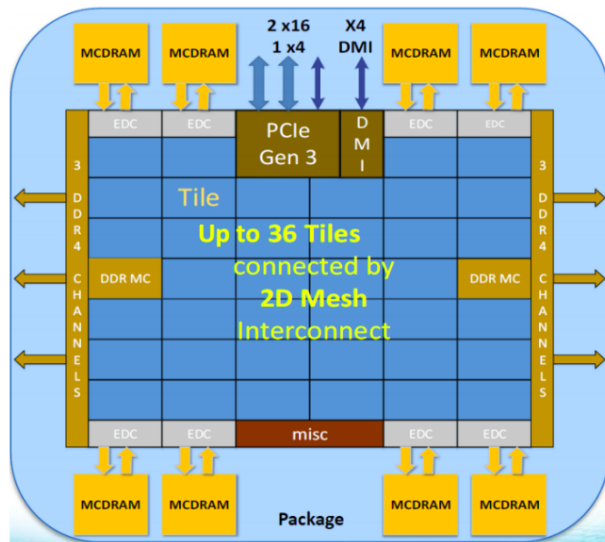


# US Condor Cluster (PS3)



# Intel Knights Landing

- Processador manycore x86
- 68 núcleos, totalizando 272 núcleos e 1088 threads, 1.4 GHz
- 96 GB DDR4 RAM + 16 GB HBM MCDRAM
- Sistema Linux próprio com comandos



# Intel Knights Landing

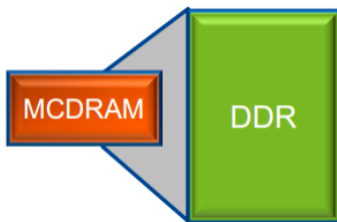
**Flat**



MCDRAM is NUMA node 1

DDR is NUMA node 0

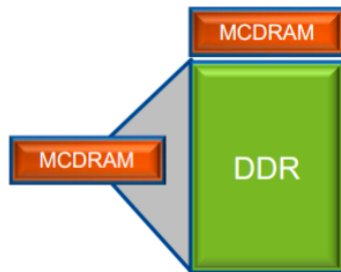
**Cache**



MCDRAM acts as memory-side cache for DDR

DDR is NUMA node 0

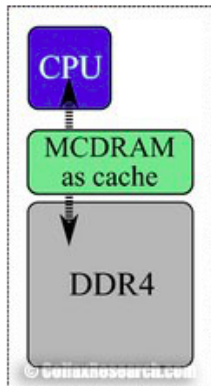
**Hybrid**



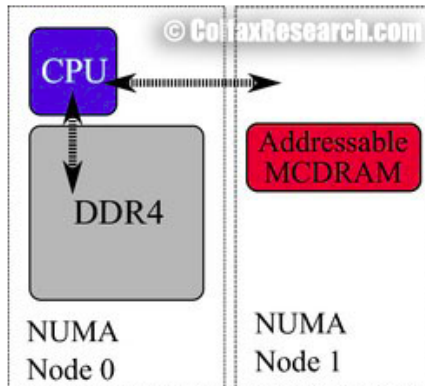
Part of MCDRAM is cache, part is NUMA node 1

DDR is NUMA node 0

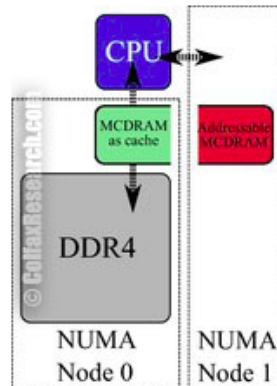
# Intel Knights Landing



Cache mode

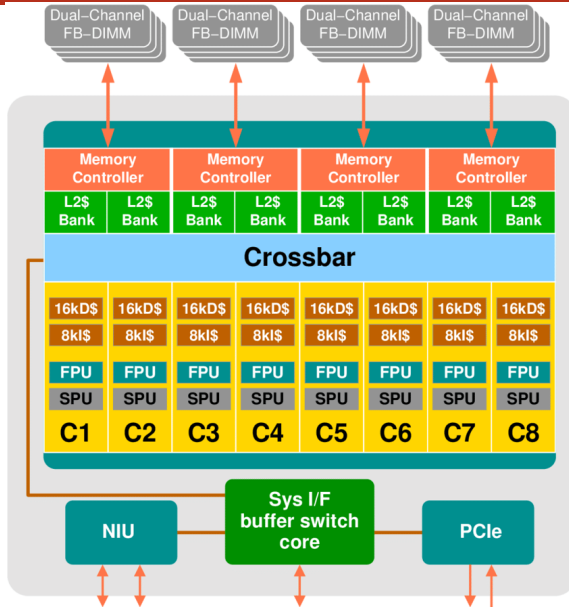


Flat mode



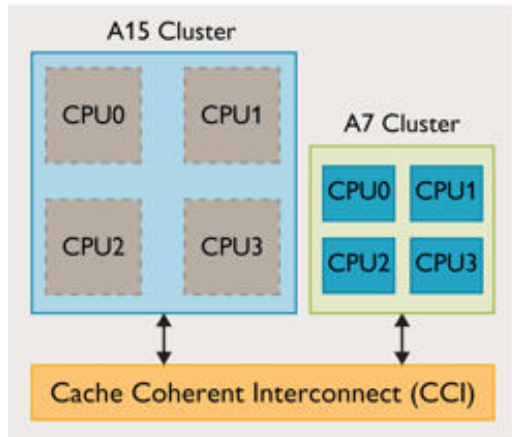
Hybrid mode

# Sun UltraSPARC T2

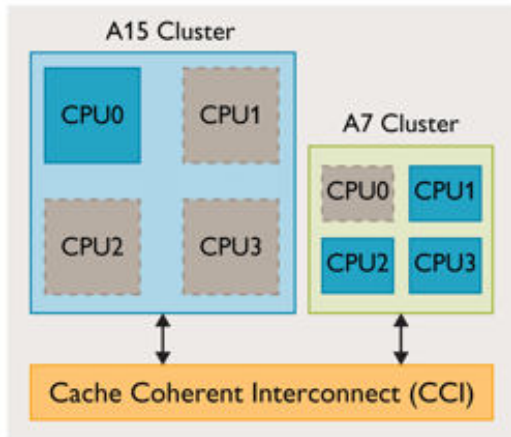


# ARM big.LITTLE

Low Load



High Load in a Single Processor



Inactive Processor



Active Processor

<https://joao-ufsm.github.io/par2023a/>

