

CRC-8

Cyclic Redundancy Check

Arquiteturas de Alto Desempenho

PRESENTED BY TP3G7
João Afonso Ferreira
João Pedro Ferreira

CRC-8 OVERALL APPROACH

• In order to develop a solution to **protect the integrity of a message**, a CRC should be implemented with a polynomial of:

$$x^{8} + x^{7} + x^{5} + x^{2} + x + 1$$

Thus, for the given CRC generator, the corresponding binary pattern is 110100111.

- The **message** and the result of the division (**remainder**) by the above polynomial are sent **together** by the **Encoder**, when sending the message, so that when it is received, the CRC **Checker** can perform the division and **compare** it with what was first received.
- If equal, the message was not corrupted during the "journey/trip" to the receiver.
- To validate the precision of the implemented CRC8 components, a series of tests were devised using Quartus Prime waveforms.

ENCODER - APPROACH

(PARALLEL)

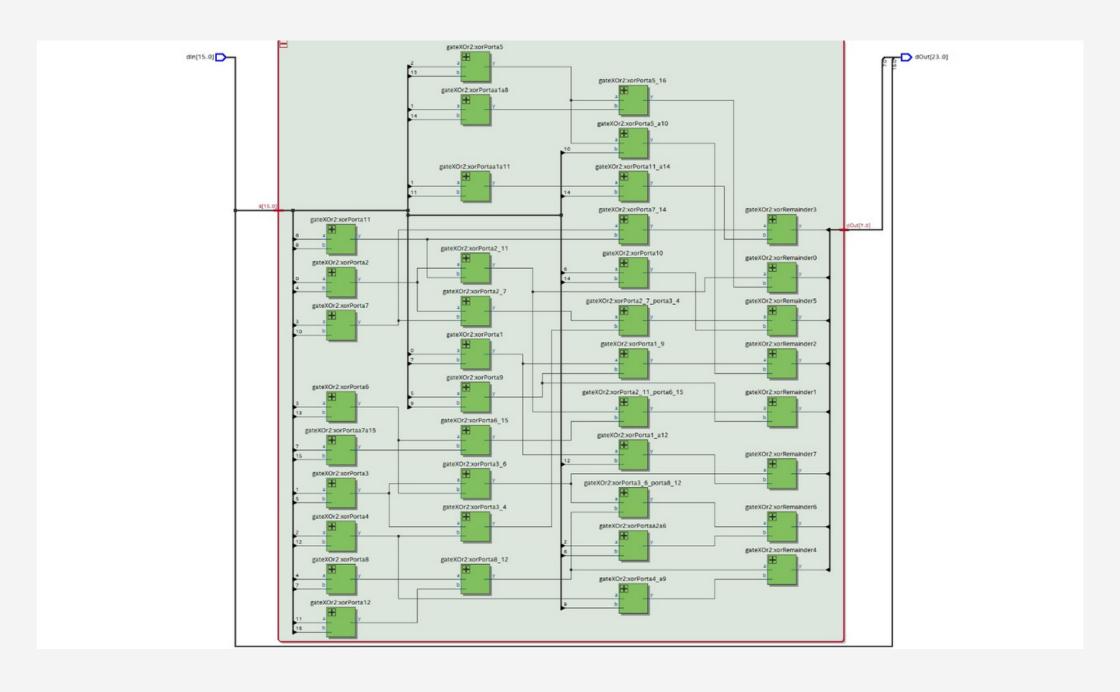
- The CRC8 Encoder circuit processes a 16-bit data word to generate an 8-bit CRC-8 Bluetooth check string. The key component is the remainder calculation block, responsible for computing the properties of the remainder as well as finding the best possible algorithm.
 - An auxiliary table was created to find out the common groups/combination of operations in order to reduce the XOR gates needed
 - Using the Parallel
 implementation, we could also
 reduce the propagation time
 delays;

				Laval O					
				Level 0	I				
		r7	r6	r5	r4	r3	r2	r1	r0
a0	x^8	1		1			1	1	1
a1	x^9	1	1	1		1			1
a2	x^10		1	1	1		1		1
a3	x^11	1	1	1		1		1	
a4	x^12		1	1	1			1	1
a5	x^13	1	1	1			1	1	
a6	x^14		1	1		1		1	1
a7	x^15	1	1		1		1	1	
a8	x^16					1		1	1
a9	x^17				1		1	1	
a10	x^18			1		1	1		
a11	x^19		1		1	1			
a12	x^20	1		1	1				
a13	x^21	1	1				1	1	1
a14	x^22			1		1			1
a15	x^23		1		1			1	

ENCODER - ARCHITECTURE

- **Input**: 16-bit data word (sent message)
- Output: 24-bit CRC-8 Bluetooth check string.

- Number of XORS: 58 → 41 XORS
- Worst Case Delay: 9 → 4 XORS



CHECKER - APPROACH

(BIT SERIAL)

- The **CRC8 Checker** serves a crucial role in validating whether the received 24-bit data word has been transmitted **without errors**.
- The previously mentioned **24-bit data word** represents the **transmitted message**, serving as the input for the CRC-8 Encoder (16 bits) **alongside** the **remainder** (8 bits), this remainder is the outcome of dividing the message by the polynomial.
- The design of the checker consists in:
 - a BinCounter 5 bit;
 - a Control Unit;
 - a LFSR (8 FLIP FLOPS in Parallel);
 - a Gate OR 8x1 (comparator);
 - a Flip FlopDPET.