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A programmable analog hearing aid system-on-chip with frequency compensation

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Abstract An analog hearing aid with the function of frequency compensation is proposed and implemented considering the human factors. Introducing the current-mode technique, a filter designed by the state space methodology is integrated in the hearing aid to offer the function which only appears in the DSP unit of digital hearing aid. Combined with the filter embedded in the driver circuit adopting the minimum current selecting technique, the enhance frequency compensation can well match to the common low-frequency hearing loss with a stopband attenuation of 80 dB/dec. Moreover, a low-noise automatic gain control (AGC) is presented to improve the programmability with discreet gains, knee points and compression ratios. To enhance the comfortable level, the attack time and release time is set 20 and 100 ms with a peak detector. The input-referred noise is below 5 μVrms. The hearing aid can drive a 16 Ω receiver at the supply voltage of 1 V. The die area is 2.3×1.5 mm^2 (AGC) and 0.93×0.86 mm^2 (driver) in a 0.13 μm standard CMOS process and 1×1 mm^2 (filter) in a 0.35 μm standard CMOS process.

Keywords Programmability · Frequency compensation · Analog hearing aid · Human factor

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1 Introduction

Every year, the need for hearing aids rises exponentially due to the dramatic number of individuals who suffer from some degree of hearing loss [1]. According to the magazine the hearing review, the hearing loss population mainly distributes in the baby boomer and elderly 75+ age brackets. In addition, the rate of new users of hearing aid has increased to 39 %, but the average income of users is less than $1,500 every year. So, the need for developing the low-cost hearing aid technology is consequently growing. Furthermore, in order to maintain the unique information of the processed sound and accord with the various needs of the individuals, the hearing aid design must consider the human factors, such as the frequency compensation, the attack and release time. The digital hearing aid can incorporate the human factors through the digital signal process (DSP) technique. However, the power is high because of the A/D, D/A, dedicated DSP and the class-D output stage [2–4]. Moreover, the prize is expensive to the low-income individuals. Although the price of analog hearing aid is low, it can not incorporate the human factors. Thus, the improved method on the human factors is highly desirable for the low-cost hearing aid.

To overcome this problem, an analog hearing aid chip is presented considering the human factors as shown in Fig. 1. Previously, we introduced a dual mode gain control (DMGC) AGC circuit for the analog hearing aid [5]. However, the previous front-end can not offer the function of frequency compensation, accurate attack and release time. So, the threshold pain of the ear can be reached when the input sound level is high in the field of the common low-frequency hearing loss. Thus, there is a need for a frequency compensation filter and an adaptive peak detector with the accurate attack and release time to

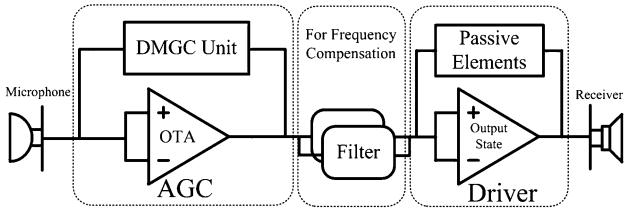

Fig. 1 The diagram of the analog hearing aid

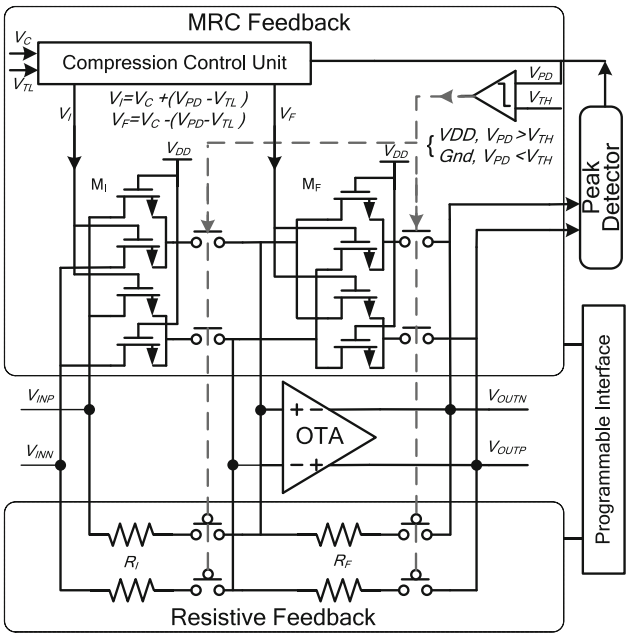

Fig. 2 The diagram of the AGC circuit

optimize the performance of the analog hearing aid. The filter is designed based on the state space methodology. In addition, a driver circuit is implemented to drive the receiver with a load impedance of 16 Ω. Where, a Rauch filter is embedded in the driver to improve the capability of noise rejecting. Moreover, a minimum current selecting technique is introduced to reduce the crossover distortion of the driver. By controlling the DMGC unit, eight gains, four knee points and four compression ratios can be achieved to enhance the programmability.

The paper is organized as follows. The AGC with DMGC technique is described in Sect. 2. The filter circuit for the frequency compensation and the driver circuit are discussed in Sects. 3 and 4, respectively. The measurement results are presented in Sect. 5. Conclusions are drawn in Sect. 6.

2 The AGC circuit

The AGC circuit with DMGC technique is implemented with a conventional operational transconductance amplifier (OTA) [6] and a DMGC unit which includes a resistive array, a MOS resistive circuit (MRC) array [7–9], a comparator, a peak detector, a compression control unit and a programmable interface, shown in the Fig. 2. The programmable interface can offer the discreet gain, knee point and compression ratio to improve the flexibility. The peak detector generates V_{PD} corresponding to the RMS value of the output voltage $V_{OUTN,P}$. The comparator is used to determine the operation mode of the AGC. If V_{PD} is larger than the knee point voltage V_{TH}, the AGC works in the MRC-feedback mode. On the other hand, it works in the resistor-feedback mode. By changing V_{TH}, the rotation knee point of the AGC can be programmed.

In the resistor-feedback mode, the gain of the AGC is

$$AGC_{Gain} = \frac{R_F}{R_I} \tag{1}$$

In the MRC-feedback mode, the input signal is compressed. The exponential gain control characteristic is required as a volume control because the human sensibility of sound operates on a logarithmic scale. To achieve the exponential gain characteristics in the case of CMOS technology, a pseudo-exponential polynomial $e^{-2x} = e^{-x}/e^{x} \approx (1-x)/(1+x)$ is used to approximate the logarithmic function. In Fig. 2, by using two MRC blocks as feedback resistors [7], the gain of the proposed preamplifier is given as follows:

$$\begin{aligned} AGC_{Gain} &= \frac{MRC_F}{MRC_I} = \frac{K_n \frac{W_I}{L_I}[V_{DD} - V_I]}{K_n \frac{W_F}{L_F}[V_{DD} - V_F]} \\ &= \frac{W_I L_F \left(1 - \frac{V_{PD} - V_{TL}}{V_{DD} - V_C}\right)}{W_F L_I \left(1 + \frac{V_{PD} - V_{TL}}{V_{DD} - V_C}\right)} \end{aligned} \tag{2}$$

where V_{DD} stands for supply voltage. W and L are the width and length of the transistor, respectively. K_n is equal to μC_{ox}, with μ the carrier effective mobility in the channel and C_{ox} the gate oxide capacitance per unit area. As shown in the Fig. 2, two differential bias voltages V_I and V_F are generated by the compression control unit to adjust the resistances of MRCs and control the gain of the amplifier. The common-mode voltage of V_I and V_F is set by V_C and differential voltage by V_{TL} and V_{PD} [5].

From Eq. (2), the gain of AGC with MRC feedback is controlled by V_{PD}–V_{TL} exponentially. V_{TL} is a reference voltage. Through adjusting the value of V_C, the gains of the two modes can be made equal right at the knee point. Thus, the 'jumps' shall be avoided and the gain transition should be smooth. In order to adjust the compression ratio of AGC, each MRC block is consist of several parallel MRCs. By controlling the number of MRCs, the equal aspect ratio (W/L) of the MRC blocks changes and the compression ratio of the AGC is programmed. As seen in the Eqs. (1)

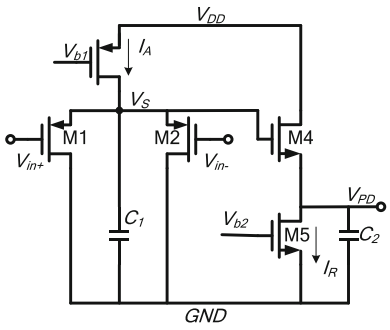

Fig. 3 The schematic of the peak detector

and (2), the resistor-feedback mode provides pro-linear amplification while the MRC-feedback mode works for compression with energy efficiency. Switching between the two modes achieves an improvement in total harmonic distortion (THD) without compromise to noise performance and power consumption [5].

The detailed circuit for peak detector is shown in Fig. 3. The MOS transistors M1, 2–4 work in the sub-threshold region. The drain current of the transistor in the sub-threshold region is given by [10]:

$$I = I_0 \exp\left(\frac{V_{GS}}{\xi U_T}\right) \tag{3}$$

where $\xi > 1$ is nonideality factor and $U_T = kT/q$ is thermodynamic voltage. V_{GS} and I stand for the gate-source voltage and the current of the transistor. I_0 is the leakage current when $V_{GS} = 0$.

As seen in Fig. 3, the current I_A is

$$\begin{aligned} I_A &= I_1 + I_2 \\ &= I_0\left[\exp\left(\frac{(V_{cm}+V_d)-V_S}{\xi U_T}\right) + \exp\left(\frac{(V_{cm}-V_d)-V_S}{\xi U_T}\right)\right] \end{aligned} \tag{4}$$

where the gate voltages of M1 and M2 are $V_{cm} + V_d$ and $V_{cm} - V_d$, with V_{cm} as the common mode voltage and V_d the differential mode voltage of the input signal. V_S is the source voltage of the differential pair. Assuming the current source I_A is constant, V_S is expressed as:

$$V_S = V_{cm} - V_d + \xi U_T \ln\left[1 + \exp\left(\frac{2V_d}{\xi U_T}\right)\right] - \xi U_T \ln\frac{I_A}{I_0} \tag{5}$$

when $|V_d| \gg 0$, the Eq. (5) is written as:

$$V_S \approx V_{cm} + |V_d| - \xi U_T \ln\frac{I}{I_0}, \text{ when } |V_d| > \ > 0 \tag{6}$$

Equation (6) shows that V_S is proportional to $|V_d|$ when the differential input voltage is large. And the minimum value is achieved at $V_d = 0$. With the help of filtering capacitor C_1, the peak detector can detect the envelope of the input signal. C_1 and C_2 determine the attack and release time, which are shown as follows.

$$\begin{cases} T_A = \dfrac{C_1}{g_{m,M1}} = \dfrac{2C_1\xi U_T}{I_A} \\ T_R = \dfrac{C_2}{g_{m,M2}} = \dfrac{C_2\xi U_T}{I_R} \end{cases} \tag{7}$$

where T_A and T_R stand for the attack and release time, respectively. In this paper, the attack time is set to 20 ms and the release time is about 100 ms considering the human factors.

3 The filter circuit

Generally, the common hearing loss focuses on the low-frequency range between 100 Hz to 1 kHz. And in the high-frequency range, the hearing loss is little, shown in the Fig. 4(a). So, the hearing aid must have the function of frequency compensation. That is, the gain of the hearing aid is high in the range between 100 Hz and ω_{c1} (the first pole) and low in the range between ω_{c2} (the second pole) to 10 kHz considering the human factors, shown in the Fig. 4(b) [11]. Between ω_{c1} and ω_{c2}, a zero is added to achieve a flat gain in the range of frequency with little hearing loss. However, the conventional analog hearing aid can not realize this function which only appears in the DSP unit of the digital hearing aid. Here, a filter for the frequency compensation integrated in the analog hearing aid is presented based on the current-mode technique.

The transfer function of the required filter is

$$H_{filter}(s) = \frac{\omega_{c2}(s + r\omega_{c1})}{r(s+\omega_{c1})(s+\omega_{c2})} \tag{8}$$

where r is equal to $(\omega_{c1} + \omega_{c2})/(2\omega_{c1})$.

The key MOS transistors of the filter work in the sub-threshold region. From Eq. (3), the relationship between I and V is linear in log-domain. This feature makes it easy to realize a filter considering the human factors in the time domain. Therefore the design method based on the state space methodology can be introduced. The filter can also be described as follows in the form of a state space equation [12].

$$\begin{cases} \dot{\mathbf{I}} = \mathbf{A}\mathbf{I} + \mathbf{B}I_{in} \\ I_{out} = \mathbf{C}\mathbf{I} + DI_{in} \end{cases} \tag{9}$$

where $\mathbf{I}$ is the state variable after the optimization. The matrixes $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and D are shown as follows after a reversible optimization.

$$\begin{cases} A = \begin{bmatrix} -\omega_{c1} & \omega_{c1} \\ 0 & -\omega_{c2} \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ \dfrac{\omega_{c2}}{r} \end{bmatrix} \\ C = \begin{bmatrix} 1 & 1 \end{bmatrix} \qquad D = 0. \end{cases} \tag{10}$$

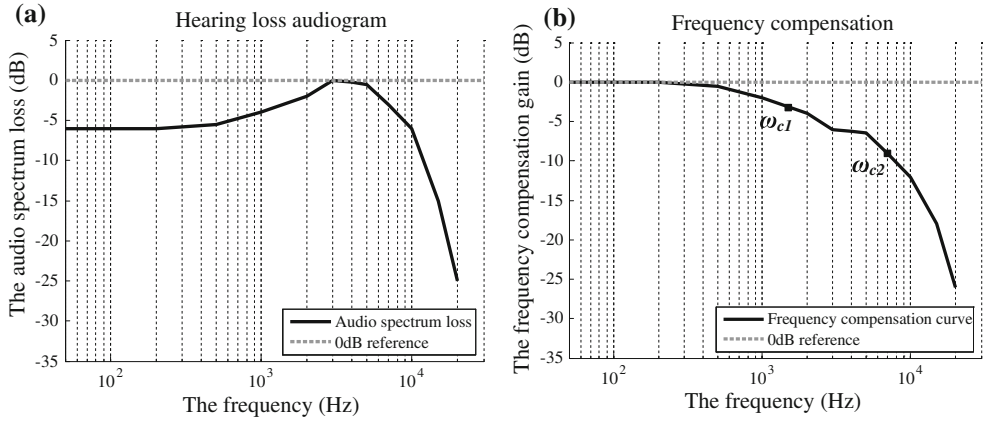

Fig. 4 **a** The diagram of the hearing loss. **b** The diagram of the frequency compensation

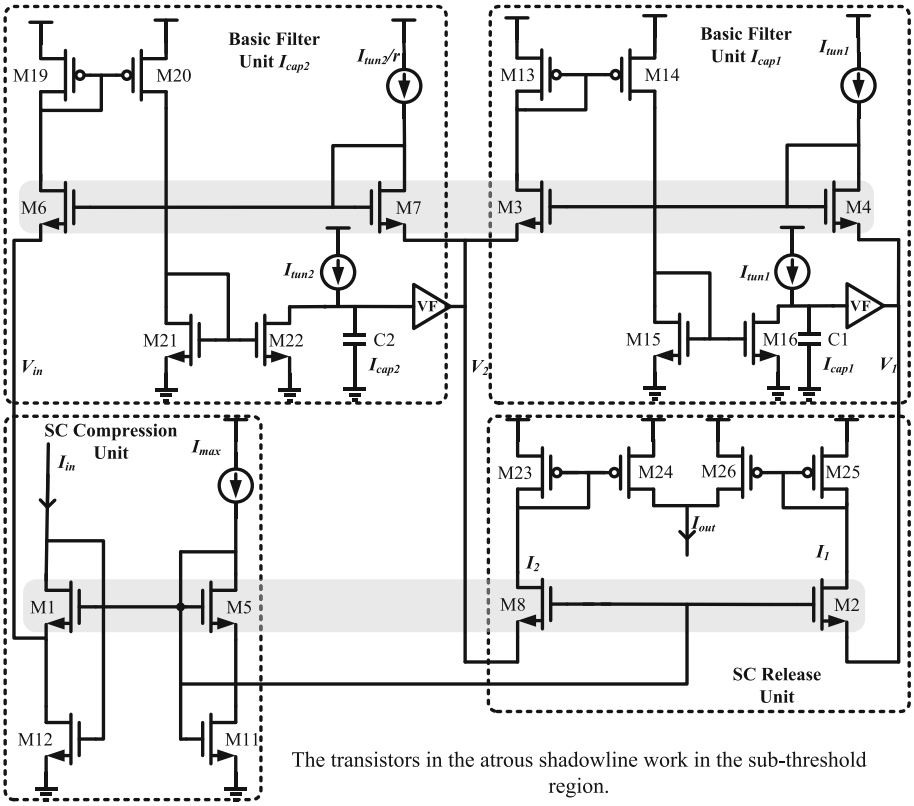

Fig. 5 The schematic diagram of the second-order filter

The transistors in the atrous shadowline work in the sub-threshold region.

Substituting the two-order state variable $\mathrm{I} = [I_1, I_2]$ into the Eq. (9), we have the final state space equation of the adaptive filter which can be directly transformed to the practical circuits, shown in the Eq. (11).

$$\begin{cases} I_{cap1} = I_{tun1} - I_{tun1}\exp[(V_1 - V_2)/U_T] \\ I_{cap2} = I_{tun2} - \dfrac{I_{tun2}}{r\exp[(V_2 - V_{in})/U_T]} \\ I_{out} = I_1 + I_2 \end{cases} \tag{11}$$

where $I_{cap1} = C_1 dV_1/dt$, $I_{cap2} = C_2 dV_2/dt$, $I_{tun1} = U_T C_1 \omega_{c1}$, $I_{tun2} = U_T C_2 \omega_{c2}$. I_1, V_1 and I_2, V_2 have the relationship based on the Eq. (3). The expression of I_{cap1} and I_{cap2} represents the basic state space equation responding to the basic filter unit of the current-mode adaptive filter. The detailed circuit of the filter is shown in the Fig. 5.

M1, M2, M3, M4, M5, M6, M7 and M8 work in the sub-threshold region. According to the Eq. (5), M1, M2 and M8 generate the interface compression voltage V_{in}, V_1 and V_2 responding to the input signal I_{in}, the state variable I_1 and I_2, respectively. M3, M4, M13, M14, M15, M16 and C1 realize the expression of I_{cap1} in the Eq. (7): the current I_{tun1} transforms to $I_{tun1}e^{(V_1-V_2)/U_t}$ through M3 and M4 and

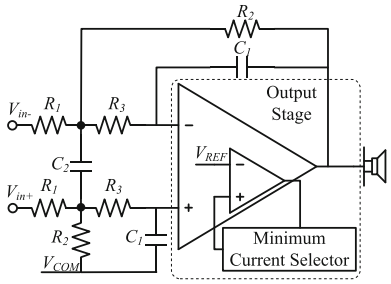

Fig. 6 The back-end circuit

Table 1 The component values of the filter

Component	Value (k Ω)	Component	Value
R_1	600	R_{LOAD}	16 Ω
R_2	300	C_1	25 p F
R_3	200	C_2	35 p F

then is subtracted from I_{tun1} on the top plate of C1, so does the I_{cap2}. Finally, the expression of I_{out} is realized by the current mirrors M23, M24, M25 and M26.

4 Driver circuit

The block diagram of the driver circuit with minimum current selecting technique is shown in the Fig. 6. In order to improve the capability of the noise rejecting, a second-order Rauch filter is embedded in it [13]. Its transfer function is

$$H(s) = \frac{-R_2/R_1}{2R_2R_3C_1C_2s^2 + (R_2 + R_3 + R_2R_3/R_1)C_1s + 1} \tag{8}$$

Assuming $R_3 = mR_2 = mR$ and $C_2 = nC_1 = nC$, the -3 dB cutoff frequency $\omega_{-3\ \mathrm{dB}}$ and the quality factor Q are

$$\begin{cases} \omega_{-3,dB} = \dfrac{1}{\sqrt{2R_2R_3C_1C_2}} = \dfrac{1}{\sqrt{2\,mn}RC} \\ Q = \dfrac{2R_2R_3C_1C_2\omega_{-3,dB}}{R_2 + R_3 + R_2R_3/R_1} = \dfrac{\sqrt{2\,mn}}{1 + 1.5\,m} \end{cases} \tag{9}$$

where the ratio of R_1/R_2 is equal to 2 because of the differential input. In order to get a good frequency and phase response, Q is set to $\sqrt{2}/2$. Since the frequency range of the common sound is between 100 and 10 kHz, the -3 dB cutoff frequency is chosen 10 kHz. Therefore, the passive components of the filter are listed in Table 1. And the impedance of the loudspeaker is 16 Ω.

The detailed schematic diagram of the output stage [14] is described in Fig. 7. It consists of three parts: a folded cascode amplifier, a minimum current selector and a class AB stage. The folded amplifier provides a voltage gain and the class AB stage provides the loudspeaker driving capability. A PMOS input stage (M1, M2) was selected for the input differential pair. The M3 and M4 are added to boost the impedance at the folding node. A diode-connected M5, together with M6, is used to bias the M3 and M4 so that the gate bias voltage can track the input common mode change. For 1 V operation, the output common-mode voltage is keep at 0.5 V to maximize the output swing. For the driver is a single-end structure, the DC point of the output node is stabilized by the feedback resistor R2. Moreover, a simple amplifier is embedded in the folded cascode amplifier so that the power can be reduced. The M14 and M15 not only are used to boost the output impedance as a cascade stage of the folded amplifier but also are selected for the differential input pair of the embedded amplifier. The transistor M20 offering a negative feedback path for the embedded amplifier, makes the M15's gate voltage follow the M14's and the drain node of the diode transistor M22 equal to V_{REF}. So the current through M22 is constant.

In order to control the quiescent current of the output stage and maintains a minimum current, the minimum current selector (M18–M22) is used [10]. M20 and M21 are used to sense the gate voltage change of output stage (M23, M24). M18 is biased in the triode region. Because M18, M19 and M20 are designed to share the same W/L and gate-source voltage, M18 and M20 could be considered as one transistor with the half W/L ratio of M19. Then, the current of M21 is twice of the current of M22. Thus, the quiescent current of output stage is given by

$$I_Q = \frac{W_{24}L_{21}}{W_{21}L_{24}}I_{21} = 2\frac{W_{24}L_{21}}{W_{21}L_{24}}I_{22} \tag{10}$$

where W_{21}, L_{21}, W_{24}, L_{24}, are width and length of M21, M24, respectively. The quiescent currents flowing in M21 and M22 are I_{21} and I_{22}.

As shown in Fig. 7, when one transistor of the output stage push out or pull in a large current, the standby current of the inactive transistor keeps to a minimum value because of the minimum current selector. If the output stage sources a large current by M23, the gate voltage of M23 and M20 becomes low so that M18 turns to operate in the saturation region. The current of M21 is equal to M22 since M18 and M19 operate as a pair of current mirror now. Because of the constant current of M22, the current of the inactive transistor M24 becomes half of quiescent current I_Q. On the other hand, if M24 pulls in a large current, the current of M21 becomes large consequently. The source voltage of M20 is pull up nearly to the positive supply voltage. Then, M23 and M20 form a current mirror. The mirror ratio between M23 and M20 is designed to be equal to the mirror ratio between M24 and M21. Thus, the current of the inactive transistor M23 is also $I_Q/2$.

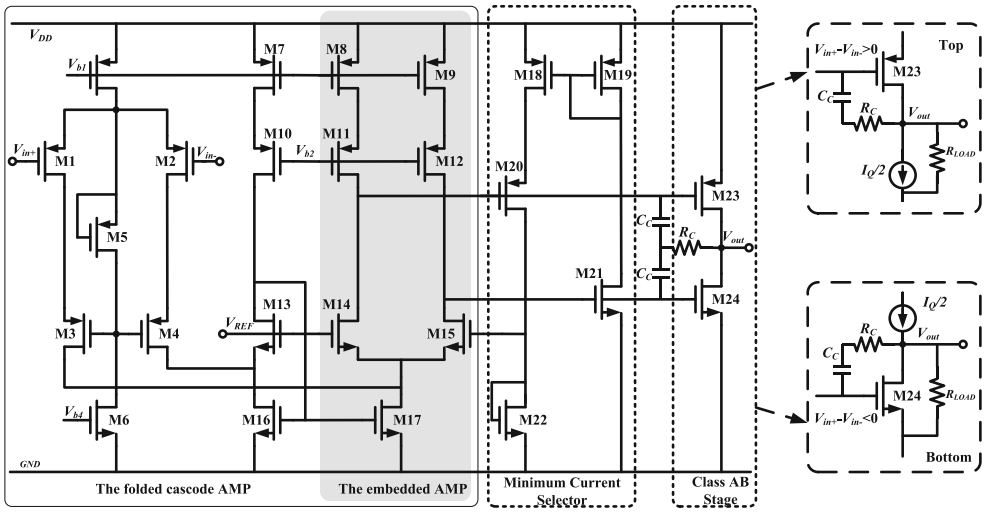

Fig. 7 The schematic diagram of the output stage

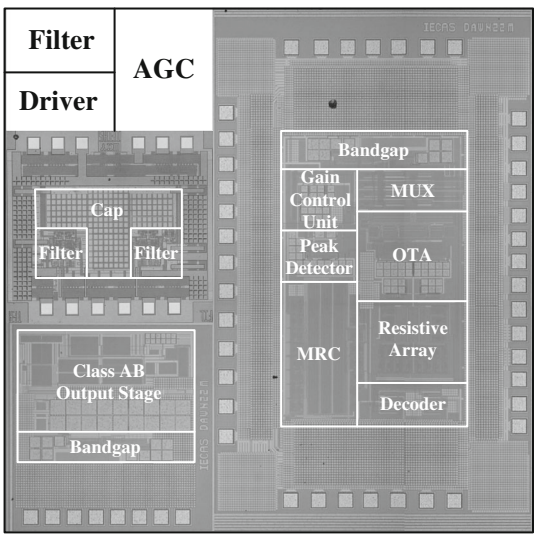

Fig. 8 The die micrographic of the analog hearing aid

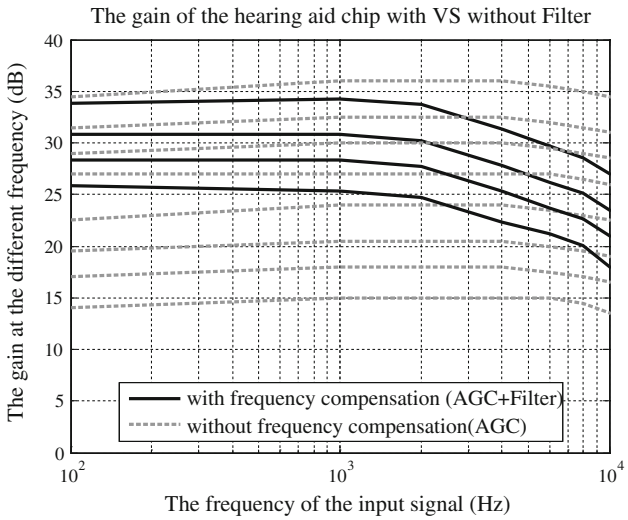

Fig. 9 The curve of the gain

The operation of the minimum current selector above results in the low power and little crossover distortion. The simulated result shows that the gain of this folded cascode amplifier is 69.7 dB and the GBW of the filter is about 1 MHz.

5 Measurement results

The analog hearing aid chip is fabricated in the standard 0.13 and 0.35 μm technology, and occupies 2.3 × 1.5 mm^2 (0.13 μm), 0.93 × 0.86 mm^2 (0.13 μm) and 1 × 1 mm^2 (0.35 μm) active die area for the AGC, driver and filter circuit, shown in Fig. 8. The whole chip is mounted on the printed circuit board (PCB) to be measured with 1 V supply voltage at a typical frequency 1 kHz.

The programmability of the hearing aid system is illustrated in Figs. 9, 10 and 11. The hearing aid has eight discrete gains (36, 33,…, 15 dB), four knee points (7, 9, 11, 13 mV) and four compression ratios (1:4, 1:6, 1:8, 1:12). This feature can greatly improve the flexibility of the hearing aid. Four representative gains (36, 33, 30, 27 dB) with frequency compensation are shown in the Fig. 9. It is seen that the filter with frequency compensation helps to compensate the common hearing loss in low frequency region and suppress the circuit gain in specified high frequency region which enhances comfortableness for hearing.

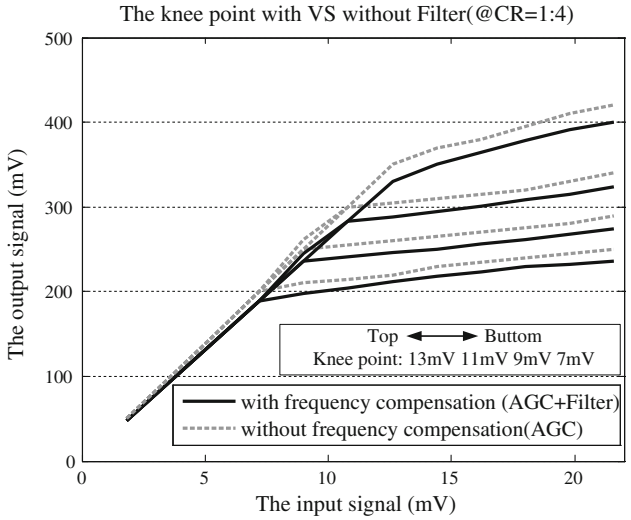

Fig. 10 The curve of knee point (@1 kHz)

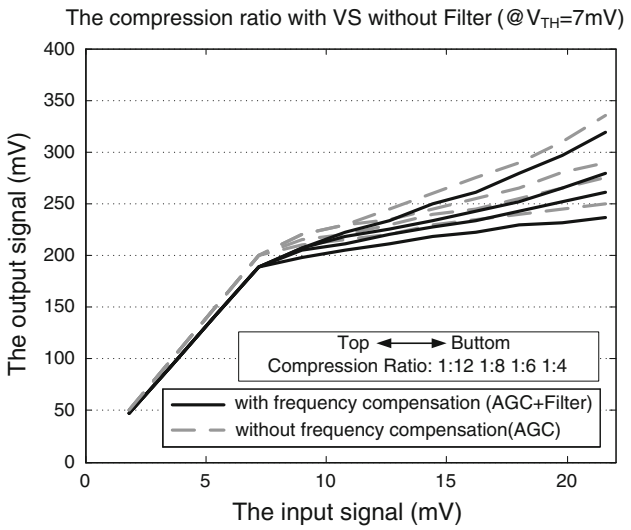

Fig. 11 The curve of compression ratio (@1 kHz)

Figure 10 shows the knee point measurement results with the fixed compression ratio of 1:4 and input signal frequency of 1 kHz. Through selecting different V_{TH} value, the knee points can be tuned from 7 to 13 mV. When input signal amplitude is larger than the setting knee point, the AGC works in the MRC-feedback mode. For example, when the compression ratio is set to 1:4 the gain of AGC is equal to 1/4. With the frequency compensation of the filter, a slight level shift is shown on the output signal due to the filter whose low-frequency gain is slightly smaller than 0 dB.

Figure 11 shows the compression ratio measurement results with input signal frequency of 1 kHz. When input signal amplitude is smaller than the setting knee point of 7 mV, the AGC works in the resistor-feedback mode and

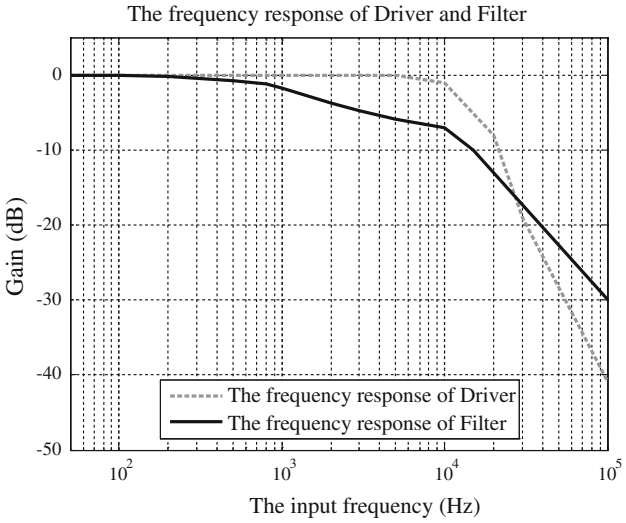

Fig. 12 The frequency response of filter and driver

the gains of the circuit are fixed. When input amplitude is larger than the knee point, AGC works in the MRC-feedback compression mode. The input signal is compressed through the AGC according the compression ratio setting.

The frequency response of the filter and driver is shown in the Fig. 12. With the implement of $C_1 = 110$ pF and $C_2 = 30$ pF, the frequency compensation is presented in the solid line. That is, the gain is around 0 dB in the range between 100 and 1 kHz and is about -5 dB in the range between 3 k and 10 kHz. Certainly, a transition band from 1 k to 3 kHz is needed. Besides, it is clear that the filter embedded in the driver is second-order from the dashed line, which can further improve the capacity of the noise rejecting.

The frequency response of the hearing aid is shown in the Fig. 13 with the solid line. Compared with the Fig. 12, the frequency compensation is enhanced with a stopband attenuation of 80 dB/dec. This is because the AGC also provides an attenuation of 20 dB/dec besides the filter and driver circuit. Therefore, the analog hearing aid can well match to the common low-frequency hearing loss shown in the dashed line.

Figure 14 shows the input-referred noise at the different gain. It is seen that the input-referred noise is below 5 μVrms in the spectrum from 100 Hz to 10 kHz. Figure 15 shows dynamic power dissipation of the hearing aid chip at the different input voltage. The power increases with the input amplitude. The static power (1.6 mV) at the 1 V operation also can be seen when the input amplitude is zero. Figure 16 shows the diagram of attack and release time. With an external capacitor of 400 nF and an internal capacitor of 5 pF, the chip allows the implement of $T_A = 100$ ms and $T_R = 20$ ms considering the human factors.

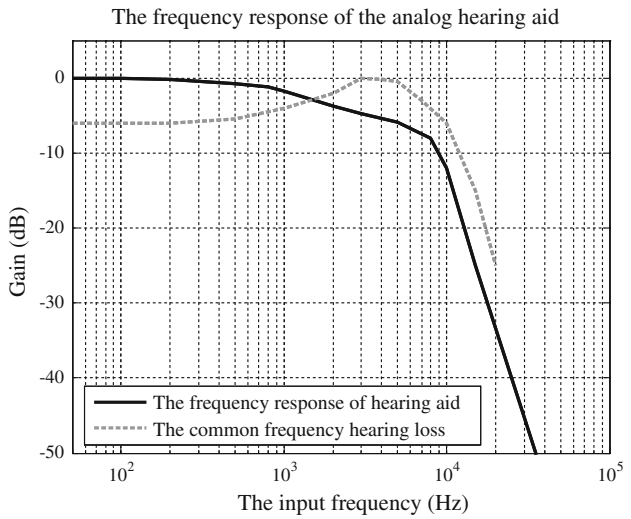

Fig. 13 The frequency response of the hearing aid

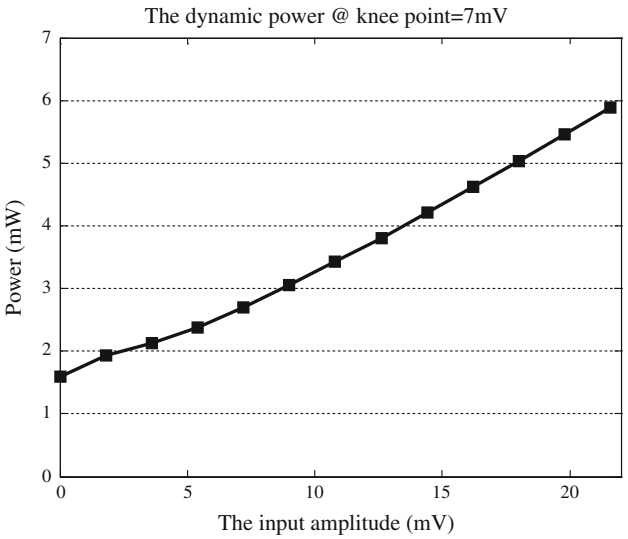

Fig. 15 The curve of dynamic power

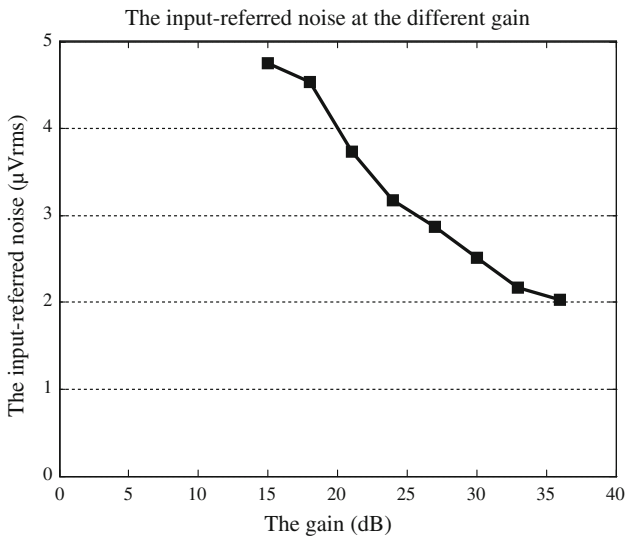

Fig. 14 The curve of input-inferred noise

Table 2 presents the performance comparison with the other works related to the hearing aid. The main point in this table is the function of frequency compensation. Therefore, a digital hearing aid [3] and an analog hearing aid [15] are selected for comparison. Compared with the conventional analog hearing aid, the fabricated analog hearing aid enables the accurate frequency compensation in the field of the common low-frequency hearing loss. The frequency compensation only appears in the DSP unit of the digital hearing aid. So, the analog hearing aid can well incorporate the human factors. Besides, the hearing aid can offer high programmability with discreet gain, knee point and compression ratio. Moreover, the input-referred noise of 5 μVrms is relatively small with the supply voltage of 1 V.

6 Conclusion

We fabricated an analog hearing aid chip considering the human factors. The current-mode filter integrated in the hearing aid can enable the frequency compensation to match to the degree of common low-frequency hearing loss. With the combination of the AGC and driver circuit, we can achieve a stopband attenuation of 80 dB/dec. The high programmable AGC uses the DMGC unit to improve the flexibility. It can offers eight gains (15, 18, …, 36 dB), four knee points (7, 9, 11, 13 mV) and four compression ratios (1:4, 1:6, 1:8, 1:12). With the capacitors of 400 nF and 5 pF, the attack time (100 ms) and release time (20 ms) is achieved according to the ear characteristics. The proposed chip has low input-referred noise (below 5 μVrms) with a supply voltage of 1 V. Therefore, it can well be accordant with the individual factors.

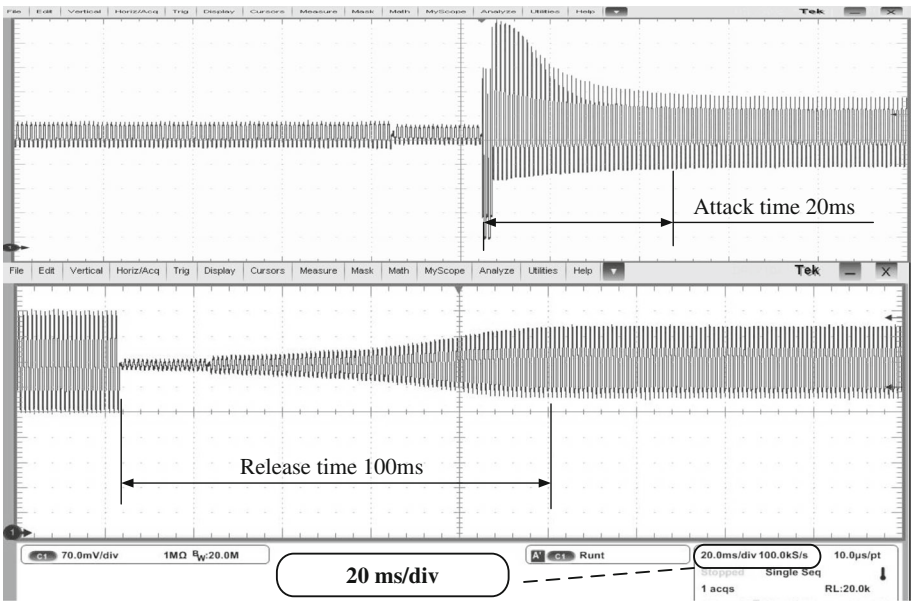

Fig. 16 The attack (*bottom*) and release (*top*) time

Table 2 Performance comparison

Reference	[3]	[15]	This work
Supply voltage	0.9 V	1 V	1 V
Programmability	High	Low	High
Noise	4.2 μVrms	6 μVrms	5 μVrms
Power	107 μW	300 μW	1.6 mW
Frequency compensation	√	×	√
Process	0.18 μm	0.25 μm	0.13 μm, 0.35 μm

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References

1. David, W., Mark, R., Tho, H., David, P., & James, N. (1992). A single-chip hearing aid with one volt switched-capacitor filter. In Proceedings of IEEE CICC, pp. 7.5.1–7.5.4.
2. Gata, D. G. (2002). A 1.1 V 270μA mixed-signal hearing aid chip. *IEEE Journal of Solid-State Circuit, 37*(12), 1670–1678.
3. Kim, S., Lee, S. J., Cho, N., Song, S.-J., & Yoo, H.-J. (2008). A fully integrated digital hearing aid chip with human factors considerations. *IEEE of Solid-State Circuits, 43*, 266–274.
4. Silva-Martinez, J., Solis-Bustos, S., & Schellenberg, M. (1999). A CMOS hearing aid device. *Analog Integrated Circuit and Signal Processing, 21*, 163–172.
5. Li, F., Yang, H., Liu, F., Yin, T., & Wang, X. (2012). Dual-mode gain control for 1 V CMOS hearing aid device with enhanced accuracy and energy-efficiency. *Analog Integrated Circuits and Signal Processing, 72*, 495–504.
6. Gata, D. G., & Sjursen, W. (2002). A 1.1-V 270-μA mixed-signal hearing aid chip. *IEEE Journal of Solid-State Circuits, 37*, 1670–1678.
7. Samet, M., Masmoudi, M., & Mouine, J. (1998). A new single chip automatic gain control for hearing aids. *Proceedings of IEEE Canadian Conference of Electrical and Computer Engineering, 2*, 758–761.
8. Kim, S., Lee, J.-Y., Song, S.-J., Cho, N., & Yoo, H.-J. (2002). An energy-efficient analog front-end circuit for a sub-1-V digital hearing aid chip. *IEEE Journal of Solid-State Circuits, 42*(4), 876–882.
9. Kim, S., & Lee, J.-Y. (2005). A 0.9 V 67 μW analog front-end using adaptive-SNR technique for digital hearing aid. *IEEE International Symposium on Circuits and Systems, 1*, 740–743.
10. Razavi, B. (2001). *Design of analog CMOS and integrated circuits*. New York: McGraw-Hill Companies Inc.
11. Gan, R. Z., Feng, B., & Sun, Q. (2004). Three-dimensional finite element modeling of human ear for sound transmission. *Annals of Biomedical Engineering, 32*(6), 847–859.
12. Katsuhiko, O. (2002). *Modern control engineering*. Upper Saddle River: Prentice-Hall Inc.
13. Kyehyung, L., Qingdong, M., et al. (2009). A 0.8 V, 2.6 mW, 88 dB dual-channel audio delta-sigma D/A converter with headphone driver. *IEEE Journal of Solid-State Circuits, 44*(3), 916–927.
14. de Langen, K.-J., & Huijsing, J. H. (1998). Compact low-voltage power-efficient operational amplifier cells for VLSI. *IEEE Journal of Solid-State Circuits, 33*(10), 1482–1496.
15. Serra-Graells, F., Gomez, L. & Farres, O. (2001). A true 1 V CMOS log-domain analog hearing-aid-on-a-chip. *ESSCIRC 2001, Proceeding of the 27 European, 405–408*.

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