Design and Analysis of a Novel Automatic Gain Control Pre-Amplifier Circuit for Hearing Aid Device

Rahul Kumar Singh
National Institute of Technology
Hamirpur, India
rahul.k.singh.2021@gmail.com

Rohit Dhiman
NIT Hamirpur, E&CE Department
Hamirpur, India
rohitdhiman.nitham@gmail.com

Rajeevan Chandel
NIT Hamirpur, E&CE Department
Hamirpur, India
rchandel@nith.ac.in

***Abstract*—In the present paper a novel automatic gain control pre-amplifier for hearing aid device is proposed and analyzed. The proposed design utilizes feedback and feed forward loop in order to control the gain of the device. Input and output thresholds have been accommodated to provide dual control. The weak input signal is amplified in three modes. High gain for low input and low gain for high input forms the basis of amplification. The measured average power dissipation of the complete pre-amplifier is 410 µW with a dual power supply of ±0.7 V in 180 nm technology node. Frequency of operation is up to 20 kHz.**

Keywords- Automatic gain control; cochlear device; fully differential Operational Amplifier; hearing aid; pre-amplifier.

I. INTRODUCTION

Digital hearing aids are now a preferred choice for cochlear devices. These devices utilize analog to digital converter (ADC) and digital signal processing (DSP) techniques (Fig. 1) in order to process the data digitally. Digital processing involves filtering of data in different bands which enables some key features such as noise and echo cancellation. Several attempts have been reported in literature to make a low power, high performance hearing aid [1-6]. All these devices require a programmable front end which consists of a pre-amplifier unit and an ADC. Reconfigurable ADCs are in demand presently for hearing aid applications and these have been utilized beautifully by researchers [7-8]. These ADCs often employ clock sources to reconfigure the ADC. Till now these clock sources are limited to ADCs only but there is a good scope that these can be utilized to reconfigure the pre-amplifier architecture also. In this work clocks have been routed to pre-amplifier circuit. Thus here a pre-amplifier is presented with convertible feedback and feed forward loop control. This pre-amplifier unit has dual function of controlling the gain as well as amplifying it faithfully. Pre-amplifier consists of a fully differential amplifier, MOS resistive circuit, comparator switches and voltage generator circuit. In section II Pre-amplifier architecture has been presented, section III describes the fully differential Operational Amplifier and close loop behavior with MOS resistive circuits. Section IV discusses the switching circuit, logic control and voltage generation circuit. Section V presents the measured results, their analysis and future scope of work.

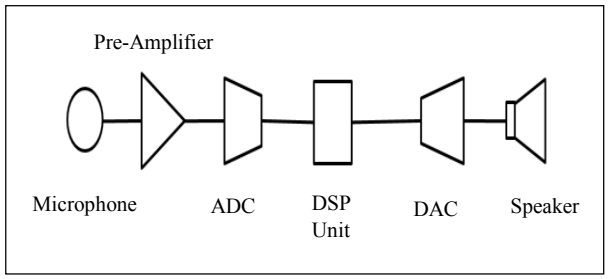

Figure 1. Block diagram of a digital hearing aid device.

II. PRE-AMPLIFIER ARCHITECTURE

Fig. 2 shows the block diagram of the complete pre-amplifier circuit. A differential input is fed to the MOS resistive circuit which acts as a variable resistor. Value of resistance can be changed by varying the control voltage input (VC) of MRC. Both MRC1 and MRC2 combine with Operational Amplifier (Op Amp) to make a close loop amplifier. To vary the gain of this amplifier, a control voltage is fed to MRC2 by control voltage circuit which generates some pre-defined voltages depending on the logic provided by switching circuit. Switching circuit has the responsibility to detect the input and output voltage levels and compare them with the desired threshold voltages. Based on the comparison it produces logic bits which help in generating the desired level of control voltage.

Some clocking mechanism is needed for switching. For this two clock signals have been used to switch between input and output signals. Thus any variation from input or output side can be detected easily and hence gain can be stabilized accordingly.

III. FULLY DIFFERENTIAL OPERATIONAL AMPLIFIER

Hearing aids are affected by noise. Therefore a fully differential Operational Amplifier is needed in order to reduce the effect of noise. Fig. 3 shows schematic of a fully differential Operational Amplifier. Design of this Op Amp is same as of a simple two stage Op Amp except the Common Mode Feedback (CMFB) circuit. Common mode feedback is needed to control the common mode signal which arises due to imbalance in current at the output stage of Op Amp. Two common mode feedback

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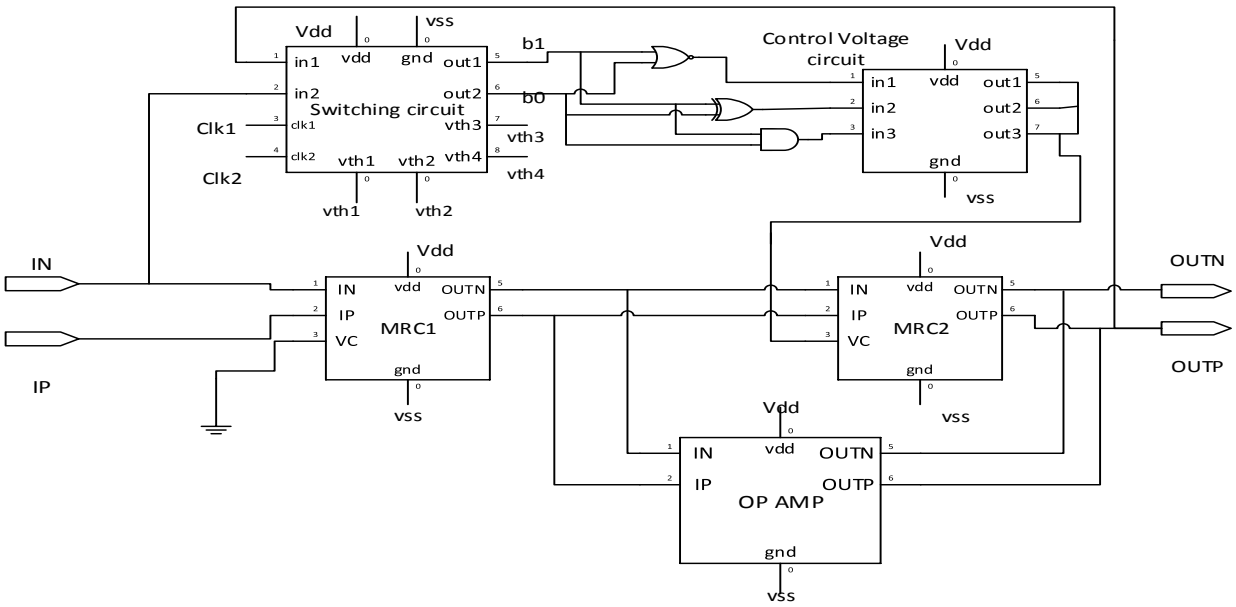

Figure 2. Block diagram of complete Pre-Amplifier.

detectors are needed at point CMFB1 and CMFB2 (Fig. 3) [9]. CMFB1 has an NMOS input detector which is actually a differential amplifier itself to detect the common mode inputs whereas CMFB2 needs a PMOS. Two RC pairs have been included at each CMFB detector where resistors are used for common mode detection and capacitors for frequency compensation. At each detector a common mode input (Cm1 and Cm2) is needed. Generally Cm2 is half the power supply value. Cm1 is kept such that it supplies the same amount of current as in M13 at the output stage of Op Amp (Fig. 3) [10].

Voltage gain and power dissipation of two input detector stage op amp can be given by the following expressions [11]

$$A_v = \frac{2g_{m4}g_{m13}}{I_5(\lambda_4+\lambda_1)(\lambda_{13}+\lambda_{14})} \quad (1)$$

$$P_{diss} = (I_5 + I_{13})(Vdd + |Vss|) \quad (2)$$

where g_m is transconductance of MOS, I is current flowing through device, λ is the channel length modulation index, V_{dd} and V_{ss} are power supply to the circuit. All the subscript refer to the MOS numbers as shown in Fig. 3.

Gain of fully differential amplifier differs from Eq. (1) due to extra CMFB circuit used in the present design. Gain decreases and power dissipation increases from computed values of the two stage Op Amp.

To vary the gain of amplifier variable resistors are needed. For such purpose two MOS resistive circuits (Fig. 1) have been used as variable resistors so that gain can be varied. A MOS resistive circuit consists of an array of transistors connected together to work as variable resistor. Schematic of circuit is shown in Fig. 4. Resistance of such a MOS resistive circuit can be given as [12]

$$R = \frac{L}{(\mu_n C_{ox} W(V_1 - V_2))} \quad (3)$$

where R is resistance of MOS resistive block, W/L is aspect ratio of MOS used, V_1 and V_2 are control voltages of the circuit.

III. SWITCHING CIRCUIT

Switching circuit detects the input and output signals and produces logic bits in order to maintain proper gain. It consists of four threshold inputs vth1, vth2, vth3 and vth4. vth1 and vth3 represent thresholds for input side whereas vth2 and vth4 represent threshold voltages for output side (Fig. 2). Fig. 5 represents the one of the comparator stage used in switching circuit. Two complementary clock sources clki and clko have been used in the circuit. When clki is on MOS M1 and M3 are on and M2 and M4 are off. Thus one input terminal of comparator is connected to the coming input signal and other is connected to the threshold vth3. Output logic bits are observed corresponding to the levels of input signal. In this configuration circuit works as feed forward loop. When clko is on, clki is off, input signal is detached from switching network. M2 and M4 conduct while M1 and M3 are in off condition. Now input terminals of comparator are connected to the feedback from output side and threshold vth4 respectively. This time circuit behaves as feedback circuit. Thus during each clock pulse feed forward and feedback paths are established alternatively and logic bits are observed at the output of comparator. This switching enables the circuit to

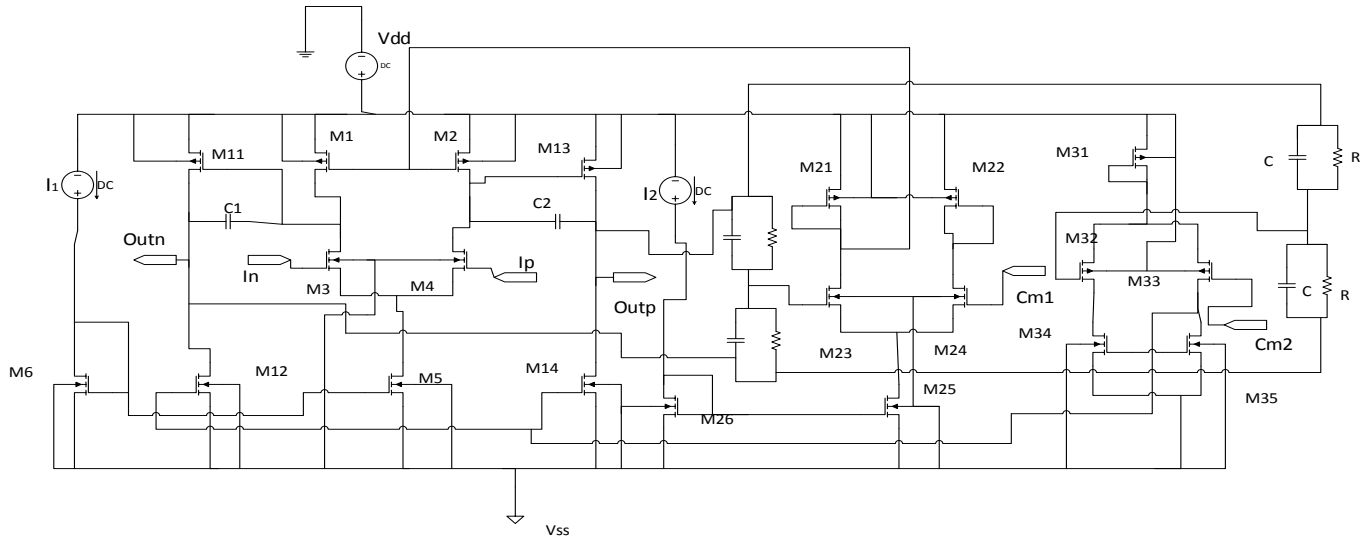

Figure 3. Schematic of a fully differential Operational Amplifier.

establish convertible feedback and feed forward paths. Two logic bits have been utilized in the present work and for this two comparator stages have been used. Continuous switching affects the output swing of the comparator switch and this leads to false triggering. Consequently, buffers have been used after the comparator stage to restore the signal. There are three possibilities from control bits that may arise. As a result three logic gates have been used to identify each possible logic levels individually (Fig. 1). Output of each gate is connected to separate input of the control voltage circuit. These control inputs manage the control signal to the fully differential amplifier and each input corresponds to a different control voltage output which varies the gain of the amplifier.

A. Voltage Generation Circuit

Three ranges of control voltages are needed to vary the gain in three modes. Fig. 6 shows the schematic of one of voltage generation circuit. A constant current source and a gate to drain connected MOS which works as a resistor, completes this circuit. Voltage generated depends on the aspect ratio of MOS and the current source. One extra MOS (M32) is attached at the output which acts as a switch. Input to this MOS is derived from the switching circuit. If input is high then only this control voltage will be available to the MRC circuit. Three such circuits have been used for control voltage generation. Output voltage of this circuit can be given by

$$Out_3 = V_{th} + V_{DS(sat)}(M32) + \sqrt{\frac{2I_D}{K'\frac{W}{L}}} \qquad (4)$$

where out_3 is the output control voltage from MOS M32, V_{th} is the MOS threshold voltage of MOS M3, $V_{DS(sat)}(M32)$ is drain to source saturated voltage of MOS M32, I_D is drain current, K' is transconductance parameter and *W/L* is the aspect ratio of MOS M3.

V. RESULTS AND DISCUSSION

CMOS 0.18µm process technology node has been used to design the circuit. It operates on ±0.7V power supply. Op Amp designed has a gain of 33 dB and CMRR is of 40 dB. Measured power dissipation for Op Amp is 70µW. Its gain bandwidth characteristics has been shown in Fig. 7.

Input to pre-amplifier has been chosen based on the observations from [7] and it varies from 1mV to 100mV. Frequency of operation is up to 20 kHz. Two complementary clocks of 5 kHz have been used for switching purpose. Clk1 and Clk2 enables us to switch between thresholds. Four thresholds have been chosen for such purpose, vth1 and vth3 for input side and vth2 and vth4 for output side. Values for vth1, vth2, vth3 and vth4 are 25 mV, 0.3V, 85 mV and 0.65 V respectively. At a given point of time only two thresholds remain active. These thresholds helps circuit in reconfiguration such that when input signal is low switching circuit detects it and produces logic bits 00 and corresponding to these bits a fixed and unique control voltage (VC) is generated by voltage generation circuit which in this case is 0.48V. Using these two bits three cases are possible to operate circuit in three different gain stages. These modes, control bits, control voltages and distribution of gain have been shown in Table I.

TABLE I. Gain Characteristics for Different Stages of Input Signal

Input	**Control bit (b1 b0)**	**Control voltage (VC)**	**Gain**
V_{in} < 35mV	00	0.48 V	High
35mV<V_{in}<85mV	01	0.59 V	Moderate
V_{in}>85mV	11	0.68 V	Low

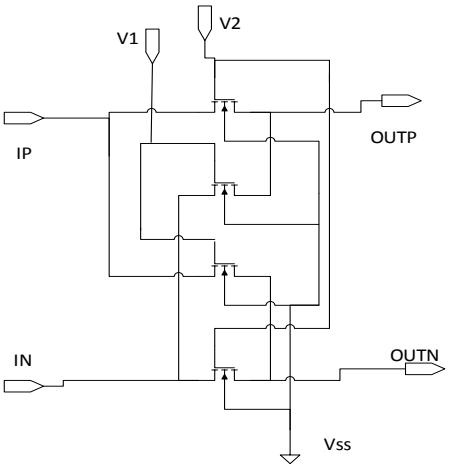

Figure 4. Schematic of a MOS Resistive Circuit (MRC).

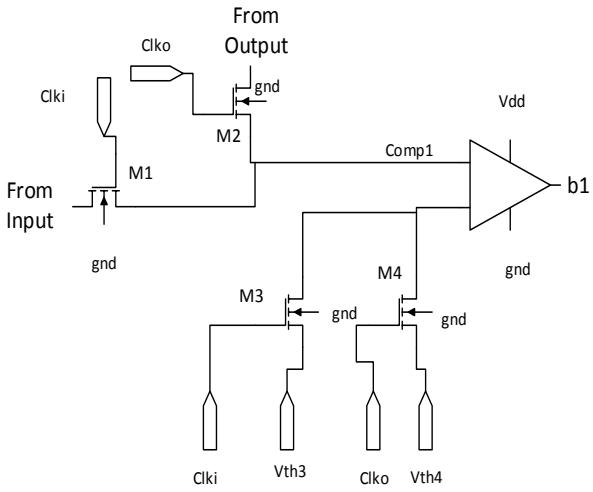

Figure 5. One of the comparator stage used in switching circuit.

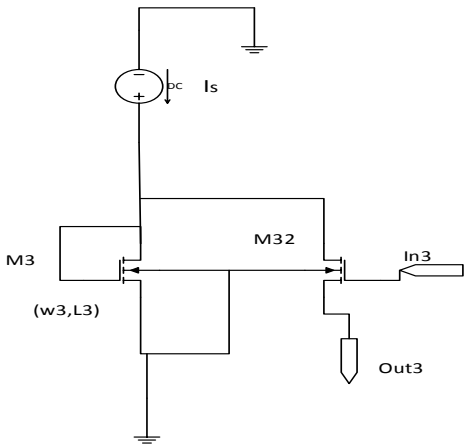

Figure 6. Schematic of a voltage generation circuit block.

Fig. 8 shows input output waveform of pre-amplifier for input of 90 mV. Here output waveform is amplified approximately 7.66 times the input signal. When input is 90mV then bit b1 remains high for all times, whereas b0 remains high only when feedback loop is active i.e. clki is low (Fig. 9). When clki is on feed forward loop becomes active and some transitions occur due to low input. For this range of input control voltage should be 0.68V as shown in Fig. 9. When input signal is low for instance 30mV the proposed circuit adapts itself and gain is increased to 22.33 times the input signal as shown in Fig. 10. This confirms the circuit operation as discussed in Table 1. Fig. 11 represents gain bandwidth characteristics of the complete pre-amplifier circuit. It shows stability of complete system and depicts that system has stable gain for desired range of frequencies.

VI. CONCLUSION

Pre-amplifier circuit has been designed, simulated, tested and analyzed for different range of inputs. It performs well for all the ranges considered. Switching between feed forward and feedback operations enables circuit to adjust quickly for various changes in input. Although switching contributes some increase in power dissipation but this can be solved by introducing some low power design techniques. The same shall be carried out further to enhance the performance of the designed circuit.

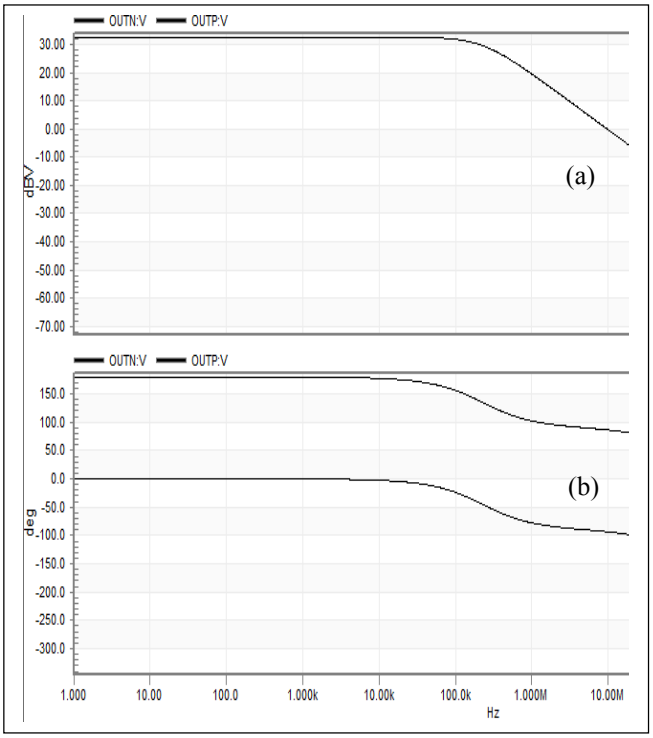

Figure 7. Fully differential amplifier gain bandwidth characteristics. (a) Magnitude characteristics and (b) Phase characteristics.

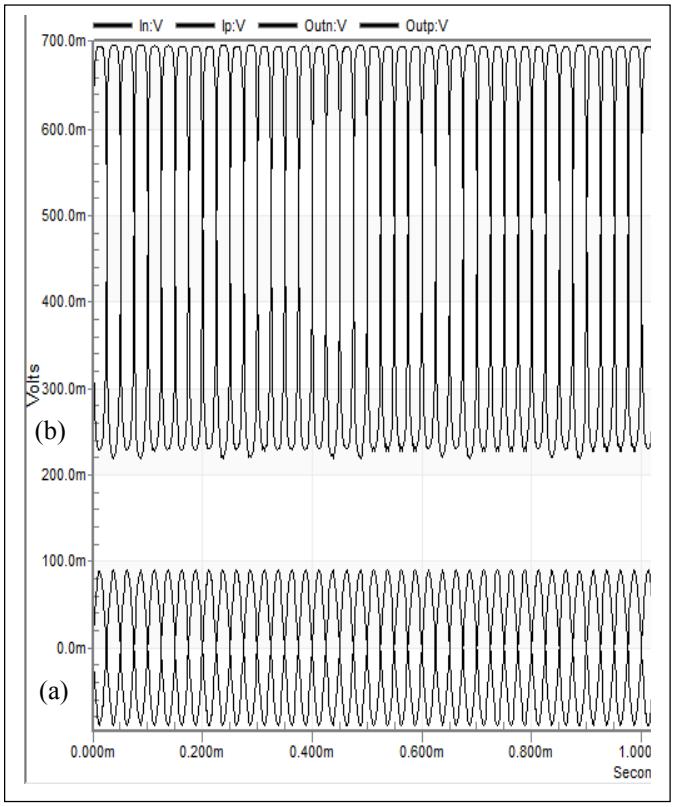

Figure 8. Pre-amplifier input output characteristics for 90 mV input. (a) Input signal to pre-amplifier (b) Amplified output of pre-amplifier.

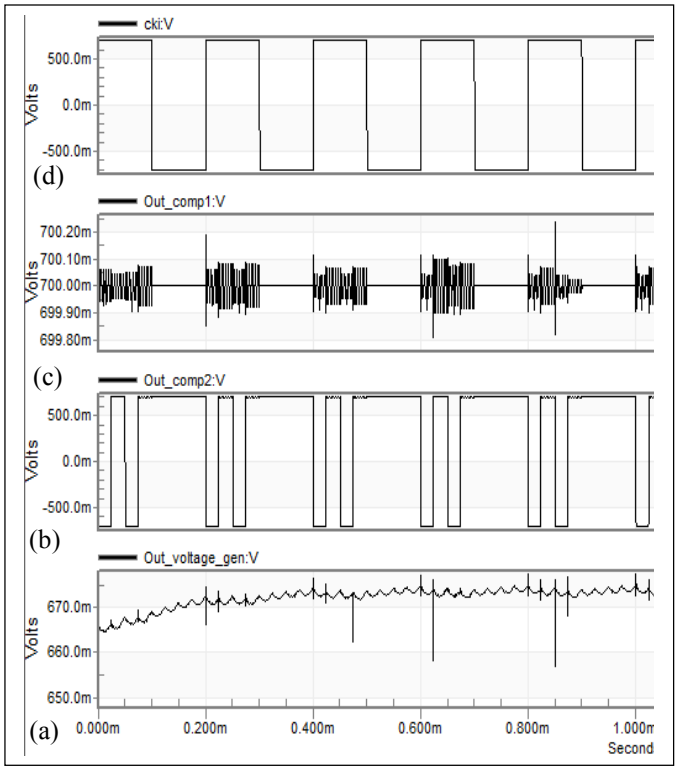

Figure 9. Pre-amplifier control bits and voltage control signals for 90 mV input. (a) Control voltage (VC) signal (b) Control bit b1 (c) Control bit b0 (d) Clock signal clki.

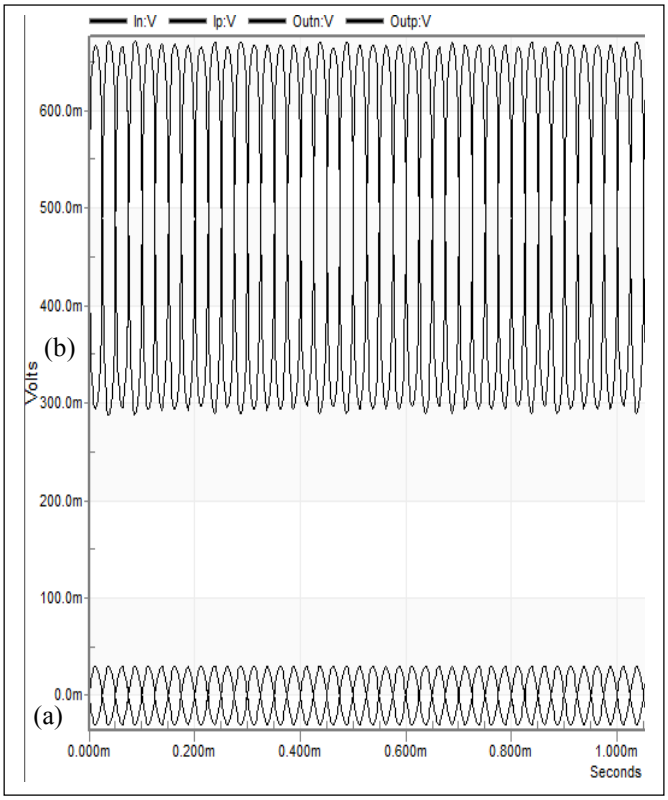

Figure 10. Pre-amplifier input output characteristics for 30 mV input. (a) Input signal to pre-amplifier (b) Amplified output of pre-amplifier.

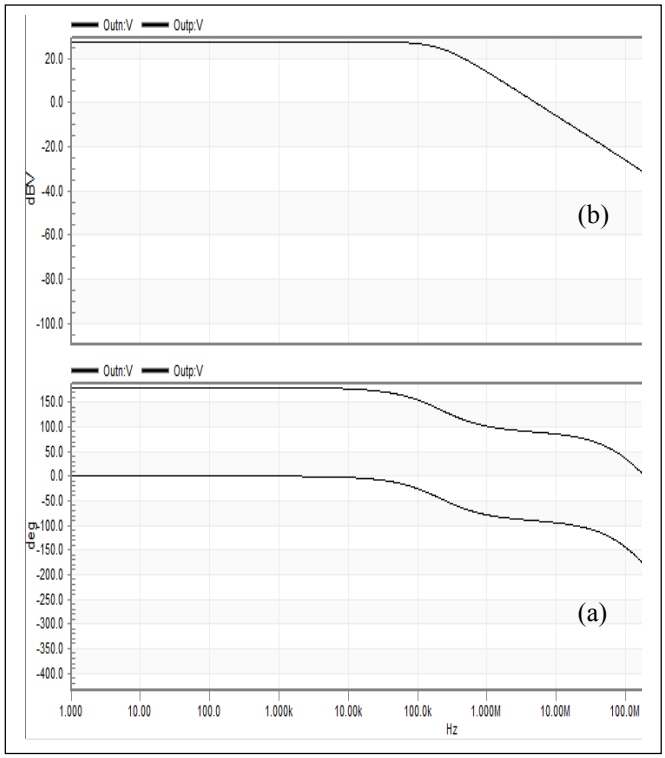

Figure 11. Pre-amplifier gain bandwidth characteristics. (a) Phase characteristics (b) Magnitude characteristics.

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