A Mixed-Mode Variable Gain Amplifier for Hearing Aid Devices

Manu Chilukuri, Sungyong Jung
Electrical Engineering Department, University of Texas Arlington
Texas, USA
manu.chilukuri@mavs.uta.edu, jung@uta.edu

***Abstract*—A mixed mode variable gain amplifier for hearing aid application is presented. It consists of main amplifier stage and a gain control circuit. Based on the output of microphone, voltage levels are categorized into two gain regions and designed circuit automatically sets the close loop gain of main amplifier. Main amplifier consists of opamp with feedback resistors and gain control circuit consists of peak detector, high speed comparator and XNOR gate. Due to high speed digital control circuitry, attack and release time are as small as 60µSec which is 33 times faster than temporal resolution of human hearing. Along with preamplifier, proposed circuit achieves a gain range of 45dB to 65dB and offers an input referred noise of 0.13µVrms, with peak SNR of 77dB and consumes a power of 172µW from 1.8V supply. Circuit is designed in 0.18µm CMOS process and occupies an area of 493µm × 184µm.**

***Index Terms*—Hearing aid, piezoelectric microphone, Automatic Gain Control, Opamp.**

I. Introduction

It has been reported by the World Health Organization that over 5% of world's population have a disabling hearing loss due to problems in the hearing pathway [1]. Sensorineural hearing loss occurs due to damage to cells in inner ear which transmit signals to brain for processing the sound. Although it can be corrected by using hearing aid devices, the global production of hearing aids is about 10% below the total demand. Hearing aids have been improved to accommodate direction functionality and facilitate improved speech recognition. However, multiple microphones are used to detect sound and its direction which needs additional readout circuits for processing thereby increasing the power consumption of the device. Kuntzman et al. [2, 3] proposed a novel piezoelectric microphone which mimics the auditory system of Ormia ochracea. It consists of a semi-rigid beam which rotates in response to pressure gradient. Four ports are provided with two input ports for left and right direction and two output ports to measure the corresponding voltage. By using a DSP processor, an algorithm can be implemented to detect effective direction of the signal. Some of the other advantages of piezoelectric microphones are high linearity and sensitivity. However, these microphones tend to produce signals of very small amplitudes which could be susceptible to noise. Several designs [4-11] have been proposed to achieve high SNR and low noise to ensure processing of signals with high accuracy. Most commonly, resistor-feedback type VGA is used for amplifying microphone signals and a DSP processor is programmed to control the gain of VGA. Based on the output of ADC, appropriate feedback resistor is selected to set the gain corresponding to the output of microphone. However, the attack and release time are large due to processing delays. In [5], Mos-Resistive Feedback (MRC) employs a MOS-Resistive-Feedback (MRF) structure and a gain control unit to achieve high accuracy and dynamic range. Some of the limitations of the circuit are limited output swing and poor noise performance. In [11], manual gain control VGA is designed. Based on the output of microphone, the operating modes of cascode transistors is switched between saturation and triode to adjust the gain. Disadvantage of this architecture is gain cannot be controlled accurately since it involves manual setting of control voltage. Also, since gate voltage of cascode transistors is changed to select the operating region, output DC level keeps shifting with change in control voltage and is unstable.

In this paper, a low noise, compact and mixed mode VGA is presented. On chip gain control circuit is designed to ensure fast processing of signals. Design is optimized to reduce noise. Due to very low input referred noise, signals in the range of nano-volts can be processed efficiently. In addition, employing high speed digital control circuit ensures very small attack/release time for controlling the gain of main amplifier, thereby, reducing processing delays. Section II explains design of proposed circuit. Section III highlights the simulation and chip test results. Section IV concludes the paper.

II. Proposed Circuit

Fig. 1 shows the characterization plot of novel piezoelectric microphone where x-axis is the sound pressure level and y-axis is corresponding output voltage of the microphone. It is observed that above 106dBSPL, the response of microphone is exponential. Thus, two gain regions are identified. Region A corresponds to the sound pressure levels below 106dBSPL and require high gain setting of main amplifier. Region B corresponds to sound pressure levels above 106dBSPL and require minimum gain setting of main amplifier.

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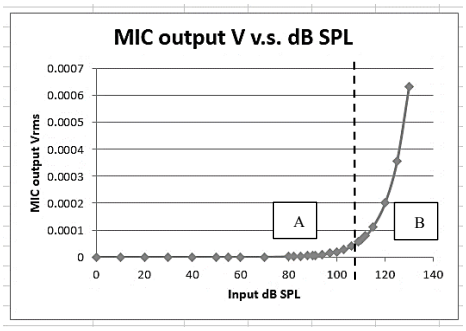

Fig. 1. Microphone Characterization

Fig. 2 shows the block diagram of designed Analog Front End employing the proposed VGA circuit. There are two sections in VGA a) a variable gain amplifier stage and b) gain control circuit to adjust close loop gain of main amplifier stage, based on the input signal. Gain control circuit (GCC) consists of a peak detector, comparator and XNOR gate. Peak detector acts as an rms-to-dc rectifier by converting sinusoidal preamplifier amplifier to a DC signal. If this DC level is smaller than the comparator's reference voltage, GCC is inactive. However, if the output of peak detector is higher than comparator's reference voltage, comparator output is set to logic 1 (1.8V). The output of XNOR gate is high when both the inputs are at logic 0 or logic 1. For signals in Region B, output of both comparators is logic 1 thus setting the output of XNOR gate to logic 1. As a result, NMOS switch S1 is turned on and the feedback resistor R3 is connected in parallel to R2. Value of R3 is chosen such that effective feedback resistance is same as R1. Therefore, close loop gain of VGA is set to unity for large input signals. Complex logic architecture is used to implement XNOR gate. Due to high speed digital control circuit, attack and release time (AT and RT) for VGA are as small as 60µSec. This is about 33 times faster than the temporal resolution of human hearing and 330 times faster than [9], which has AT and RT of 20mSec and 100mSec respectively. The VGA output is then fed to a second order ΔΣ ADC which filters out quantization noise from the frequency band of interest, leading to high SNR and accuracy.

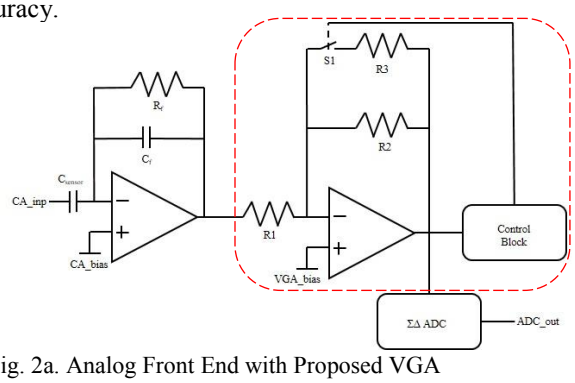

Fig. 2a. Analog Front End with Proposed VGA

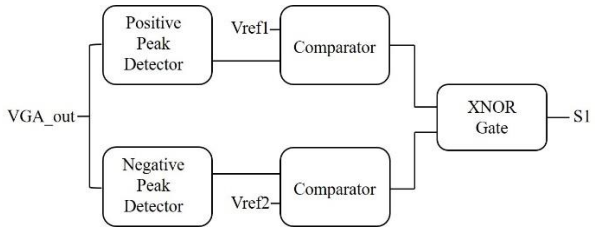

Fig. 2b. Gain Control Circuit

Fig. 3 shows schematic of opamp. Two stage opamp is used to achieve high gain, consume low power and achieve wide output swing. A shunt-feedback output stage [12] is used to achieve rail to rail output swing and reduce output impedance of opamp. This is essential in order to use smaller feedback resistor values, resulting in lower thermal noise due to the resistors. Designed opamp is further optimized to improve noise performance. Major sources of noise are transistors in the signal path and feedback resistors. Since the frequency range of interest is from 1Hz to 20kHz, the focus is on reducing flicker noise as it is more dominant than thermal noise. (1) shows input voltage noise spectral for gain stage.

$$\overline{V_{n,tot}^2} = \left[\left\{\frac{16kT}{\sqrt[3]{2\mu_n c_{ox}\left(W_1/L_1\right) I_{DS1}}}\right\} \times \left\{1 + \sqrt{\frac{2\mu_p\left(W_3/L_3\right)}{\mu_n\left(W_1/L_1\right)}}\right\}\right] + \left[\left\{\frac{2k_{fn}\Delta f}{c_{ox}(W_1 L_1) f}\right\} \times \left\{1 + \frac{2\mu_p k_{fp} L_1^2}{\mu_n k_{fn} L_3^2}\right\}\right] \quad (1)$$

(2) shows the noise spectral for output stage circuit.

$$\overline{V_{n,tot}^2} \approx \left[\left\{\frac{16kT}{\sqrt[3]{2\mu_n c_{ox}\left(W_{11}/L_{11}\right) I_{DS11}}}\right\} \times \left\{1 + \sqrt{\frac{\mu_p\left(W_{13}/L_{13}\right)}{\mu_n\left(W_{11}/L_{11}\right)}}\right\}\right] + \left[\left\{\frac{2k_{fn}}{c_{ox}(W_{11} L_{11}) f}\right\} \times \left\{1 + \frac{\mu_p k_{fp} L_{11}^2}{\mu_n k_{fn} L_{13}^2}\right\}\right] \quad (2)$$

Thus, by increasing size of input transistors and decreasing the size of PMOS load devices, noise contribution is minimized.

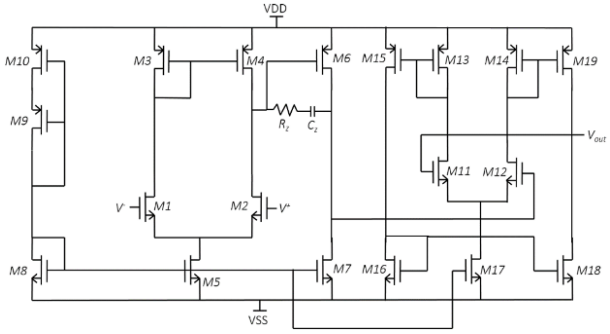

Fig. 3. Opamp Design

III. Simulation And Test Results

Fig. 4 shows the frequency response of designed opamp. It achieves a gain of 90dB, phase margin of 64˚ and an output swing of 0V to 1.71V. Designed VGA has a THD of 0.13% and consumes a power of 172µW from 1.8V supply. Fig. 5 shows the frequency response of VGA. Along with the preamplifier, designed AFE has a gain range of 45dB to 65dB. Fig. 6 shows the noise spectrum measured at the output node of VGA. Integrating over a frequency range from 1Hz to 20kHz, the output noise is calculated to be 23µVrms. Thus, the equivalent input referred noise is 0.13µVrms and calculated SNR is 77dB. Fig. 7 shows the fabricated chip with proposed circuit highlighted. Proposed circuit occupies an area of 493µm × 184µm, including bondpads which have a size of 67µm × 67µm each.

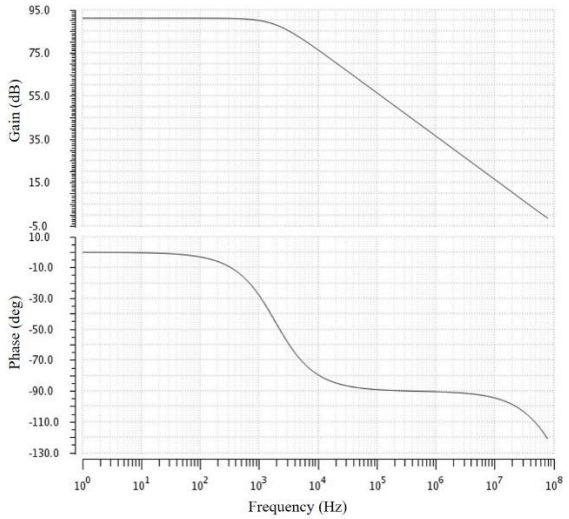

Fig. 4. Frequency Response of Opamp

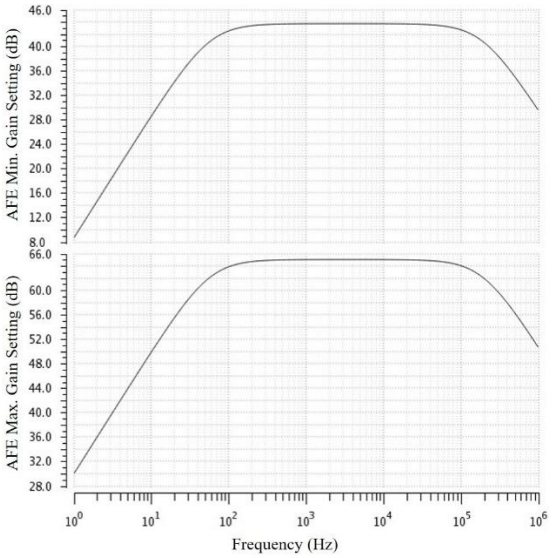

Fig. 5. AFE Frequency Response

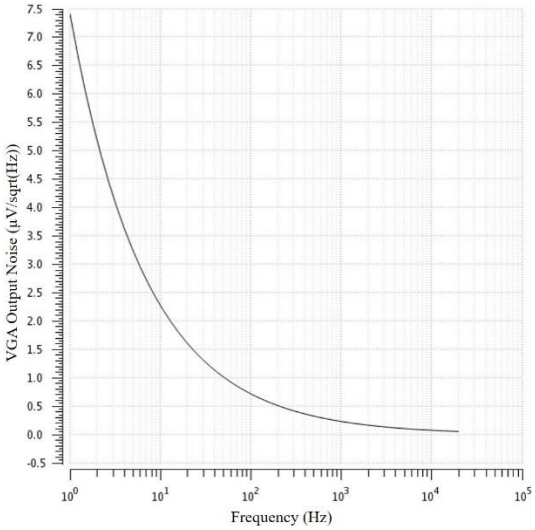

Fig. 6. VGA Output Noise

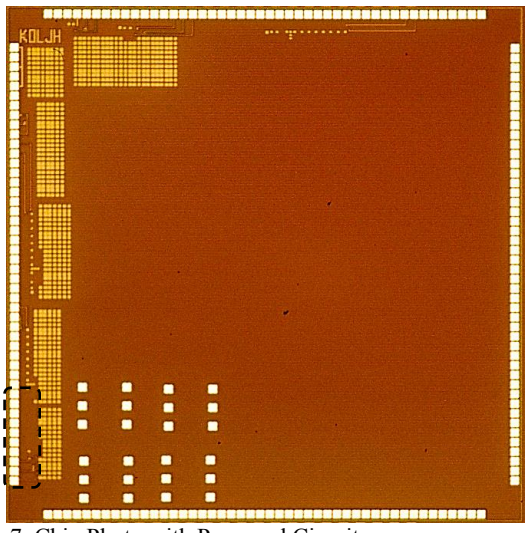

Fig. 7. Chip Photo with Proposed Circuit

Fig. 8 shows the comparison between expected output and measured output of VGA for different gain conditions. Agilent E3620A is used to power up the circuit and Keithley 2400 Sourcemeter is used to provide bias voltage. Agilent 33250A waveform generator is used to provide input to test the circuit and output is measured on Agilent DSO-X 2014A oscilloscope. For high gain condition, a sinusoidal input of 158µVpp at 8kHz, which corresponds to 94dB SPL (Region A), is applied to input of charge amplifier and output of VGA is measured on oscilloscope. Expected output of VGA is 250mVpp and measured output is 249mVpp. For low gain condition, a sinusoidal input of 2mVpp at a frequency of 8kHz, which corresponds to 130dB SPL (Region B), is applied to input of charge amplifier and output of VGA is measured on oscilloscope. Expected output of preamplifier is 320mVpp and the

measured output is 318mVpp. Small errors between simulation and measurement results are because of package and breadboard parasitics.

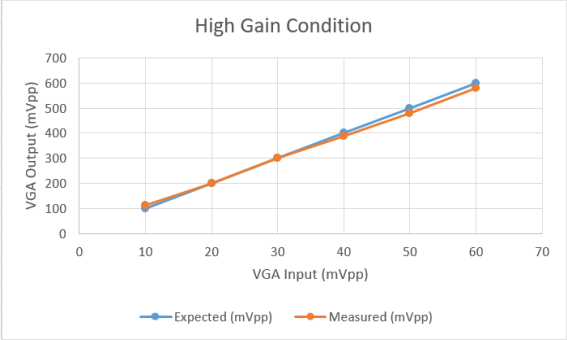

Fig. 8a. VGA output in high gain condition

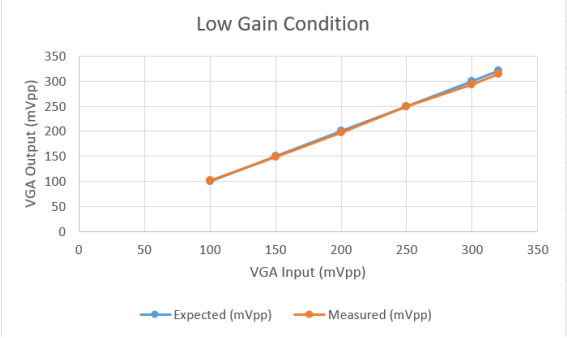

Fig. 8b. VGA output in low gain condition

Table 1 compares the performance of designed VGA with existing circuits. It can be seen that designed VGA has superior noise performance and faster processing capability.

TABLE I
VARIABLE GAIN AMPLIFIER PERFORMANCE COMPARISON

Parameters	**VGA Performance Comparison**		
	[4]	[5]	This Work
Input Referred Noise	NA	4.2µVrms	0.13µVrms
Power Consumption	222µW	70µW	172µW
Peak SNR	42dB	81dB	77dB
Attack and Release Time	N/A	N/A	60µSec
Supply	1.4V	0.9V	1.8V
Technology	0.35µm	0.18µm	0.18µm

IV. CONCLUSION

A mixed mode variable gain amplifier for hearing aid application is designed. It consists of main amplifier stage and a gain control circuit. Based on the output of microphone, voltage levels are categorized into two gain regions and designed circuit automatically sets the close loop gain of main amplifier. Main amplifier consists of opamp with feedback resistors and gain control circuit consists of peak detector, high speed comparator and XNOR gate. Due to high speed digital control circuitry, attack and release time are as small as 60µSec which is 33 times faster than temporal resolution of human ear, thereby achieving faster processing capability. Along with preamplifier, proposed circuit achieves a gain range of 45dB to 65dB and offers an input referred noise of 0.13µVrms, with peak SNR of 77dB and consumes a power of 172µW from 1.8V supply. Fabricated chip has been successfully tested to verify simulation results.

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