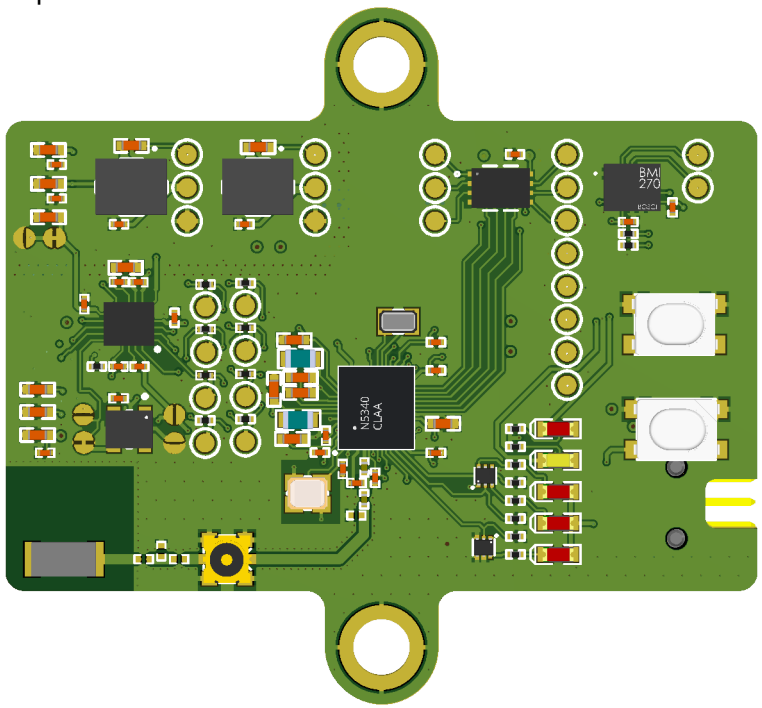
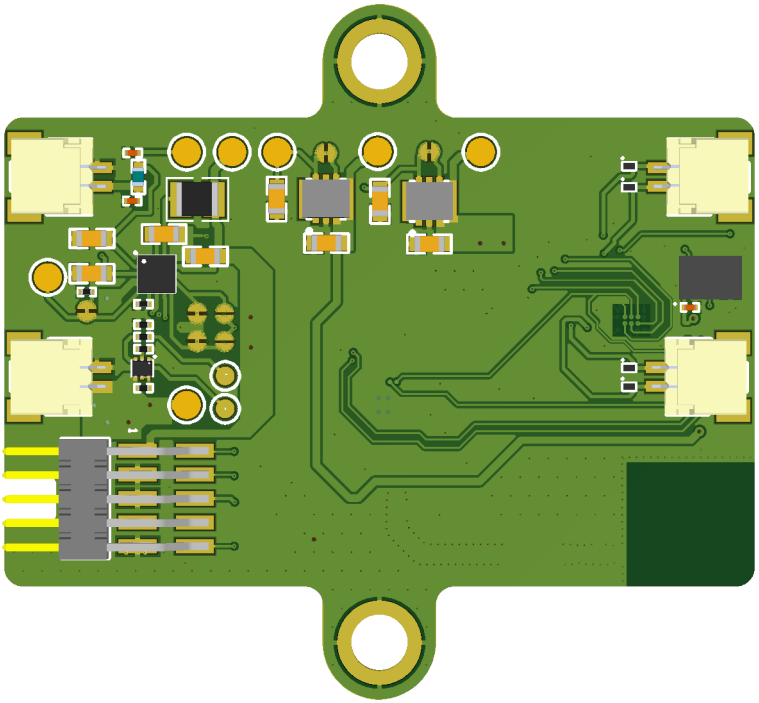
Tiresias Hearing Device Prototype - Hardware Documentation

Top View



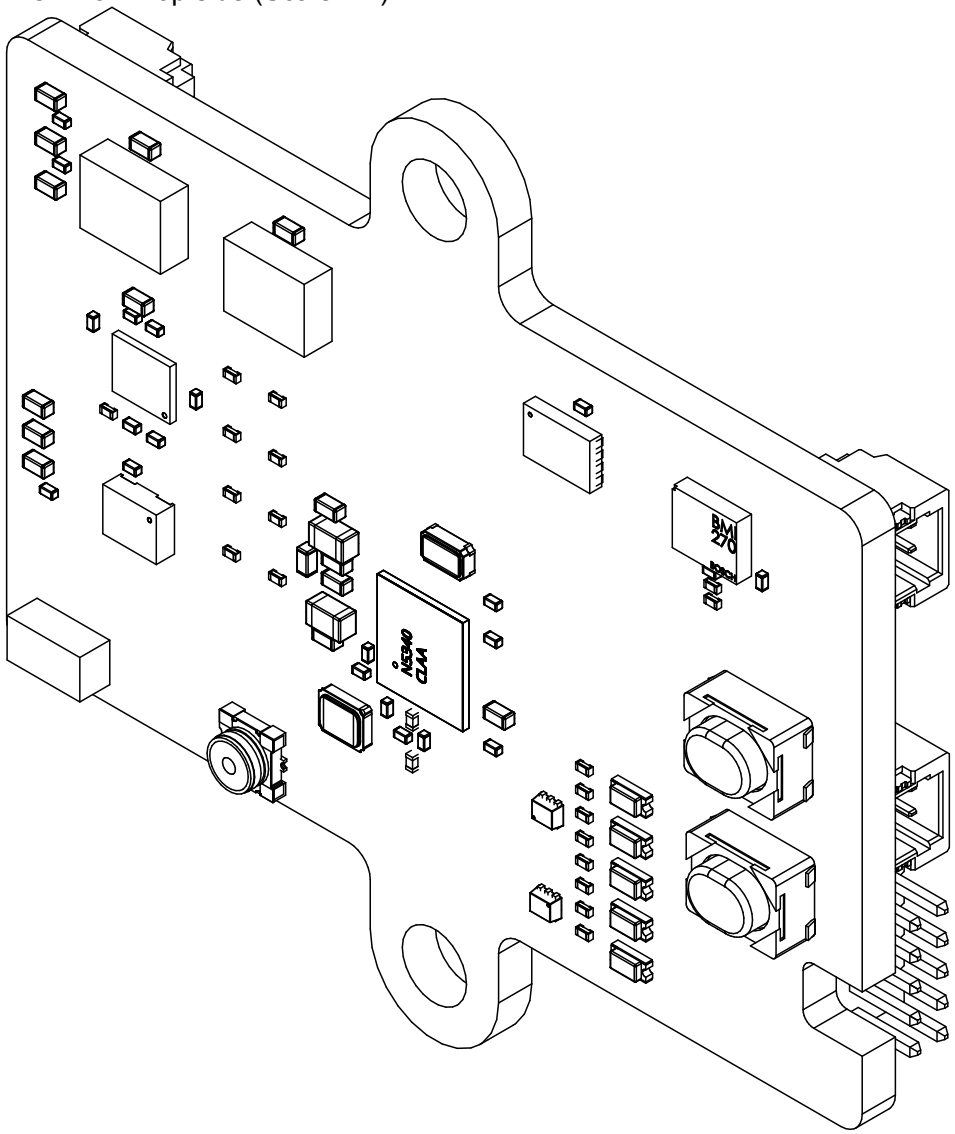
Bottom View



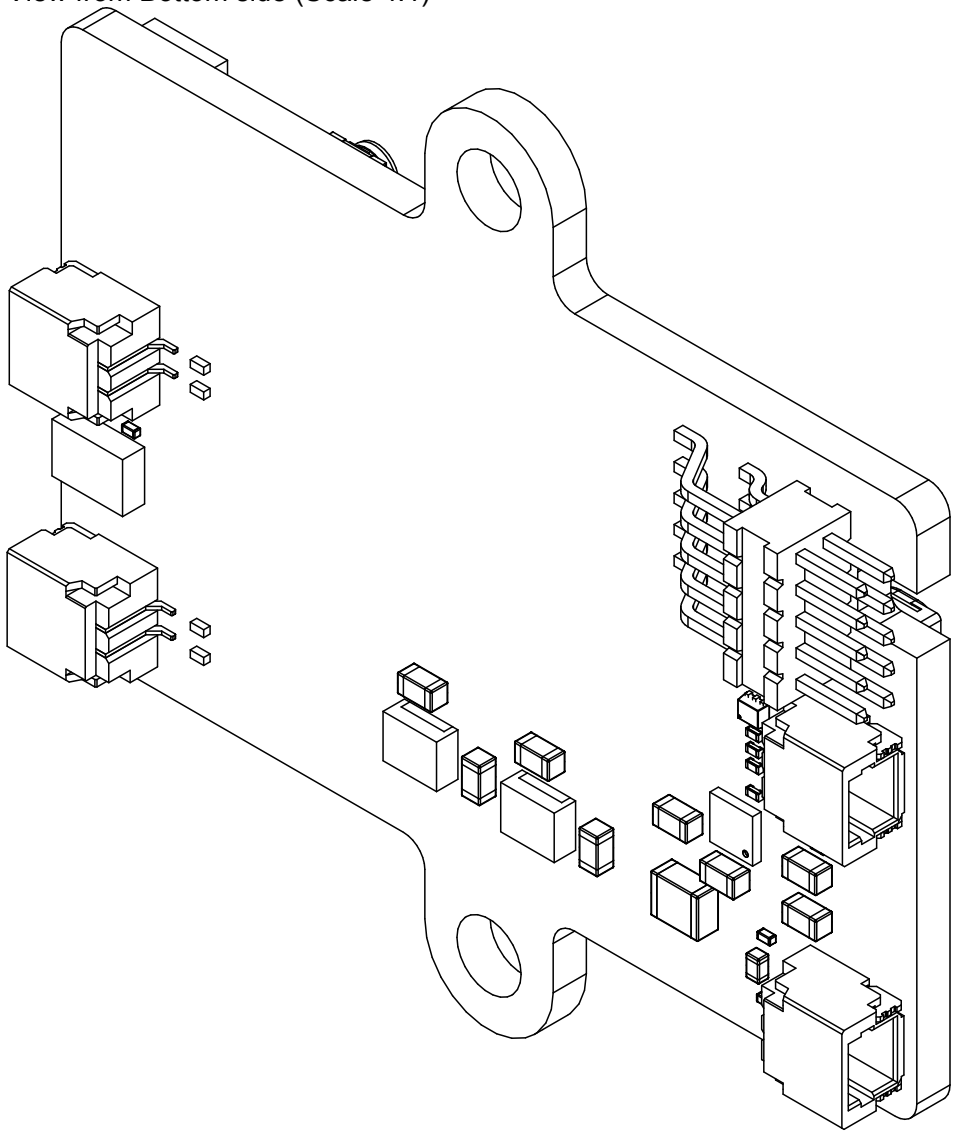
Engineer: João Victor Colombari Carlet

ISO View

View from Top side (Scale 4:1)



View from Bottom side (Scale 4:1)

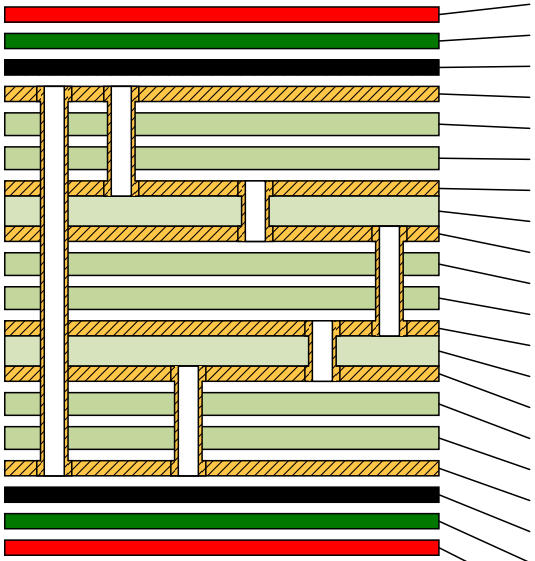


Stack-Up and Impedance

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Substack	Clearance	Target Tolerance
1	Coated Coplanar Waveguide With Ground	50	49.99	Top Layer	0.55mm	0.55mm	Int4 (GND)	Board Layer Stack	0.13mm	10%
2	Coated Coplanar Waveguide With Ground	50	49.99	Bottom Layer	0.55mm	0.55mm	Int1 (GND)	Board Layer Stack	0.13mm	10%

Layer Stack Legend

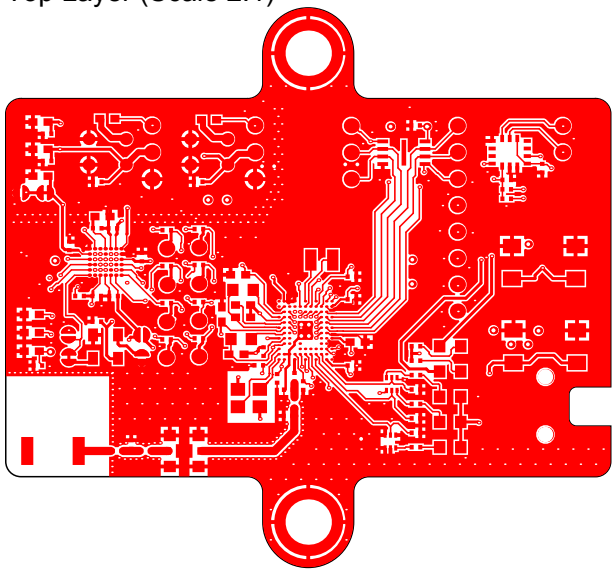


Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.03mm	SM-002	Solder Mask	GTS
Nickel, Gold	Top Surface Finish	0.00mm		Surface Finish	
CF-004	**Top Layer**	**0.04mm**		**Signal**	**GTL**
Prepreg		*0.07mm*	*PP-006*	*Dielectric*	
Prepreg		*0.07mm*	*PP-006*	*Dielectric*	
CF-004	**Int1 (GND)**	**0.04mm**		**Signal**	**G1**
Core		*0.46mm*	*Core-035*	*Dielectric*	
CF-004	**Int2 (PWR)**	**0.04mm**		**Signal**	**G2**
Prepreg		*0.07mm*	*PP-006*	*Dielectric*	
Prepreg		*0.07mm*	*PP-006*	*Dielectric*	
CF-004	**Int3 (SIG)**	**0.04mm**		**Signal**	**G3**
Core		*0.46mm*	*Core-035*	*Dielectric*	
CF-004	**Int4 (GND)**	**0.04mm**		**Signal**	**G4**
Prepreg		*0.07mm*	*PP-006*	*Dielectric*	
Prepreg		*0.07mm*	*PP-006*	*Dielectric*	
CF-004	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**
Nickel, Gold	Bottom Surface Finish	0.00mm		Surface Finish	
Surface Material	Bottom Solder	0.03mm	SM-002	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

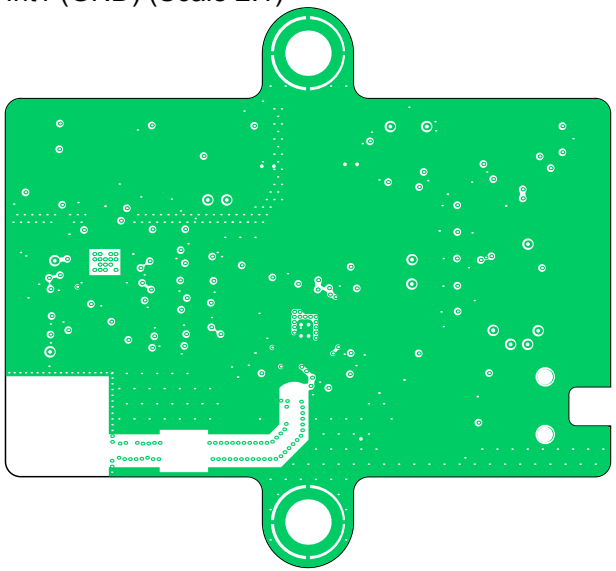
Total thickness: 1.61mm

Layers

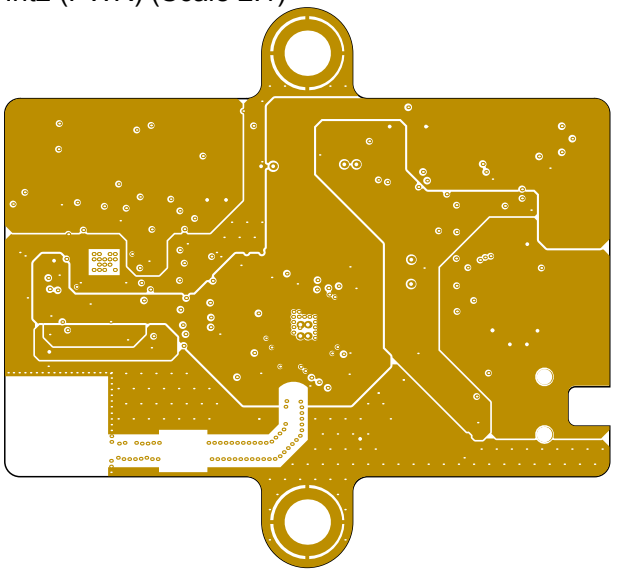
Top Layer (Scale 2:1)



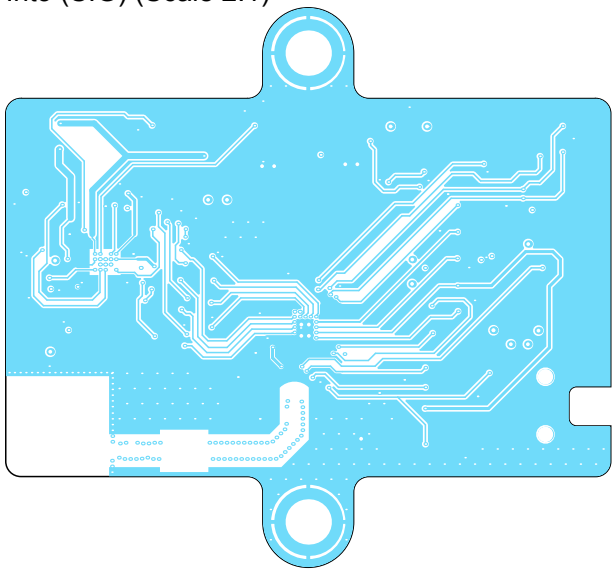
Int1 (GND) (Scale 2:1)



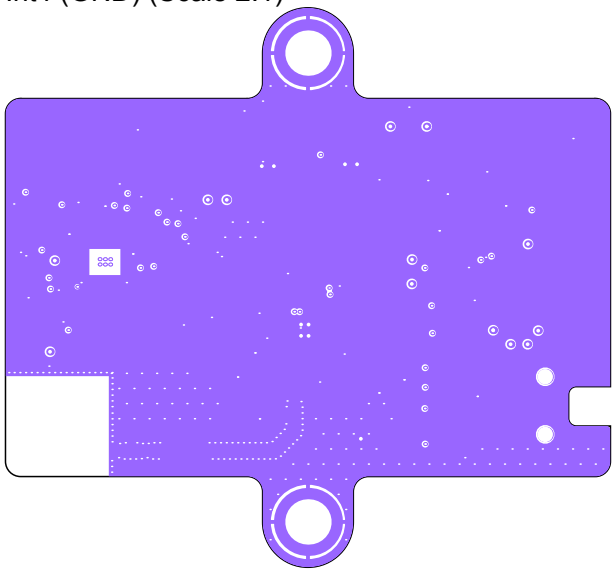
Int2 (PWR) (Scale 2:1)



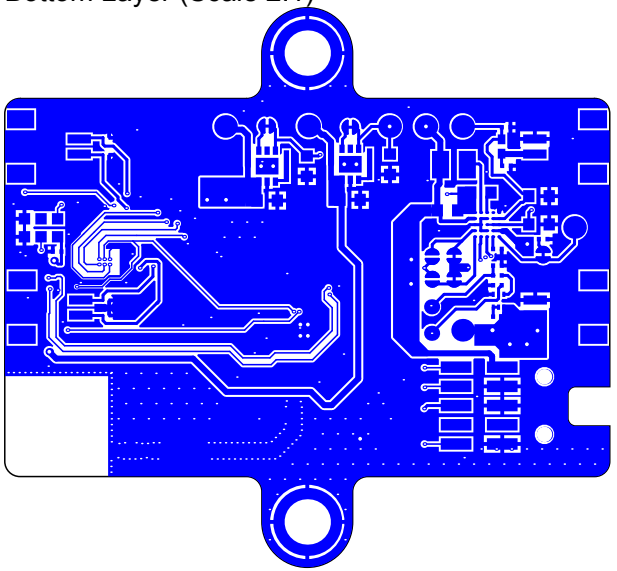
Int3 (SIG) (Scale 2:1)



Int4 (GND) (Scale 2:1)



Bottom Layer (Scale 2:1)

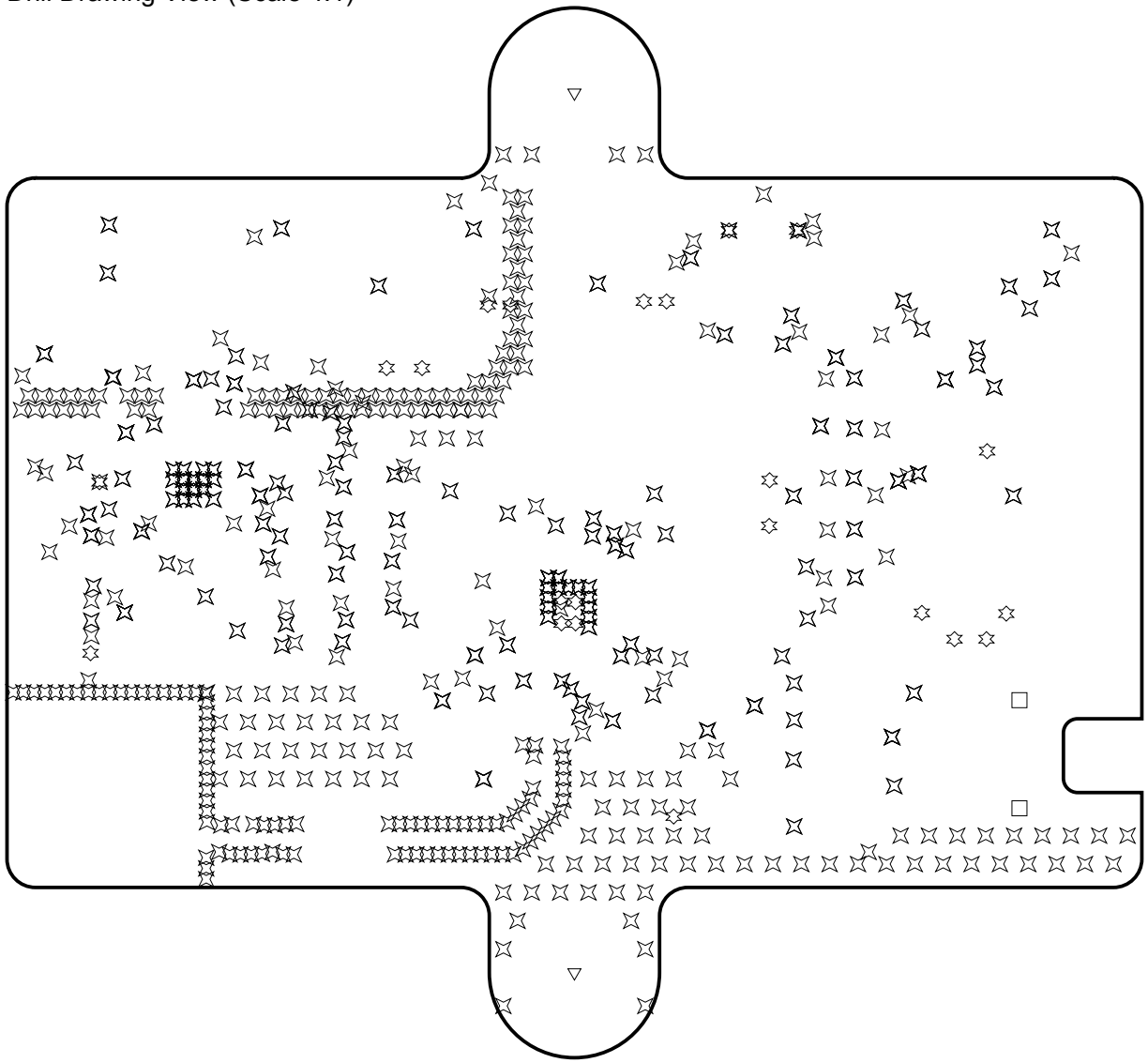


Drills

Drill Table

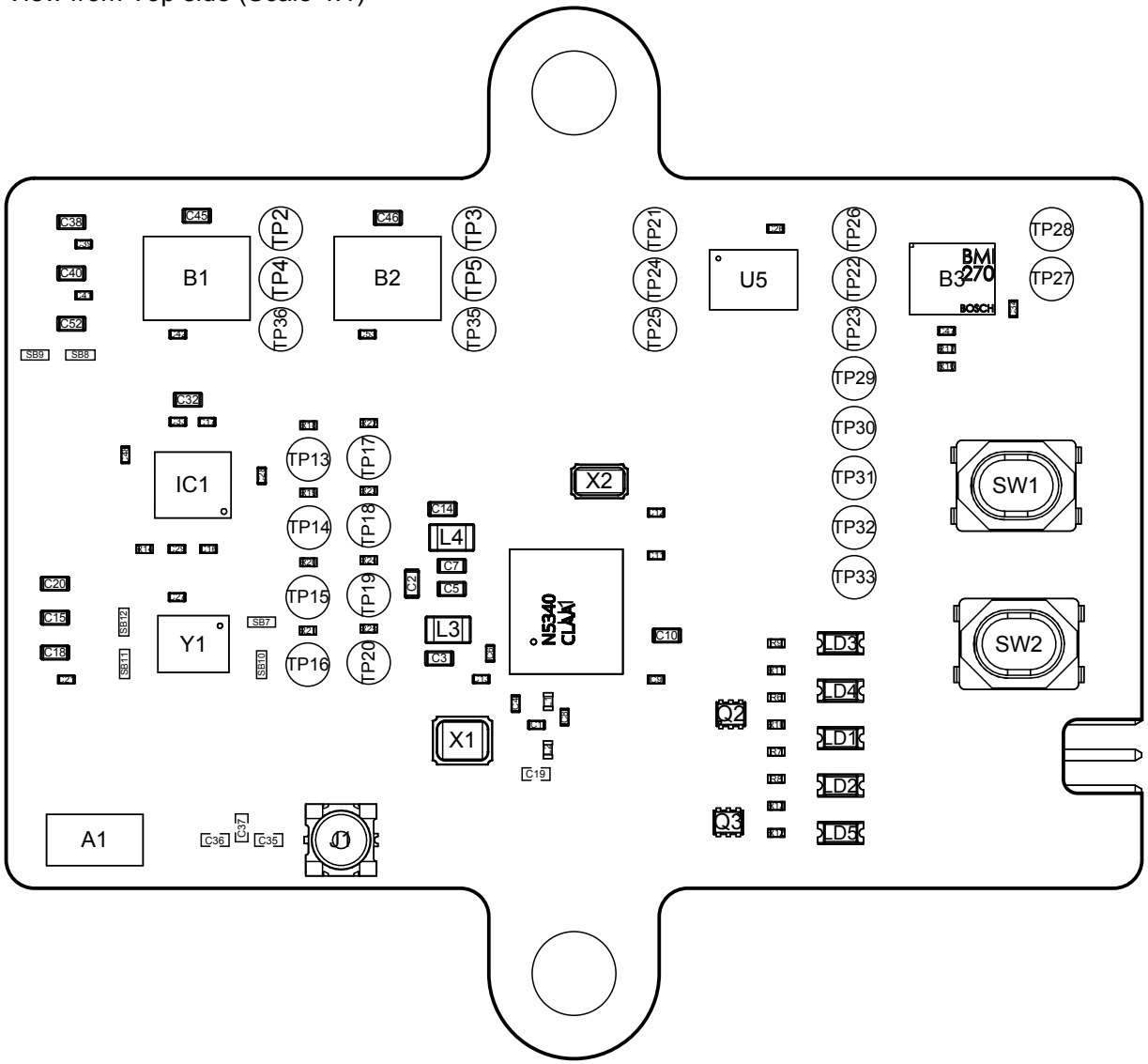
Symbol	Count	Hole Size	Plated	Hole Tolerance
☒	801	0.10mm	Plated	
✡	22	0.25mm	Plated	
□	2	1.02mm	Non-Plated	
▽	2	3.00mm	Plated	
	827 Total			

Drill Drawing View (Scale 4:1)



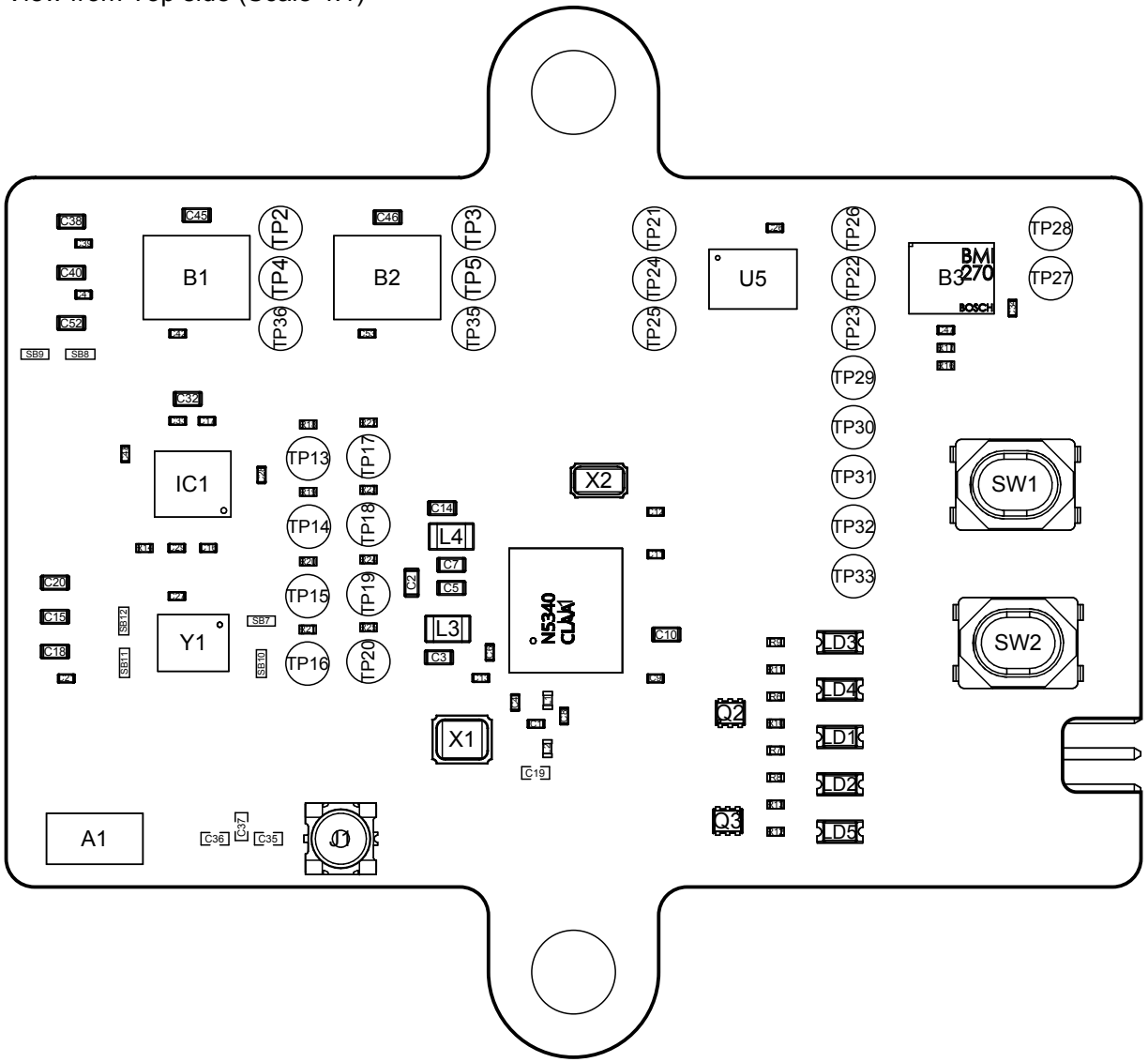
Assembly Top

View from Top side (Scale 4:1)



Assembly Bottom

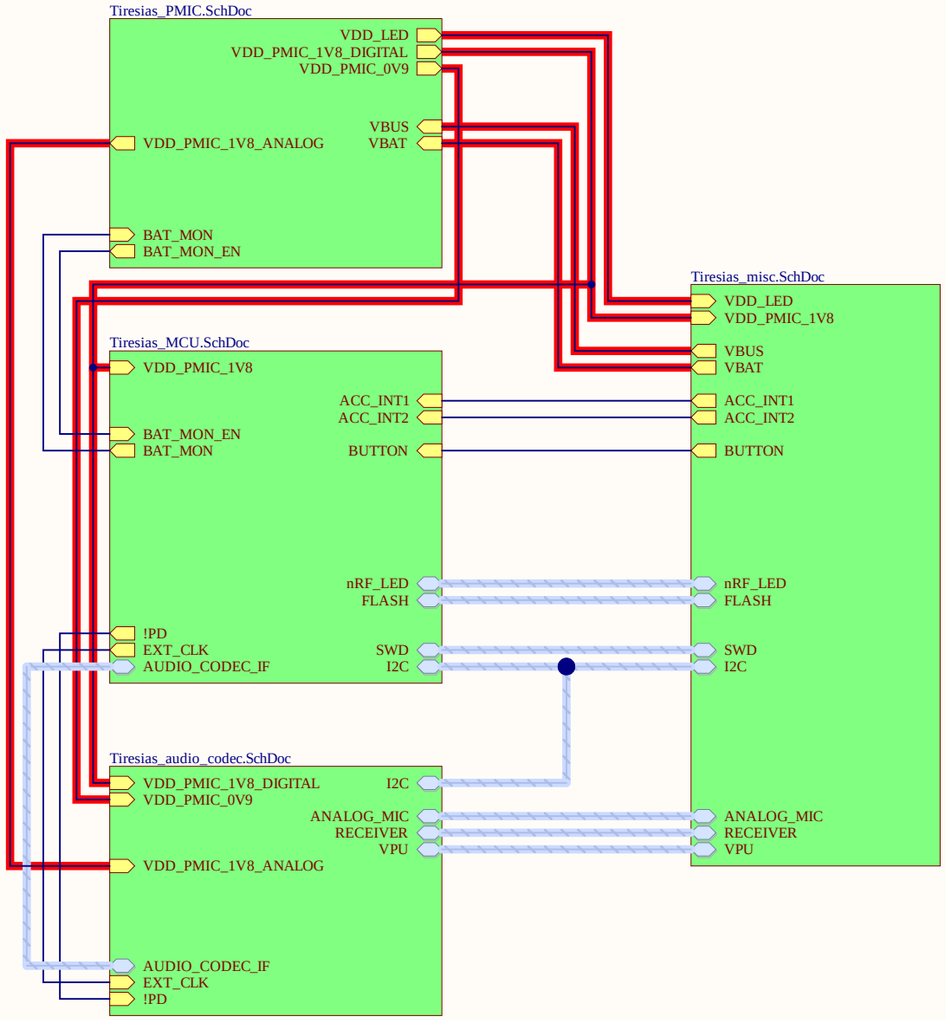
View from Top side (Scale 4:1)



Metamaterials Group: Microwaves and Optics

Tiresias Hearing Device Prototype

Sheet 1: Cover
Sheet 3: MCU
Sheet 4: Audio Codec
Sheet 5: PMIC
Sheet 6: Miscellaneous



- Power Signals
- Analog Signals
- Serial Communication
- RF

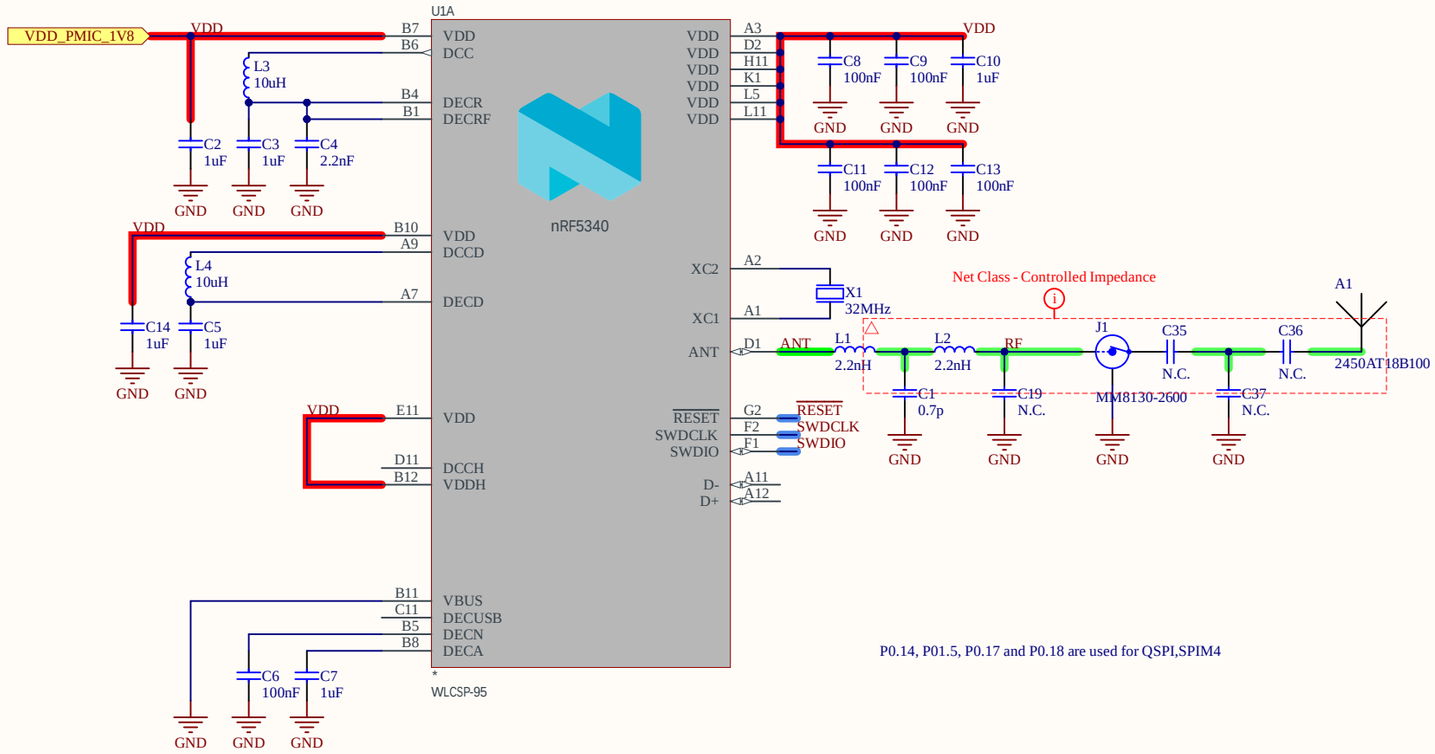
The No ERC object is a design directive.
This directive is placed on a node in the circuit to suppress reported warnings and/or error violation conditions that are detected when the schematic project is compiled.

The DIFFPAIR object is a design directive.
This directive is placed on a differential pair so that they are routed accordingly.

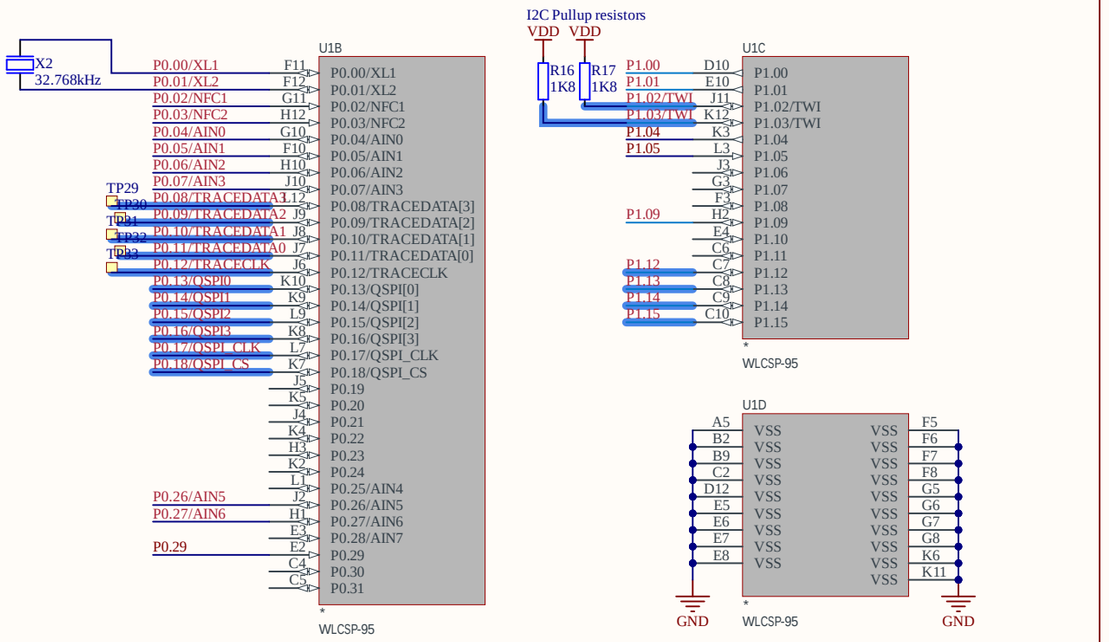
These are fiducial marks

Title: **Tiresias Cover Letter**			*GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 31/01/2025	Time: 16:25:36	Sheet 1 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_Cover_letter.SchDoc			

Nordic nRF52811 MCU

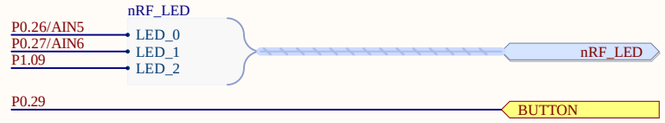


MCU Peripherals



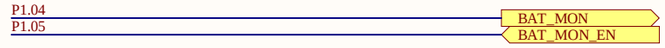
OBS

User Interface

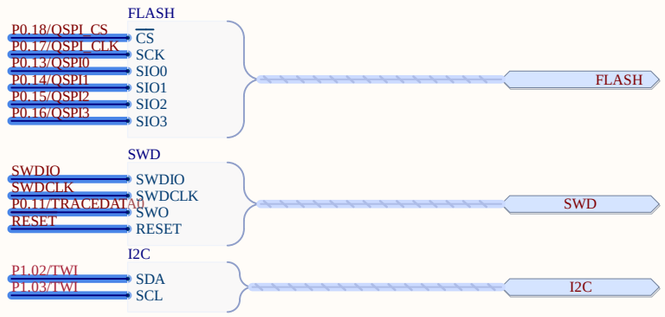


Accelerometer

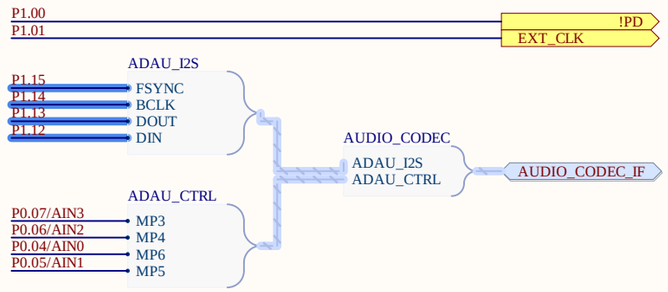
PMIC



Serial Communication



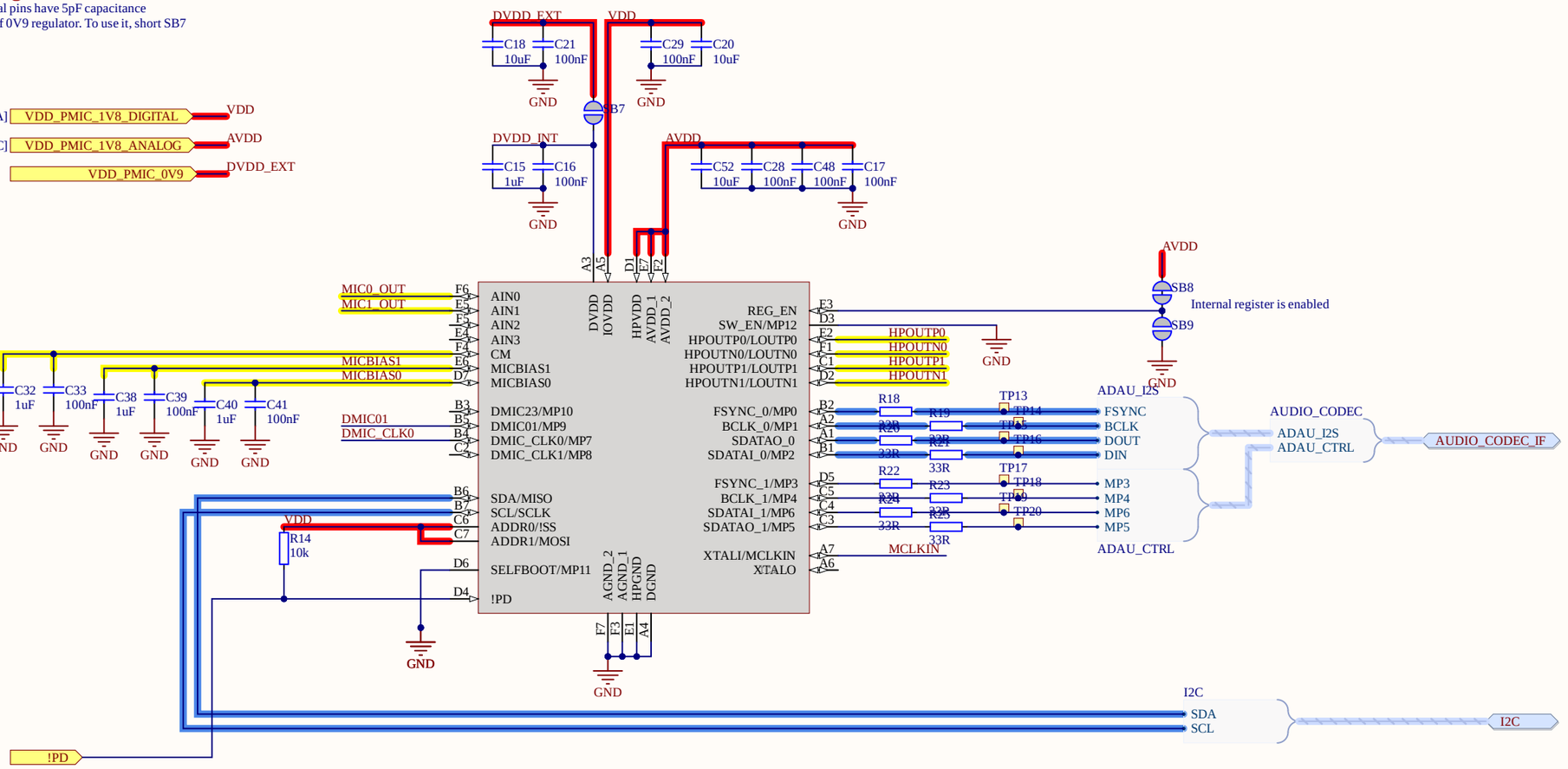
Audio Codec



Title: **MCU**			*GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 31/01/2025	Time: 16:25:36	Sheet 2 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_MCU.SchDoc			

Analog Devices ADAU1787 Audio Codec

All digital pins have 5pF capacitance
Output of 0V9 regulator. To use it, short SB7



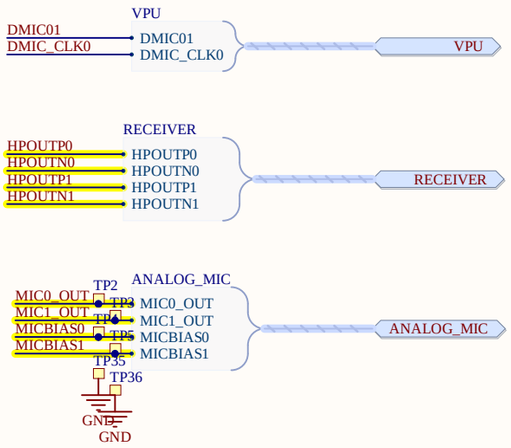
OBS

- For CLK use PWM from NRF. XTALO is open and crystal oscillator reg must be disabled
- REG_EN can be grounded to disable 0.9V LDO if DVDD is supplied
- Do not power up IOVDD when power is not applied to AVDD.
- I2C/SPI Enable (SW_EN). Connect this pin to DGND.

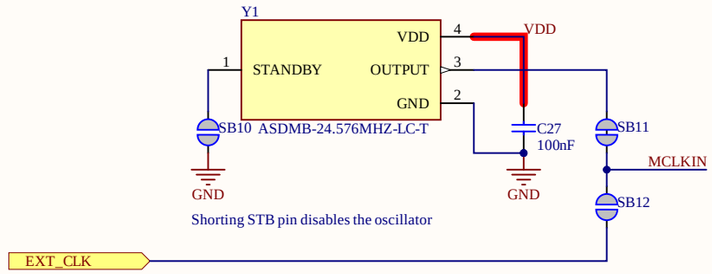
Configurations

- **1 - Using two analog inputs with passives recomended by PUI audio. Do not forget to use a PUI with lower than 1.6V spec**
- 2 - Bypassed power. DVDD is bypassed even if internal reg is used. IOVDD and AVDD are both connected to 1V8
- 4 - Falta a gravação com int e ext, mas por enquanto prefiro fazer com o interno.
  REG_EN - Regulator Enable. Tie this pin to AVDD to enable the regulator, and tie this pin to ground to disable the regulator
  The IC can be put into I2C and/or SPI mode by tying the SW_EN pin to DGND
- 5 - CM bypassed. Could also be used for external amp common mode adjust
- 6 - Selfboot puts ADAU on master mode so that it boots using the EEPROM. Not used here
- 7 - PD control via microcontroller
- 8 - For the I2S remember to use compatible GPIO on the nordic side
- 9 - I2C adderes set to 0x2B with both ADDR0 and ADDR1 connected to IOVDD
- 10 - CLK
- 11 - DMIC connections for using one vesper VPU alone

Audio Codec Peripherals

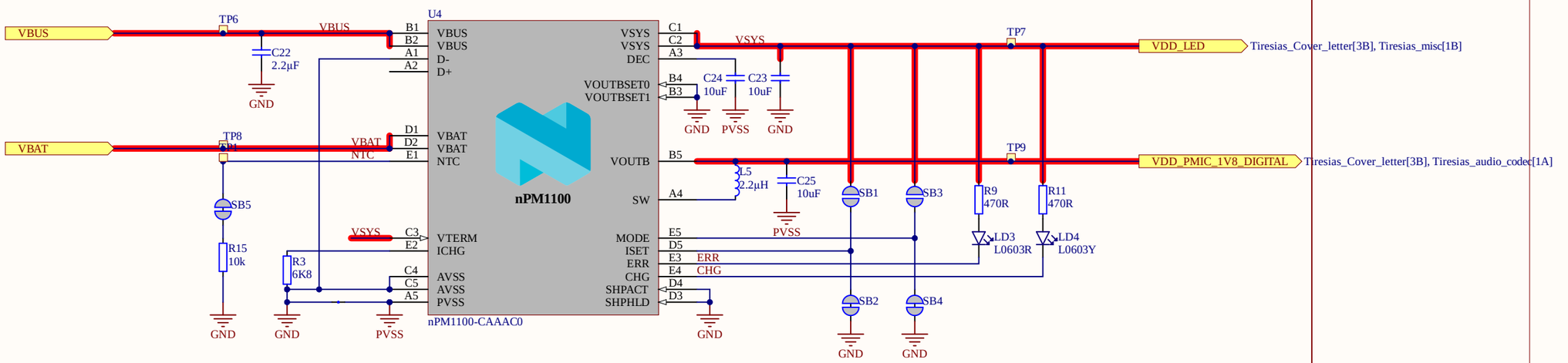


Audio Codec CLK

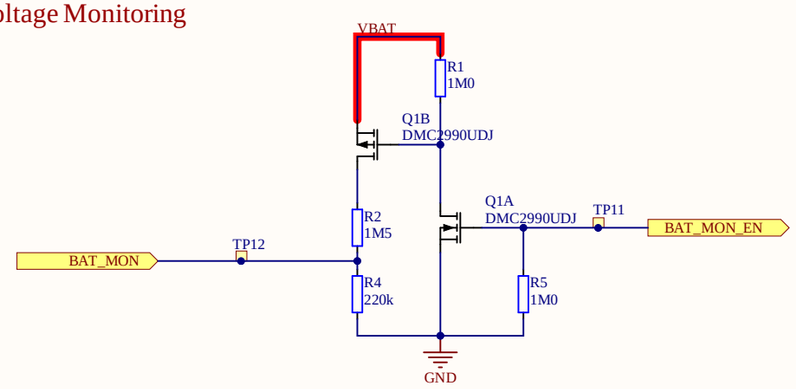


Title: **Audio Codec**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 31/01/2025	Time: 16:25:36	Sheet 3 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_audio_codec.SchDoc			

nPM1100 PMIC



Voltage Monitoring



Reference

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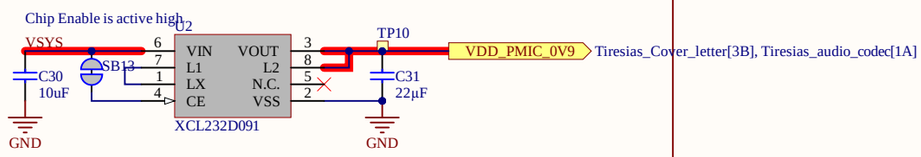
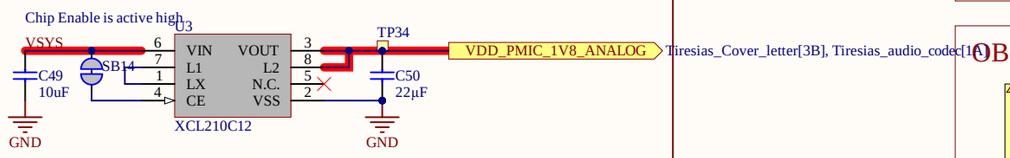
Audio Codec DVDD Regulator



Audio Codec AVDD Regulator



Configurations

For fixed VBUS current options:
D+=NC; D-=AVSS and either:
ISET=AVSS for 100mA or
ISET=VSYS for 500mA

- VTERM high - 4.2V charge termination
- 3V7 LiIon or LiPo battery

- RCHG = 625/current_limit-1562.5
For 6K8 resistor current is 75mA, which is right above 70mA for the min I found at mouser

- Added NTC short and TP for external

Mode Low Automatic selection between Hysteretic and PWM modes. Since . In PWM mode, BUCK provides a clean supply operation, there are SB for an eventual change

VOUTBSET 0 and 1 to Low = 1V8 VOUTB output

If Ship mode is not required, then SHPACT and SHPHLD pins may be tied to AVSS.

NTC
10kR +- 15 at 25 Celcius
B25/50 constant 3380K
B25/85 constant 3434 to 3435K

If the thermal protection feature is not used, then a 10 kΩ, ≤20% accuracy resistor should be connected between NTC and AVSS pins.

An application should not be supplied directly from VBAT because it can disturb the battery charging process and may cause incorrect behavior from the charger. Instead, VOUTB and/or VSYS should be used to supply an application.

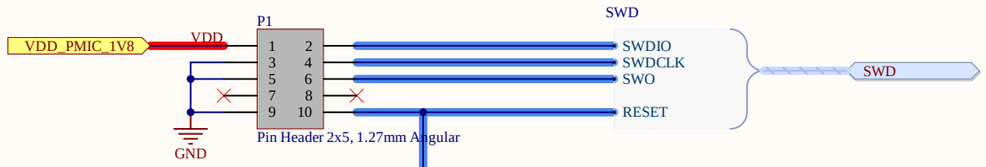
OBS

The VDD pin allows the debugger (e.g., a programmer or debug probe) to detect the operating voltage of the target system. This ensures that the debugger can adjust its signal levels (for SWDIO and SWCLK) to match the target device's logic levels, preventing damage due to mismatched voltages.
The VSYS and DEC pins must not be externally supplied

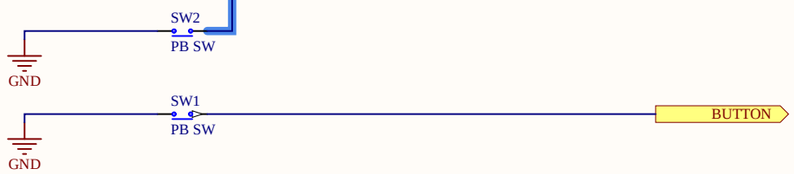
Product must have standard Vterm spec

Title: **Tiresias PMIC**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 31/01/2025	Time: 16:25:37	Sheet 4 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_PMIC.SchDoc			

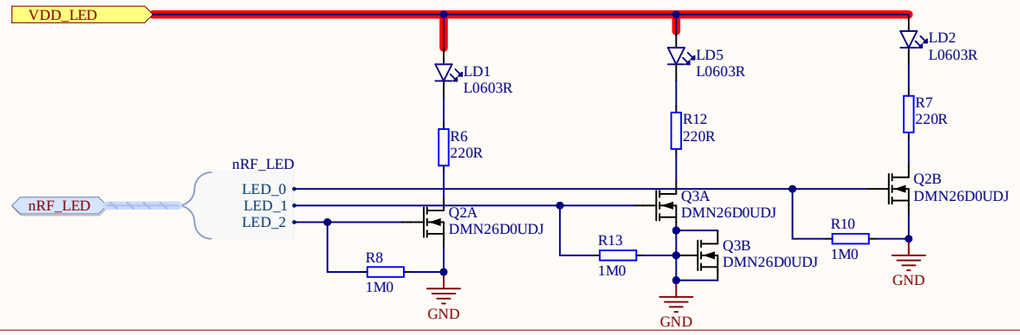
SWD Interface



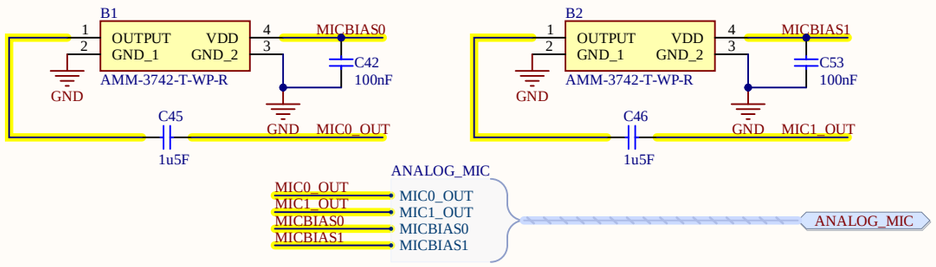
Push Button



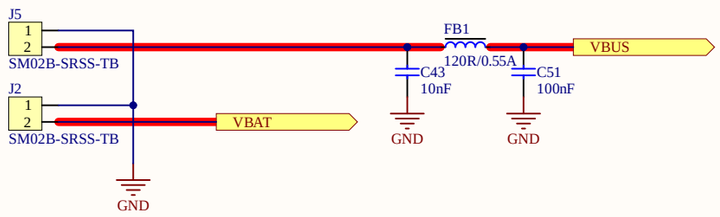
LEDs



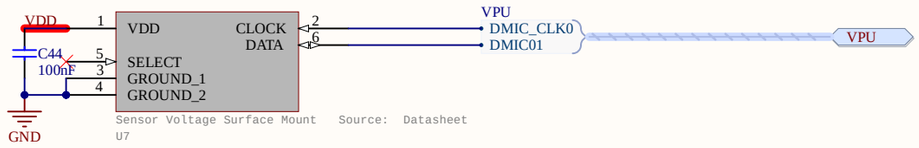
Analog Microphones



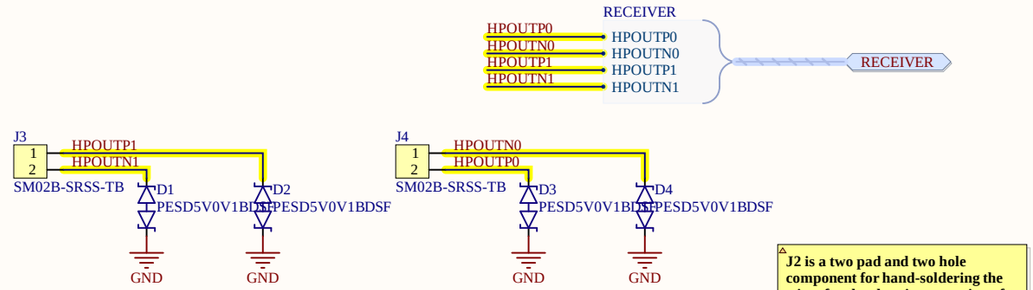
Power Connectors



VPU



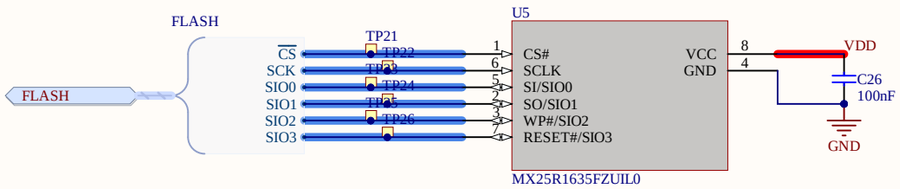
Receiver Connector



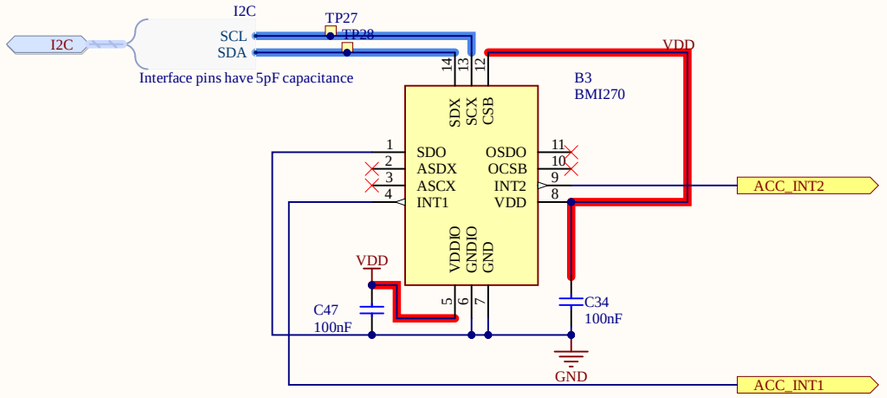
J2 is a two pad and two hole component for hand-soldering the wires for the chassis connection of a 2-pin headphone connector

Flash Memory

Cannot open file C:\Users\alunos\Desktop\MACRONIX.PNG. File does not exist.



Accelerometer



ACC - The default I²C address of the device is 0b1101000 (0x68). It is used if the SDO pin is pulled to ´GND´. The alternative address 0b1101001 (0x69) is selected by pulling the SDO pin to ´VDDIO´

CSB - Chip select for SPI mode. Connects to VDDIO**
**** DNC is also possible due to an internal pull-up, as long as the voltage never drops below VIH.**

Title: **Tiresias Miscellaneous**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 31/01/2025	Time: 16:25:37	Sheet 5 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_misc.SchDoc			

Comment	Description	Designator	Footprint	LibRef	Quantity
2450AT18B100	2.45 GHz chip antenna	A1	2450AT18B100	Johanson 2450AT18B100	1
AMM-3742-T-WP-R	Microphones MICROPHONE -42 DB 2 VDC 200 UA 300 OHM, 20 Hz ~ 20 kHz Analog Microphone, MEMS (Silicon) 1.5 V ~ 3.6 V Omnidirectional (-42dB +/-1dB) Solder Pads	B1, B2	AMM3742TWPR	AMM-3742-T-WP-R	2
BMI270	IMUs - Inertial Measurement Units Smart Ultra-Low Power Inertial Measurement Unit (IMU) for Wearable Applications	B3	BMI270	BMI270	1
0.7p	Capacitor, NP0, ±2%	C1	CAPC0603X03L_C	CAP_0201_0p7	1
1uF	Capacitor, X5R, ±5%	C2, C3, C5, C7, C10, C14, C15, C32, C38, C40	CAPC1005X04L	CAP_0402_1uF	10
2.2nF	Capacitor, NP0, ±2%	C4	CAPC0603X03L_C	CAP_0201_2n2	1
100nF	Capacitor, NP0, ±2%	C6, C8, C9, C11, C12, C13, C16, C17, C21, C26, C27, C28, C29, C33, C34, C39, C41, C42, C44, C47, C48, C51, C53	CAPC0603X03L_C	CAP_0201_100nF	23
10uF	Capacitor, X5R, ±5%	C18, C20, C52	CAPC1005X04L	CAP_0402_10uF	3
N.C.	Capacitor, NP0, ±2%	C19, C35, C36, C37	CAPC0603X03L_C NC	CAP_0201_NC	4
2.2µF	Capacitor, Ceramic, X5R, ±10%, 10V	C22	CAPC1608X06L	CAP_0603_2u2F	1
10uF	Capacitor, X5R, ±10%	C23, C24, C25, C30, C49	CAPC1608X06L	CAP_0603_10uF	5
22µF	Capacitor, X5R, ±20%, 6.3V	C31, C50	CAPC1608X06L	CAP_0603_22uF	2
10nF	Capacitor, NP0, ±2%	C43	CAPC0603X03L_C	CAP_0201_10nF	1
1u5F	Capacitor, X5R, ±5%	C45, C46	CAPC1005X04L	CAP_0402_1u5F	2
PESD5V0V1BDSF	Very low capacitance bidirectional ESD protection diode	D1, D2, D3, D4	DFN40P60X30-2N	PESD5V0V1BDSF	4
120R/0.55A	Ferrite Bead, 120 Ohm @ 100MHz, 500mA, 250 mOhm Max	FB1	INDC1005X04L	FB0402-120R@100M-500mA	1
General Purpose Audio Codec 4ADC / 2DAC Ch 42-Pin WLCSP T/R Source: Datasheet		IC1	BGA42C35P7X6_270X232X53	ADAU1787BCBZRL	1
MM8130-2600	Coaxial Connector with Switch	J1	COAXIAL-SWF	MM8130-2600	1
SM02B-SRSS-TB	1.0mm pitch connector side entry SMD	J2, J3, J4, J5	SM02B-SRSS-TB(LF)(SN)	SM02B-SRSS-TB	4
2.2nH	High frequency chip inductor ±5%	L1, L2	INDC0603X03L_C	IND_0201_2n2H	2
10uH	Chip inductor, IDC,min = 50 mA, ±20%	L3, L4	INDC1608X06L	IND_0603_10uH	2
2.2µH	FIXED IND 2.2UH 2.5A 87MOHM SMD	L5	INDC2016X10N	IND_0806_2u2H	1
L0603R	LED, SMD, 0603, RED	LD1, LD2, LD3, LD5	LED_0603_R	LED_0603_RED	4
L0603Y	LED, Yellow, 0603, 590nm, Vf=2.0V, I20mcd, -40 to +85°C	LD4	LED_0603_Y	LED_0603_YEL	1
Pin Header 2x5, 1.27mm Angular	Pin Header 2x5, 1.27mm (50mil), SMD, Keying Shroud Angular	P1	HDR_2x5-SMD-1.27mm-ANG	Pin Header 2x5 SMD, 1.27mm, ANG	1
DMC2990UDJ	MOSFET, Dual N and P-Channel, 20V, 450mA/310mA, 990mOhm, 350mW	Q1	SOTFL35P100X50-6N	DMC2990UDJ-7	1
DMN26D0UDJ	MOSFET, Dual N-Channel, 20V, 240mA, 1050mOhm, 300mW	Q2, Q3	SOTFL35P100X50-6N	DMN26D0UDJ-7	2
1M0	Resistor, ±1%, 0.05W	R1, R5, R8, R10, R13	RESC0603X03L_C	RES_0201_1M0	5
1M5	Resistor, ±1%, 0.05W	R2	RESC0603X03L_C	RES_0201_1M5	1
6K8	Resistor, ±1%, 0.05W	R3	RESC0603X03L_C	RES_0201_6K8	1
220k	Resistor, ±1%, 0.05W	R4	RESC0603X03L_C	RES_0201_220K	1
220R	Resistor, ±1%, 0.05W	R6, R7, R12	RESC0603X03L_C	RES_0201_220R	3
470R	Resistor, ±1%, 0.05W	R9, R11	RESC0603X03L_C	RES_0201_470R	2
10k	Resistor, ±1%, 0.05W	R14, R15	RESC0603X03L_C	RES_0201_10K	2
1K8	Resistor, ±1%, 0.05W	R16, R17	RESC0603X03L_C	RES_0201_1K8	2
33R	Resistor, ±1%, 0.05W	R18, R19, R20, R21, R22, R23, R24, R25	RESC0603X03L_C	RES_0201_33R	8
PB SW	Tactile Switch, SPNO, SMD, 160gf, 4.2x3.3x2.5mm	SW1, SW2	KLS-TS3401	KLS7-TS3401-2.5-160R	2
	Multi-protocol Bluetooth Low Energy, IEEE 802.15.4, ANT and 2.4GHz proprietary system-on-chip	U1	BGA95C35P12X11_437X397X50	nRF5340-CLAA	1
XCL232D091	0.9V Ultra-Low Quiescent Current, Inductor Built-in Step-Down DC/DC Converter, CL-2025-03 Source: Datasheet	U2	CL-2025	XCL232D091KR-G	1
XCL210C12	1.8V, 200mA Inductor Built-in Step-Down "micro DC/DC" Converter	U3	CL-2025	XCL210C18	1
nPM1100-CAAAC0	Li-Ion/Li-Polymer USB battery charger with a high efficiency buck regulator	U4	BGA25C40P5X5_200X200X50	nPM1100-CAAAC0	1
MX25R1635FZUIL0	Wide Vcc Range 16M-BIT [x 1/x 2/x 4] CMOS MXSMIO (SERIAL MULTI I/O) FLASH MEMORY	U5	USON-8L-2X3X0P6_MAC-L	MX25R1635FZUIL0	1
Sensor Voltage Surface Mount Source: Datasheet		U7	V2S200D18	V2S200D-1-8	1
32MHz	XTAL SMD 2016, 32MHz, CI=8pF, Total Tol: ±40ppm	X1	BT-XTAL_2016	XTAL_SMD2016_32MHz	1
32.768kHz	XTAL SMD 2012, 32.768kHz, CI=9pF, Total Tol: ±50ppm	X2	XTAL_2012	XTAL_SMD2012_32k768Hz	1
ASDMB-24.576MHZ-LC-T		Y1	XTAL_ASDMB-24.576MHZ-LC-T	ASDMB-24.576MHZ-LC-T	1