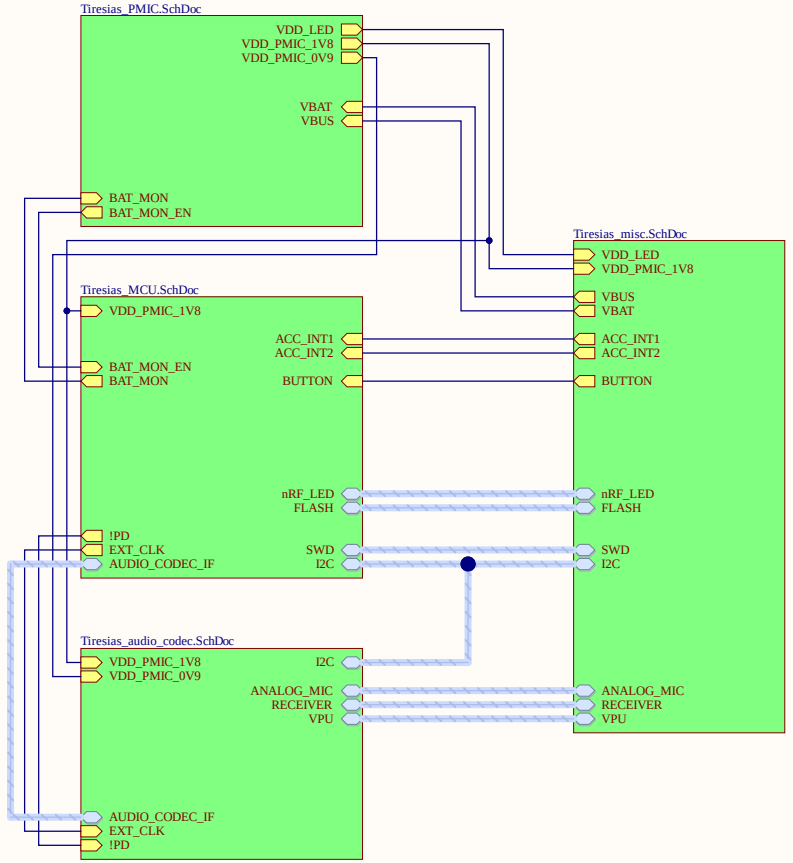
Metamaterials Group: Microwaves and Optics

Tiresias Hearing Device Prototype

Sheet 1:	Cover
Sheet 3:	MCU
Sheet 4:	Audio Codec
Sheet 5:	PMIC
Sheet 6:	Miscellaneous



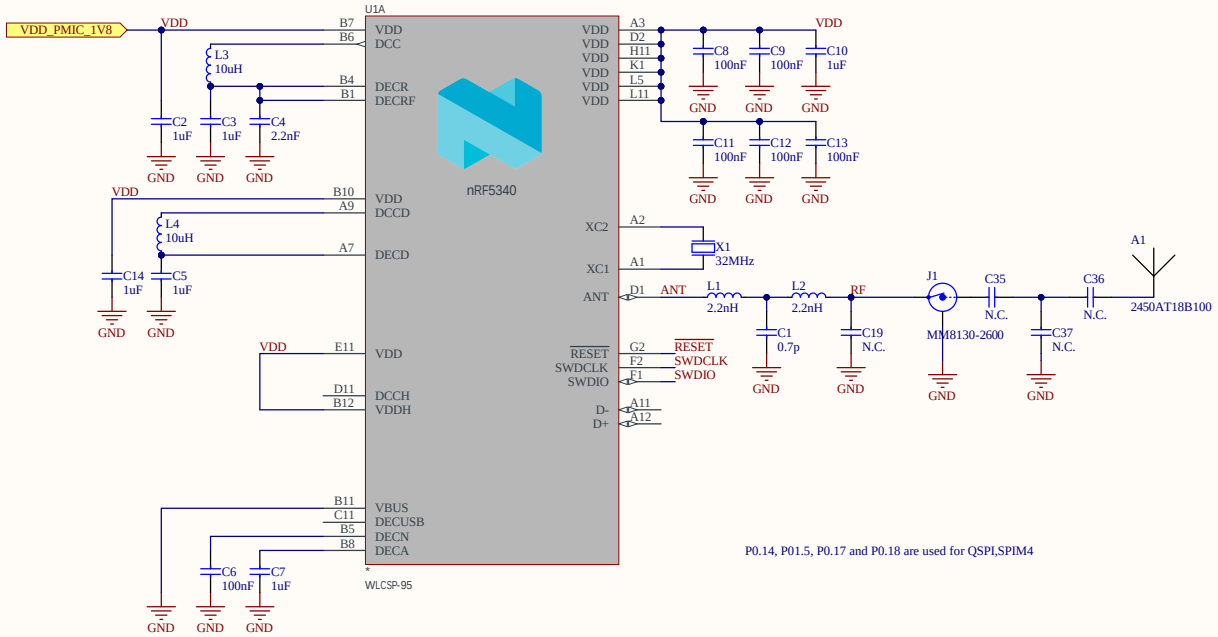
The No ERC object is a design directive.
This directive is placed on a node in the circuit to suppress reported warnings and/or error violation conditions that are detected when the schematic project is compiled.

The DIFFPAIR object is a design directive.
This directive is placed on a differential pair so that they are routed accordingly.

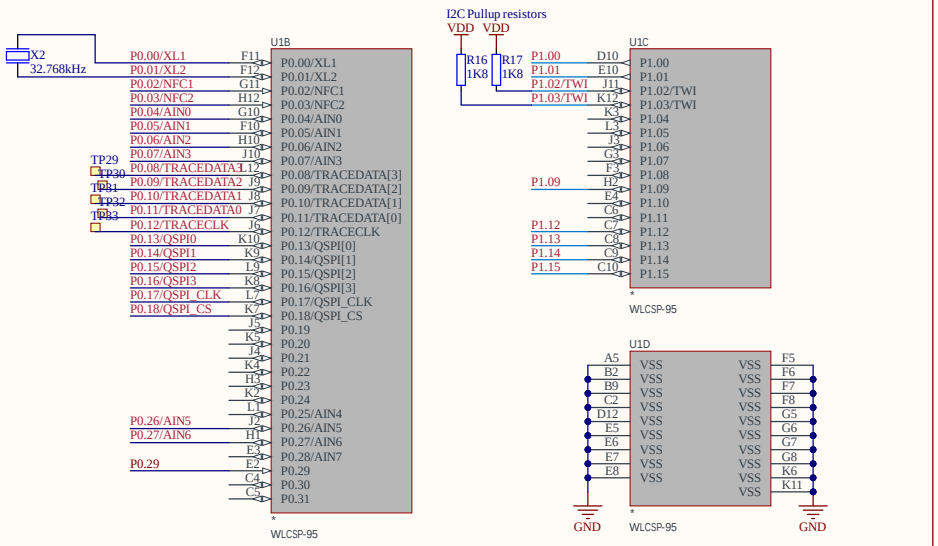
These are fiducial marks

Title: **Tiresias Cover Letter**			*GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 17/01/2025	Time: 09:23:10	Sheet 1 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_Cover_letter.SchDoc			

Nordic nRF52811 MCU

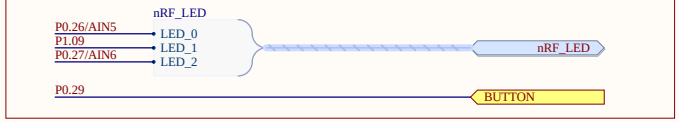


MCU Peripherals

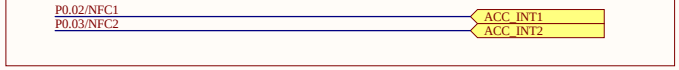


OBS

User Interface

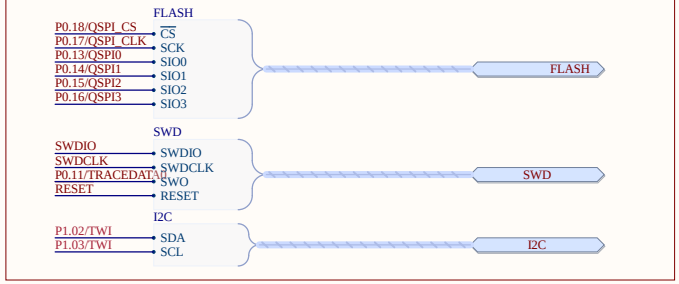


Accelerometer

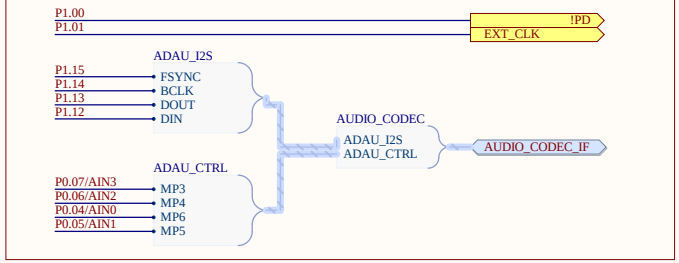


PMIC

Serial Communication

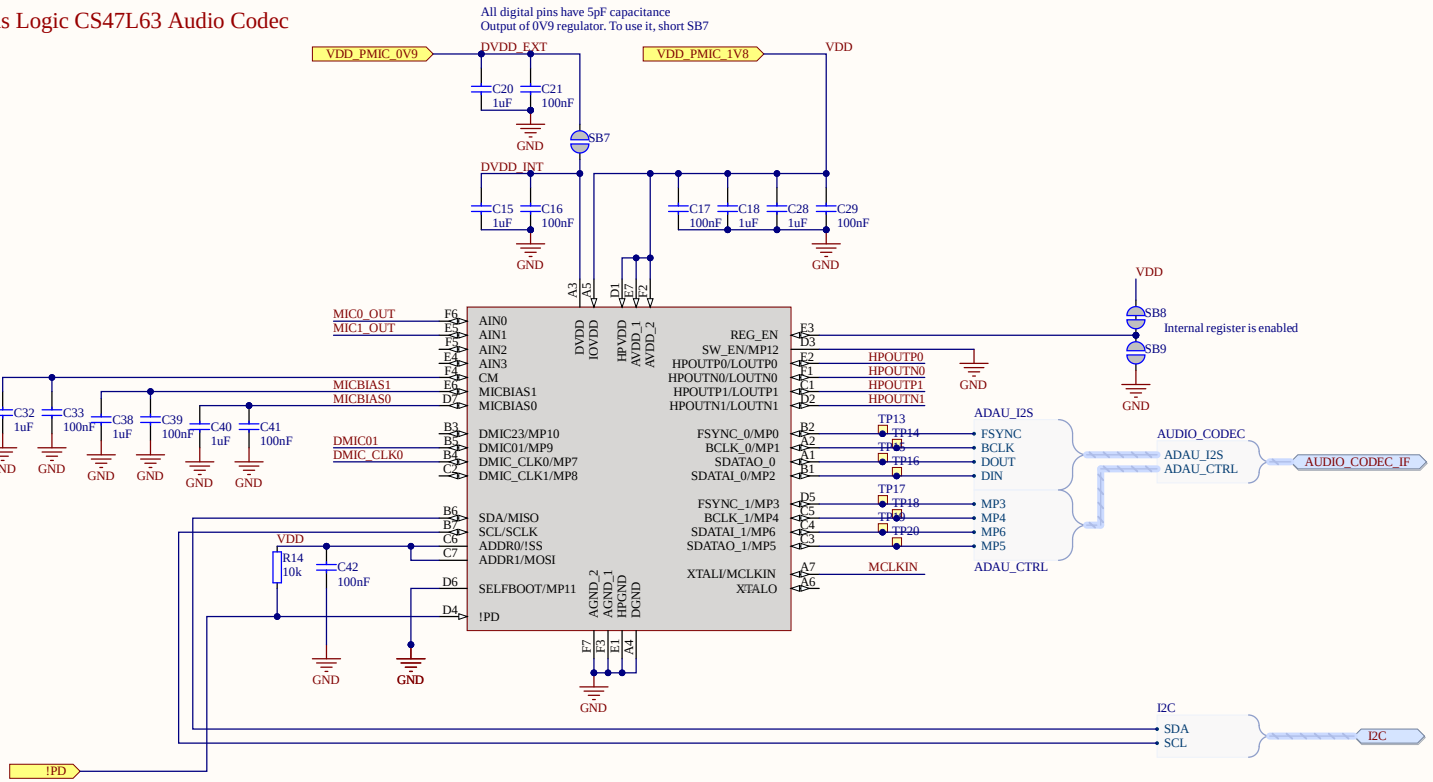


Audio Codec



Title: **MCU**			*GMETA*
Drawn By: João Victor Colombari Carlet			*EESC - USP*
Size: A3	Number: *	Revision: 0	*400, Trabalhador São-Carlense Av.*
Date: 17/01/2025	Time: 09:23:10	Sheet 2 of 5	*13566-590, São Carlos*
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_MCU.SchDoc			*São Paulo, Brazil*
			Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/

Cirrus Logic CS47L63 Audio Codec



OBS

- For CLK use PWM from NRF. XTALO is open and crystal oscillator reg must be disabled
- REG_EN can be grounded to disable 0.9V LDO if DVDD is supplied
- Do not power up IOVDD when power is not applied to AVDD.
- I2C/SPI Enable (SW_EN). Connect this pin to DGND.

Configurations

1 - Using two analog inputs with passives recomended by PUI audio. Do not forget to use a PUI with lower than 1.6V spec

2 - Bypassed power. DVDD is bypassed even if internal reg is used. IOVDD and AVDD are both connected to 1V8

4 - Falta a gravação com int e ext, mas por enquanto prefiro fazer com o interno.
REG_EN - Regulator Enable. Tie this pin to AVDD to enable the regulator, and tie this pin to ground to disable the regulator
The IC can be put into I2C and/or SPI mode by tying the SW_EN pin to DGND

5 - CM bypassed. Could also be used for external amp common mode adjust

6 - Selfboot puts ADAU on master mode so that it boots using the EEPROM. Not used here

7 - PD control via microcontroller

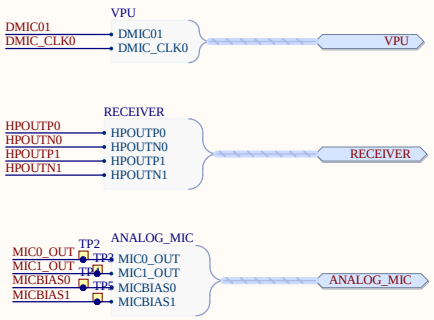
8 - For the I2S remember to use compatible GPIO on the nordic side

9 - I2C adderes set to 0x2B with both ADDR0 and ADDR1 connected to IOVDD

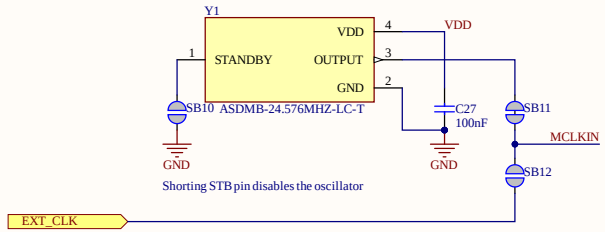
10 - CLK

11 - DMIC connections for using one vesper VPU alone

Audio Codec Peripherals

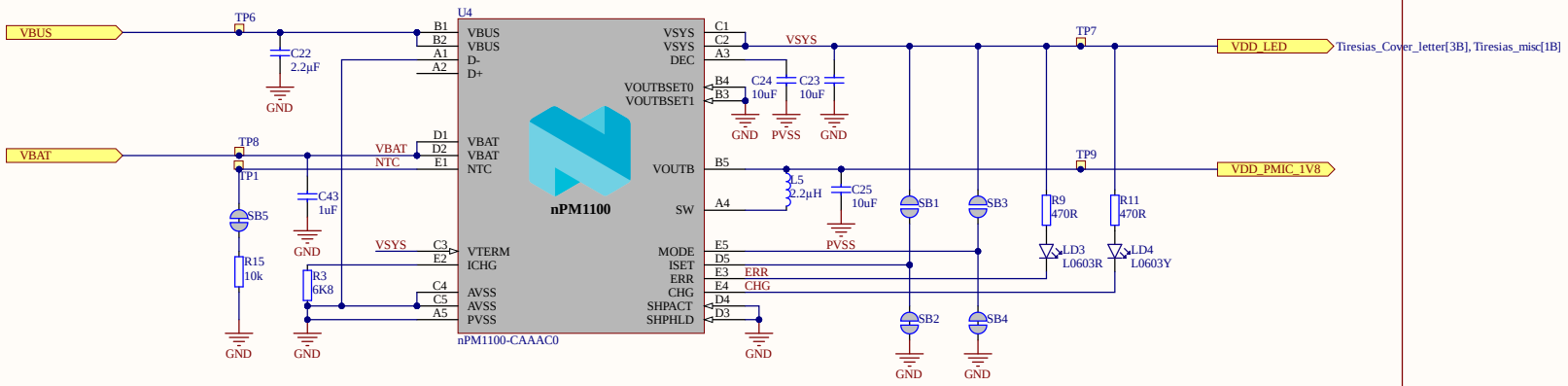


Audio Codec CLK



Title: **Audio Codec**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 17/01/2025	Time: 09:23:11	Sheet 3 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_audio_codec.SchDoc			

nPM1100 PMIC



Configurations

For fixed VBUS current options:
D+=NC; D-=AVSS and either:
ISET=AVSS for 100mA or
ISET=VSYS for 500mA

- VTERM high - 4.2V charge termination
- 3V7 LiIon or LiPo battery

- RCHG = 625/current_limit-1562.5
For 6K8 resistor current is 75mA, which is right above 70mA for the min I found at mouser

- Added NTC short and TP for external

Mode Low Automatic selection between Hysteretic and PWM modes. Since . In PWM mode, BUCK provides a clean supply operation, there are SB for an eventual change

VOUTBSET 0 and 1 to Low = 1V8 VOUTB output

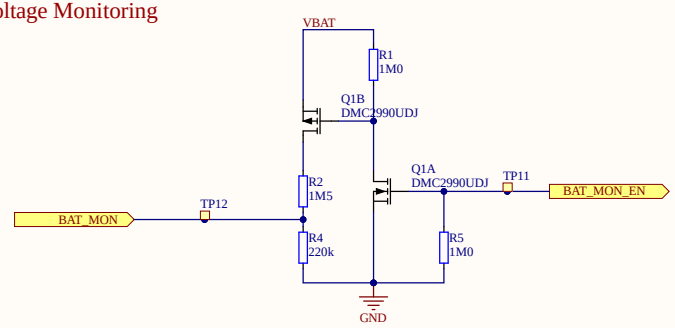
If Ship mode is not required, then SHPACT and SHPHLD pins may be tied to AVSS.

NTC
10kR +- 15 at 25 Celcius
B25/50 constant 3380K
B25/85 constant 3434 to 3435K

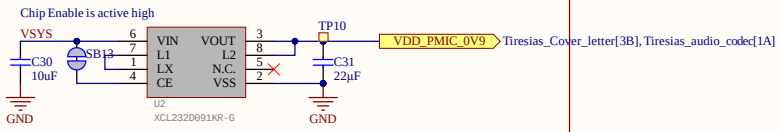
If the thermal protection feature is not used, then a 10 kΩ, ≤20% accuracy resistor should be connected between NTC and AVSS pins.

An application should not be supplied directly from VBAT because it can disturb the battery charging process and may cause incorrect behavior from the charger. Instead, VOUTB and/or VSYS should be used to supply an application.

Voltage Monitoring



Audio Codec DVDD Regulator



Reference

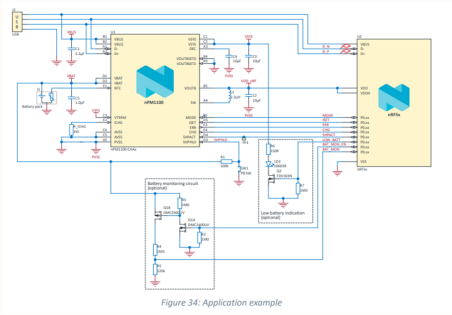


Figure 34: Application example

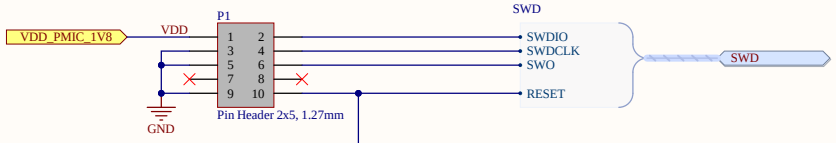
OBS

The VDD pin allows the debugger (e.g., a programmer or debug probe) to detect the operating voltage of the target system. This ensures that the debugger can adjust its signal levels (for SWDIO and SWCLK) to match the target device's logic levels, preventing damage due to mismatched voltages.
The VSYS and DEC pins must not be externally supplied

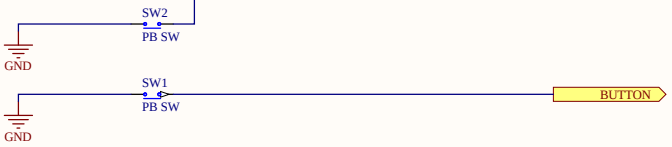
Product must have standard Vterm spec

Title: **Tiresias PMIC**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 17/01/2025	Time: 09:23:12	Sheet 4 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_PMIC.SchDoc			

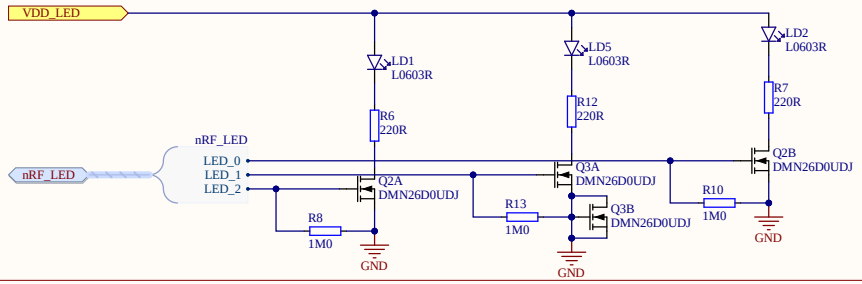
SWD Interface



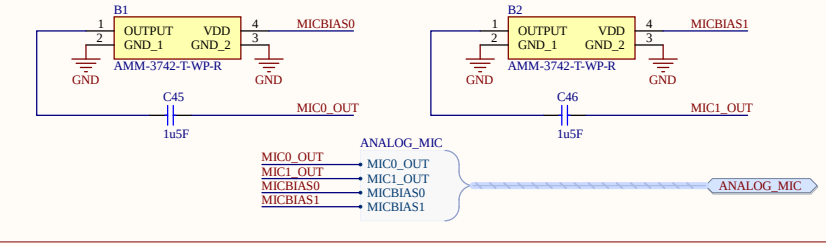
Push Button



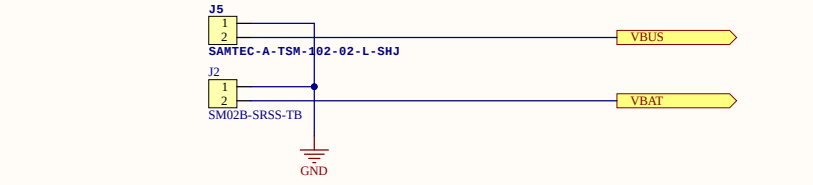
LEDs



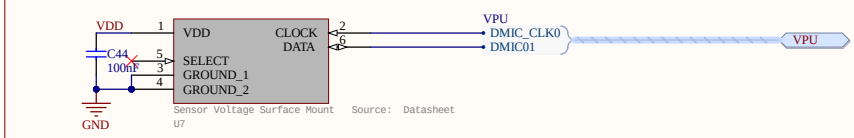
Analog Microphones



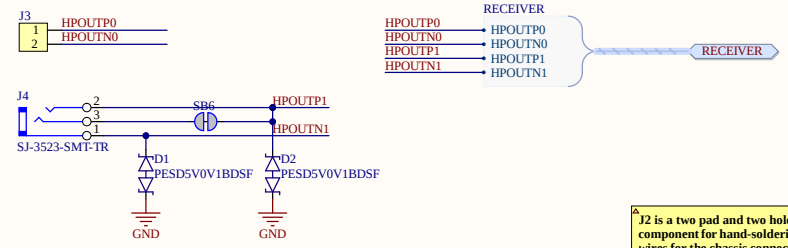
Power Connectors



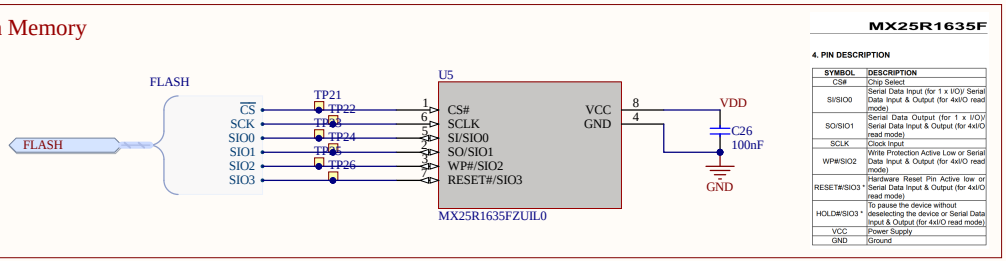
VPU



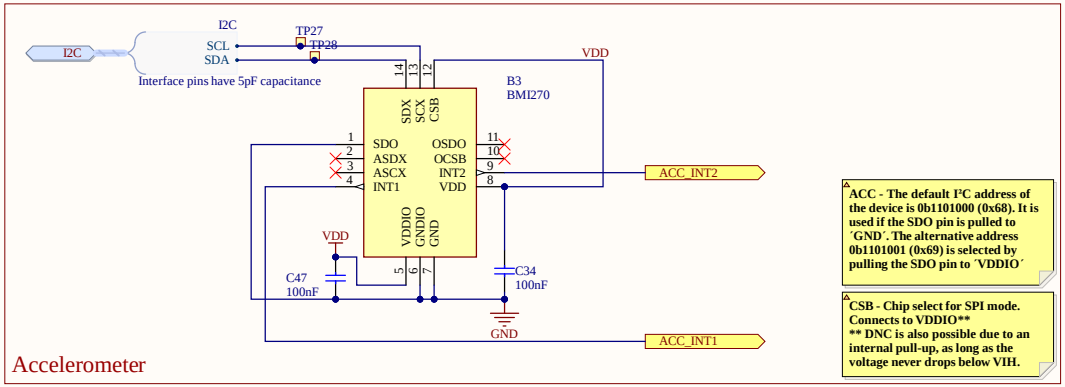
Receiver Connector



Flash Memory



Accelerometer



Title: **Tiresias Miscellaneous**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 17/01/2025	Time: 09:23:13	Sheet 5 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias\Tiresias_misc.SchDoc			