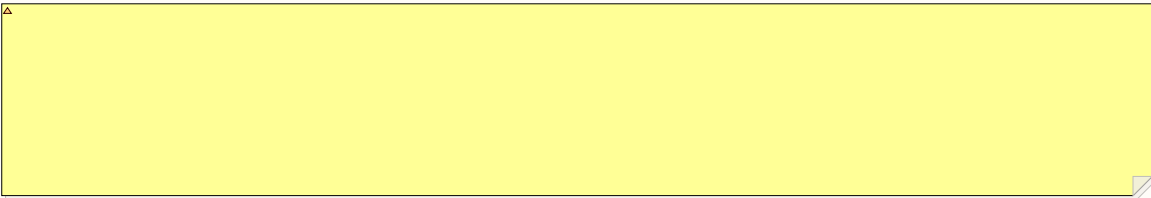


Metamaterials Group: Microwaves and Optics

Tiresias Hearing Device Prototype

Sheet 1:	Cover
Sheet 3:	MCU
Sheet 4:	Audio Codec
Sheet 5:	PMIC
Sheet 6:	Miscellaneous

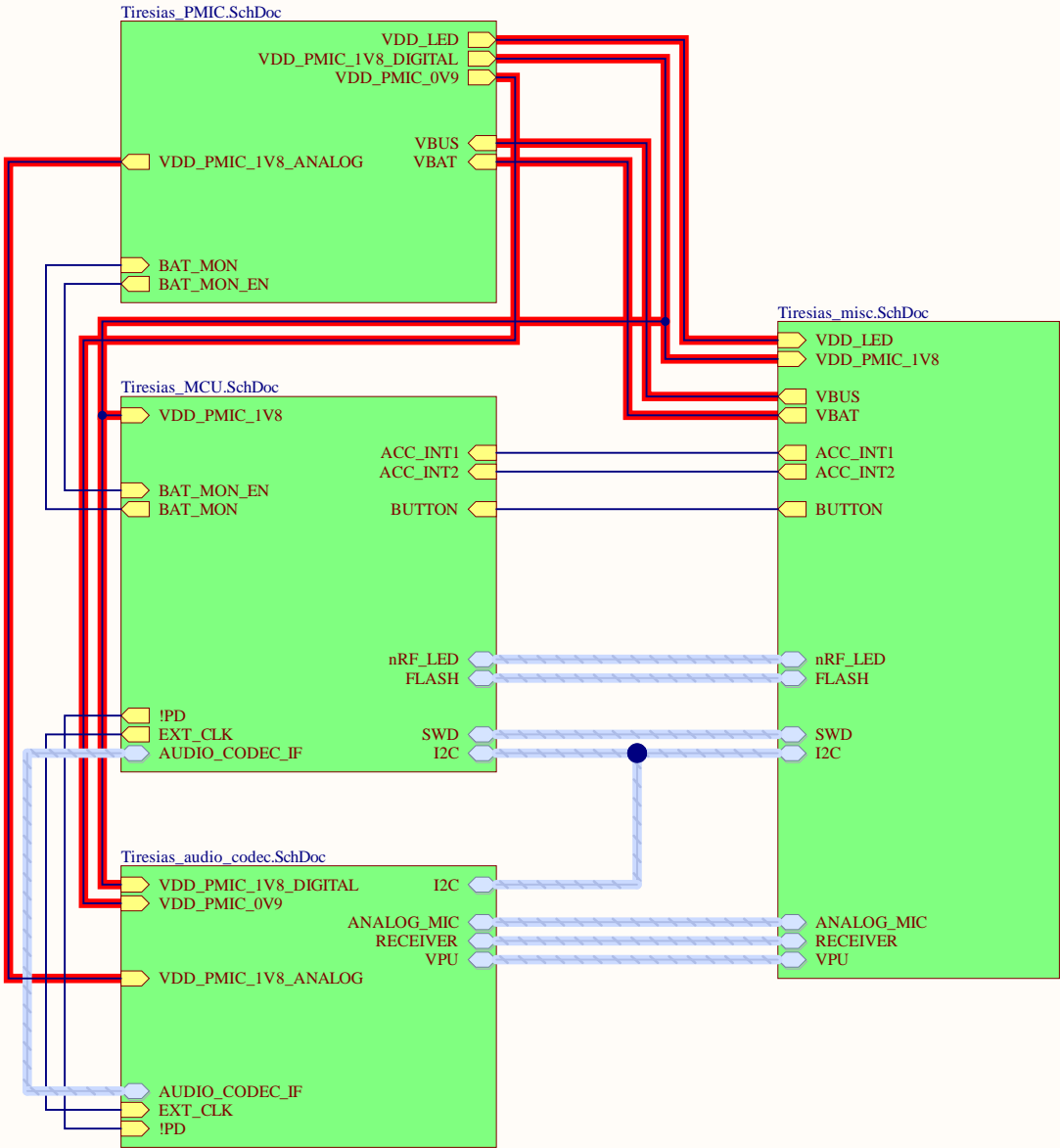
- Power Signals
- Analog Signals
- Serial Communication
- RF

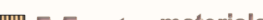


✗ The No ERC object is a design directive.
This directive is placed on a node in the circuit to suppress reported warnings and/or error violation conditions that are detected when the schematic project is compiled.

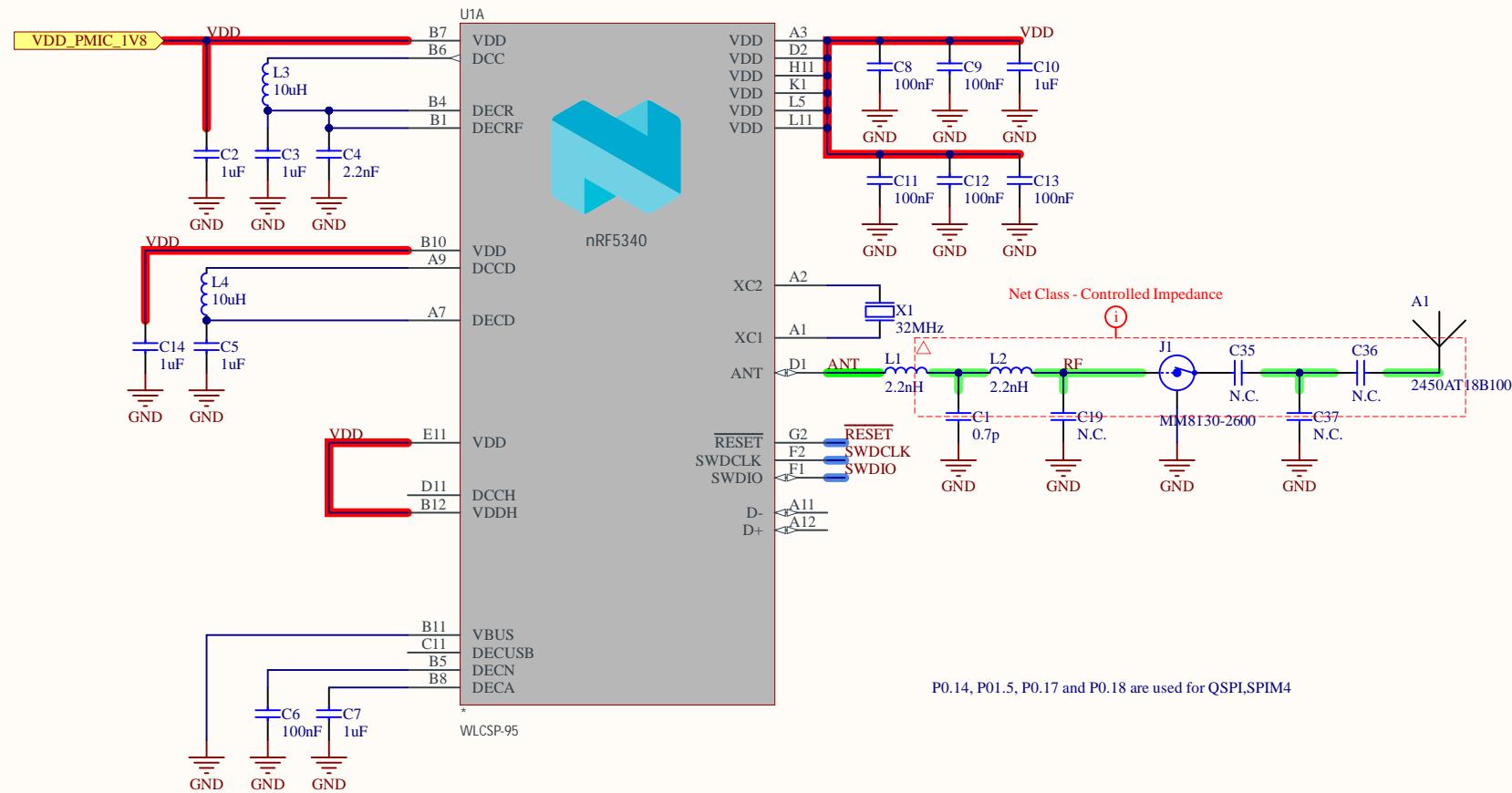
⚡ The DIFFPAIR object is a design directive.
This directive is placed on a differential pair so that they are routed accordingly.

These are fiducial marks

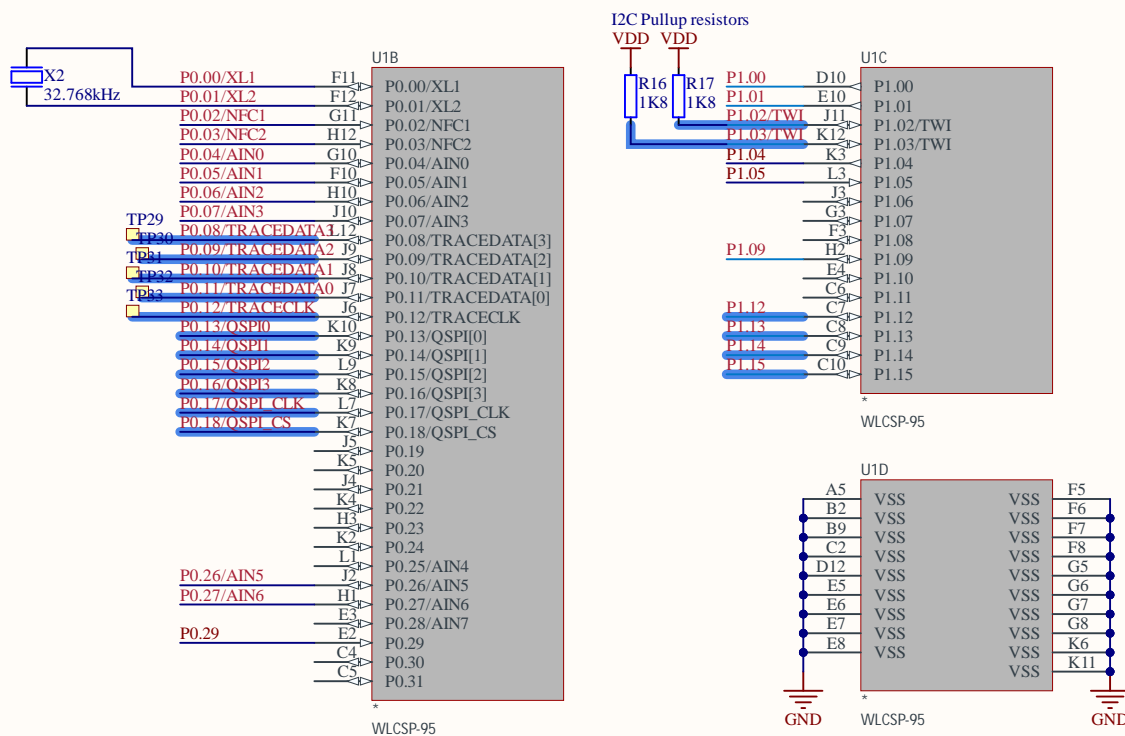


Title: Tiresias Cover Letter			<div>GMETA EESC - USP 400, Trabalhador São-Carlense Av. 13566-590, São Carlos São Paulo, Brazil</div> <div></div>
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision:0	<div>Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/</div>
Date: 10/02/2025	Time: 10:17:58	Sheet 1 of 5	
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_Cover_letter.SchDoc			

Nordic nRF52811 MCU

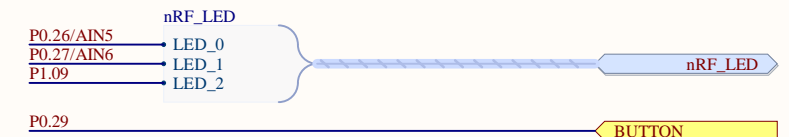


MCU Peripherals

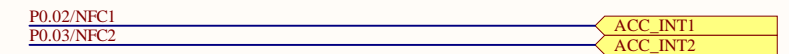


OBS

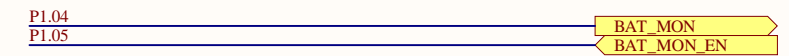
User Interface



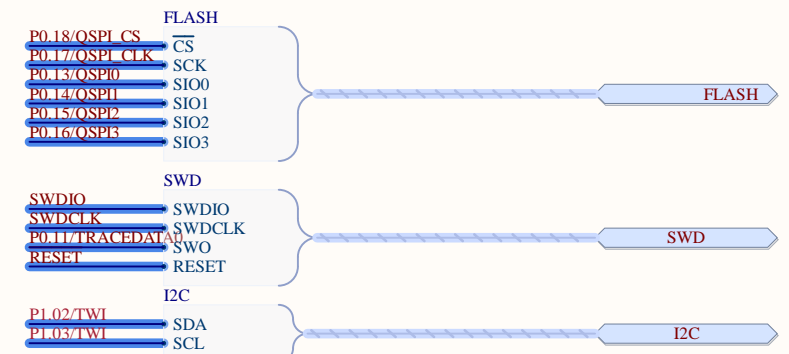
Accelerometer



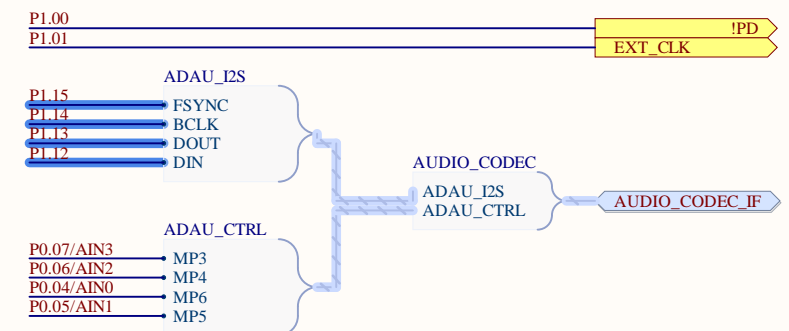
PMIC




Serial Communication



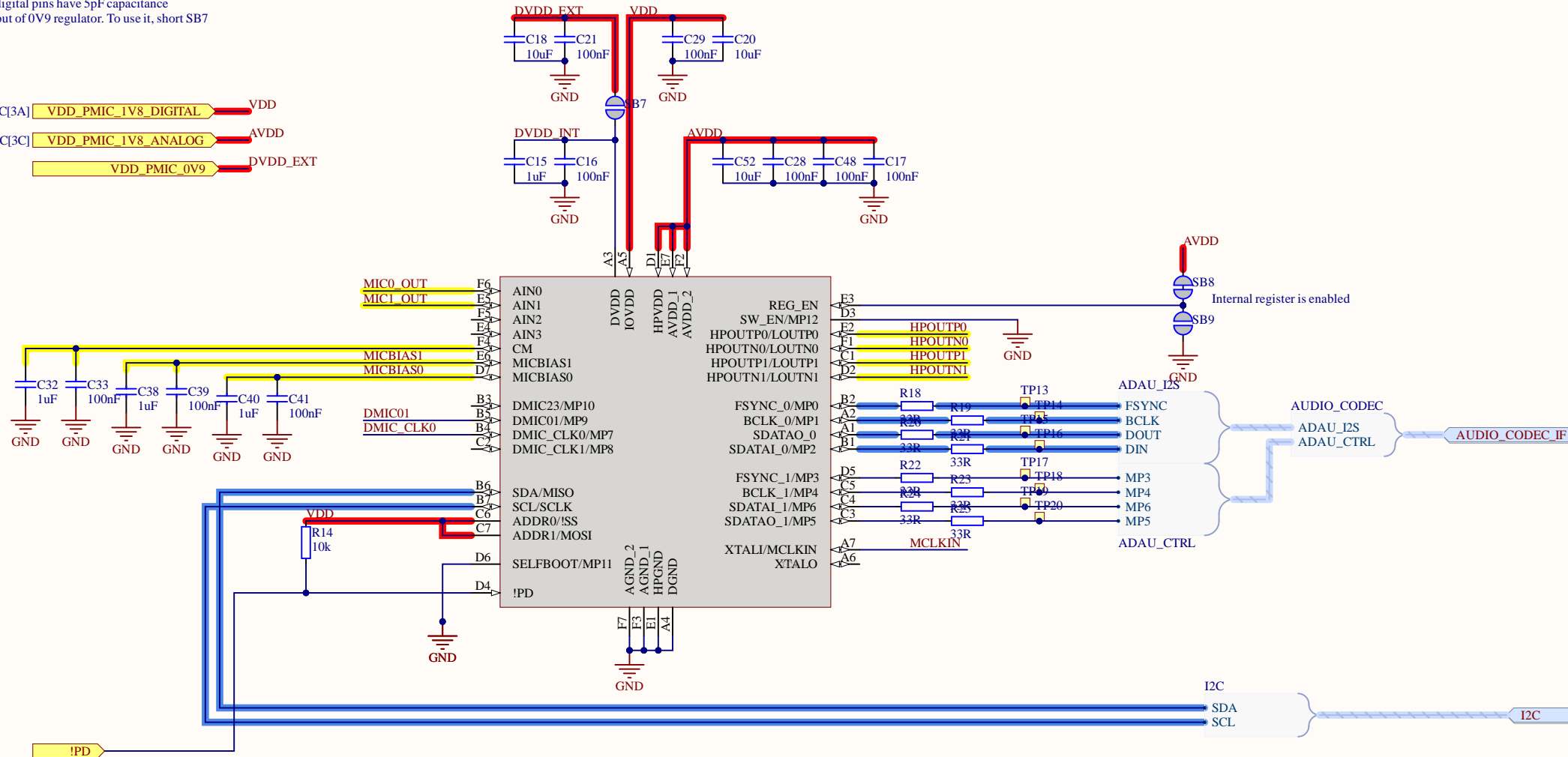
Audio Codec



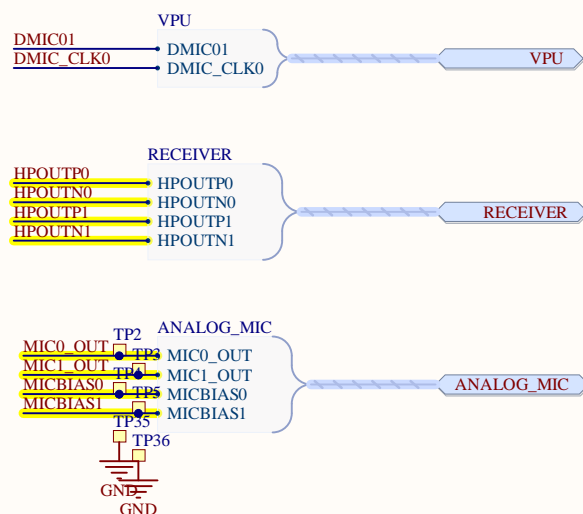
Title: MCU			
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 10/02/2025	Time: 10:17:58	Sheet 2 of 5	GMETA <i>EESC - USP</i> <i>400, Trabalhador São-Carlense Av.</i> <i>13566-590, São Carlos</i> <i>São Paulo, Brazil</i> Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_MCU.SchDoc			

Analog Devices ADAU1787 Audio Codec

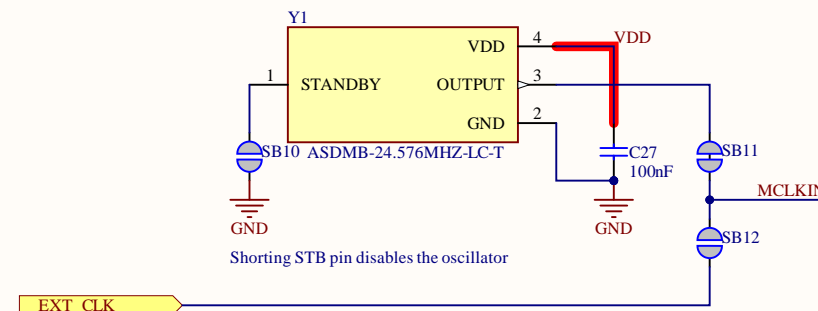
All digital pins have 5pF capacitance
Output of 0V9 regulator. To use it, short SB7



Audio Codec Peripherals



Audio Codec CLK



Title: Audio Codec			
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 10/02/2025	Time: 10:17:58	Sheet 3 of 5	
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_audio_codec.SchDoc			R&D GMETA <i>EESC - USP</i> 400, Trabalhador São-Carlos Av. 13566-590, São Carlos São Paulo, Brazil Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/

OBS

▲ For CLK use PWM from NRF.
XTALO is open and crystal oscillator
reg must be disabled

REG_EN can be grounded to disable 0.9V LDO if DVDD is supplied

⚠ Do not power up IOVDD when power is not applied to AVDD.

▲ I2C/SPI Enable (SW_EN). Connect this pin to DGND.

Configurations

1 - Using two analog inputs with passives recommended by PUI audio. Do not forget to use a PUI with lower than 1.6V spec

2 - Bypassed power. DVDD is bypassed even if internal reg is used. IOVDD and AVDD are both connected to 1V8

4 - Falta a gravação com int e ext, mas por enquanto prefiro fazer com o interno.

REG_EN - Regulator Enable. Tie this pin to AVDD to enable the regulator, and tie this pin to ground to disable the regulator

The IC can be put into I2C and/or SPI mode by tying the SW_EN pin to DGND

5 - CM bypassed. Could also be used for external amp common mode adjust

6 - Selfboot puts ADAU on master mode so that it boots using the EEPROM. Not used here

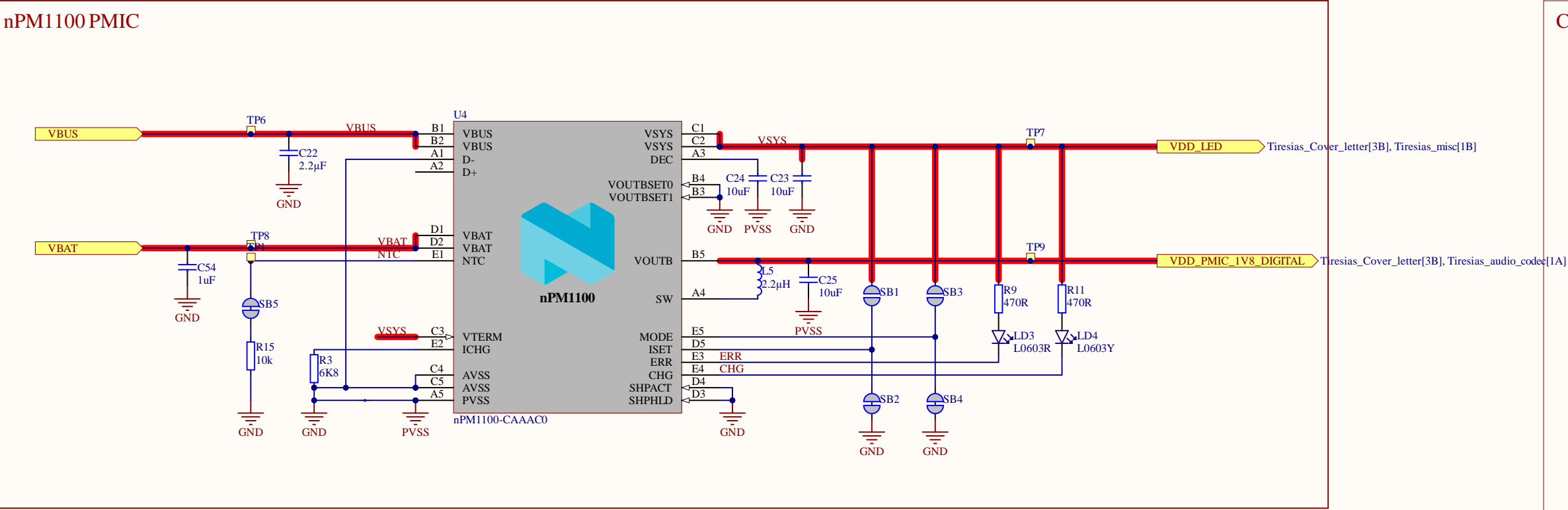
7 - PD control via microcontroller

8 - For the I2S remember to use compatible GPIO on the nordic side

9 - I2C addreses set to 0x2B with both ADDR0 and ADDR1 connected to IOVDD

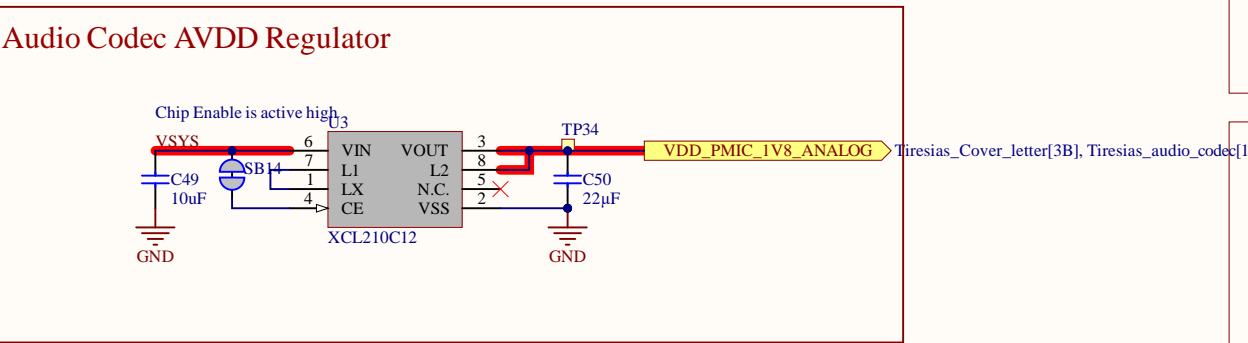
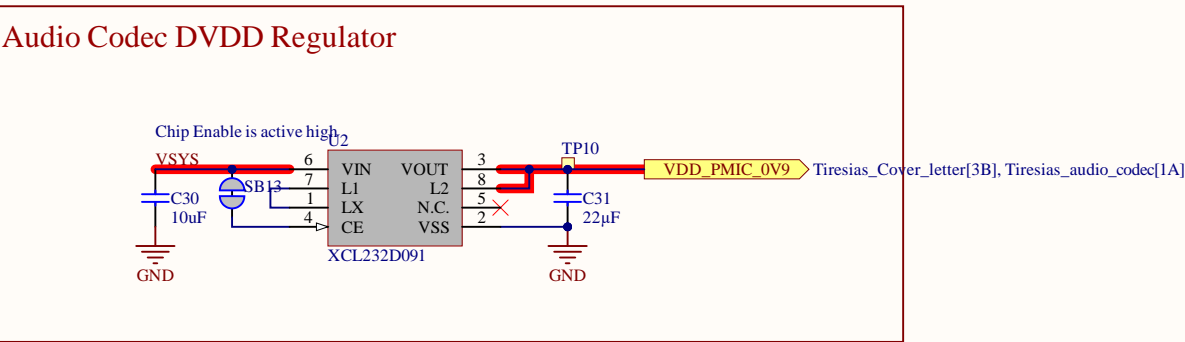
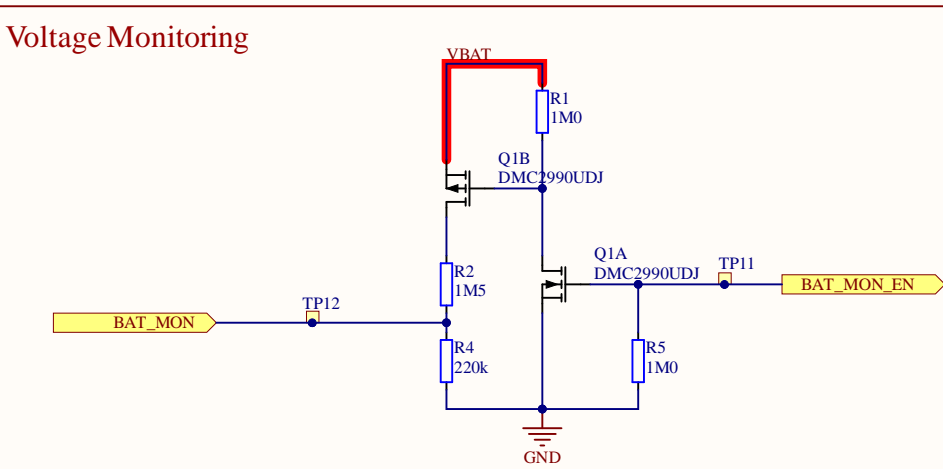
10 - CLK	
----------	--

11 - DMIC connection
vesper VPU alone



- ### Configurations
- For fixed VBUS current options:
D+=NC; D-=AVSS and either:
ISET=AVSS for 100mA or
ISET=VSYS for 500mA
 - VTERM high - 4.2V charge termination
- 3V7 Lilon or LiPo battery
 - RCHG = 625/current_limit-1562.5
For 6K8 resistor current is 75mA, which is right above 70mA for the min I found at mouser
 - Added NTC short and TP for external
 - Mode Low Automatic selection between Hysteretic and PWM modes. Since . In PWM mode, BUCK provides a clean supply operation, there are SB for an eventual change
 - VOUTBSET 0 and 1 to Low = 1V8 VOUTB output
 - If Ship mode is not required, then SHPACT and SHPHLD pins may be tied to AVSS.
 - NTC
10kR +- 15 at 25 Celcius
B25/50 constant 3380K
B25/85 constant 3434 to 3435K

If the thermal protection feature is not used, then a 10 kΩ, ≤20% accuracy resistor should be connected between NTC and AVSS pins.
 - An application should not be supplied directly from VBAT because it can disturb the battery charging process and may cause incorrect behavior from the charger. Instead, VOUTB and/or VSYS should be used to supply an application.

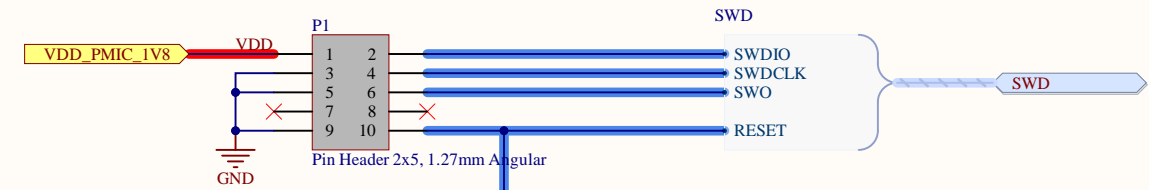


Reference

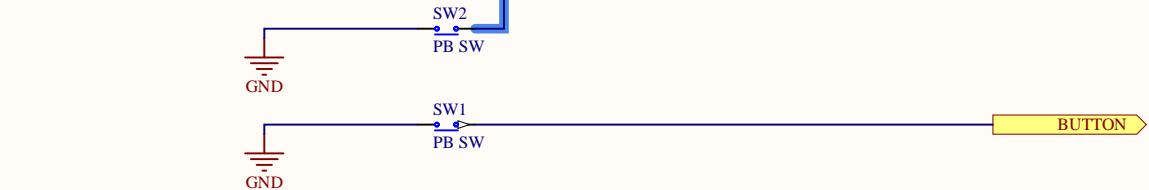
Cannot open file C:\Users\alunos\Desktop\reference.PNG. File does not exist.

- ### OBS
- The VDD pin allows the debugger (e.g., a programmer or debug probe) to detect the operating voltage of the target system. This ensures that the debugger can adjust its signal levels (for SWDIO and SWCLK) to match the target device's logic levels, preventing damage due to mismatched voltages. The VSYS and DEC pins must not be externally supplied
 - Product must have standard Vterm spec

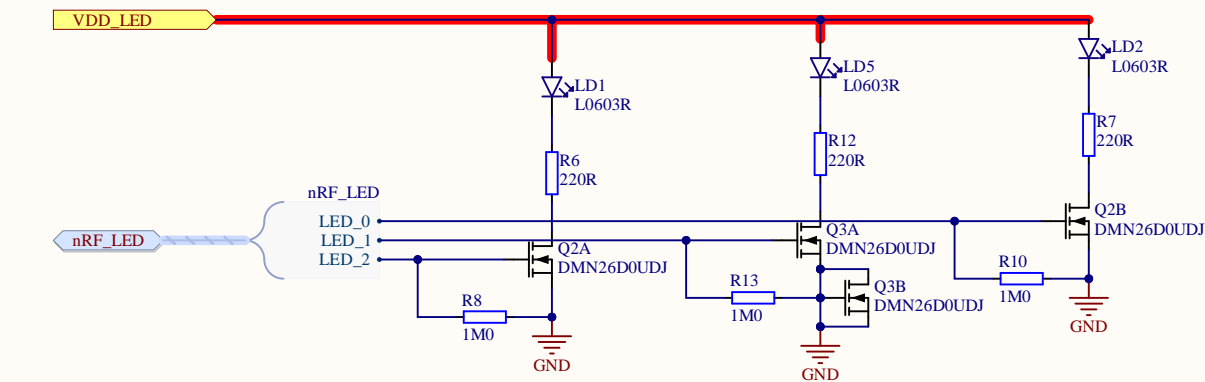
SWD Interface



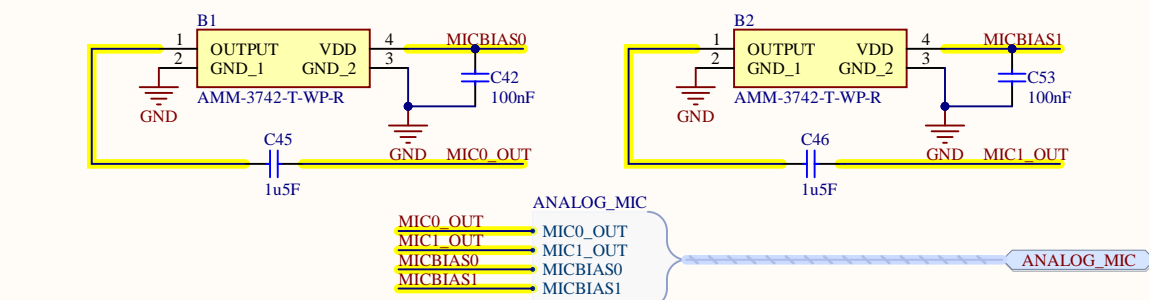
Push Button



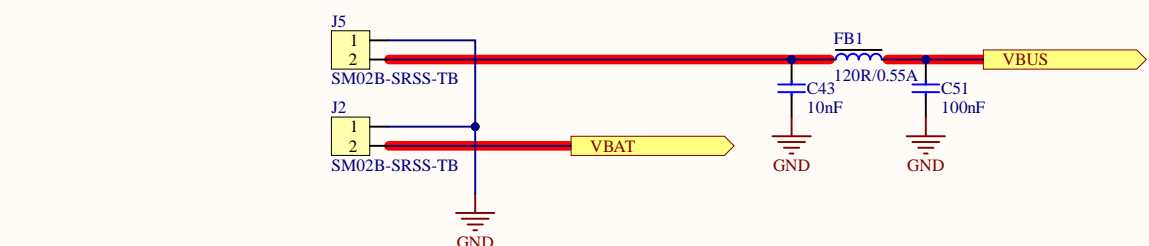
LEDs



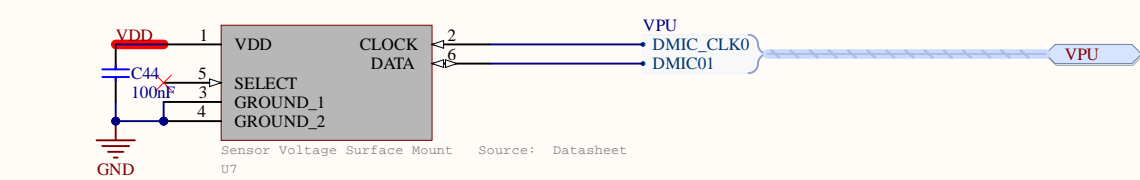
Analog Microphones



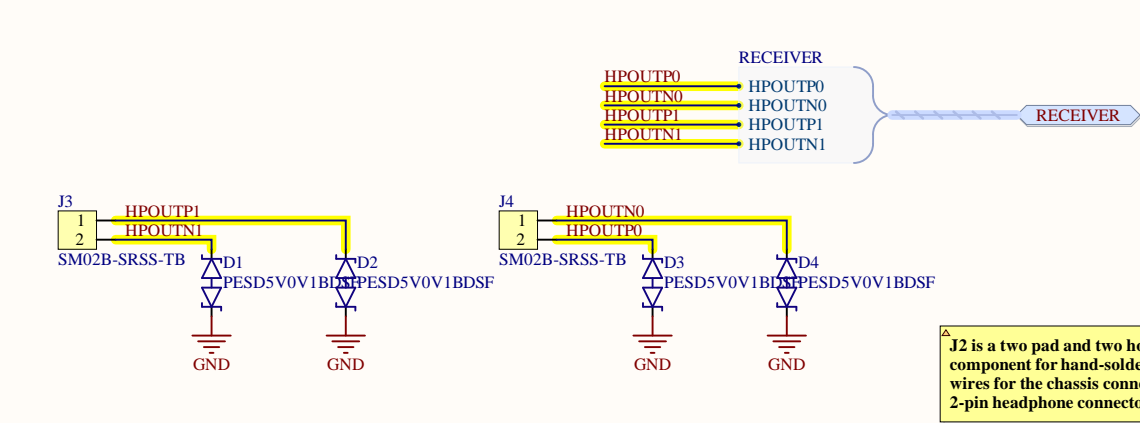
Power Connectors



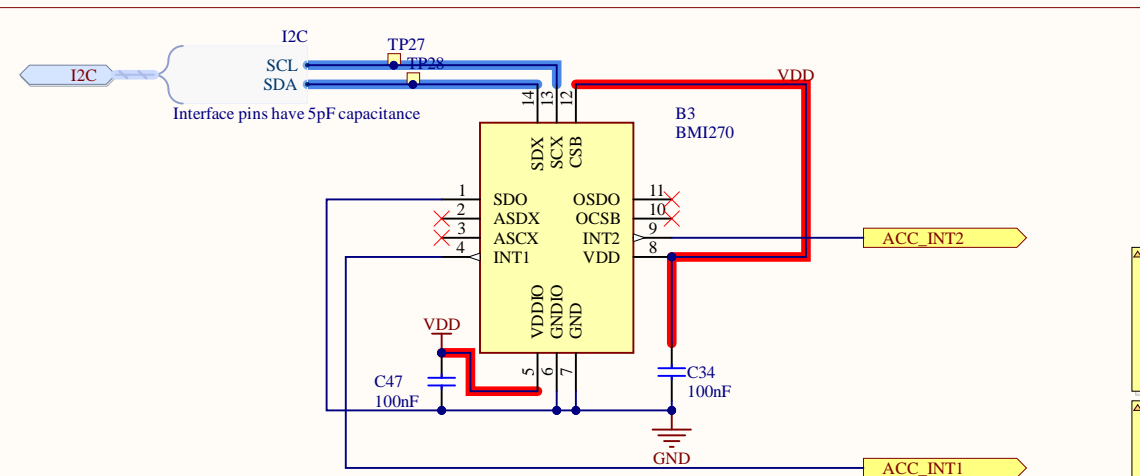
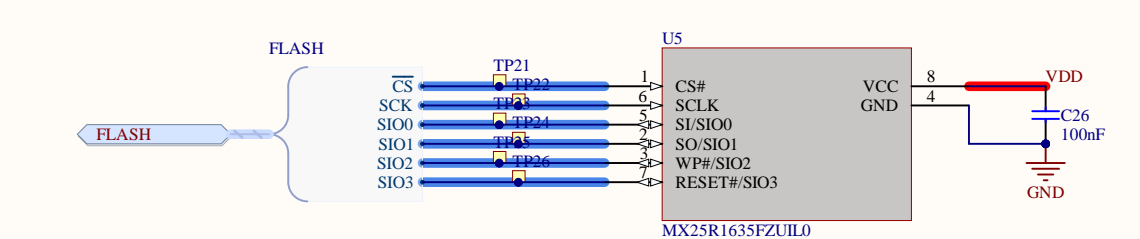
VPU



Receiver Connector



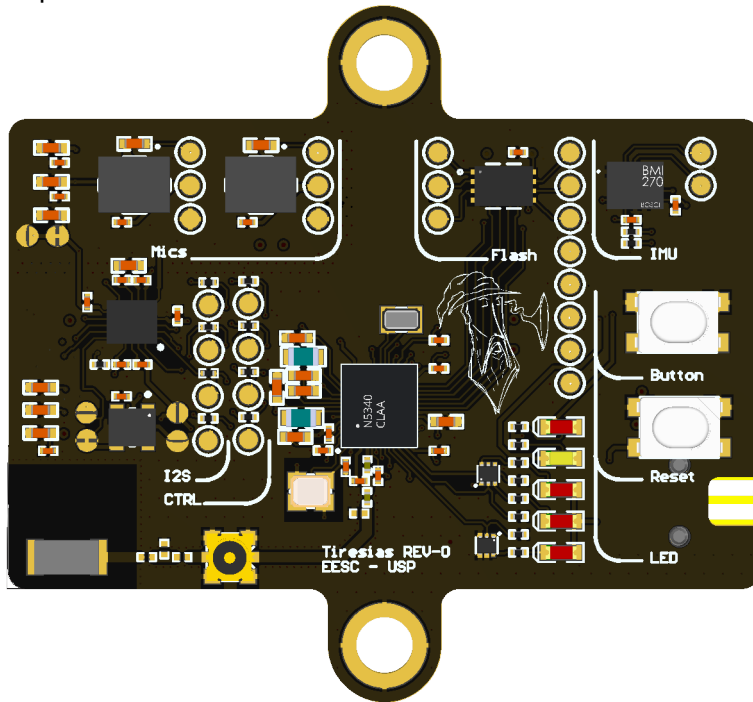
Flash Memory



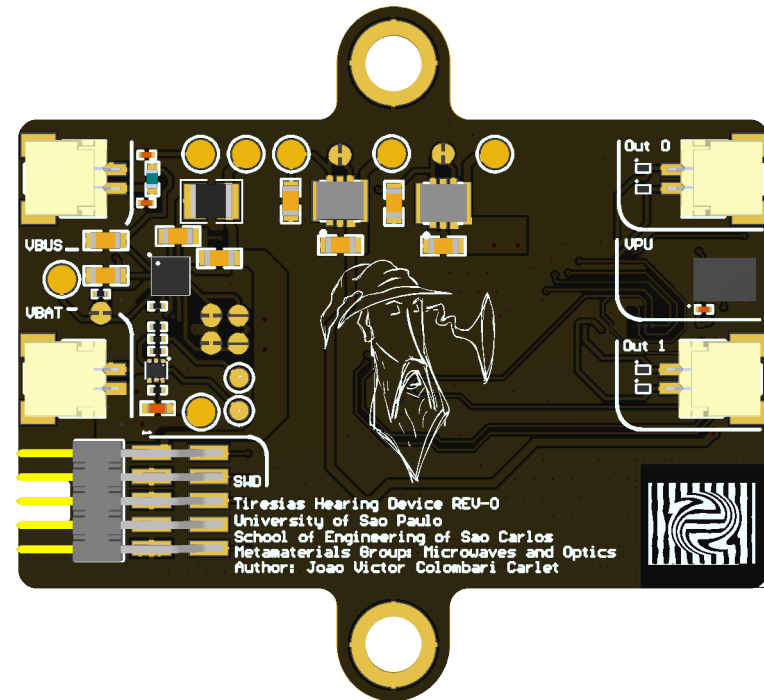
Accelerometer

Tiresias Hearing Device Prototype - Hardware Documentation

Top View



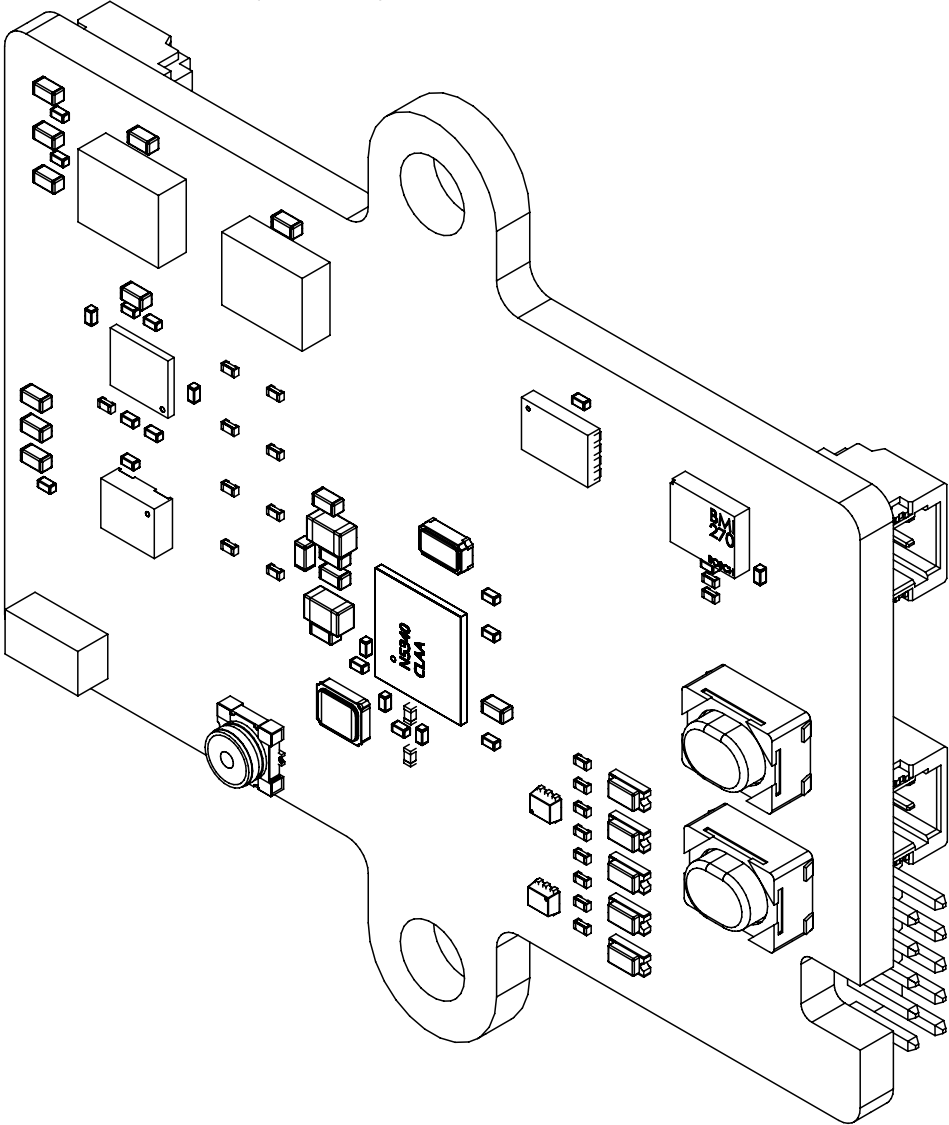
Bottom View



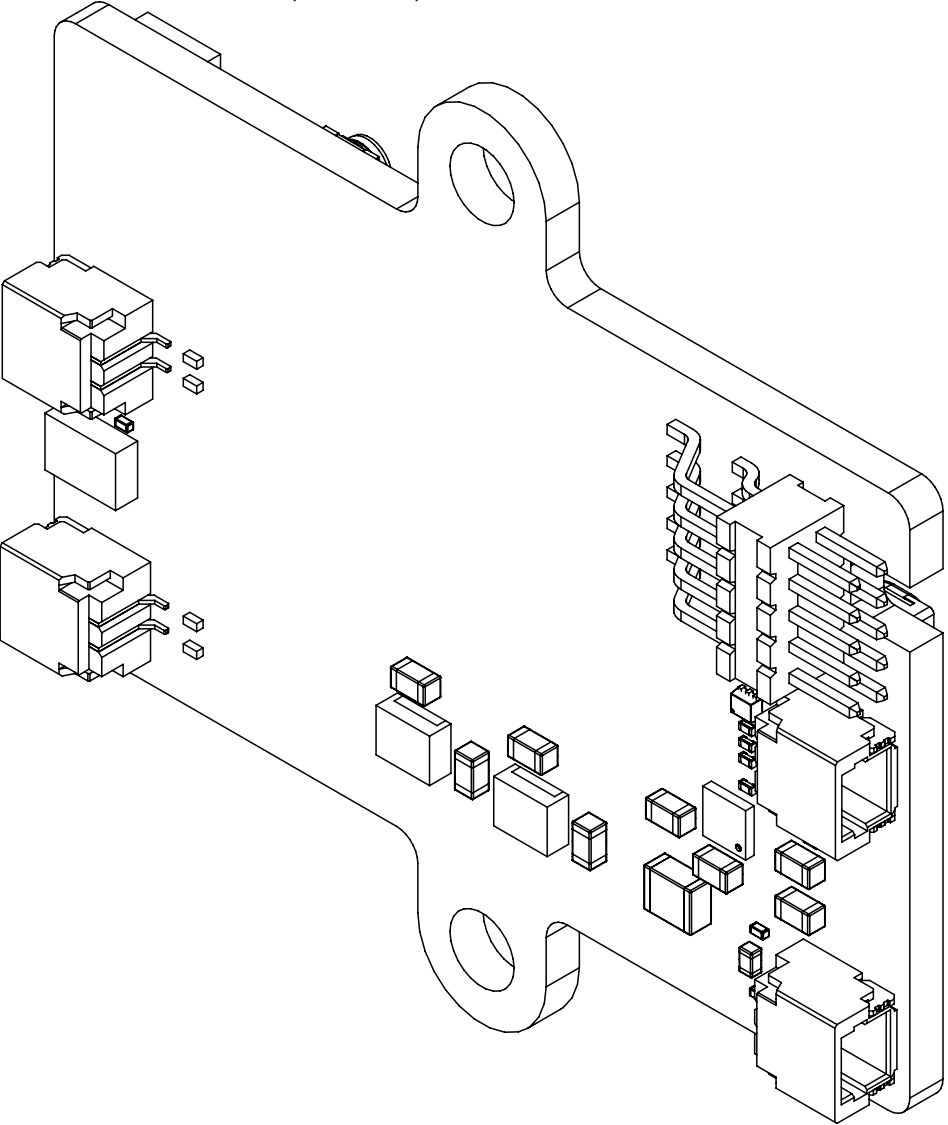
Engineer: João Victor Colombari Carlet

ISO View

View from Top side (Scale 4:1)



View from Bottom side (Scale 4:1)










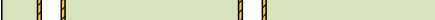





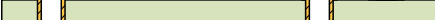






Stack-Up and Impedance

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Substack	Clearance	Target Tolerance
1	Coated Coplanar Waveguide With Ground	50	49.99	Top Layer	0.55mm	0.55mm	Int4 (GND)	Board Layer Stack	0.13mm	10%
2	Coated Coplanar Waveguide With Ground	50	49.99	Bottom Layer	0.55mm	0.55mm	Int1 (GND)	Board Layer Stack	0.13mm	10%

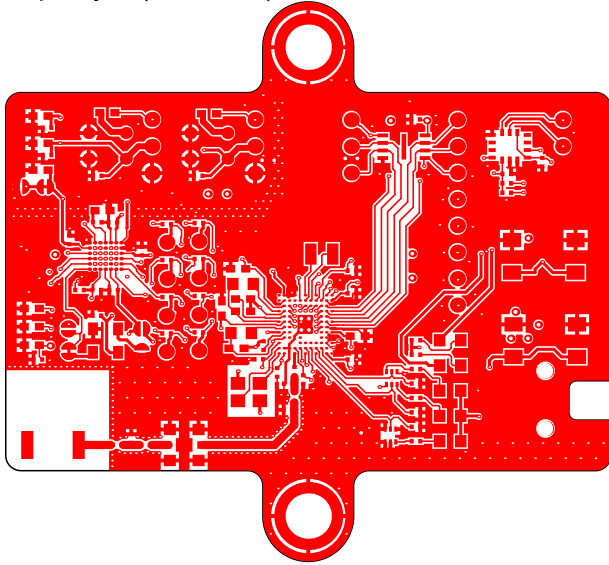
Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
		Top Overlay			Legend	GTO
	Surface Material	Top Solder	0.03mm	SM-002	Solder Mask	GTS
	Nickel, Gold	Top Surface Finish	0.00mm		Surface Finish	
	CF-004	Top Layer	0.04mm		Signal	GTL
	Prepreg		0.07mm	PP-006	Dielectric	
	Prepreg		0.07mm	PP-006	Dielectric	
	CF-004	Int1 (GND)	0.04mm		Signal	G1
	Core		0.46mm	Core-035	Dielectric	
	CF-004	Int2 (PWR)	0.04mm		Signal	G2
	Prepreg		0.07mm	PP-006	Dielectric	
	Prepreg		0.07mm	PP-006	Dielectric	
	CF-004	Int3 (SIG)	0.04mm		Signal	G3
	Core		0.46mm	Core-035	Dielectric	
	CF-004	Int4 (GND)	0.04mm		Signal	G4
	Prepreg		0.07mm	PP-006	Dielectric	
	Prepreg		0.07mm	PP-006	Dielectric	
	CF-004	Bottom Layer	0.04mm		Signal	GBL
	Nickel, Gold	Bottom Surface Finish	0.00mm		Surface Finish	
	Surface Material	Bottom Solder	0.03mm	SM-002	Solder Mask	GBS
		Bottom Overlay			Legend	GBO

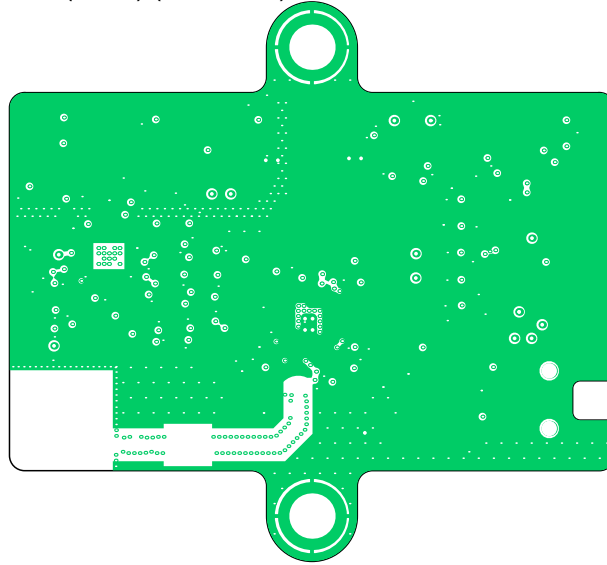
Total thickness: 1.61mm

Layers

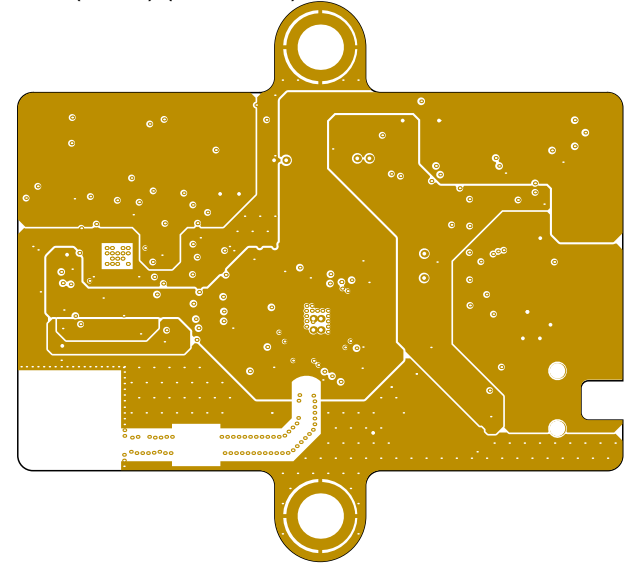
Top Layer (Scale 2:1)



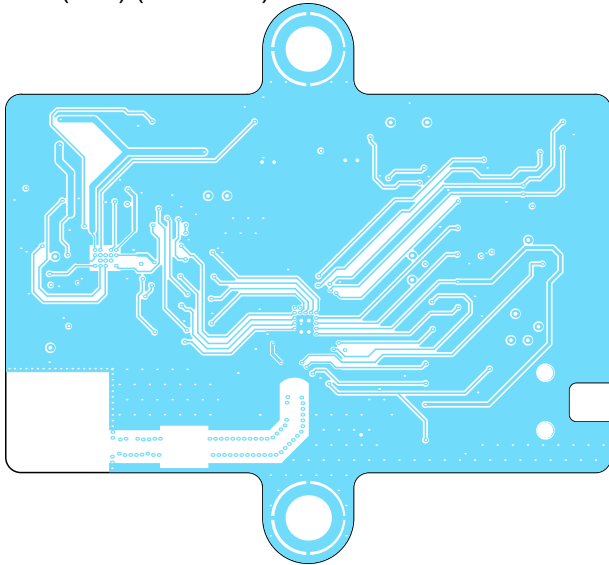
Int1 (GND) (Scale 2:1)



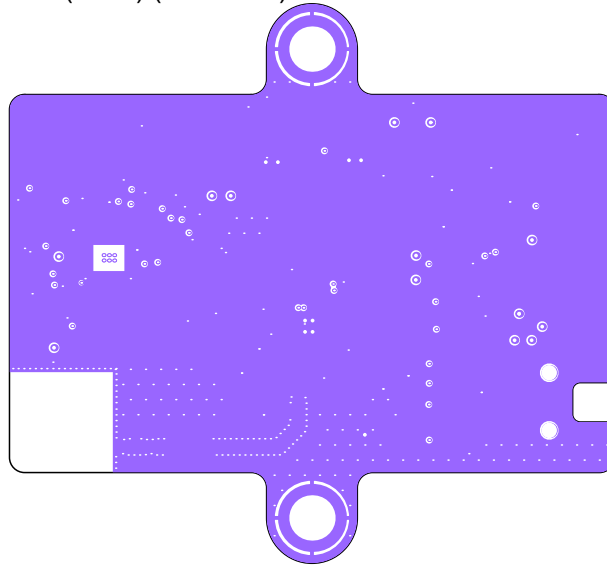
Int2 (PWR) (Scale 2:1)



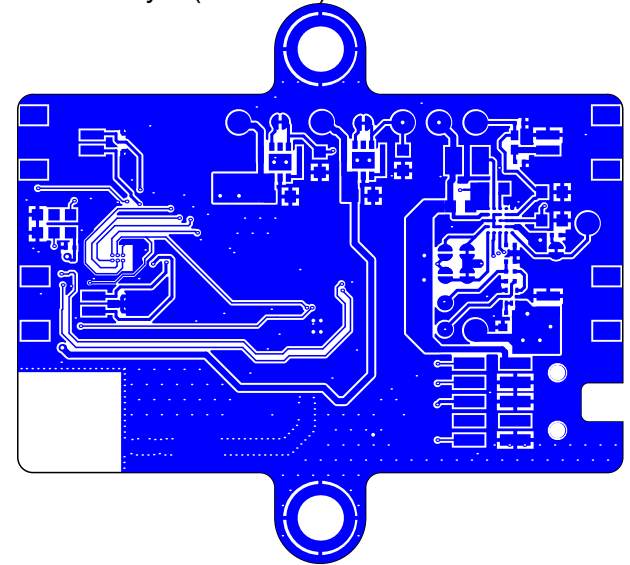
Int3 (SIG) (Scale 2:1)



Int4 (GND) (Scale 2:1)



Bottom Layer (Scale 2:1)

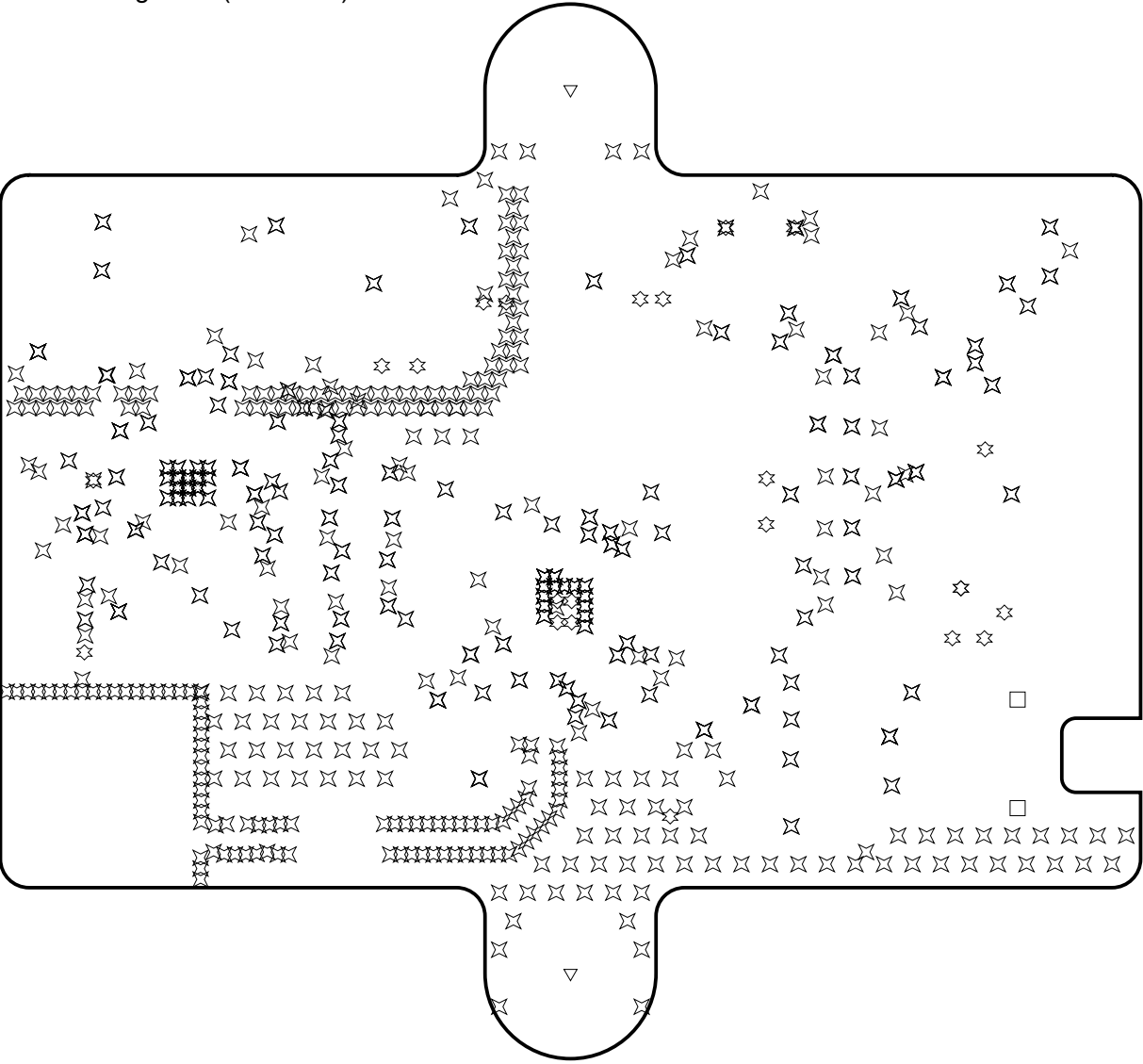


Drills

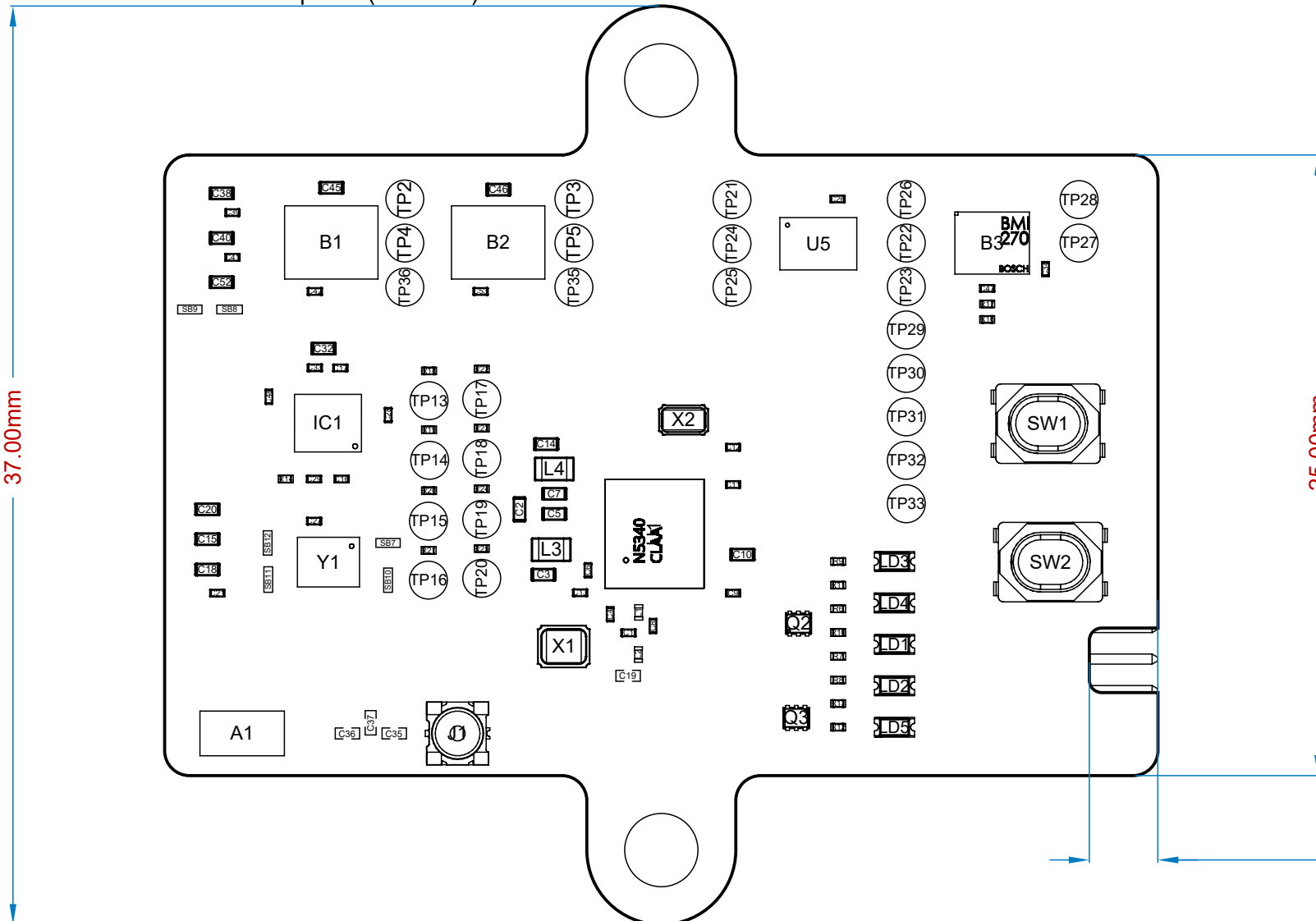
Drill Drawing View (Scale 4:1)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
✧	802	0.10mm	Plated	
☆	23	0.25mm	Plated	
□	2	1.02mm	Non-Plated	
▽	2	3.00mm	Plated	
	829 Total			



F



Assembly Bottom

