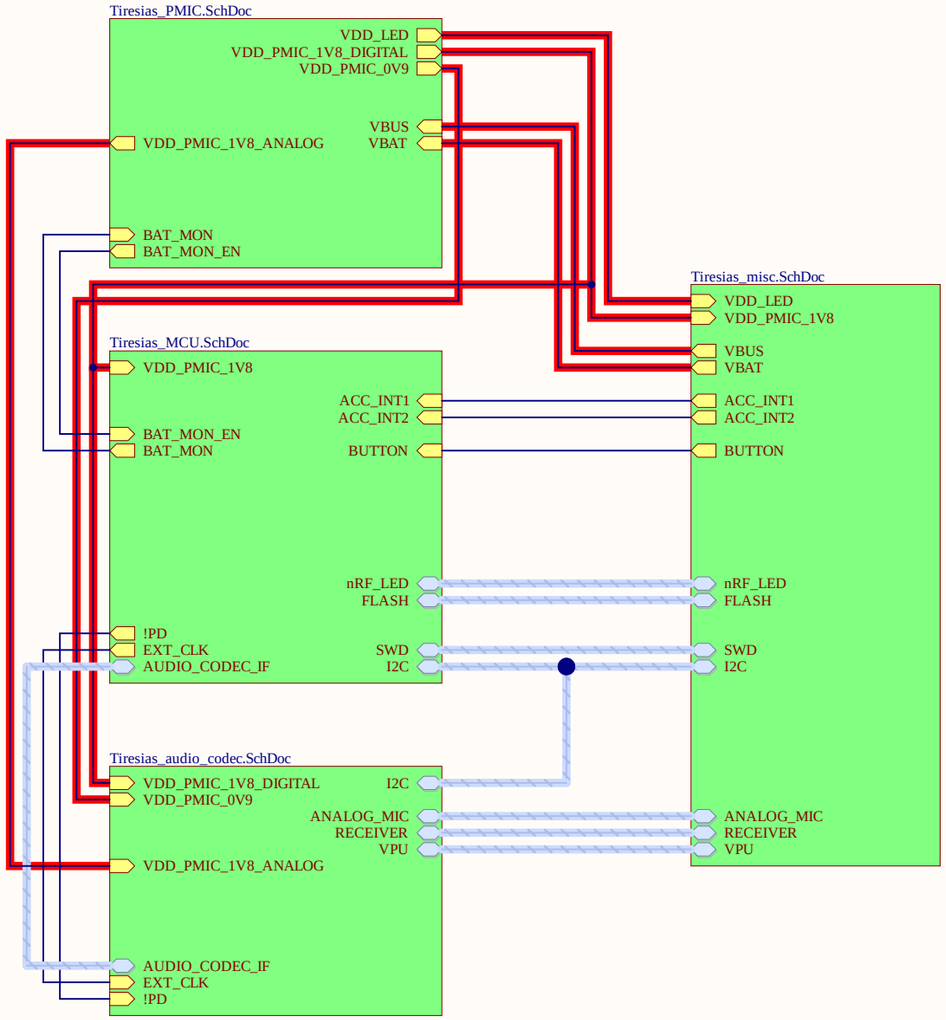
Metamaterials Group: Microwaves and Optics

Tiresias Hearing Device Prototype

Sheet 1: Cover
Sheet 3: MCU
Sheet 4: Audio Codec
Sheet 5: PMIC
Sheet 6: Miscellaneous



- Power Signals
- Analog Signals
- Serial Communication
- RF

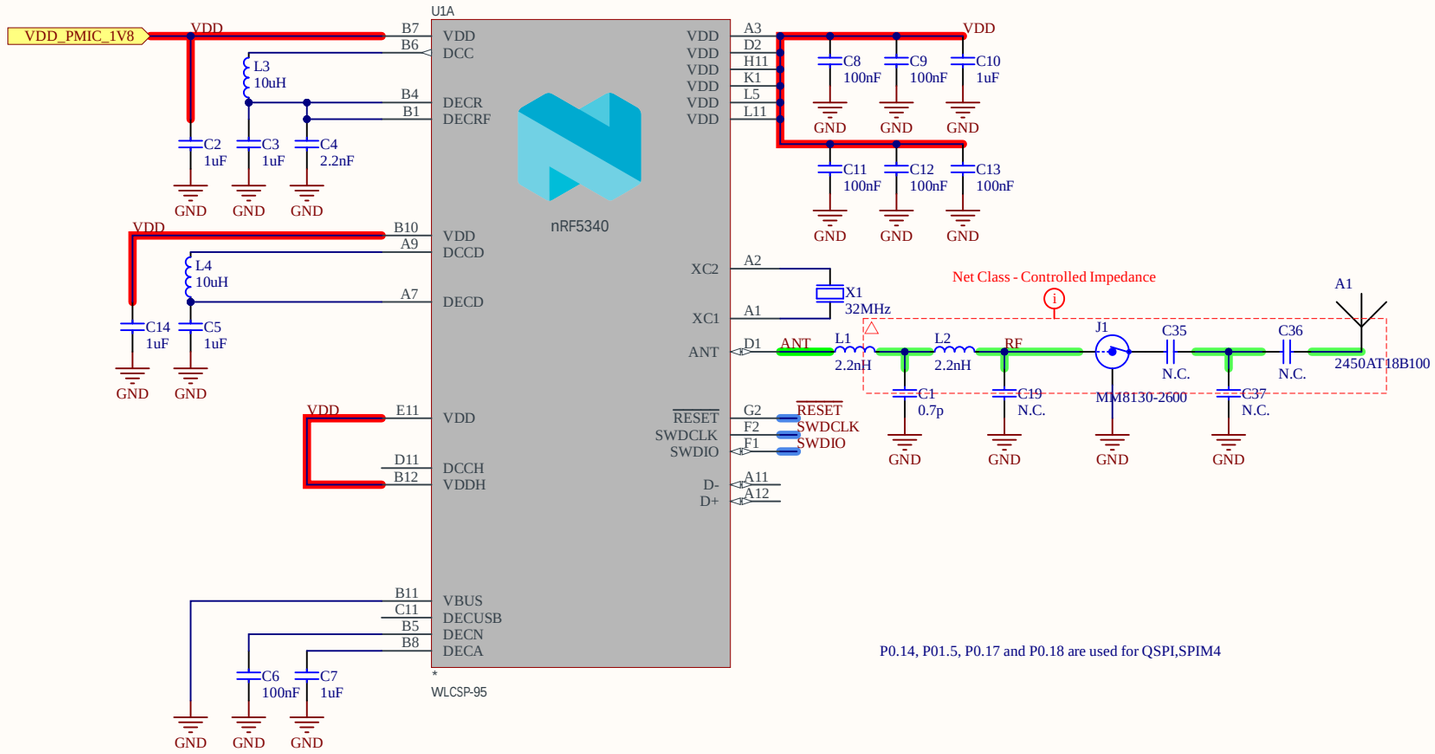
The No ERC object is a design directive.
This directive is placed on a node in the circuit to suppress reported warnings and/or error violation conditions that are detected when the schematic project is compiled.

The DIFFPAIR object is a design directive.
This directive is placed on a differential pair so that they are routed accordingly.

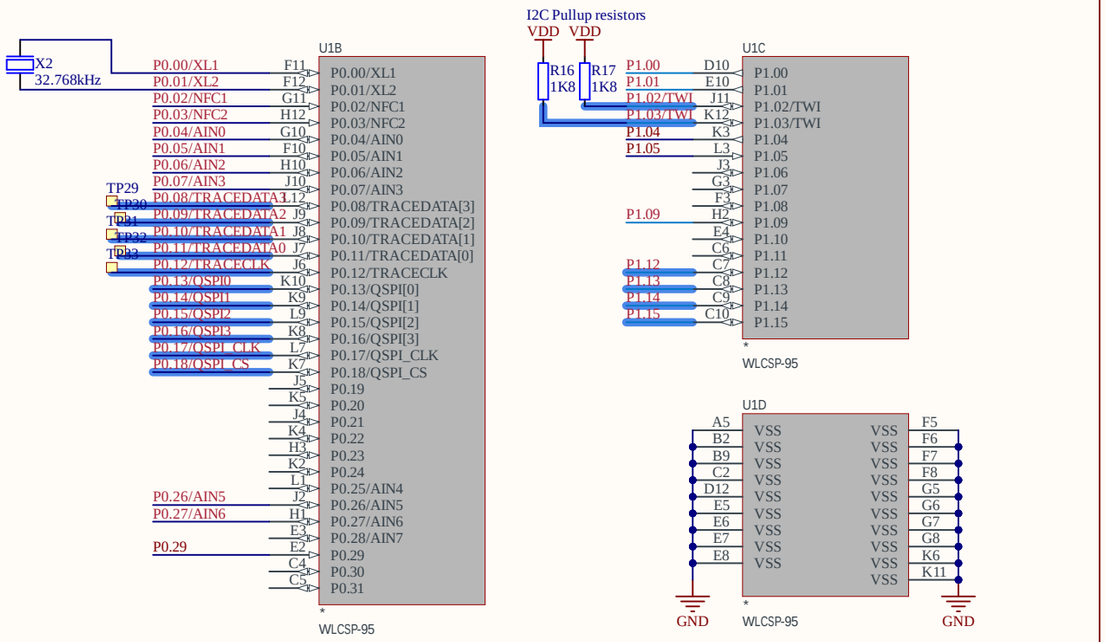
These are fiducial marks

Title: **Tiresias Cover Letter**			*GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 13/02/2025	Time: 15:18:43	Sheet 1 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_Cover_letter.SchDoc			

Nordic nRF5340 MCU



MCU Peripherals

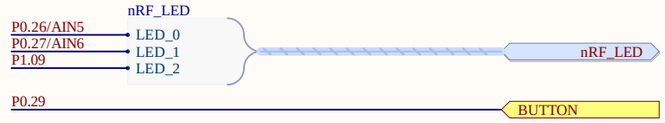


- Normal voltage mode on page 42 - Powers the device through the VDD pin
- High voltage mode on page 43 - Powers the device through the VDDH pin

VDDH pin is connected to a high voltage source (3V) and supplies it to VDD after an internal regulator - VREGH. This output is then fed to two internal regulators - VREGRADIO and VREGMAIN. The first feeds the network core, while the second feeds the application core. For normal voltage mode. an external power supply is connected to both VDD and VDDH pins, thus only the VREGMAIN and VREGRADIO are used. In this case, VREGH IS AUTOMATICALLY DEACTIVATED.
In normal voltage mode, each regulator can operate in LDO or DC/DC mode. The VREGMAIN and VREGRADIO regulators operate in LDO mode by default.

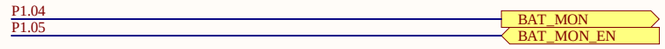
OBS

User Interface

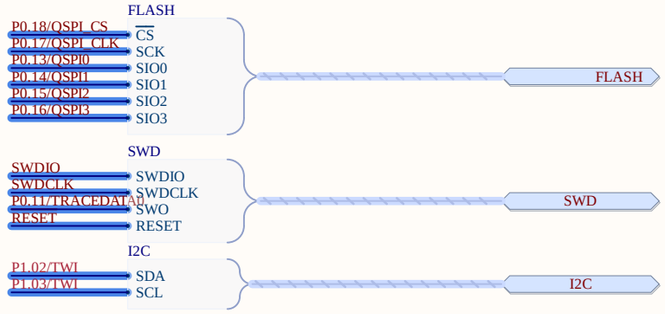


Accelerometer

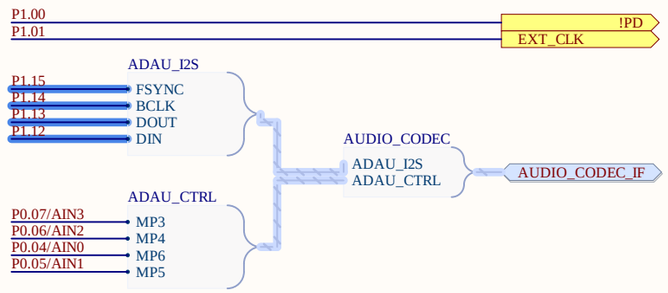
PMIC



Serial Communication



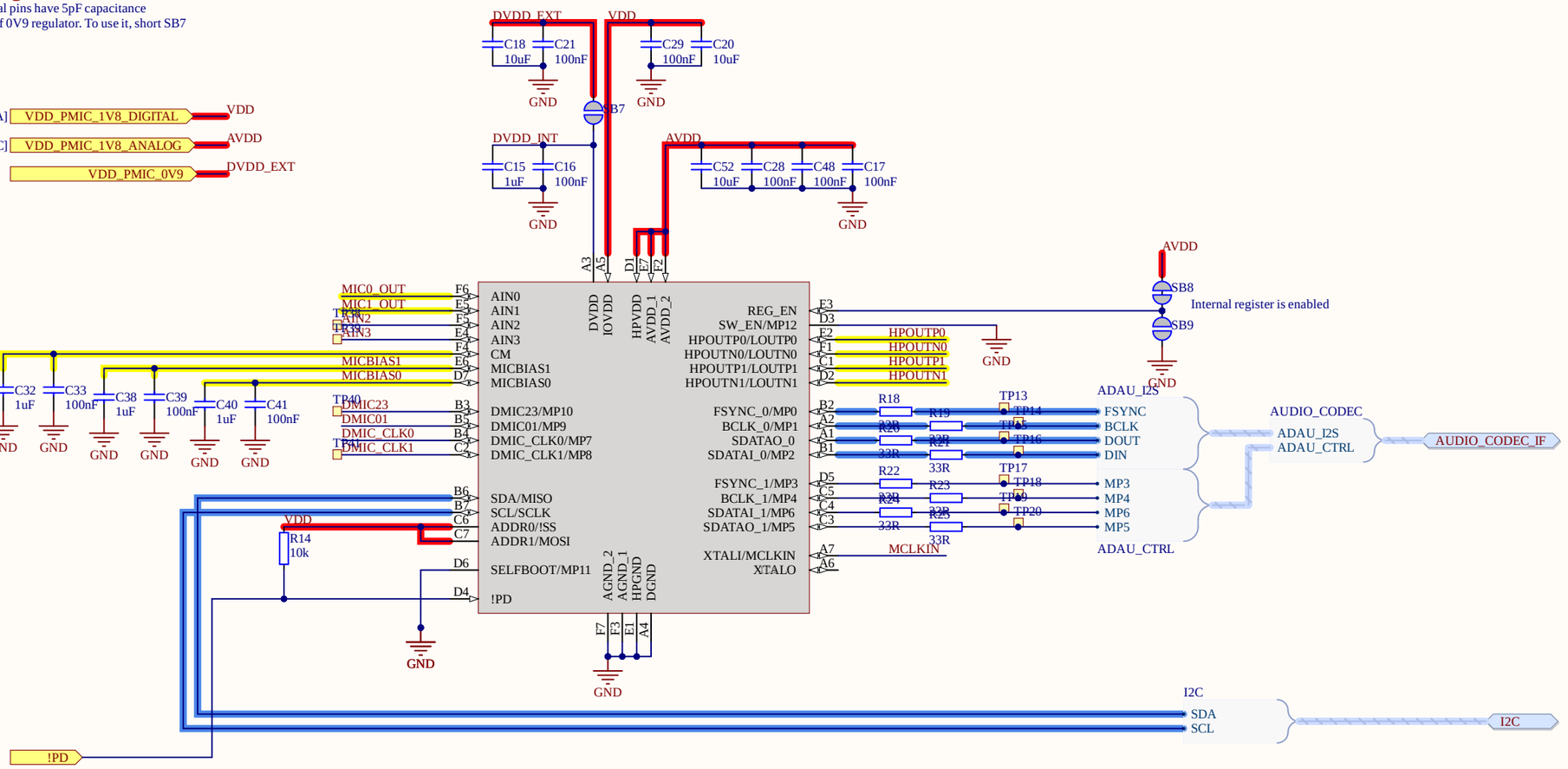
Audio Codec



Title: **MCU**			*GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 13/02/2025	Time: 15:18:43	Sheet 2 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_MCU.SchDoc			

Analog Devices ADAU1787 Audio Codec

All digital pins have 5pF capacitance
Output of 0V9 regulator. To use it, short SB7



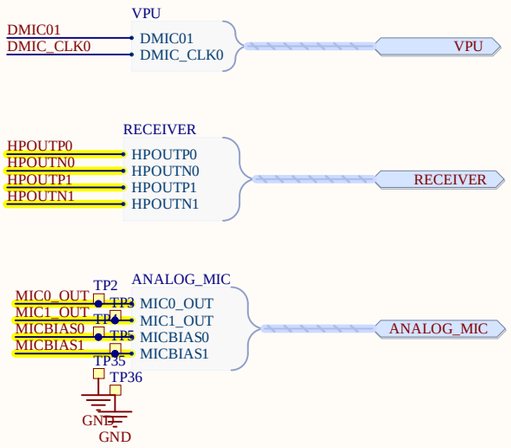
OBS

- For CLK use PWM from NRF. XTALO is open and crystal oscillator reg must be disabled
- REG_EN can be grounded to disable 0.9V LDO if DVDD is supplied
- Do not power up IOVDD when power is not applied to AVDD.
- I2C/SPI Enable (SW_EN). Connect this pin to DGND.

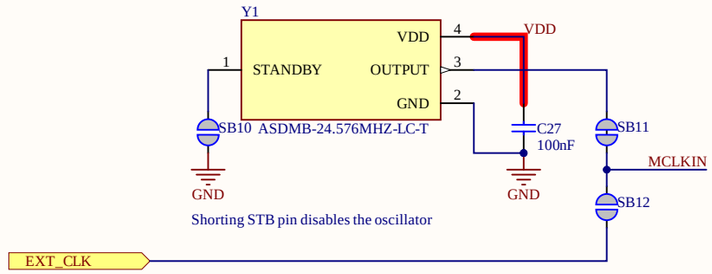
Configurations

- **1 - Using two analog inputs with passives recomended by PUI audio. Do not forget to use a PUI with lower than 1.6V spec**
- 2 - Bypassed power. DVDD is bypassed even if internal reg is used. IOVDD and AVDD are both connected to 1V8
- 4 - Falta a gravação com int e ext, mas por enquanto prefiro fazer com o interno.
  REG_EN - Regulator Enable. Tie this pin to AVDD to enable the regulator, and tie this pin to ground to disable the regulator
  The IC can be put into I2C and/or SPI mode by tying the SW_EN pin to DGND
- 5 - CM bypassed. Could also be used for external amp common mode adjust
- 6 - Selfboot puts ADAU on master mode so that it boots using the EEPROM. Not used here
- 7 - PD control via microcontroller
- 8 - For the I2S remember to use compatible GPIO on the nordic side
- 9 - I2C adderes set to 0x2B with both ADDR0 and ADDR1 connected to IOVDD
- 10 - CLK
- 11 - DMIC connections for using one vesper VPU alone

Audio Codec Peripherals

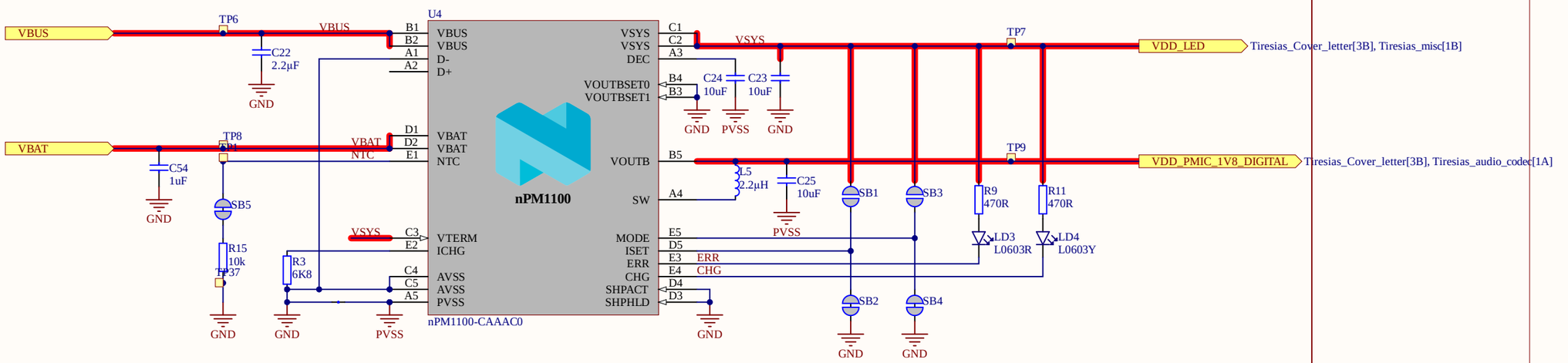


Audio Codec CLK

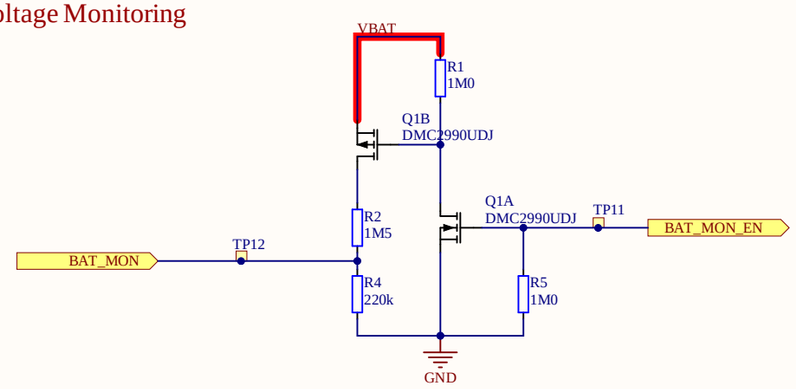


Title: **Audio Codec**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 13/02/2025	Time: 15:18:44	Sheet 3 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_audio_codec.SchDoc			

nPM1100 PMIC



Voltage Monitoring



Reference

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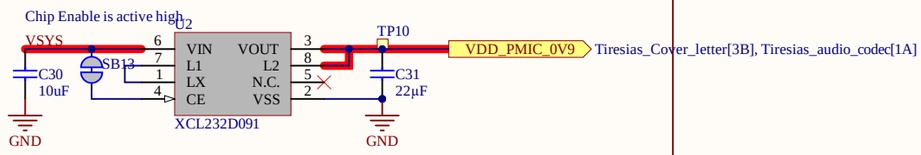
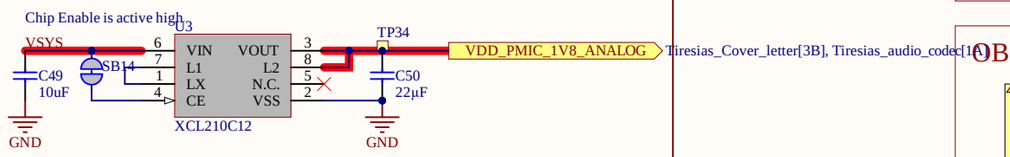
Audio Codec DVDD Regulator



Audio Codec AVDD Regulator



Configurations

For fixed VBUS current options:
D+=NC; D-=AVSS and either:
ISET=AVSS for 100mA or
ISET=VSYS for 500mA

- VTERM high - 4.2V charge termination
- 3V7 LiIon or LiPo battery

- RCHG = 625/current_limit-1562.5
For 6K8 resistor current is 75mA, which is right above 70mA for the min I found at mouser

- Added NTC short and TP for external

Mode Low Automatic selection between Hysteretic and PWM modes. Since . In PWM mode, BUCK provides a clean supply operation, there are SB for an eventual change

VOUTBSET 0 and 1 to Low = 1V8 VOUTB output

If Ship mode is not required, then SHPACT and SHPHLD pins may be tied to AVSS.

NTC
10kR +- 15 at 25 Celcius
B25/50 constant 3380K
B25/85 constant 3434 to 3435K

If the thermal protection feature is not used, then a 10 kΩ, ≤20% accuracy resistor should be connected between NTC and AVSS pins.

An application should not be supplied directly from VBAT because it can disturb the battery charging process and may cause incorrect behavior from the charger. Instead, VOUTB and/or VSYS should be used to supply an application.

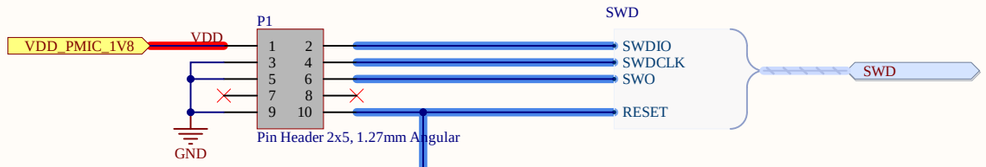
OBS

The VDD pin allows the debugger (e.g., a programmer or debug probe) to detect the operating voltage of the target system. This ensures that the debugger can adjust its signal levels (for SWDIO and SWCLK) to match the target device's logic levels, preventing damage due to mismatched voltages.
The VSYS and DEC pins must not be externally supplied

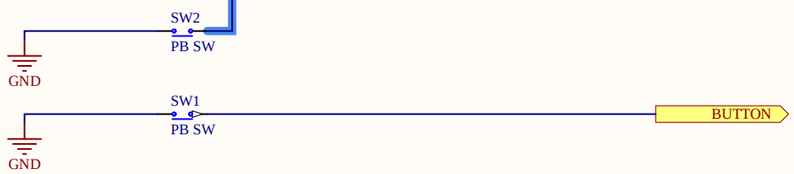
Product must have standard Vterm spec

Title: **Tiresias PMIC**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
Size: A3	Number: *	Revision: 0	
Date: 13/02/2025	Time: 15:18:44	Sheet 4 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_PMIC.SchDoc			

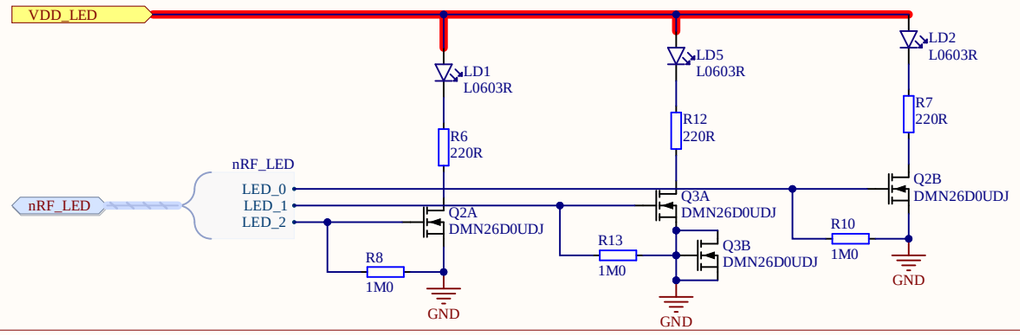
SWD Interface



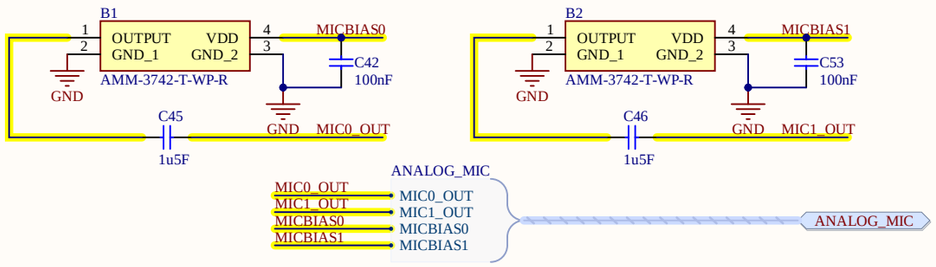
Push Button



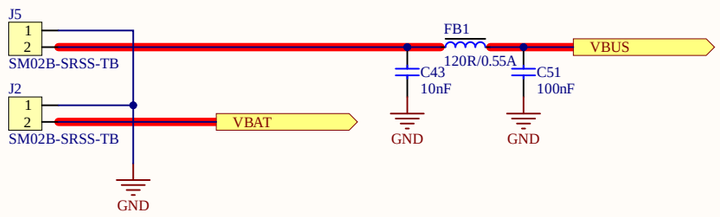
LEDs



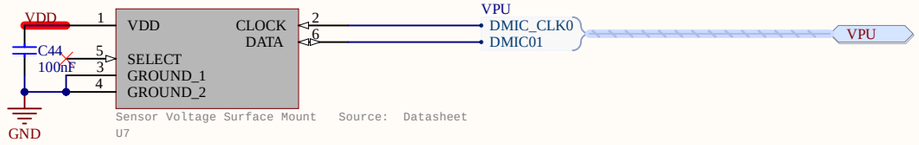
Analog Microphones



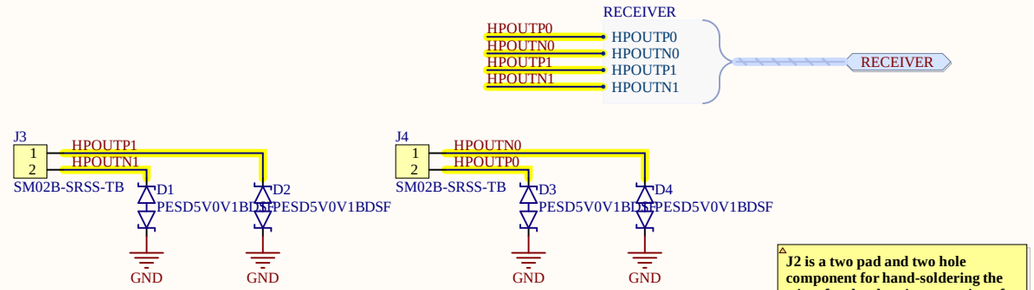
Power Connectors



VPU



Receiver Connector



J2 is a two pad and two hole component for hand-soldering the wires for the chassis connection of a 2-pin headphone connector

Flash Memory

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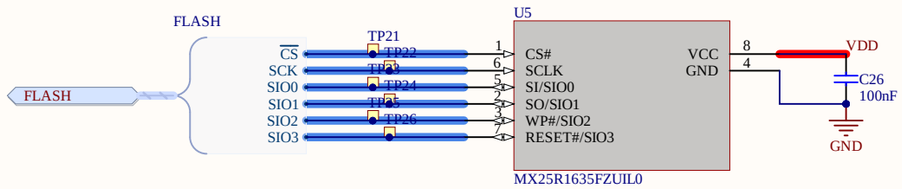
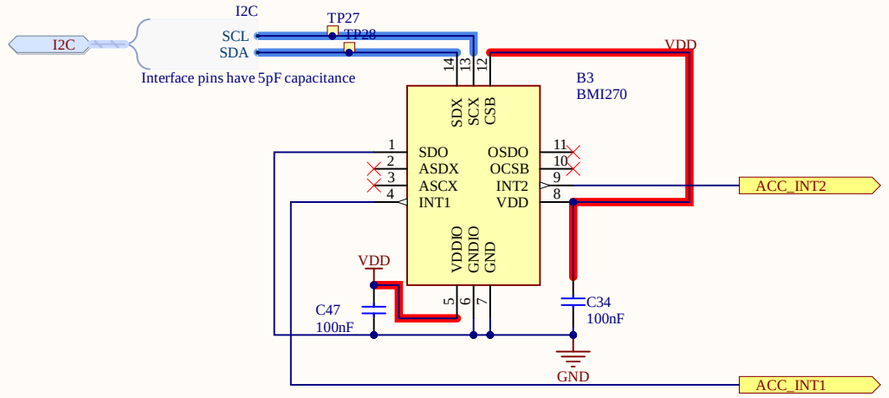


Accelerometer



ACC - The default I²C address of the device is 0b1101000 (0x68). It is used if the SDO pin is pulled to ´GND´. The alternative address 0b1101001 (0x69) is selected by pulling the SDO pin to ´VDDIO´

CSB - Chip select for SPI mode. Connects to VDDIO**
**** DNC is also possible due to an internal pull-up, as long as the voltage never drops below VIH.**

Title: **Tiresias Miscellaneous**			*R&D GMETA* *EESC - USP* *400, Trabalhador São-Carlense Av.* *13566-590, São Carlos* *São Paulo, Brazil*
Drawn By: João Victor Colombari Carlet			
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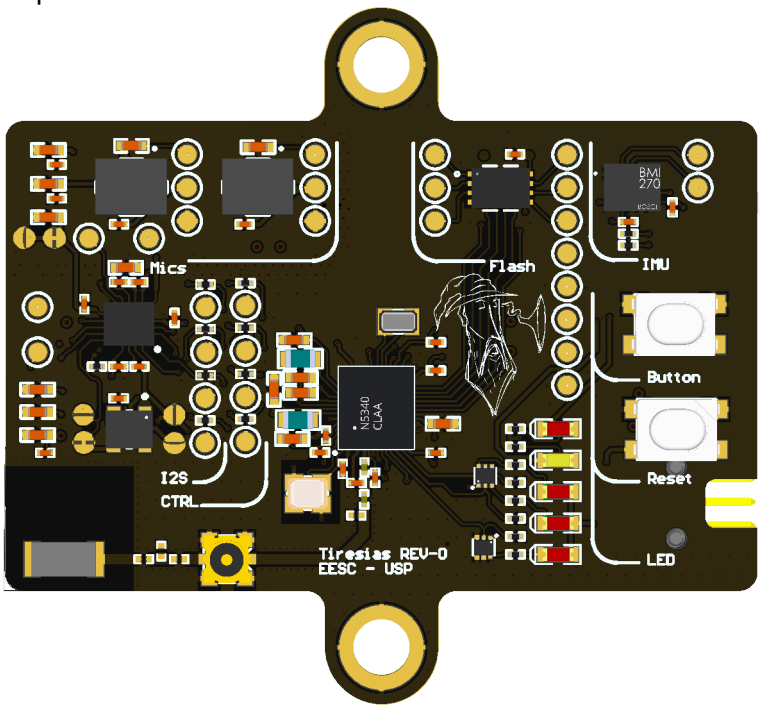
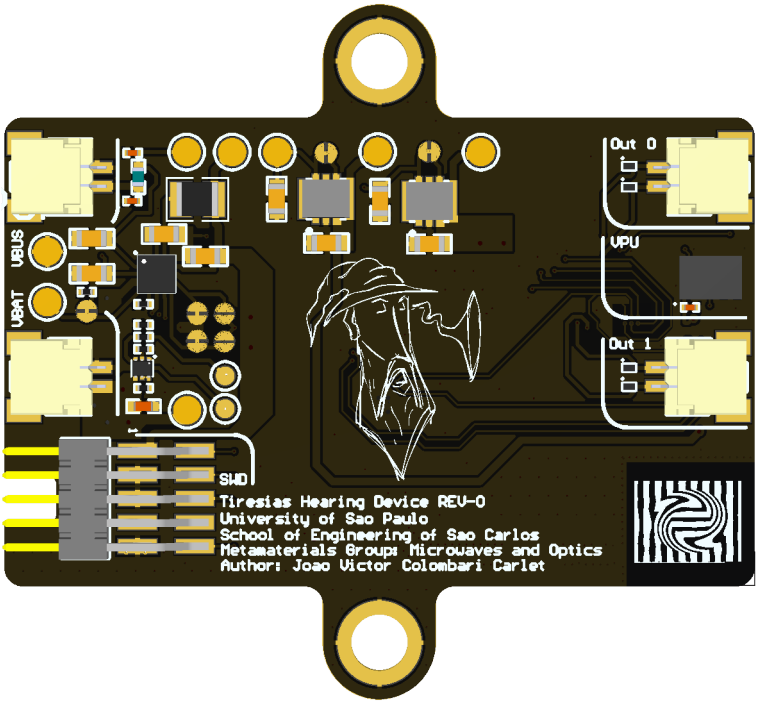
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_misc.SchDoc			

Tiresias Hearing Device Prototype - Hardware Documentation

Top View



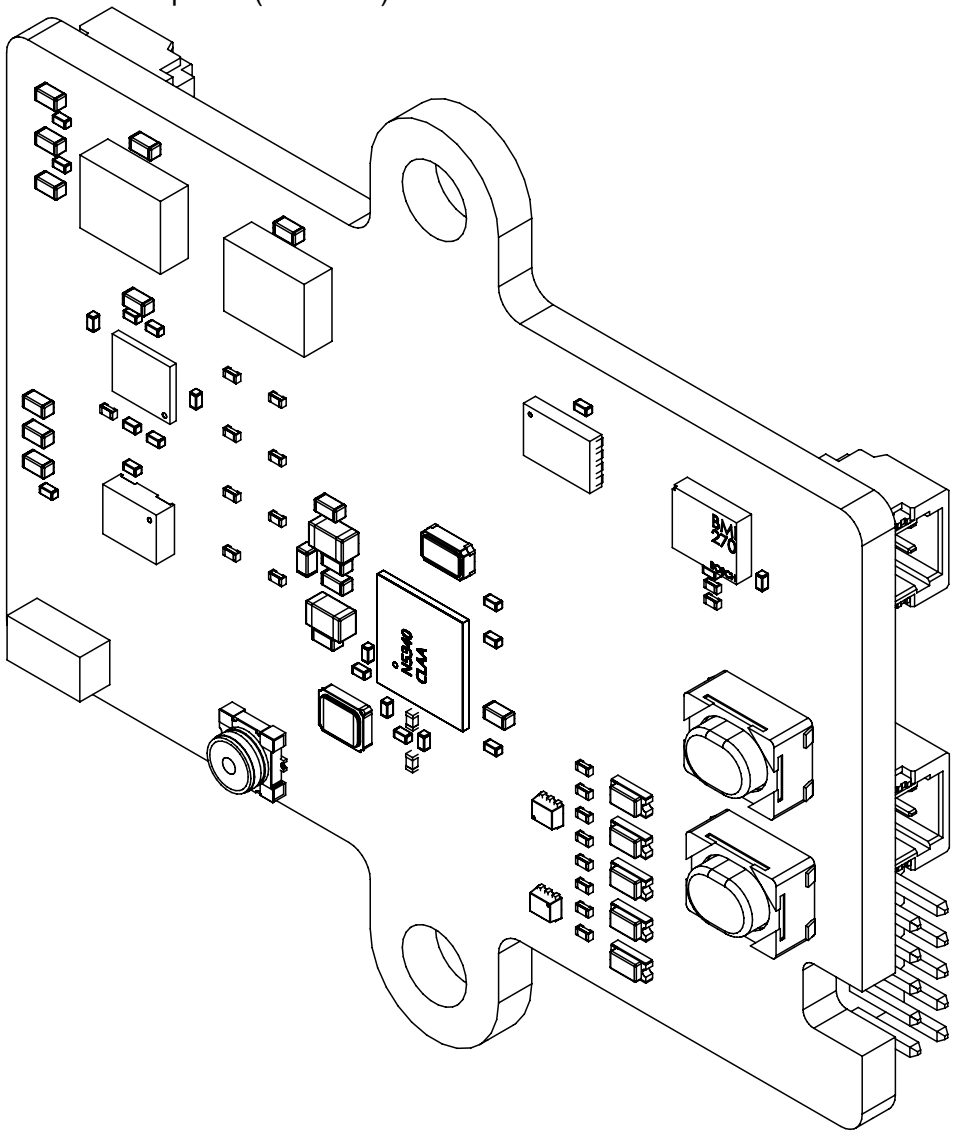
Bottom View



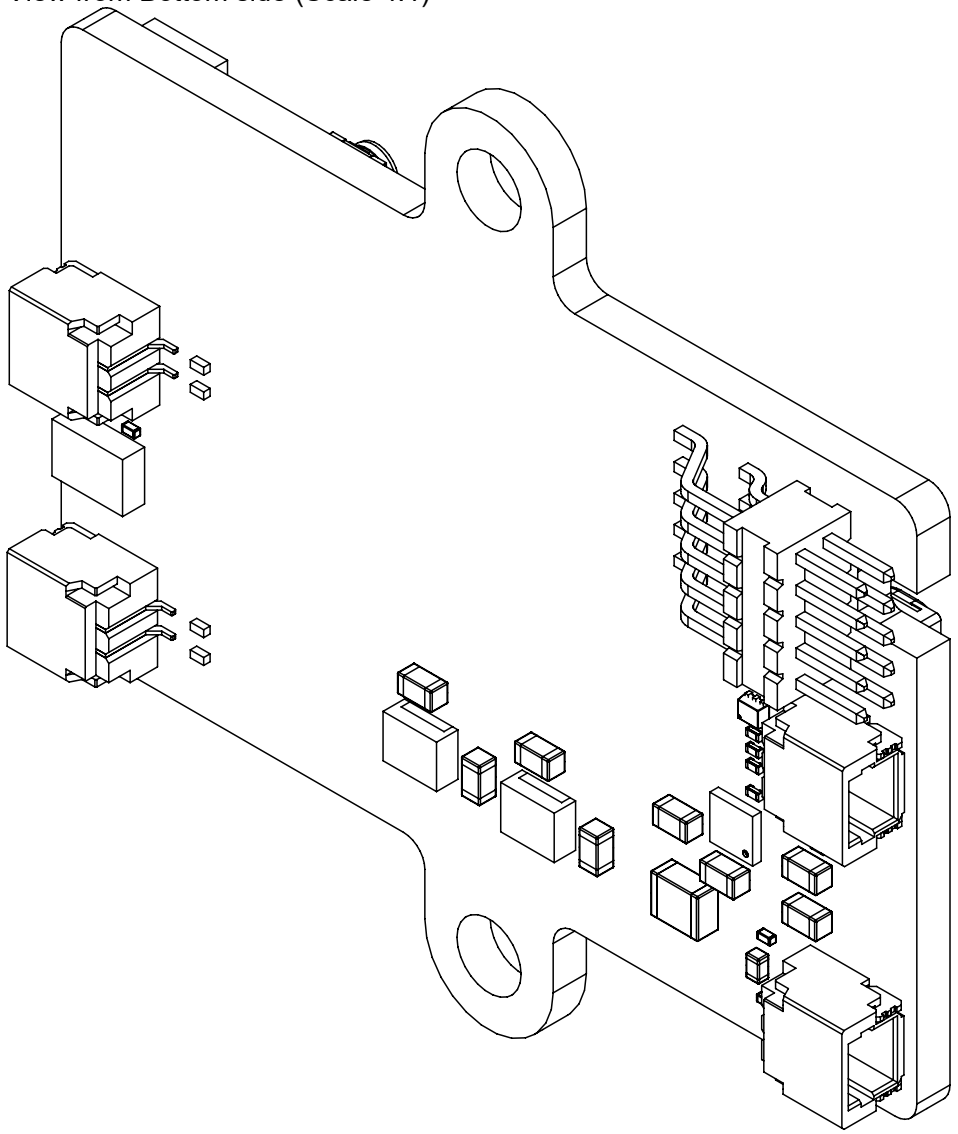
Engineer: João Victor Colombari Carlet

ISO View

View from Top side (Scale 4:1)



View from Bottom side (Scale 4:1)

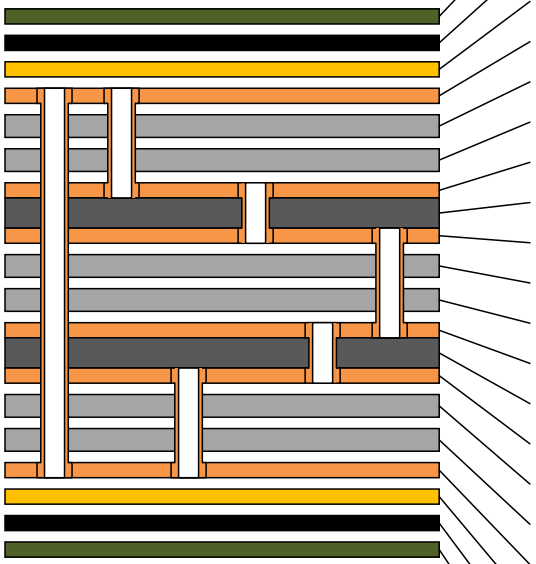


Stack-Up and Impedance

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Substack	Clearance	Target Tolerance
1	Coated Coplanar Waveguide With Ground	50	49.99	Top Layer	0.55mm	0.55mm	Int4 (GND)	Board Layer Stack	0.13mm	10%
2	Coated Coplanar Waveguide With Ground	50	49.99	Bottom Layer	0.55mm	0.55mm	Int1 (GND)	Board Layer Stack	0.13mm	10%

Layer Stack Legend

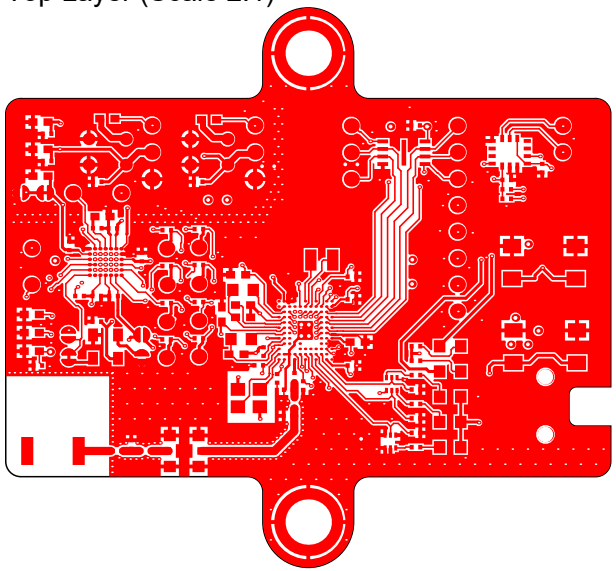


Material	Layer	Thickness	Dielectric Material	Type	Gerber	Weight	Df	Dk
	Top Overlay			Legend	GTO	0.125oz		
Surface Material	Top Solder	0.03mm	SM-002	Solder Mask	GTS	0.125oz	0,03	4
Nickel, Gold	Top Surface Finish	0.00mm		Surface Finish				
CF-004	**Top Layer**	**0.04mm**		**Signal**	**GTL**	**1oz**		
Prepreg		*0.07mm*	*PP-006*	*Dielectric*		*0.125oz*	*0,02*	*4,1*
Prepreg		*0.07mm*	*PP-006*	*Dielectric*		*0.125oz*	*0,02*	*4,1*
CF-004	**Int1 (GND)**	**0.04mm**		**Signal**	**G1**	**1oz**		
Core		*0.46mm*	*Core-035*	*Dielectric*		*0.125oz*	*0,02*	*4,7*
CF-004	**Int2 (PWR)**	**0.04mm**		**Signal**	**G2**	**1oz**		
Prepreg		*0.07mm*	*PP-006*	*Dielectric*		*0.125oz*	*0,02*	*4,1*
Prepreg		*0.07mm*	*PP-006*	*Dielectric*		*0.125oz*	*0,02*	*4,1*
CF-004	**Int3 (SIG)**	**0.04mm**		**Signal**	**G3**	**1oz**		
Core		*0.46mm*	*Core-035*	*Dielectric*		*0.125oz*	*0,02*	*4,7*
CF-004	**Int4 (GND)**	**0.04mm**		**Signal**	**G4**	**1oz**		
Prepreg		*0.07mm*	*PP-006*	*Dielectric*		*0.125oz*	*0,02*	*4,1*
Prepreg		*0.07mm*	*PP-006*	*Dielectric*		*0.125oz*	*0,02*	*4,1*
CF-004	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**	**1oz**		
Nickel, Gold	Bottom Surface Finish	0.00mm		Surface Finish				
Surface Material	Bottom Solder	0.03mm	SM-002	Solder Mask	GBS	0.125oz	0,03	4
	Bottom Overlay			Legend	GBO	0.125oz		

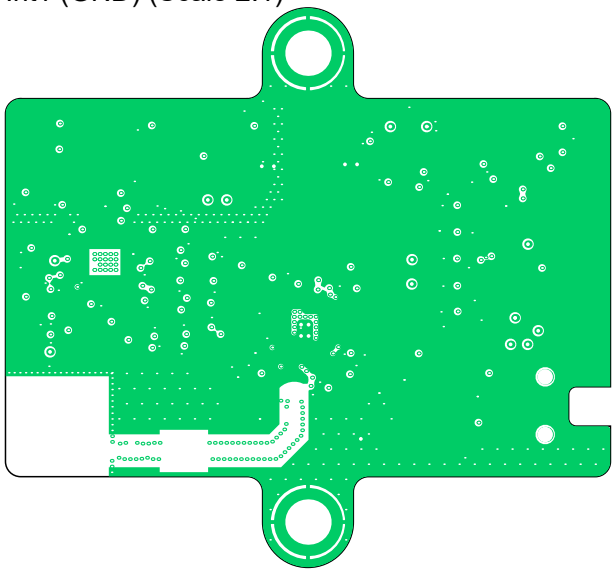
Total thickness: 1.61mm

Layers

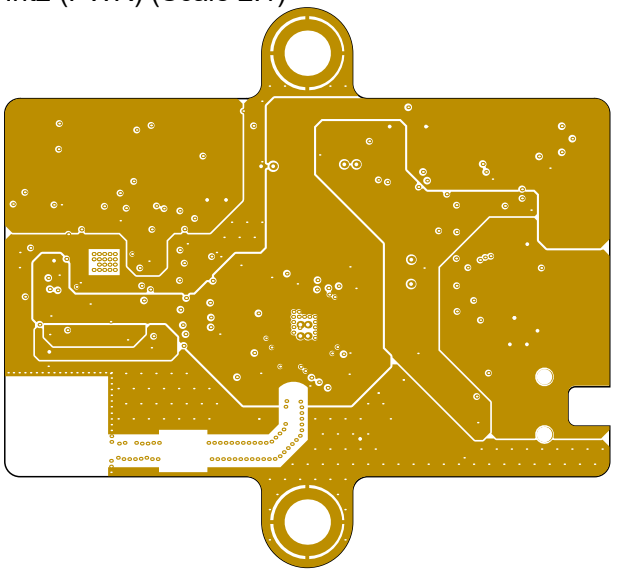
Top Layer (Scale 2:1)



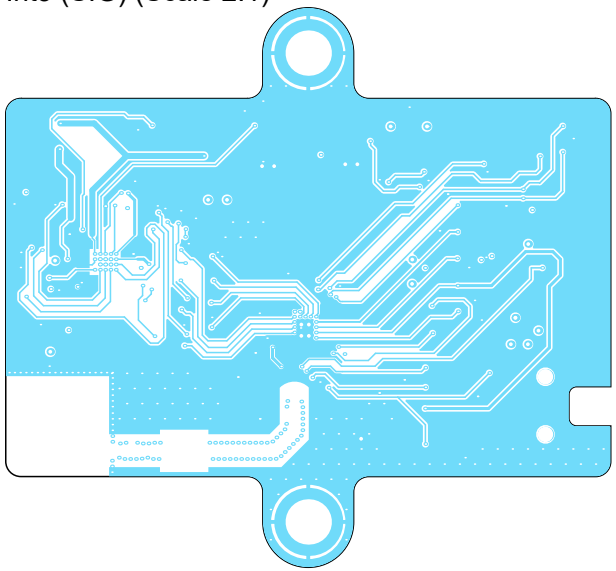
Int1 (GND) (Scale 2:1)



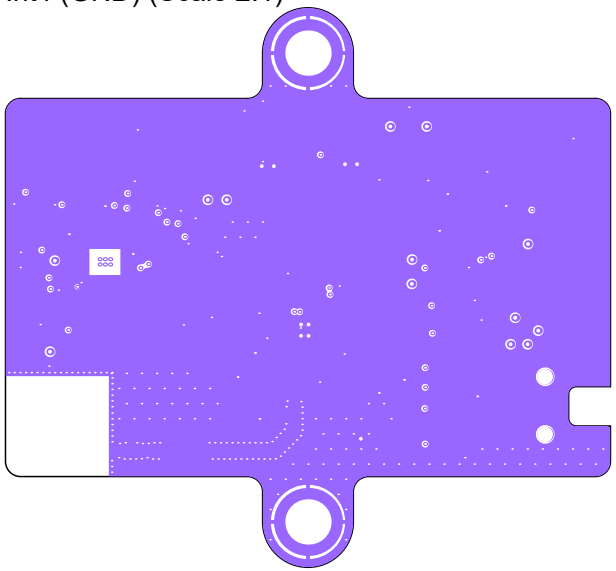
Int2 (PWR) (Scale 2:1)



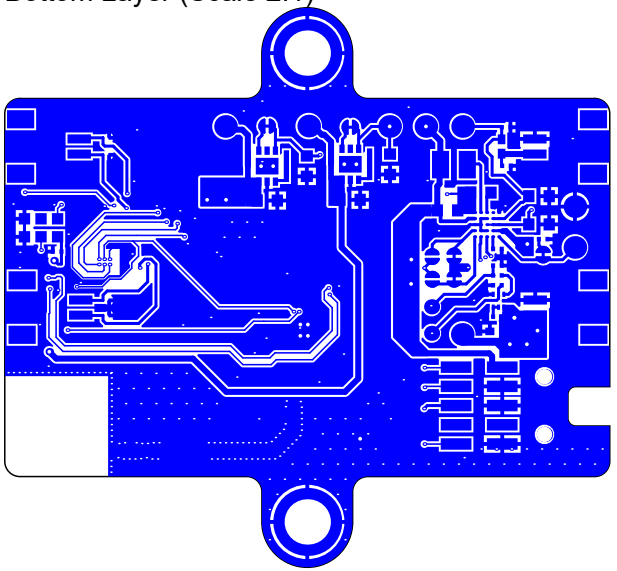
Int3 (SIG) (Scale 2:1)



Int4 (GND) (Scale 2:1)



Bottom Layer (Scale 2:1)

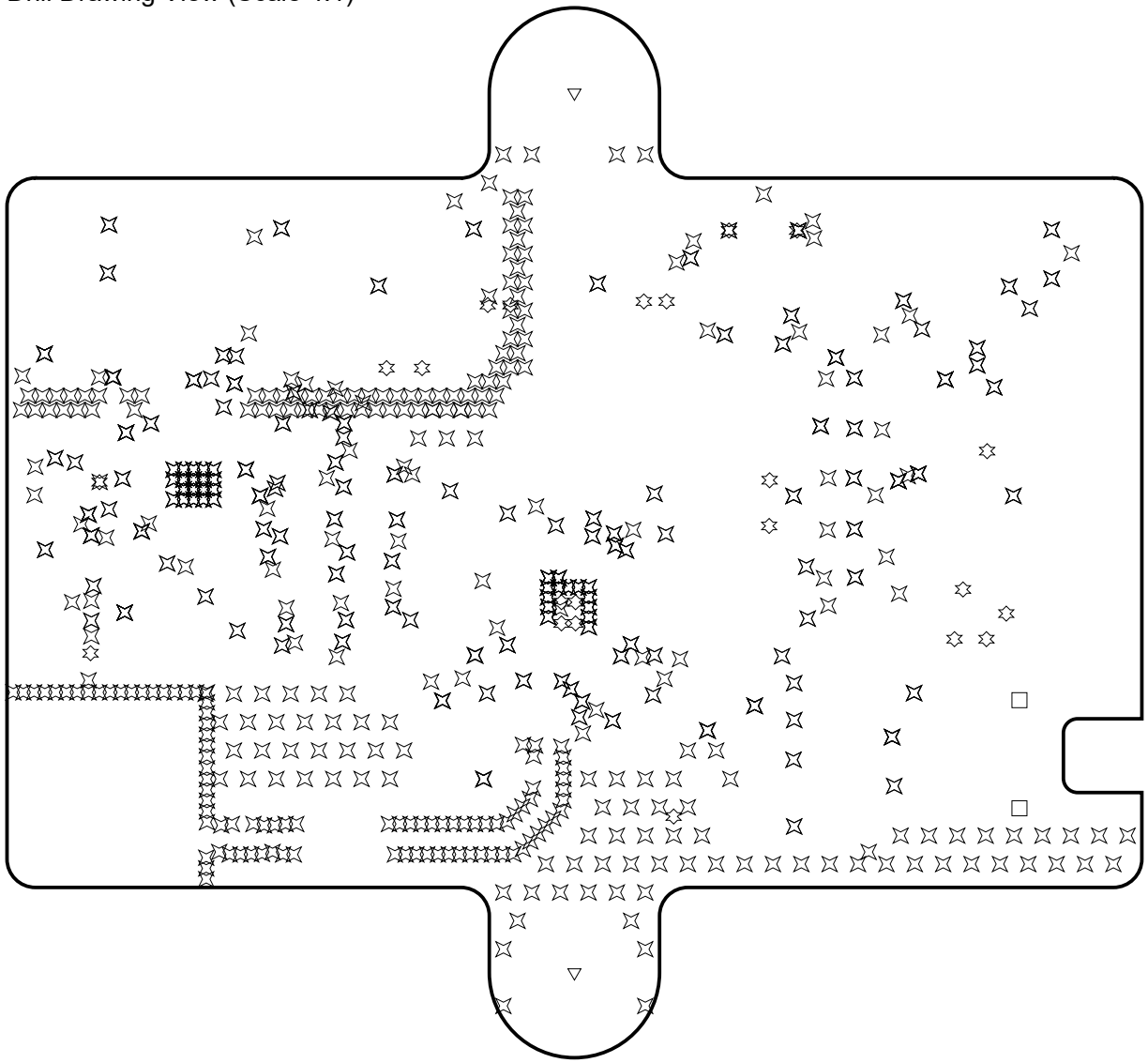


Drills

Drill Table

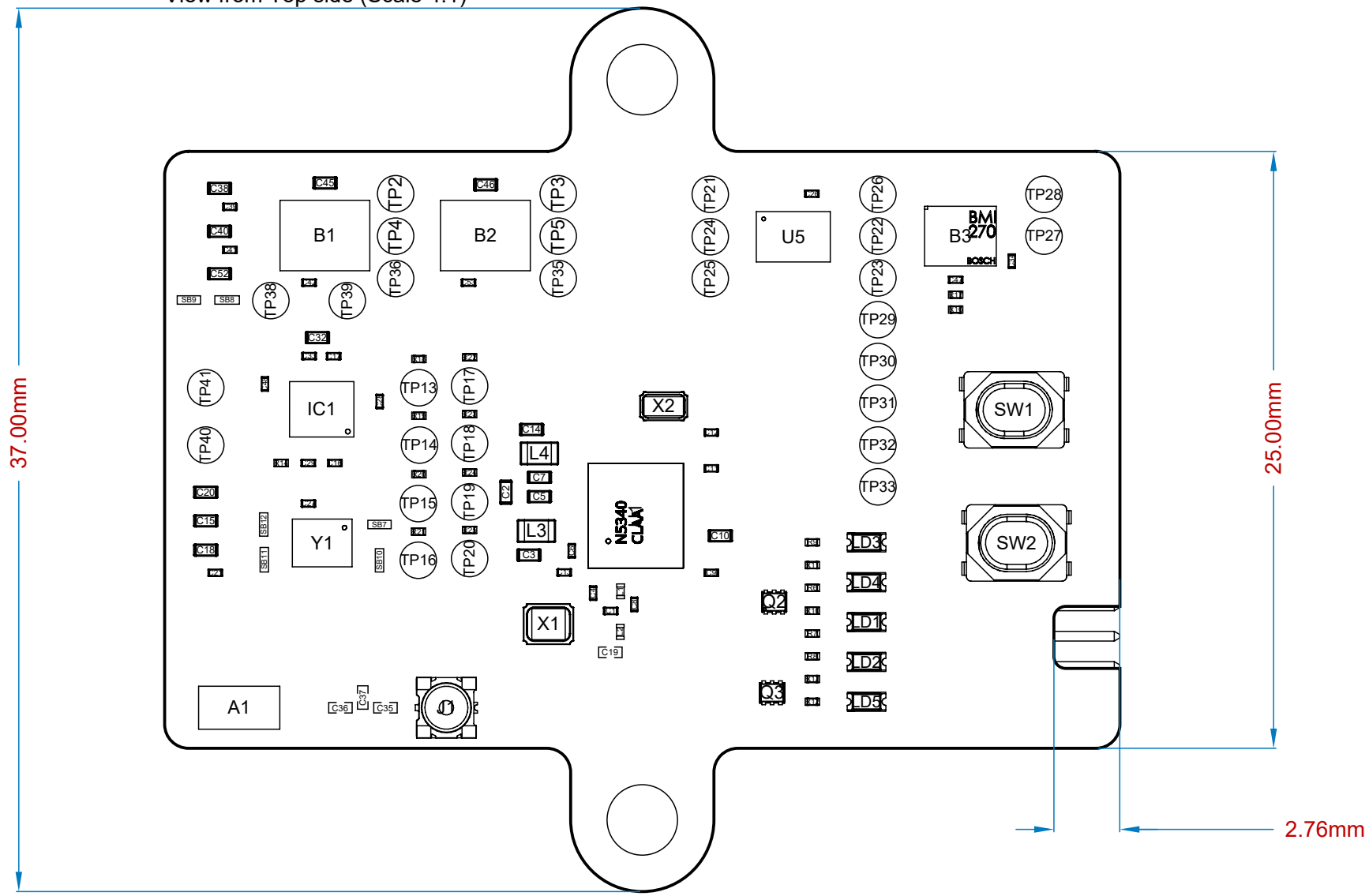
Symbol	Count	Hole Size	Plated	Hole Tolerance
☒	816	0.10mm	Plated	
✡	22	0.25mm	Plated	
□	2	1.02mm	Non-Plated	
▽	2	3.00mm	Plated	
	842 Total			

Drill Drawing View (Scale 4:1)



Assembly Top

View from Top side (Scale 4:1)



Assembly Bottom