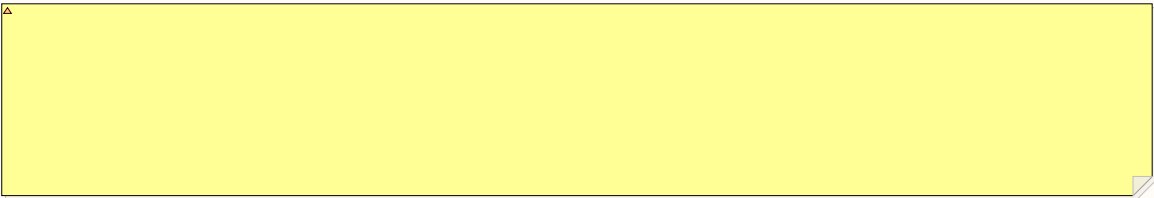


Metamaterials Group: Microwaves and Optics

Tiresias Hearing Device Prototype

Sheet 1:	Cover
Sheet 3:	MCU
Sheet 4:	Audio Codec
Sheet 5:	PMIC
Sheet 6:	Miscellaneous

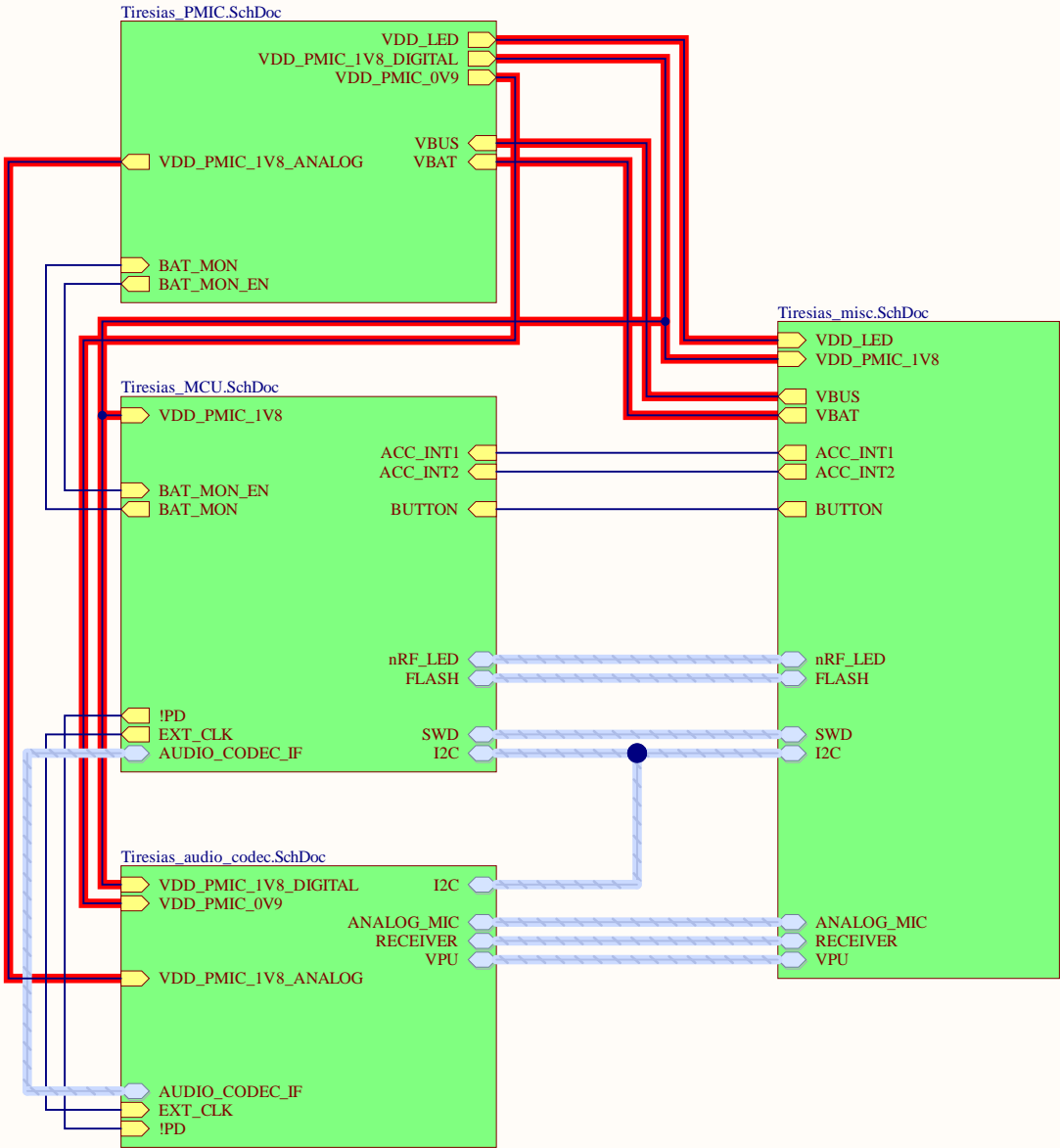
- Power Signals
- Analog Signals
- Serial Communication
- RF

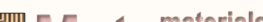


✗ The No ERC object is a design directive.
This directive is placed on a node in the circuit to suppress reported warnings and/or error violation conditions that are detected when the schematic project is compiled.

⚡ The DIFFPAIR object is a design directive.
This directive is placed on a differential pair so that they are routed accordingly.

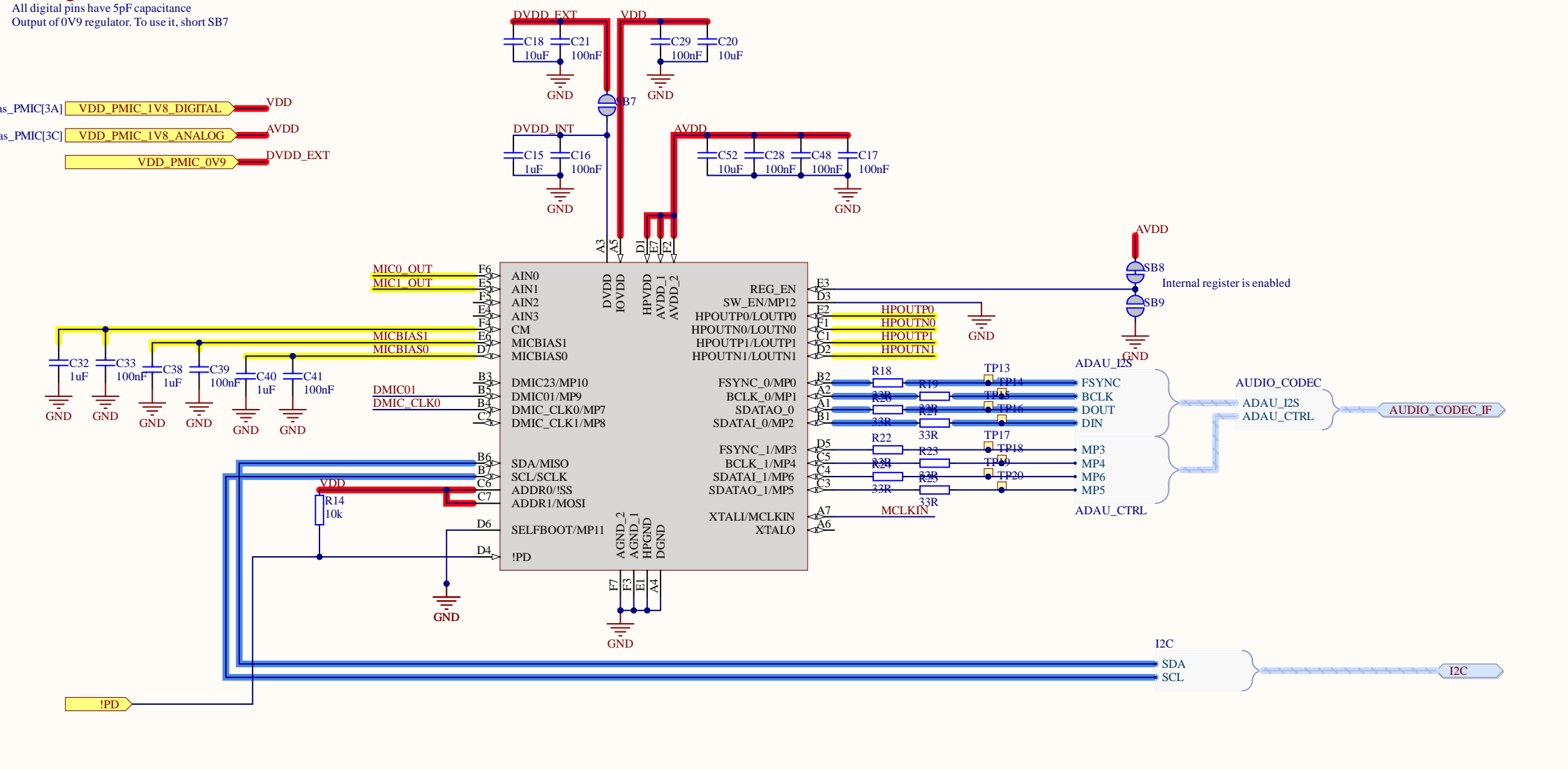
These are fiducial marks



Title: Tiresias Cover Letter			GMETA <i>EESC - USP</i> 400, Trabalhador São-Carlense Av. 13566-590, São Carlos São Paulo, Brazil	
Drawn By: João Victor Colombari Carlet				
Size: A3	Number: *	Revision:0		
Date: 12/02/2025	Time: 16:04:17	Sheet 1 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/	
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_Cover_letter.SchDoc				

Analog Devices ADAU1787 Audio Codec

All digital pins have 5pF capacitance
Output of 0V9 regulator. To use it, short SB7



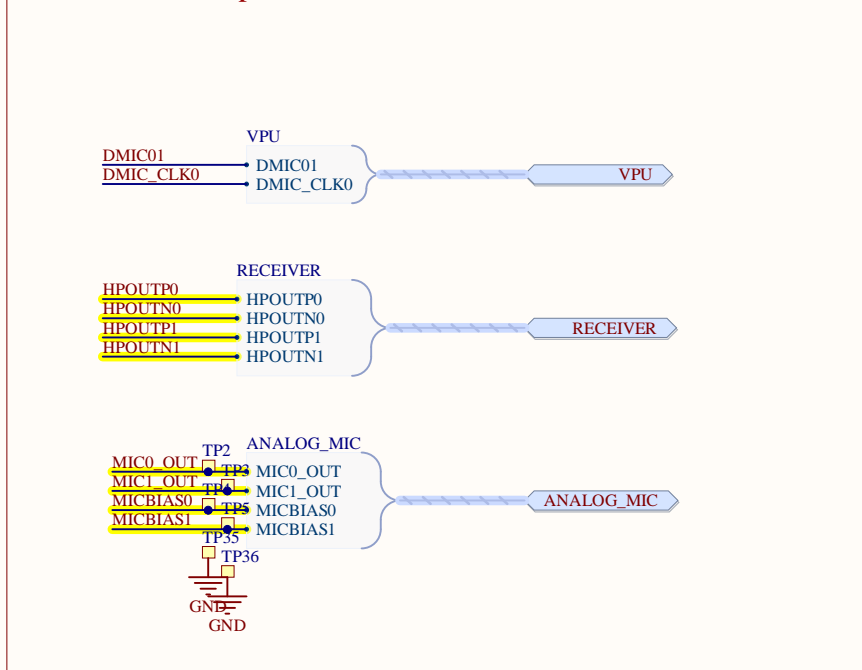
OBS

- For CLK use PWM from NRF. XTALO is open and crystal oscillator reg must be disabled
- REG_EN can be grounded to disable 0.9V LDO if DVDD is supplied
- Do not power up IOVDD when power is not applied to AVDD.
- I2C/SPI Enable (SW_EN). Connect this pin to DGND.

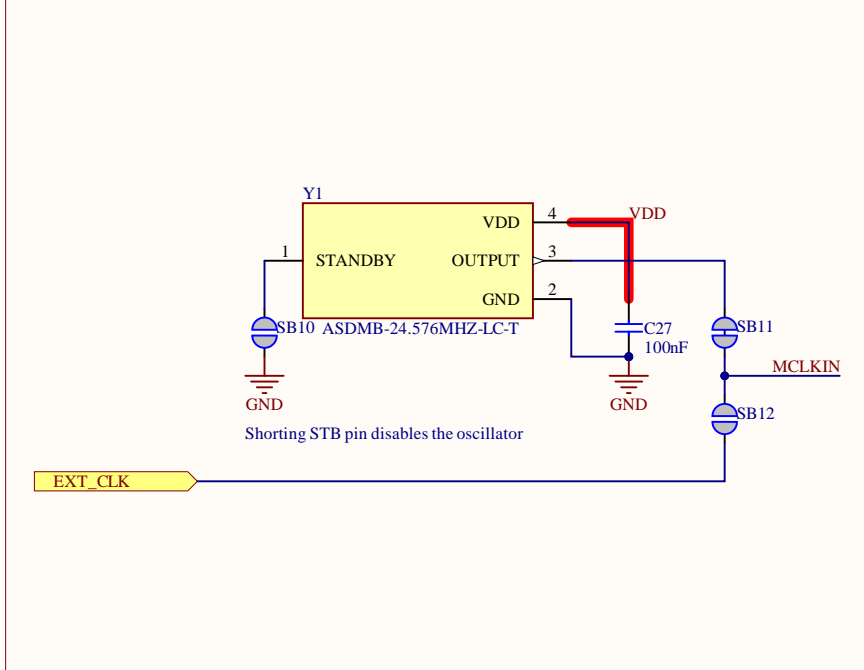
Configurations

- Using two analog inputs with passives recommended by PUI audio. Do not forget to use a PUI with lower than 1.6V spec
- Bypassed power. DVDD is bypassed even if internal reg is used. IOVDD and AVDD are both connected to 1V8
- Falta a gravação com int e ext, mas por enquanto prefiro fazer com o interno. REG_EN - Regulator Enable. Tie this pin to AVDD to enable the regulator, and tie this pin to ground to disable the regulator. The IC can be put into I2C and/or SPI mode by tying the SW_EN pin to DGND
- CM bypassed. Could also be used for external amp common mode adjust
- Selfboot puts ADAU on master mode so that it boots using the EEPROM. Not used here
- PD control via microcontroller
- For the I2S remember to use compatible GPIO on the nordic side
- I2C addreses set to 0x2B with both ADDR0 and ADDR1 connected to IOVDD
- CLK
- DMIC connections for using one vesper VPU alone

Audio Codec Peripherals



Audio Codec CLK



Title: Audio Codec			R&D GMETA EESC - USP 400, Trabalhador São-Carlense Av. 13566-590, São Carlos São Paulo, Brazil		
Drawn By: João Victor Colombari Carlet					
Size: A3	Number: *	Revision:0			
Date: 12/02/2025	Time: 16:04:17	Sheet 3 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/		
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_audio_codec.SchDoc					

<p>For fixed VBUS current options: D+=NC; D-=AVSS and either: ISET=AVSS for 100mA or ISET=VSYS for 500mA</p>	
<p>- VTERM high - 4.2V charge termination - 3V7 Lilon or LiPo battery</p>	
<p>- RCHG = 625/current_limit-1562.5 For 6K8 resistor current is 75mA, which is right above 70mA for the min I found at mouser</p>	
<p>- Added NTC short and TP for external</p>	
<p>Mode Low Automatic selection between Hysteretic and PWM modes. Since . In PWM mode, BUCK provides a clean supply operation, there are SB for an eventual change</p>	
<p>VOUTBSET 0 and 1 to Low = 1V8 VOUTB output</p>	
<p>If Ship mode is not required, then SHPACT and SHPHLD pins may be tied to AVSS.</p>	
<p>NTC 10kR +/- 15 at 25 Celcius B25/50 constant 3380K B25/85 constant 3434 to 3435K</p> <p>If the thermal protection feature is not used, then a 10 kΩ, ≤20% accuracy resistor should be connected between NTC and AVSS pins.</p>	
<p>An application should not be supplied directly from VBAT because it can disturb the battery charging process and may cause incorrect behavior from the charger. Instead, VOUTB and/or VSYS should be used to supply an application.</p>	

Chip Enable is active high (U3)

VVS3 6V

C49 10uF

SB 4

XCL210C12

VIN 6V

VOUT 3.3V

L1 7V

L2 8V

LX 1V

N.C. 5V

CE 4V

VSS 2V

TP34

C50 22uF

VDD_PMIC_1V8_ANALOG

Tiresias_Cover_letter[3B], Tiresias_audio_codec[3B]

Cannot open file C:\Users\alunos\Desktop\reference.PNG. File does not exist.

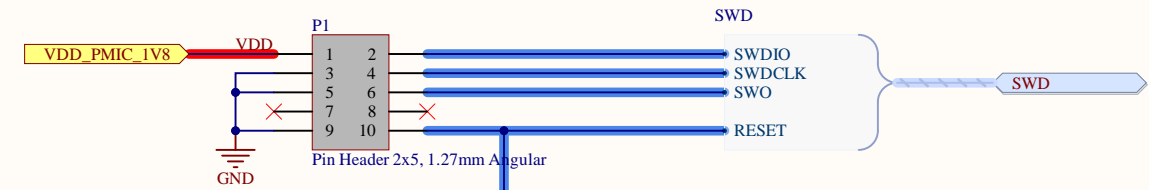
△ The VDD pin allows the debugger (e.g., a programmer or debug probe) to detect the operating voltage of the target system. This ensures that the debugger can adjust its signal levels (for SWDIO and SWCLK) to match the target device's logic levels, preventing damage due to mismatched voltages.

The VSYS and DEC pins must not be externally supplied

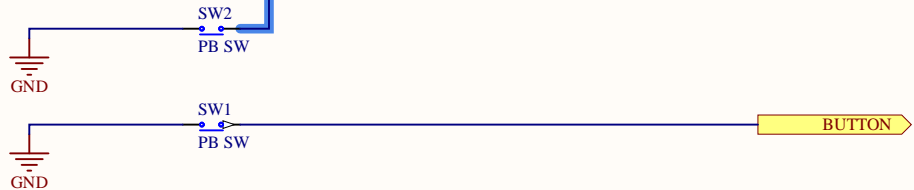
△ **Product must have standard Vterm spec**

Title: Tiresias PMIC			<i>R&D GMETA</i> <i>EESC - USP</i> <i>400, Trabalhador São-Carlense Av.</i> <i>13566-590, São Carlos</i> <i>São Paulo, Brazil</i>	
Drawn By: João Victor Colombari Carlet				
Size: A3	Number: *	Revision: 0		
Date: 12/02/2025	Time: 16:04:17	Sheet 4 of 5	Website: http://www.sel.eesc.usp.br/jcarmo/metamaterials/	
File: C:\Users\Public\Documents\Altium\Tiresias_HW\Tiresias_PMIC.SchDoc				

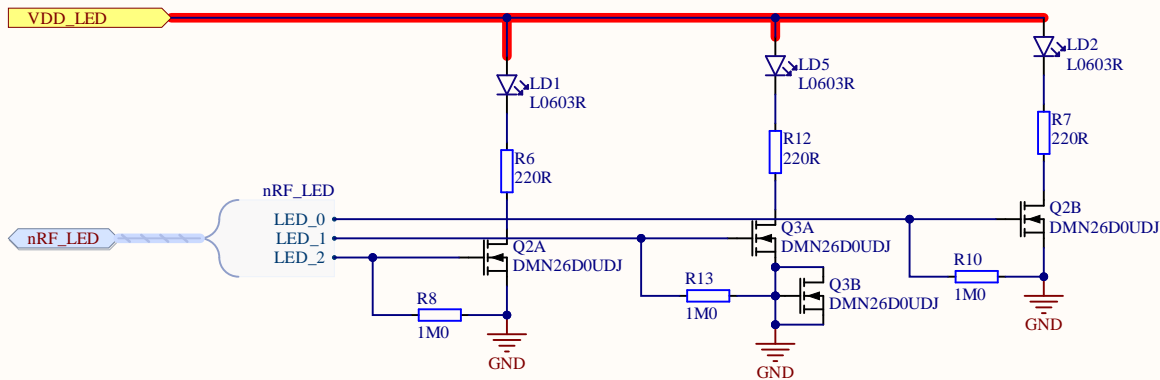
SWD Interface



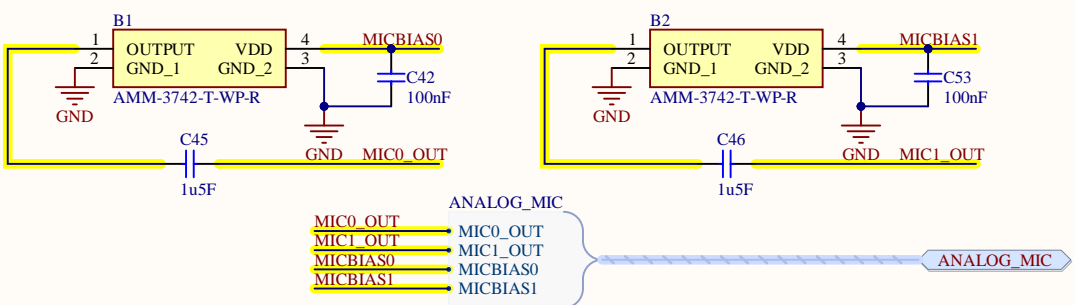
Push Button



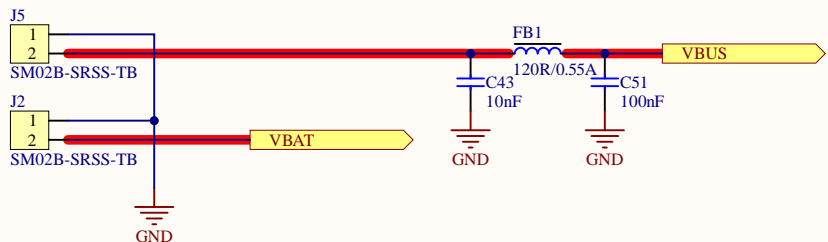
LEDs



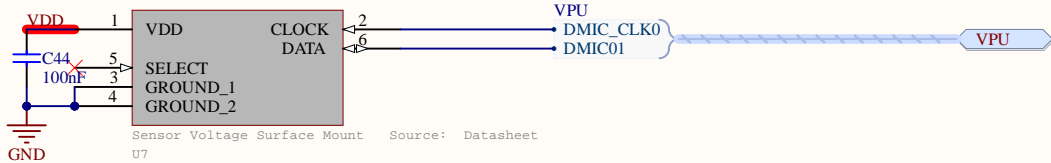
Analog Microphones



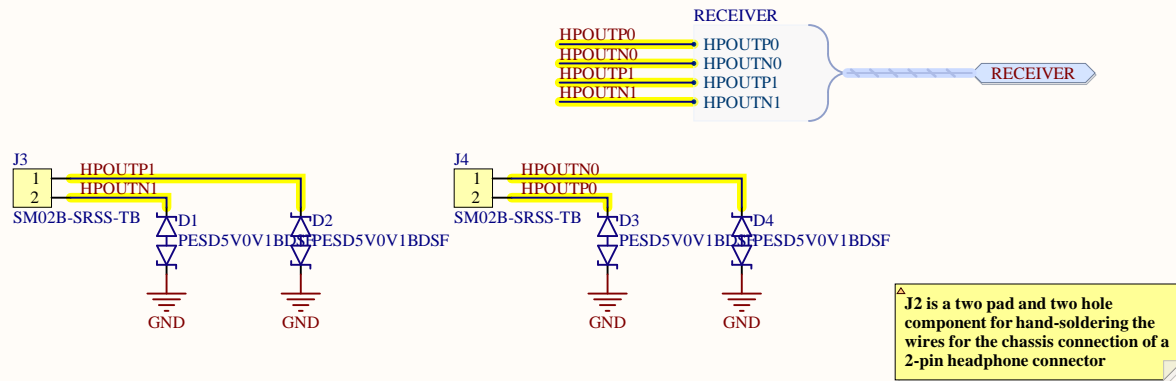
Power Connectors



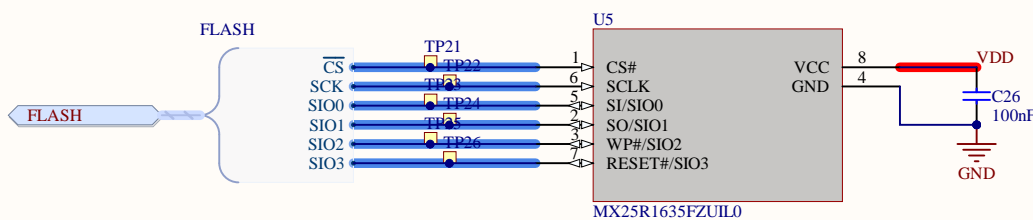
VPU



Receiver Connector

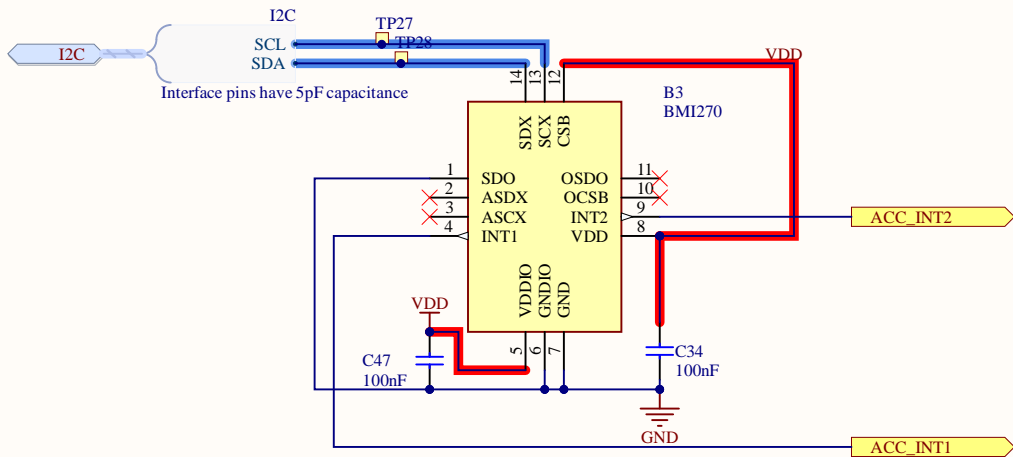


Flash Memory



Cannot open file
C:\Users\alunos\Desktop\MACRO
NIX.PNG. File does not exist.

Accelerometer

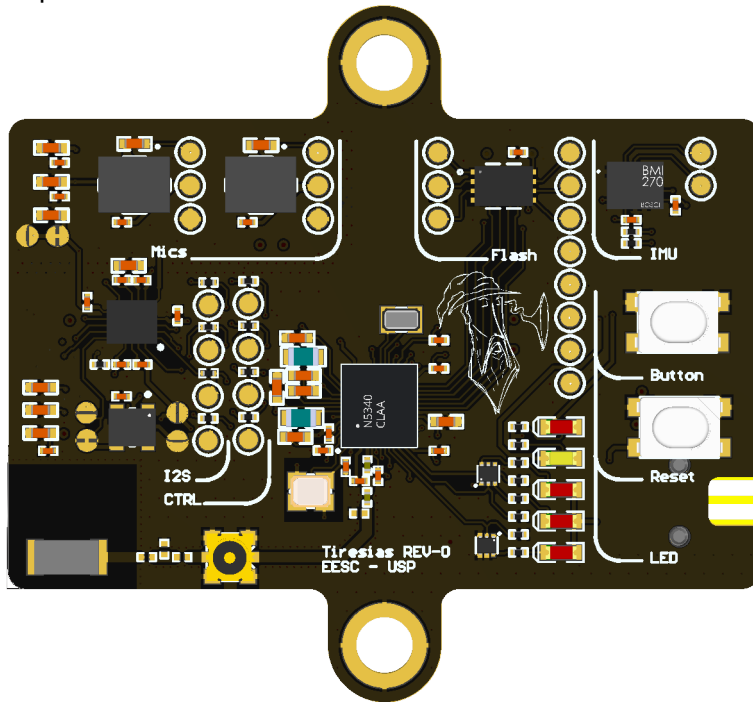


ACC - The default I²C address of the device is 0b1101000 (0x68). It is used if the SDO pin is pulled to 'GND'. The alternative address 0b1101001 (0x69) is selected by pulling the SDO pin to 'VDDIO'.

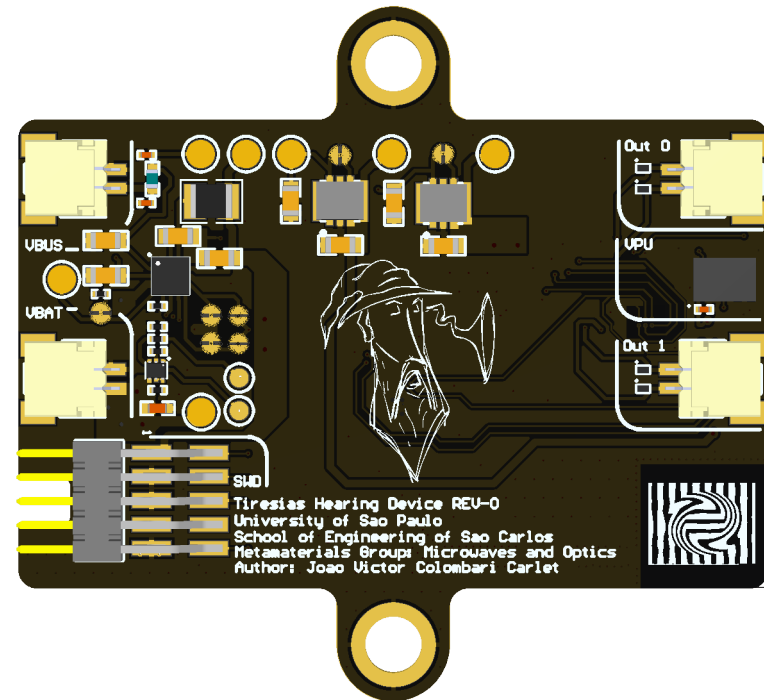
CSB - Chip select for SPI mode. Connects to VDDIO**
** DNC is also possible due to an internal pull-up, as long as the voltage never drops below VIH.

Tiresias Hearing Device Prototype - Hardware Documentation

Top View



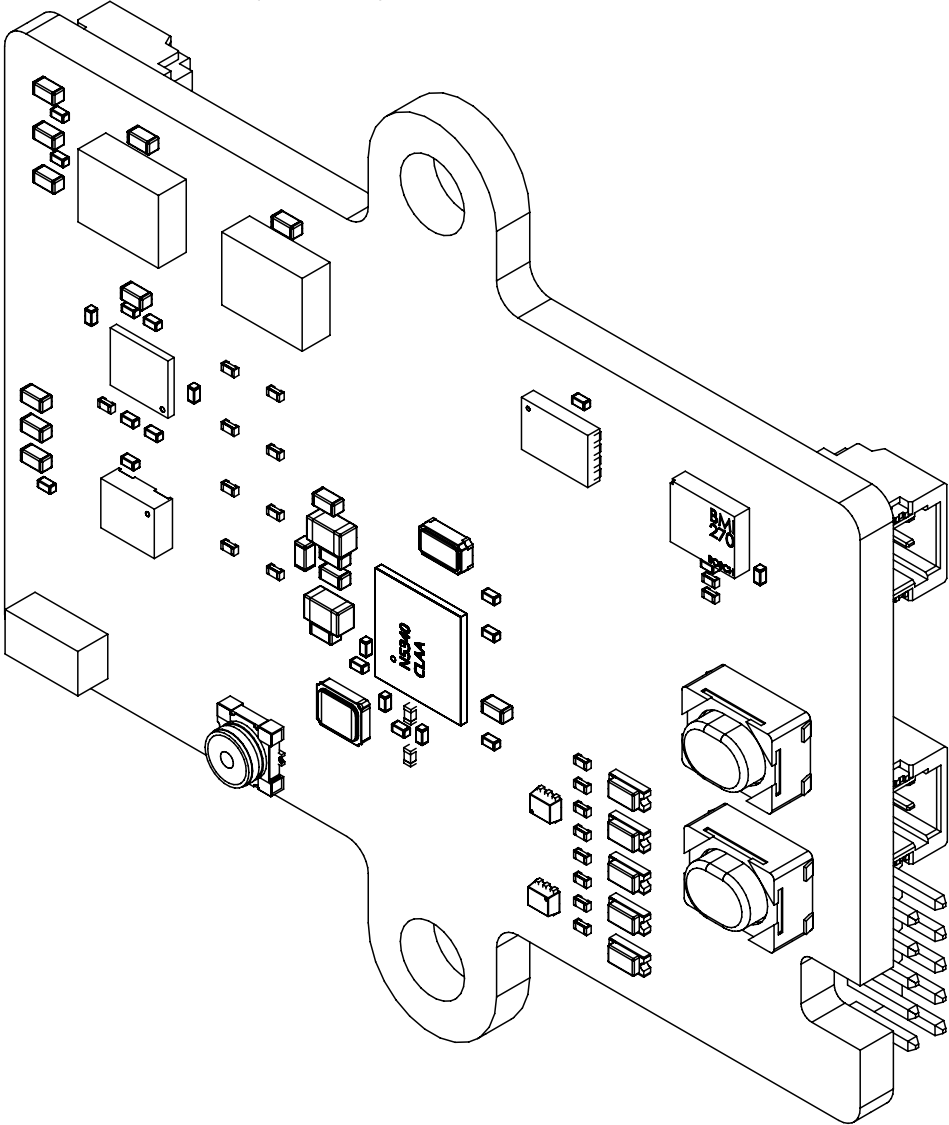
Bottom View



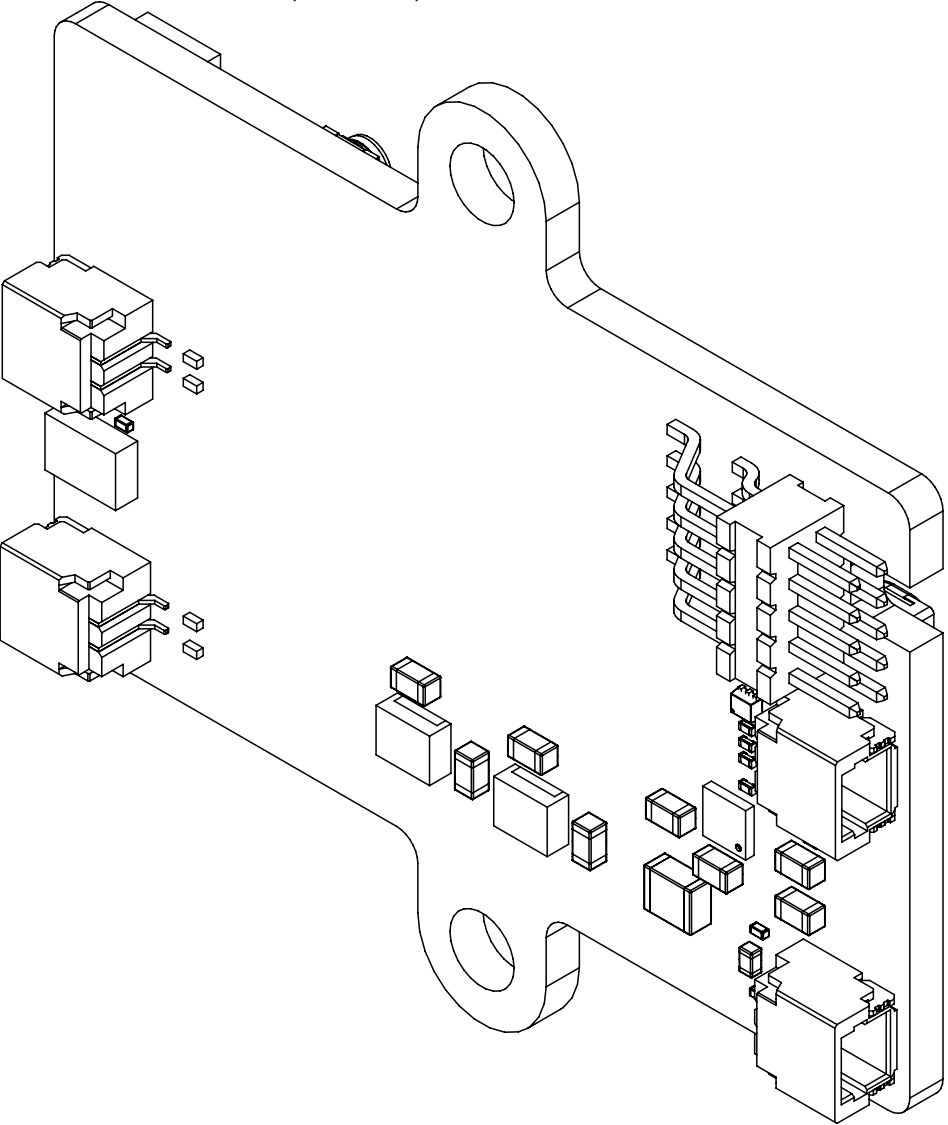
Engineer: João Victor Colombari Carlet

ISO View

View from Top side (Scale 4:1)



View from Bottom side (Scale 4:1)



1

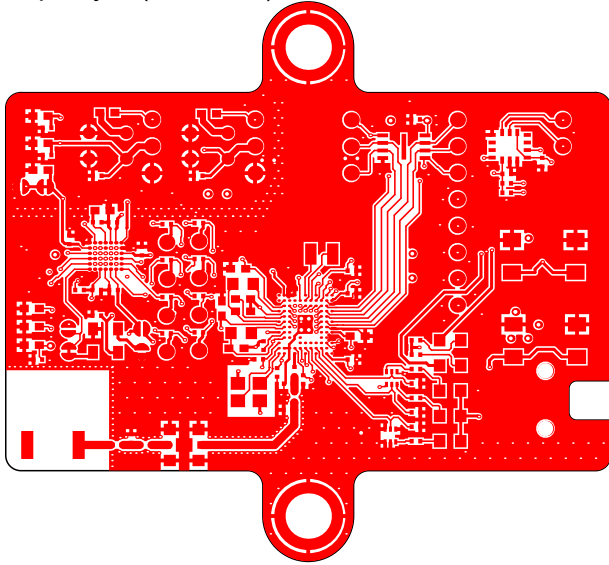
4

3

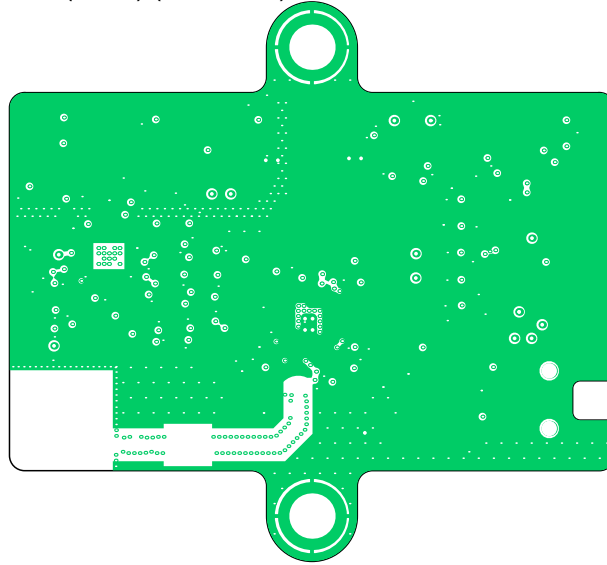


Layers

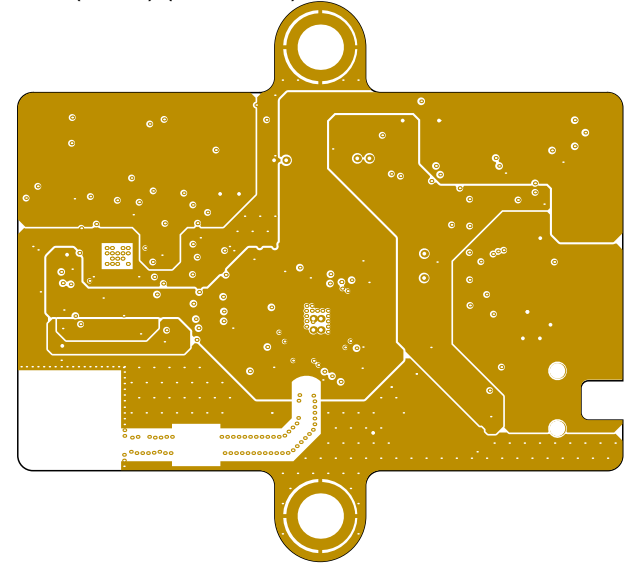
Top Layer (Scale 2:1)



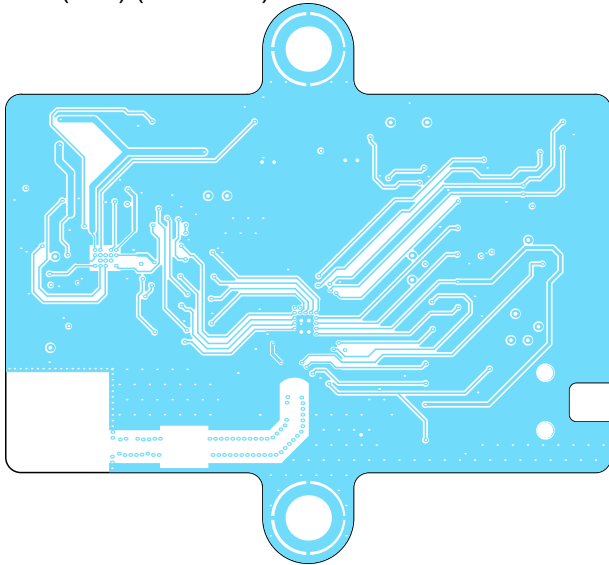
Int1 (GND) (Scale 2:1)



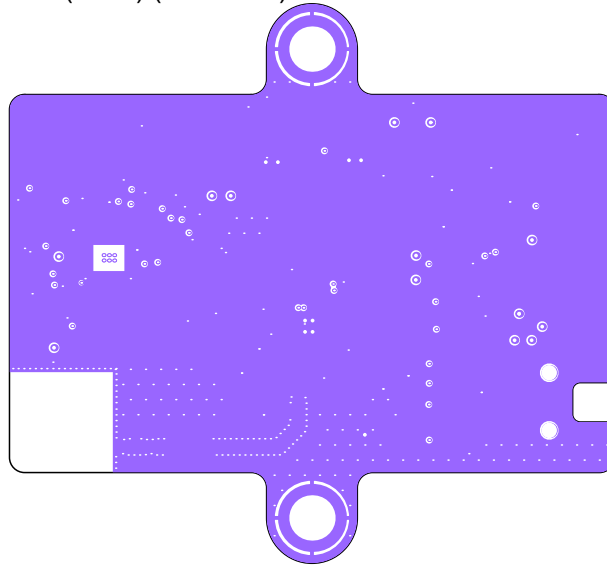
Int2 (PWR) (Scale 2:1)



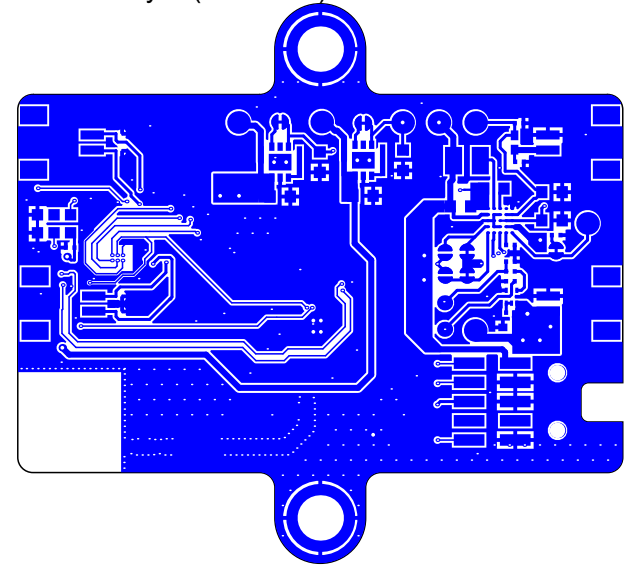
Int3 (SIG) (Scale 2:1)



Int4 (GND) (Scale 2:1)



Bottom Layer (Scale 2:1)

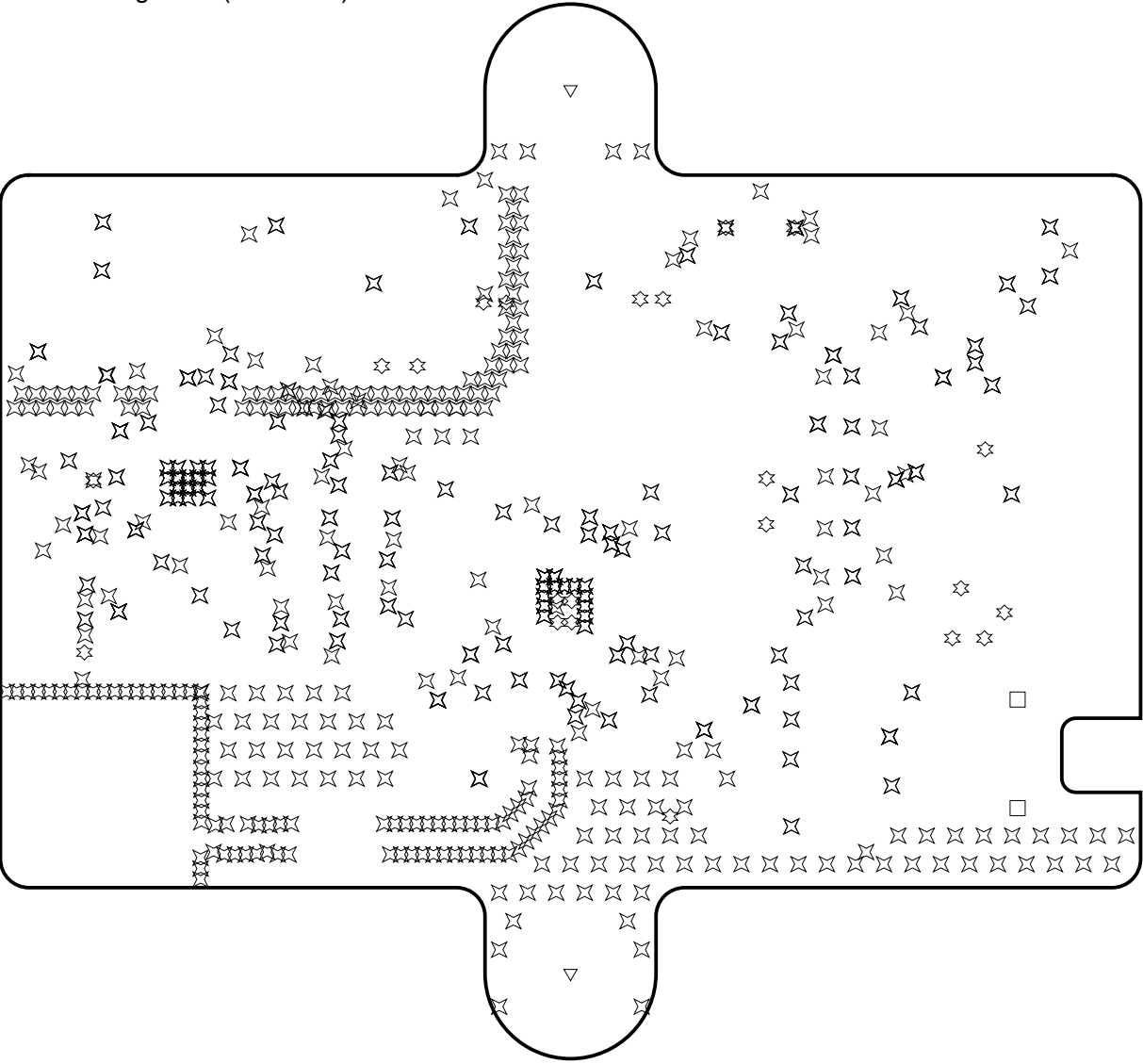


Drills

Drill Drawing View (Scale 4:1)

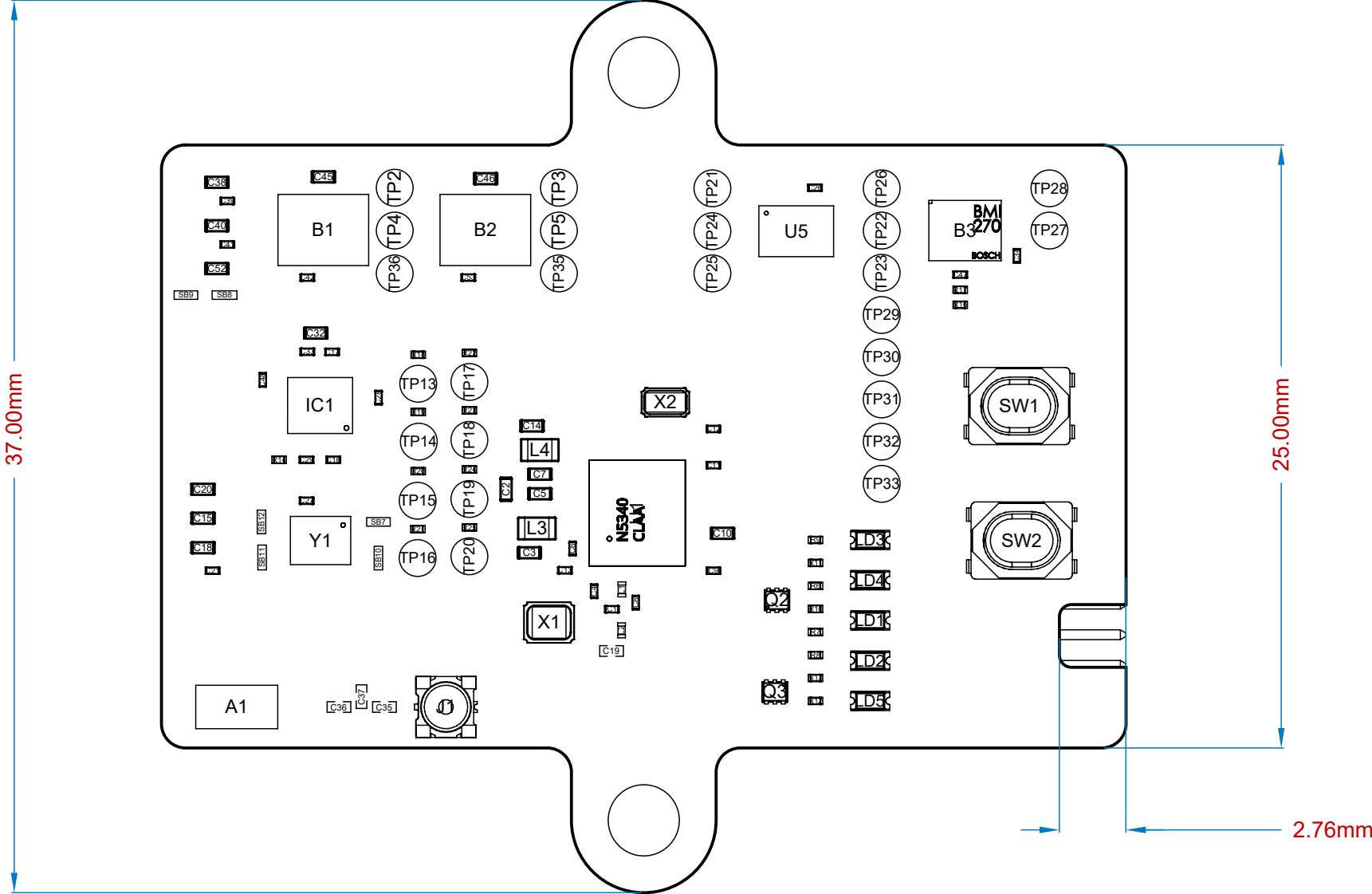
Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
✧	802	0.10mm	Plated	
☆	22	0.25mm	Plated	
□	2	1.02mm	Non-Plated	
▽	2	3.00mm	Plated	
	828 Total			



Assembly Top

View from Top side (Scale 4:1)



Assembly Bottom

